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(54) Title: A METHOD OF MANUFACTURING A PHOTOVOLTAIC CELL

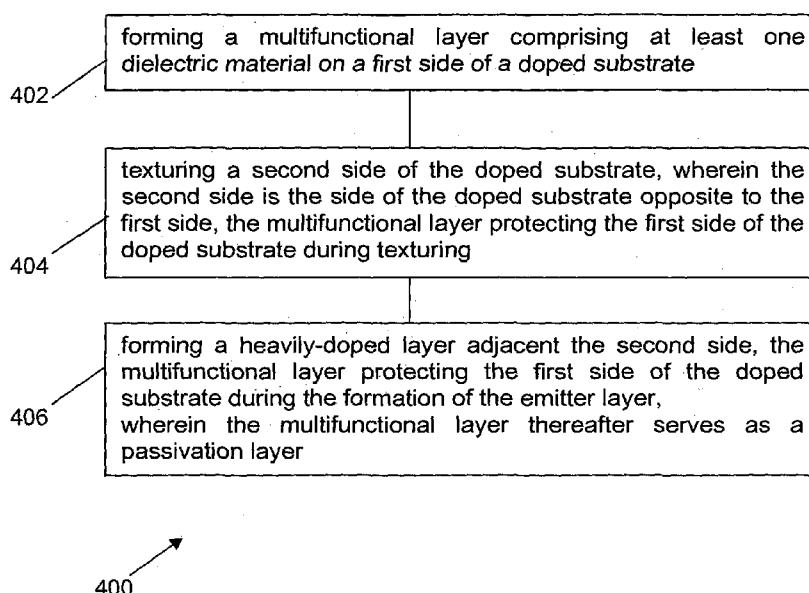


Figure 4

(57) Abstract: A method of manufacturing a photovoltaic cell, the method comprising the steps of: forming a multifunctional layer comprising at least one dielectric material on a first side of a doped substrate; texturing a second side of the doped substrate, wherein the second side is the side of the doped substrate opposite to the first side, the multifunctional layer protecting the first side of the doped substrate during texturing; and forming an heavily-doped layer adjacent the second side, the multifunctional layer protecting the first side of the doped substrate during the formation of the emitter layer, wherein the multifunctional layer thereafter serves as a passivation layer.



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A METHOD OF MANUFACTURING A PHOTOVOLTAIC CELL

5 TECHNICAL FIELD

The present invention relates broadly to a method of manufacturing a photovoltaic cell.

10 BACKGROUND

A photovoltaic (PV) cell or a solar cell is an electrical device that converts solar radiation to electrical energy. Conventionally, a PV cell comprises of a moderately doped ($5 \times 10^{14} \text{cm}^{-3}$ – $5 \times 10^{16} \text{cm}^{-3}$) substrate, e.g. a bulk silicon substrate, and a thin heavily-doped emitter layer on the bulk silicon substrate, forming a p-n junction. Heavily-doped p⁺-type silicon can be formed by diffusion of boron with three valence electrons into crystalline silicon, whilst heavily-doped n⁺-type silicon can be formed by diffusion of phosphorus with five valence electrons into the crystalline silicon. The PV cell may (although not necessarily) comprise of a back surface field – a heavily-doped layer, which is a high-low junction. If the PV cell is exposed to sunlight, the photons of sunlight pass the energy to the electrons, thereby generating pairs of free electrons and holes. The electric field formed across the p-n junction pushes the free electrons and holes to opposite sides of the photovoltaic cell. If an external circuit is connected from the p-type electrode to the n-type electrode, the free electrons are allowed to flow through the external circuit to reunite with the free holes to produce an electrical current.

PV electricity is becoming increasingly cost-effective for applications in most parts of the world, compared to electricity generation by other methods. Typically, the solar energy industry is supported by government policies such as the feed-in tariff in Germany to be more commercially viable. To become more cost-competitive, there is a need for cost reduction of PV electricity by reducing the upstream costs (e.g. by making the PV cells cheaper), or by reducing the downstream costs (e.g. by making more efficient cells), or both.

Silicon wafer solar cells account for approximately 90% of the market share in the solar energy industry. In some existing manufacturing processes of high-efficiency silicon wafer solar cells, single side or front side processing is typically implemented. In other words, there is a need for single side texturing and single side n⁺-type or p⁺-type doping of a silicon substrate. Typically, sacrificial masks are deposited at one side of the silicon substrate to allow single side processing, e.g. texturing and diffusion of the other side of the substrate. For example, a dielectric film such as thermal silicon oxide (SiO₂), plasma deposited silicon oxide (SiO_x) or silicon nitride (SiN_x) is deposited at the opposite side of the silicon substrate to serve as a sacrificial layer before the diffusion or texturing process is carried out. The sacrificial layer is then removed by chemical or dry etching e.g. after each of the texturing or diffusion processes.

The manufacturing of a high efficiency silicon wafer solar cell usually involves many process steps. The deposition of the dielectric film is one of the most costly process steps in the manufacturing of silicon wafer solar cells. Furthermore, several such sacrificial dielectric films may be deposited and removed during the course of manufacturing a solar cell.

A need therefore exists to provide a method of manufacturing a photovoltaic cell that seeks to address at least some of the problems above or to provide a useful alternative.

SUMMARY

According to a first aspect of the present invention, there is provided a method of manufacturing a photovoltaic cell, the method comprising the steps of:

forming a multifunctional layer comprising at least one dielectric material on a first side of a doped substrate;

texturing a second side of the doped substrate, wherein the second side is the side of the doped substrate opposite to the first side, the multifunctional layer protecting the first side of the doped substrate during texturing; and

forming a heavily-doped layer adjacent the second side, the multifunctional layer protecting the first side of the doped substrate during the formation of the heavily-doped layer,

wherein the multifunctional layer thereafter serves as a passivation layer.

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The heavily-doped layer may comprise one of an emitter layer, a back surface field, or a front surface field.

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The at least one dielectric material may be both chemical resistant and thermal resistant.

The multifunctional layer may comprise at least one chemical resistant dielectric material and at least one thermal resistant dielectric material.

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The chemical resistant dielectric material may comprise one selected from a group consisting of silicon nitride, silicon oxide, thermal silicon oxide, silicon oxynitride, aluminium oxide, aluminium nitride, aluminium oxynitride, aluminium fluoride, amorphous silicon and doped equivalents.

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The thermal resistant dielectric material may comprise one selected from a group consisting of silicon nitride, silicon oxide, thermal silicon oxide, silicon oxynitride, aluminium oxide, aluminium nitride, aluminium oxynitride, aluminium fluoride, amorphous silicon and doped equivalents.

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Depositing the multifunctional layer may comprise the steps of:
depositing the at least one thermal resistant dielectric material on the first side of the doped substrate; and
depositing the at least one chemical resistant dielectric material on the deposited at least one thermal resistant dielectric material.

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Depositing the multifunctional layer may comprise using one selected from a group consisting of chemical vapour deposition techniques, atomic layer depositions, physical vapour depositions and growth techniques.

Texturing the second side of the doped substrate may comprise forming a plurality of surface structures on the second side of the doped substrate.

Forming the heavily-doped layer may comprise using one selected from a group consisting of ion implantation, laser doping, laser chemical processing, doped dielectric layer deposition and diffusion.

The method may further comprise the steps of:

forming a passivation and anti-reflection coating on the heavily-doped layer;

and

forming electrodes adjacent the multifunctional layer and the heavily-doped layer respectively.

Forming the electrodes may comprise using one selected from a group consisting of screen-printing, stencil-printing, physical vapor deposition, plating and inkjet printing, aerosol-printing.

According to a second aspect of the present invention, there is provided a solar cell manufactured using the method as defined in the first aspect.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention will be better understood and readily apparent to one of ordinary skill in the art from the following written description, by way of example only, and in conjunction with the drawings, in which:

Figure 1 shows a flow chart illustrating a method of manufacturing a solar cell according to an example embodiment.

Figure 2A shows a schematic diagram illustrating a sectional view of the wafer obtained from step 102 of Figure 1.

Figure 2B shows a schematic diagram illustrating a sectional view of the wafer obtained from step 104 of Figure 1.

5 Figure 2C shows a schematic diagram illustrating a sectional view of the wafer obtained from step 106 of Figure 1.

Figure 2D shows a schematic diagram illustrating a sectional view of the wafer obtained from step 108 of Figure 1.

10 Figure 2E shows a schematic diagram illustrating a sectional view of the wafer obtained from step 112 of Figure 1.

Figure 2F shows a schematic diagram illustrating a sectional view of the wafer obtained from step 114 of Figure 1.

15 Figure 2G shows a schematic diagram illustrating a sectional view of the wafer obtained from step 116 of Figure 1.

20 Figure 2H shows a schematic diagram illustrating a sectional view of the wafer obtained from step 118 of Figure 1.

Figure 2I shows a schematic diagram illustrating a sectional view of the wafer obtained from step 120 of Figure 1.

25 Figure 3 shows a column chart illustrating dielectric thermal stability of an example multifunctional layer according to an example embodiment.

Figure 4 shows a flow chart illustrating a method of manufacturing a photovoltaic cell according to an example embodiment.

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DETAILED DESCRIPTION

Figure 1 shows a flow chart 100 illustrating a method of manufacturing a PV/solar cell according to an example embodiment. At step 102, a moderately doped substrate, e.g. a silicon wafer, is etched to remove saw damage. For example, the silicon substrate is n-type doped. At step 104, a multifunctional layer is formed, e.g. deposited or grown, on a first side of the doped silicon substrate. At step 106, a second side of the doped silicon substrate is textured, e.g. by alkaline etching, wherein the second side is the side of the doped silicon substrate opposite to the first side. At step 108, the second side of the doped silicon substrate is doped, e.g. by boron diffusion using boron tribromide (BBr_3) for forming a heavily-doped layer, e.g. an emitter layer, a back surface field or a front surface field, depending on the structure of the final solar cell. At step 110, the silicon wafer is cleaned e.g. by dipping the wafer into hydrofluoric acid (HF) for about 10 seconds. At step 112, the first side of the doped silicon substrate (where the multifunctional dielectric was deposited in step 104) is patterned to form at least one cavity, e.g. using laser processing or etching paste or photolithography. At step 114, n^+ doped region is formed at the cavities made in step 112 to serve as a localized back surface field, e.g. by phosphorous diffusion using phosphoryl chloride (POCl_3). At step 116, a coating e.g. a dielectric material is deposited on the textured second side of the doped silicon substrate to form e.g. a front passivation and anti-reflection coating. At step 118, at least one electrode is formed adjacent the first side of the doped silicon substrate, e.g. by screen-printing. At step 120, at least one electrode is formed adjacent the second side of the doped silicon substrate, e.g. by screen-printing. At step 122, the electrodes are thermally treated, e.g. by industrial firing. The method of manufacturing a silicon wafer solar cell according to exemplary embodiments of the present invention will be discussed in further detail with reference to Figures 2A-2I.

Figure 2A shows a schematic diagram illustrating a sectional view of the silicon wafer obtained from step 102 of Figure 1. Here, a doped substrate, e.g. N-type substrate in the form of silicon wafer substrate 202, has undergone etching to remove saw damage, as discussed above with respect to Figure 1. The doped silicon substrate 202 has a typical resistivity of 0.5 Ohm-cm to 10 Ohm-cm and thickness of 50 μm to 250 μm , and maybe $\langle 100 \rangle$ oriented. However, it will be

appreciated that the silicon substrate 202 may have other resistivity and thickness values.

In alternate embodiments, e.g. where the final solar cell may have a different structure, the silicon substrate 202 may be p-type doped. Any relevant substances can be used as doping agent, as will be understood by persons skilled in the art. The choice of Si substrate can be Monocrystalline, Multicrystalline or quasi-Monocrystalline.

Figure 2B shows a schematic diagram illustrating a sectional view of the silicon wafer obtained from step 104 of Figure 1. A multifunctional layer 204 comprising at least one dielectric material is formed, e.g. deposited or grown, on a first side 206 of the doped silicon substrate 202 (shown in Figure 2A). Suitable deposition techniques include, but are not limited to, plasma-enhanced chemical vapour deposition, low-pressure chemical vapour deposition, atomic layer deposition, and physical vapour deposition. Preferably, the multifunctional layer 204 is able to withstand various processes in the manufacture of the PV cell, including cleaning processes involving dipping in hydrofluoric acid. For example, the thickness of the multifunctional layer 204 is sufficient such that the multifunctional layer 204 remains in the final PV cell, and serves to reduce rear surface recombination and improve rear surface internal reflection in the PV cell.

In a preferred implementation, the multifunctional layer 204 comprises at least one chemical resistant dielectric material and at least one thermal resistant dielectric material. Typically, the thermal resistant dielectric material is formed, e.g. deposited or grown, first on the first side of the doped silicon substrate 202, and the chemical resistant dielectric material is then formed, e.g. deposited or grown, on the thermal resistant dielectric material. However, in different implementations, the multifunctional layer 204 can be a single layer, e.g. a dielectric material that is both thermally and chemically resistant, or a stack comprising multiple layers of dielectric materials which include, but are not limited to, amorphous silicon (a-Si), aluminium oxide (AlO_x), thermal silicon oxide (SiO_2), silicon oxide (SiO_x), silicon nitride (SiN_x), silicon oxynitride (SiO_xN_y), aluminium nitride (AlN_x), aluminum oxynitride (AlO_xN_y) and aluminium fluoride (AlF_x). All these dielectrics can also be doped with n-type or p-type dopants e.g. boron or phosphorous. An example stack may include AlO_x and

SiN_x, or AlO_x and SiO_x and may have a thickness of about 10 nanometers (nm) to 300 nm. It will be appreciated that the thickness may vary depending on, e.g. how much material is removed during the various manufacturing steps, and how much material is desired to remain in the final PV cell.

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Figure 2C shows a schematic diagram illustrating a sectional view of the silicon wafer obtained from step 106 of Figure 1. During this step, a second side 208 of the doped silicon substrate 202 is textured e.g. by alkaline etching using an alkaline substance such as potassium hydroxide, sodium hydroxide or tetramethylammonium hydroxide (TMAH). The texturing process leads to formation of a plurality of surface structures, e.g. pyramidal-shaped or random-shaped structures 209 with <111> orientation and typical height in the range of about 4 μm to 10 μm on the second side 208 of the doped silicon substrate 202. Such surface structures 209 can help to reduce the weighted surface reflection losses in the final PV cell from approximately 30% (before texturing) to about 10 to 12% (after texturing). The multifunctional layer 204 protects the first side 206 of the doped silicon substrate 202 during the texturing process.

In alternate embodiments, e.g. where the final solar cell may have a multicrystalline silicon substrate 202, the texturing process can be performed by standard acid texturing. Any relevant chemical can be used as a texturing agent, as will be understood by persons skilled in the art.

Figure 2D shows a schematic diagram illustrating a sectional view of the silicon wafer obtained from step 108 of Figure 1. After texturing as discussed above, in this example embodiment the second side 208 of the doped silicon substrate 202 undergoes high temperature p⁺-type doping, e.g. by boron diffusion using boron tribromide (BBr₃), to form a heavily-doped layer, e.g. an emitter layer, a back surface field or a front surface field, depending on the structure of the final solar cell. In this example, the heavily-doped layer is in the form of an emitter layer 210. The emitter layer 210 forms a p-n junction with the remaining portions of the doped silicon substrate 202 upon completion of the diffusion process. During the diffusion process, the multifunctional layer 204 serves as a protective layer to protect the first side 206 of the

doped silicon substrate 202, thereby enabling single-side processing of the silicon wafer solar cell.

It will be appreciated that the choice of the dopant-type and doping agent depends on the polarity of the doped silicon substrate 202. Here, for n-type silicon substrate, boron diffusion (p^+) is used to dope the second side 208. On the other hand, for p-type silicon substrate, phosphorus diffusion (n^+) may be used to dope the second side 208. Other substances may also be used as doping agent to form the p-type or n-type emitter layer 210, respectively, as will be understood by persons skilled in the art.

The emitter layer 210 can be a homogenous emitter or a selective emitter. In alternate embodiments, a homogenous emitter may be formed (although not limited to) using ion implantation, doped dielectric or laser doping, while a selective emitter may be formed (although not limited to) using laser doping, laser chemical processing or doped dielectric layer deposition. Preferably, the p-n junction has a surface doping of about $1 \times 10^{21} \text{ cm}^{-3}$ to $5 \times 10^{18} \text{ cm}^{-3}$ for n-type doped (e.g. phosphorous) emitter layer 210, and p-type doped (e.g. boron) emitter layer 210. The p-n junction may have a typical junction depth of about $0.2 \text{ }\mu\text{m}$ to $3 \text{ }\mu\text{m}$, resulting in sheet resistance of the emitter layer 210 to be in the range of 30 to 250 Ω/square .

Subsequently, the doped silicon substrate 202 together with the randomly-shaped structures 209, emitter layer 210 and multifunctional layer 204 are cleaned e.g. by dipping the wafer into hydrofluoric acid (HF) for about 10 seconds, as discussed above with respect to step 110 of Figure 1. The multifunctional layer 204 protects the first side 206 of the doped silicon substrate 202 during the cleaning process. With reference to Figures 2C and 2D, it will be appreciated that other texturing and/or cleaning techniques may be used, but in each case, the multifunctional dielectric layer acts as a protective mask for the first side 206 of the doped silicon substrate 202, thereby allowing single-side processing.

Figure 2E shows a schematic diagram illustrating a sectional view of the silicon wafer obtained from step 112 of Figure 1. As shown in Figure 2E, a plurality of cavities 212 are formed at the second side 208 of the doped silicon substrate 202. For example, the multifunctional layer 204 is patterned using laser-ablation to create lines of approximately $20 \text{ }\mu\text{m}$ to $3000 \text{ }\mu\text{m}$ wide or points with a diameter of approximately $20 \text{ }\mu\text{m}$.

μm to $3000\ \mu\text{m}$ on the multifunctional layer 204. The lines or openings in the multifunctional layer 204 are then wet-chemically etched and cleaned to remove the potential laser damage. In one implementation, a hydrofluoric acid (HF) dip is used to remove the glassy layer left after the laser ablation process. Then, a caustic etch using e.g. concentrated potassium hydroxide (KOH), sodium hydroxide (NaOH), tetramethylammonium hydroxide (TMAH), or another substance with similar properties as etching agent, is used to etch about $0.1\ \mu\text{m}$ to $5\ \mu\text{m}$ of the doped silicon substrate 202.

Figure 2F shows a schematic diagram illustrating a sectional view of silicon wafer obtained from step 114 of Figure 1. In this embodiment, in case of a silicon wafer solar cell with n-type silicon substrate (n-p⁺ solar cell), a line diffusion or point diffusion for localised back-surface field (BSF) can be provided using e.g. liquid/solid source diffusion, ion-implantation, doped dielectric, laser doping using spin-on technique or laser chemical processing. The back surface field in the this embodiment is n⁺ doped region 214 is formed at the first side 206 of doped silicon substrate 202 at the cavities 212 to serve as a localized back surface field 214, e.g. by phosphorous diffusion using phosphoryl chloride (POCl₃). In case of p-type silicon substrate 202 (p-n⁺ solar cell), the back surface field will be p⁺ doped region. This enables the formation of a passivated emitter and rear locally diffused (PERL) structure, which is suitable for either n-type or p-type wafer. In this case of a PERL cell the local doping/diffusion at the rear can assist in the collection of the majority charge carriers at the rear of the solar cells and reduce the recombination activity of this contact.

In an alternate embodiment with silicon wafer solar cell with p-type silicon substrate 202 (p-n⁺ solar cell), instead applying addition doping process for formation of localised back-surface field (as used in PERL structure), a full area or localized area aluminium 218 paste can be applied, e.g. by screen-printing, at the first side 206 of doped silicon substrate 202. After a thermal treatment, e.g. by industrial firing, the aluminium paste 214 can serve both as local back-surface field (BSF) and at the same time a rear-contact electrode in the resulting aluminium local back surface field solar cell (Al-LBSF solar cell). This alternative embodiment may be used for the manufacture of passivated emitter and rear contact (PERC) when the majority carriers are collected at

by a direct contact between the metal (e.g. Al) and the lightly doped silicon bulk without formation of local back surface field.

Figure 2G shows a schematic diagram illustrating a sectional view of the silicon wafer obtained from step 116 of Figure 1. As shown in Figure 2G, a coating 216, e.g. for front passivation and anti-reflection, is deposited on the emitter layer 210 adjacent the second side 208 of the doped silicon substrate 202. The passivation and anti-reflection coating 216 can be a single-layer or multi-layer (stack) coating comprising a dielectric material such as silicon nitride, aluminium oxide or silicon oxide. Typically, the deposition of the passivation and anti-reflection coating 216 can further reduce the weighted surface reflection losses in the PV cell from approximately 10-12% (textured but without coating) to about 1.5% to 2% (with coating).

Figure 2H shows a schematic diagram illustrating a sectional view of the silicon wafer obtained from step 118 of Figure 1. As shown in Figure 2H, a plurality of metal electrodes 218 are formed at the first side 206 of the doped silicon substrate 202. In one implementation, the metal electrodes 218 are formed by screen-printing. In alternate embodiments, the metal electrodes 218 can be formed using techniques that include, but are not limited to, physical vapor deposition, plating or inkjet printing.

Figure 2I shows a schematic diagram illustrating a sectional view of the silicon wafer obtained from step 120 of Figure 1. As shown in Figure 2I, a plurality of metal electrodes 220 are formed at the second side 208 of the doped silicon substrate 202. In one implementation, the metal electrodes 220 are formed by screen-printing. In alternate embodiments, the metal electrodes 220 can be formed using techniques that include, but are not limited to stencil-printing, physical vapor deposition, plating and inkjet printing, aerosol-printing.

A thermal treatment such as high-temperature firing step in a fast-firing furnace is carried out after the formation of the metal electrodes 218, 220. The multifunctional layer 204 again protects the first side 206 of the doped silicon substrate 202 during the thermal treatment.

As illustrated in Figures 2A to 2I, the multifunctional layer 204 in the example embodiments not only can serve as a texturing and diffusion mask, but also remains as the passivation layer in the final solar cell. The use of multifunctional layer is of course not limited to the solar cell structures in the embodiments discussed above (both example and alternative). For example, in another embodiment with a different structure, this multifunctional layer can be used preferentially for interdigitated back contact (IBC) cell and bifacial solar cells (p^+nn^+ or n^+pp^+ solar cells). The use of such a multifunctional layer in the method of manufacturing a silicon wafer solar cell according to the example embodiments can advantageously result in lower manufacturing costs while still resulting in a higher efficiency solar cell.

The multifunctional layer 204 as described above comprises dielectric materials that have both chemical and thermal resistant properties, thereby allowing it to protect the doped silicon substrate 202 during manufacturing and yet remains in the final PV cell to serve as the passivation layer. Figure 3 shows a column chart 300 illustrating dielectric thermal stability of an example multifunctional layer 204 for use in the method of the example embodiments after being subjected to various thermal treatments. Here, the multifunctional layer 204 is a dielectric stack comprising 30 nm of aluminium oxide and 70 nm of silicon nitride. The level of surface passivation of a material is quantified by the effective upper-limit surface recombination velocity ($S_{eff,max}$), where a lower value is indicative of better surface passivation.

Column 302 shows the reference surface passivation performance of the multifunctional layer as deposited, i.e. no thermal treatment. Column 304 shows the surface passivation performance of the multifunctional layer after being subjected to a thermal annealing in an inline diffusion furnace at a temperature above 900°C for about 40 minutes, and without using a doping source (e.g. H_3PO_4 based phosphorus doping). As can be seen from column 304, the surface passivation performance is similar to the reference surface passivation performance. No improvement or degradation of surface passivation is observed.

Column 306 shows the surface passivation performance of the multifunctional layer after being subjected to a thermal annealing in an inline diffusion furnace at a temperature above 900°C for about 40 minutes, and with a doping source (e.g. H_3PO_4

based phosphorus doping). The surface passivation is reduced significantly, probably due to a reaction between the phosphoric acid (H_3PO_4) and the dielectric stack.

Column 308 shows the surface passivation performance of the multifunctional layer after being subjected to a 70 Ω /square phosphoryl chloride tube diffusion (POCl_3) at a temperature of about 850°C for about 2 hours. The effective upper-limit surface recombination velocity ($S_{\text{eff,max}}$) decreases from the reference value to 16.7 cm/s after this thermal treatment. In other words, the surface passivation performance has improved, and both the thermal treatment and the exposure to phosphoryl chloride do not degrade the level of surface passivation provided by the multifunctional dielectric layer.

Column 310 shows the surface passivation performance of the multifunctional layer after being subjected to a standard industrial firing (fired) at a temperature above 800 °C for a few seconds. The upper-limit surface recombination velocity ($S_{\text{eff,max}}$) decreases to 7.5 cm/s, indicating a very good surface passivation.

Column 312 shows the surface passivation performance of the multifunctional layer after being subjected to a forming gas annealing (FGA) at about 450-500°C for 20-25 minutes. The upper-limit surface recombination velocity ($S_{\text{eff,max}}$) decreases to 4.7 cm/s, indicating excellent surface passivation.

As shown in Figure 3, the multifunctional layer as described can serve as a protective mask for high-temperature processing steps and retain high-quality passivation performance.

Figure 4 shows a flow chart 400 illustrating a method of manufacturing a photovoltaic cell according to a further embodiment. At step 402, a multifunctional layer comprising at least one dielectric material is formed on a first side of a doped substrate. At step 404, a second side of the doped substrate is textured, wherein the second side is the side of the doped substrate opposite to the first side, the multifunctional layer protecting the first side of the doped substrate during texturing. At step 406, a heavily-doped layer is formed adjacent the second side, the multifunctional layer protecting the first side of the doped substrate during the

formation of the heavily-doped layer. The multifunctional layer thereafter serves as a passivation layer.

Embodiments of the present invention provide a multifunctional layer that can
5 serve both as a surface passivation layer and optical film in the final PV cell (herein interchangeably referred to as solar cell), and as a protective mask during the solar cell manufacturing process. As a result, various process steps involving sacrificial mask formation and removal in the manufacturing of high-efficiency silicon wafer solar cells, and their associated costs, may be avoided. In other words, in addition to
10 being the surface passivation layer and optical film in the final solar cell, the multifunctional layer can serve as diffusion and texturing mask.

It will be appreciated by a person skilled in the art that numerous variations and/or modifications may be made to the present invention as shown in the specific
15 embodiments without departing from the spirit or scope of the invention as broadly described. The present embodiments are, therefore, to be considered in all respects to be illustrative and not restrictive.

CLAIMS

1. A method of manufacturing a photovoltaic cell, the method comprising
5 the steps of:

forming a multifunctional layer comprising at least one dielectric material on a first side of a doped substrate;

texturing a second side of the doped substrate, wherein the second side is the side of the doped substrate opposite to the first side, the multifunctional layer
10 protecting the first side of the doped substrate during texturing; and

forming a heavily-doped layer adjacent the second side, the multifunctional layer protecting the first side of the doped substrate during the formation of the heavily-doped layer,

wherein the multifunctional layer thereafter serves as a passivation layer.

2. The method as claimed in claim 1, wherein the heavily-doped layer comprises one of an emitter layer, a back surface field, or a front surface field.

3. The method as claimed in claim 1 or 2, wherein the at least one
20 dielectric material is both chemical resistant and thermal resistant.

4. The method as claimed in claim 1 or 2, wherein the multifunctional layer comprises at least one chemical resistant dielectric material and at least one thermal resistant dielectric material.

5. The method as claimed in claim 4, wherein the chemical resistant dielectric material comprises one selected from a group consisting of silicon nitride, silicon oxide, thermal silicon oxide, silicon oxynitride, aluminium oxide, aluminium nitride, aluminium oxynitride, aluminium fluoride, amorphous silicon and doped
30 equivalents.

6. The method as claimed in claim 4, wherein the thermal resistant dielectric material comprises one selected from a group consisting of silicon nitride, silicon oxide, thermal silicon oxide, silicon oxynitride, aluminium oxide, aluminium

nitride, aluminium oxynitride, aluminium fluoride, amorphous silicon and doped equivalents.

7. The method as claimed in any one of claims 4 to 6, wherein forming
5 the multifunctional layer comprises the steps of:

forming the at least one thermal resistant dielectric material on the first side
of the doped substrate; and

forming the at least one chemical resistant dielectric material on the
deposited at least one thermal resistant dielectric material.

8. The method as claimed in any one of the preceding claims, wherein
forming the multifunctional layer comprises using one selected from a group
consisting of chemical vapor deposition techniques, atomic layer depositions,
physical vapour depositions and growth techniques.

9. The method as claimed in any one of the preceding claims, wherein
texturing the second side of the doped substrate comprises forming a plurality of
surface structures on the second side of the doped substrate.

10. The method as claimed in any one of the preceding claims, wherein
forming the heavily-doped layer comprises using one selected from a group
consisting of ion implantation, laser doping, laser chemical processing, doped dielectric
layer deposition and diffusion.

11. The method as claimed in any one of the preceding claims, further
comprising the steps of:

forming a passivation and anti-reflection coating on the heavily-doped layer;
and

forming electrodes adjacent the multifunctional layer and the heavily-doped
layer respectively.

12. The method as claimed in claim 11, wherein forming the electrodes
comprises using one selected from a group consisting of screen-printing, stencil-
printing, physical vapor deposition, plating and inkjet printing, aerosol-printing.

13. A solar cell manufactured using the method as claimed in any one of the preceding claims.

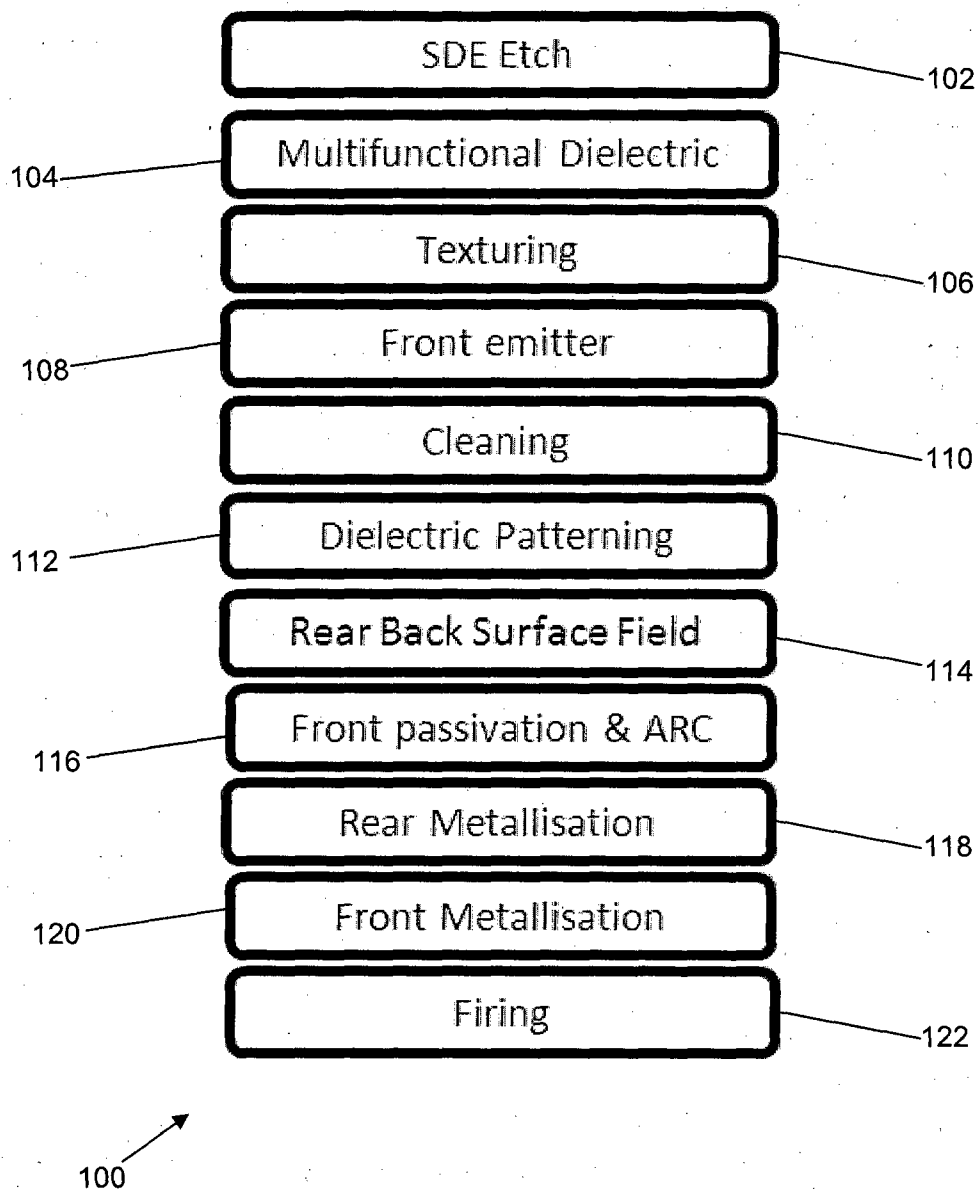


Figure 1

Figure 2A

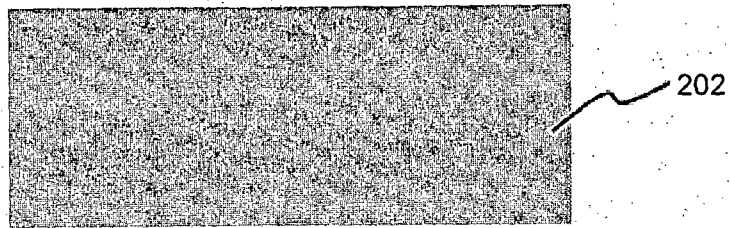


Figure 2B

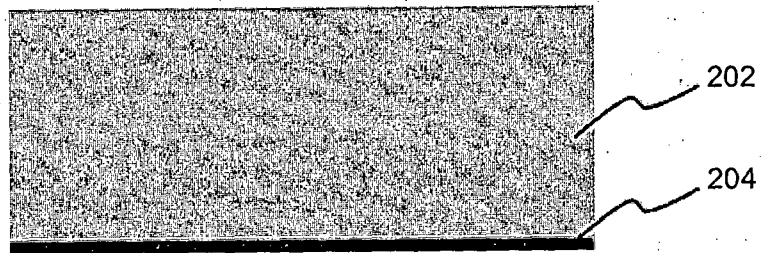
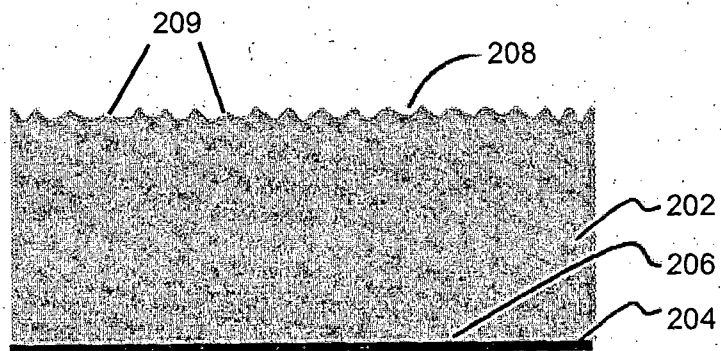


Figure 2C



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Figure 2D

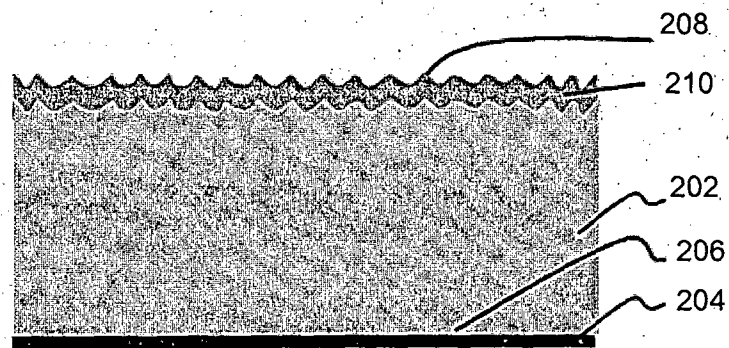


Figure 2E

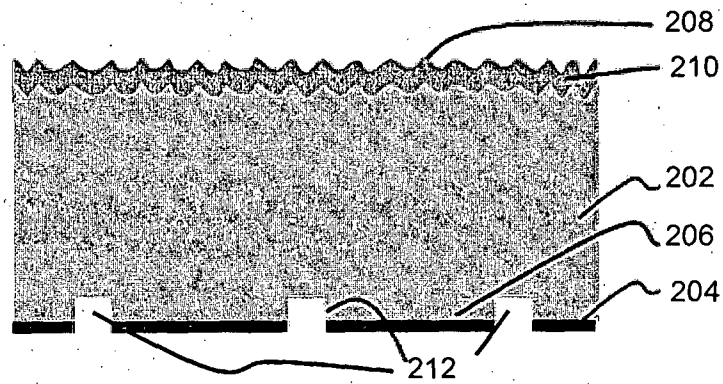


Figure 2F

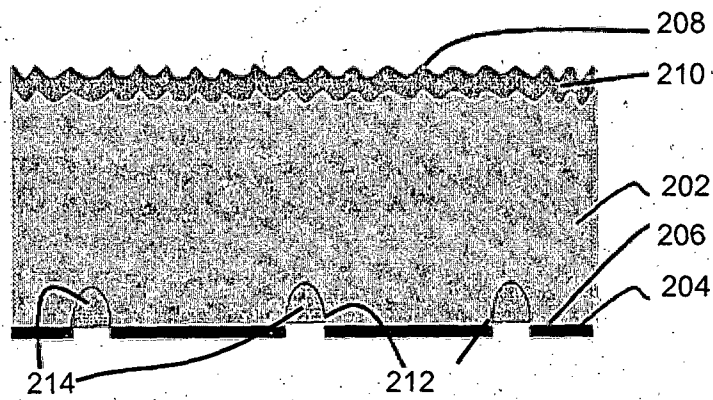


Figure 2G

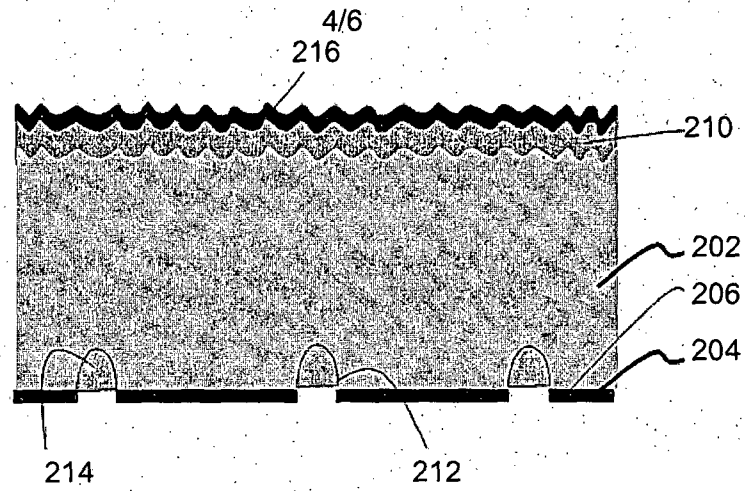


Figure 2H

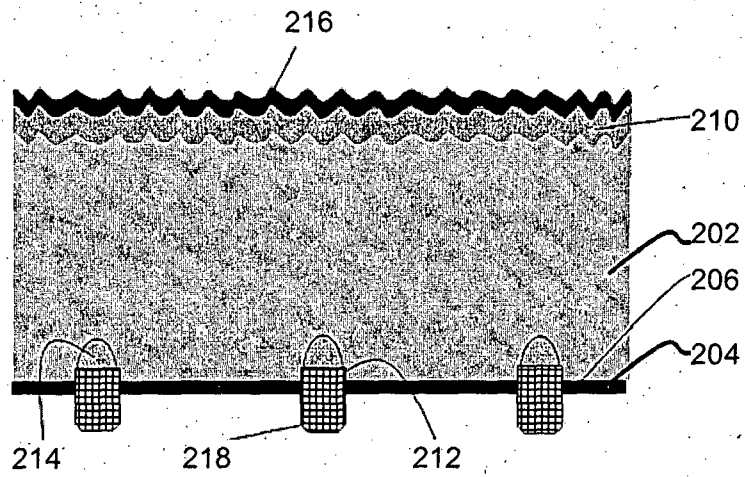
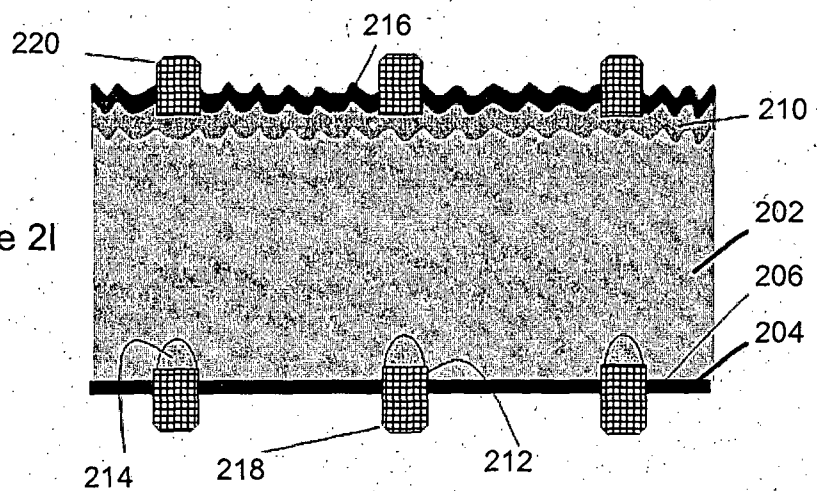


Figure 2I



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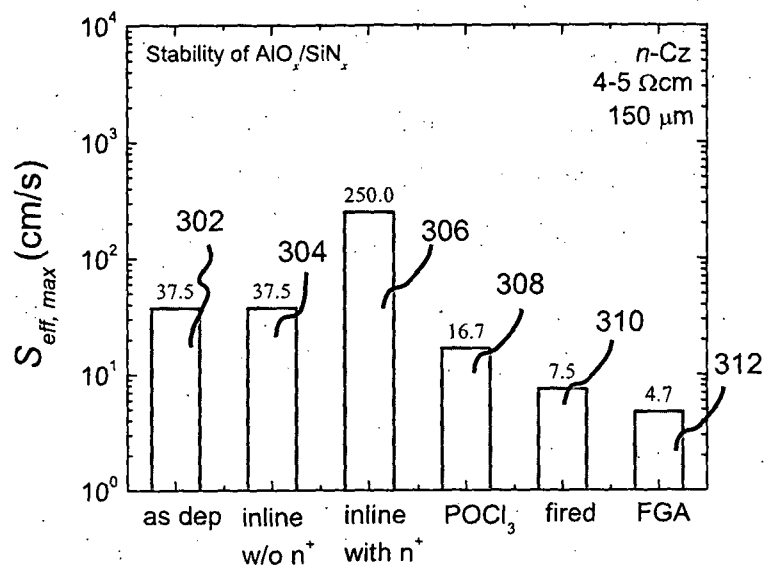


Figure 3

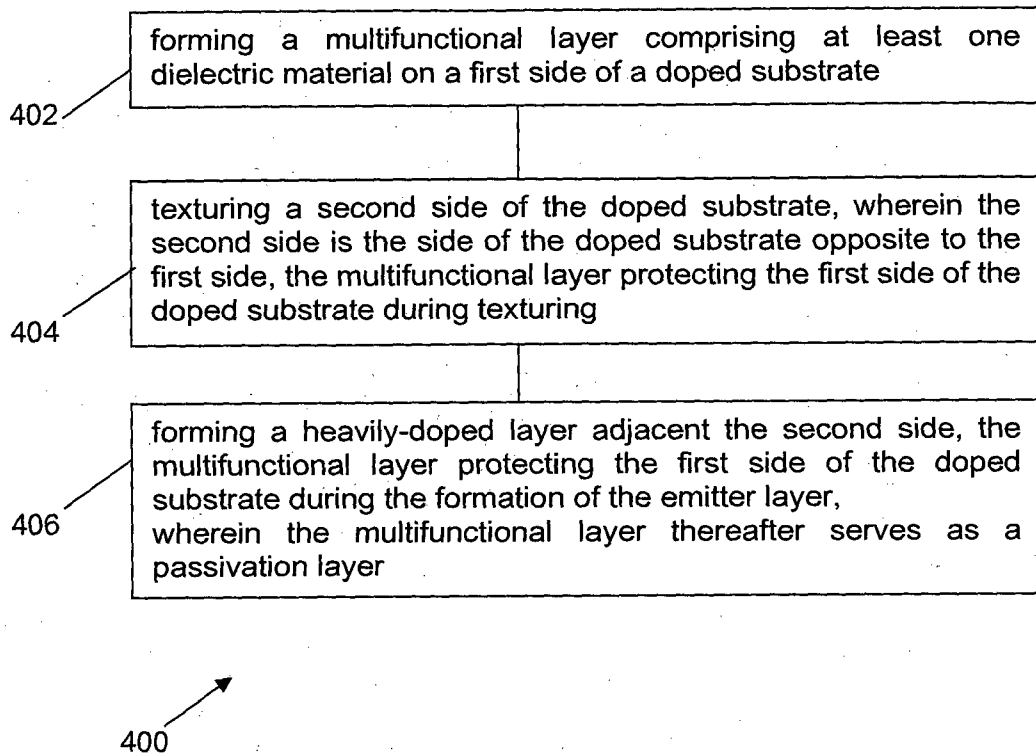


Figure 4

INTERNATIONAL SEARCH REPORT

International application No.

PCT/SG2013/000527

A. CLASSIFICATION OF SUBJECT MATTER

H01L 31/18 (2006.01) H01L 33/44 (2010.01) H01L 21/31 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Databases: WPI, EPDOC, INSPEC & keywords: Solar cell, PV, photo-voltaic, photo-electric, dielectric, passivation, oxide, nitride, coating, layer, film, deposit, back-surface-field, BSF, front-surface-field, FSF, dop, substrate, texture, pattern, contact, electrode, metal and similar terms.

Google search & Keywords: rear passivation, solar cell, BSF, FSF, emitter.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	Documents are listed in the continuation of Box C	



Further documents are listed in the continuation of Box C



See patent family annex

* Special categories of cited documents:	
"A" document defining the general state of the art which is not considered to be of particular relevance	"I" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"E" earlier application or patent but published on or after the international filing date	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O" document referring to an oral disclosure, use, exhibition or other means	"&" document member of the same patent family
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search
7 March 2014

Date of mailing of the international search report
07 March 2014

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INTERNATIONAL SEARCH REPORT		International application No.
C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		PCT/SG2013/000527
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010/0236613 A1 (LEE ET AL.) 23 September 2010 Figs. 6A-6F, paragraphs 0037-0040, Fig. 7 and the associated text	1-13
A	Seo J. W. et al., "Investigation of Passivation Properties of Thermal Al ₂ O ₃ and SiN _x Stack Layers Deposited on Solar Grade p-Type CZ Si Wafers", 37th IEEE Photovoltaic Specialists Conference (PVSC), 19-24 June 2011, pages 001512-001514. Fig. 2 and the associated text	4-8
A	Rentsch J., "Technology Route Towards Industrial Application of Rear Passivated Silicon Solar Cells", IEEE 4th World Conference on Photovoltaic Energy conversion, May 2006, volume 1, pages 1008 - 1011. Figs. 1-2 and the associated text	4-8, 11-12

Form PCT/ISA/210 (fifth sheet) (July 2009)

INTERNATIONAL SEARCH REPORT Information on patent family members		International application No. PCT/SG2013/000527	
This Annex lists known patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.			
Patent Document/s Cited in Search Report		Patent Family Member/s	
Publication Number	Publication Date	Publication Number	Publication Date
US 2010/0236613 A1	23 Sep 2010	US 2010236613 A1	23 Sep 2010
		US 8288645 B2	16 Oct 2012
		US 2012211063 A1	23 Aug 2012
End of Annex			
Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001. Form PCT/ISA/210 (Family Annex)(July 2009)			