(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
24 November 2011 (24.11.2011)

PCT

(10) International Publication Number
WO 2011/145467 A1

(51) International Patent Classification:
H01L 29/786 (2006.01) *H01L 21/336* (2006.01)
G02F 1/1368 (2006.01) *H01L 51/50* (2006.01)
G09F 9/30 (2006.01) *H05B 33/14* (2006.01)
H01L 21/316 (2006.01)

(21) International Application Number:
PCT/JP2011/060682

(22) International Filing Date:
27 April 2011 (27.04.2011)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
2010-116952 21 May 2010 (21.05.2010) JP

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ,

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(54) Title: SEMICONDUCTOR DEVICE

FIG. 1A

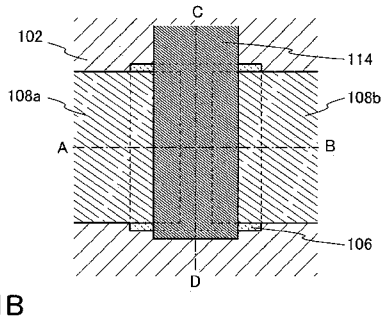


FIG. 1B

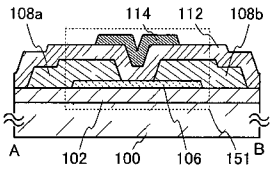
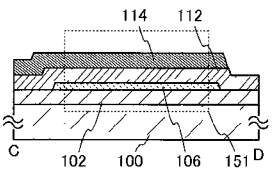


FIG. 1C



(57) Abstract: An object of the present invention is to manufacture a semiconductor device where fluctuation in electrical characteristics is small and reliability is high in a transistor in which an oxide semiconductor is used. An insulating layer from which oxygen is released by heating is used as a base insulating layer of an oxide semiconductor layer which forms a channel. Oxygen is released from the base insulating layer, whereby oxygen deficiency in the oxide semiconductor layer and an interface state between the base insulating layer and the oxide semiconductor layer can be reduced. Thus, a semiconductor device where fluctuation in electrical characteristics is small and reliability is high can be manufactured.

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TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

DESCRIPTION

SEMICONDUCTOR DEVICE

TECHNICAL FIELD

[0001]

The present invention relates to a semiconductor device and a manufacturing method thereof.

[0002]

In this specification, a semiconductor device means a general device which can function by utilizing semiconductor characteristics, and an electrooptic device, a semiconductor circuit, and an electronic device are all semiconductor devices.

BACKGROUND ART

[0003]

A technique by which transistors are formed using semiconductor thin films formed over a substrate having an insulating surface has been attracting attention. Such transistors are applied to a wide range of electronic devices such as an integrated circuit (IC) and an image display device (display device). As semiconductor thin films applicable to the transistors, silicon-based semiconductor materials have been widely used, but oxide semiconductors have been attracting attention as alternative materials.

[0004]

For example, disclosed is a transistor whose active layer is formed using an amorphous oxide containing indium (In), gallium (Ga), and zinc (Zn) and having an electron carrier concentration of lower than 10^{18} /cm^3 (see Patent Document 1).

[0005]

A transistor including an oxide semiconductor is known to have a problem of low reliability because of high possibility of fluctuation in electrical characteristics, although the transistor including an oxide semiconductor can be operated at higher speed than a transistor including amorphous silicon and can be manufactured more easily than a transistor including polycrystalline silicon. For example, the threshold voltage of the transistor fluctuates between before and after a bias-temperature stress

test (BT test). Note that in this specification, a "threshold voltage" refers to a gate voltage which is needed to turn on a transistor. "Gate voltage" refers to a potential difference between a source electrode and a gate electrode when the potential of the source electrode is used as a reference potential.

[Reference]

[0006]

[Patent Document 1] Japanese Published Patent Application No. 2006-165528

DISCLOSURE OF INVENTION

[0007]

Fluctuation in the threshold voltage due to a BT test of the transistor including an oxide semiconductor reduces the reliability of the transistor including an oxide semiconductor. Therefore, an object of one embodiment of the present invention is to improve the reliability of a semiconductor device including an oxide semiconductor.

[0008]

One embodiment of the present invention is a semiconductor device or a method thereof based on the following technical idea: an insulating layer from which oxygen is released by heating is formed as an insulating layer which is a base layer of an oxide semiconductor layer (also referred to as a base insulating layer).

[0009]

"Being possible to release oxygen by heating" means that the released amount of oxygen molecules (also referred to as O_2) is greater than or equal to $1 \times 10^{18}/cm^3$, preferably greater than or equal to $3 \times 10^{20}/cm^3$ in thermal desorption spectroscopy (TDS).

[0010]

By supplying oxygen from the base insulating layer to the oxide semiconductor layer, an interface state between the base insulating layer and the oxide semiconductor layer can be reduced. As a result, it is possible to sufficiently suppress trapping of charge or the like, which can be generated due to the operation of a semiconductor device, or the like, at an interface between the base insulating layer and the oxide

semiconductor layer.

[0011]

Further, charge is generated due to oxygen deficiency in the oxide semiconductor layer in some cases. Oxygen deficiency in the oxide semiconductor layer generally becomes donors and electrons which are carriers are generated. As a result, a threshold voltage of a transistor shifts in a negative direction. Oxygen is sufficiently released from the base insulating layer, whereby oxygen deficiency in the oxide semiconductor layer which causes the shift of the threshold voltage in a negative direction can be compensated by oxygen supplied from the base insulating layer.

[0012]

In other words, when oxygen deficiency is generated in the oxide semiconductor layer, it becomes difficult to suppress trapping of charge at the interface between the base insulating layer and the oxide semiconductor layer; however, by providing the insulating layer from which oxygen is released by heating as the base insulating layer, an interface state and oxygen deficiency in the oxide semiconductor layer can be reduced and an adverse effect of trapping of charge at the interface between the oxide semiconductor layer and the base insulating layer can be reduced.

[0013]

Thus, the advantageous effect of one embodiment of the present invention is attributed to the base insulating layer from which oxygen is released by heating.

[0014]

Since the trapping of a charge at the interface between the base insulating layer and the oxide semiconductor layer can be suppressed, which is described above as the advantageous effect, an off-state current of the transistor including an oxide semiconductor can be increased and malfunctions such as fluctuation in the threshold voltage can be suppressed, and further the reliability of the semiconductor device can be improved.

[0015]

Note that the insulating layer from which oxygen is released by heating preferably has an enough thickness with respect to the oxide semiconductor layer. This is because when the thickness of the insulating layer from which oxygen is released by heating is smaller than that of the oxide semiconductor layer, oxygen is not

sufficiently supplied to the oxide semiconductor layer in some cases.

[0016]

Another embodiment of the present invention is a semiconductor device including a base insulating layer, an oxide semiconductor layer over the base insulating layer, a source electrode and a drain electrode which are electrically connected to the oxide semiconductor layer, a gate insulating layer part of which is in contact with the oxide semiconductor layer, and a gate electrode over the gate insulating layer. The base insulating layer is an insulating layer from which oxygen is released by heating. More preferably, an insulating layer from which oxygen is released by heating is used as the gate insulating layer.

[0017]

In the above structure, the base insulating layer can be a single layer or a stacked layer formed using one or more of silicon oxide, silicon oxynitride, silicon nitride oxide, and aluminum oxide. The gate insulating layer can be a single layer or a stacked layer formed using one or more of silicon oxide, silicon oxynitride, aluminum oxide, and hafnium oxide.

[0018]

In this specification, silicon oxynitride refers to a substance that contains more oxygen than nitrogen and for example, silicon oxynitride includes oxygen, nitrogen, silicon, and hydrogen at concentrations ranging from greater than or equal to 50 atomic% and less than or equal to 70 atomic%, greater than or equal to 0.5 atomic% and less than or equal to 15 atomic%, greater than or equal to 25 atomic% and less than or equal to 35 atomic%, and greater than or equal to 0 atomic% and less than or equal to 10 atomic%, respectively. Further, silicon nitride oxide refers to a substance that contains more nitrogen than oxygen and for example, silicon nitride oxide includes oxygen, nitrogen, silicon, and hydrogen at concentrations ranging from greater than or equal to 5 atomic% and less than or equal to 30 atomic%, greater than or equal to 20 atomic% and less than or equal to 55 atomic%, greater than or equal to 25 atomic% and less than or equal to 35 atomic%, and greater than or equal to 10 atomic% and less than or equal to 25 atomic%, respectively. Note that rates of oxygen, nitrogen, silicon, and hydrogen fall within the above ranges in the cases where measurement is performed

using Rutherford backscattering spectrometry (RBS) or hydrogen forward scattering spectrometry (HFS). In addition, the total of the percentages of the constituent elements does not exceed 100 atomic%.

[0019]

In the above structure, an insulating layer (also referred to as a protective insulating layer) which covers the gate insulating layer and the gate electrode may be provided. The protective insulating layer is preferably an insulating layer from which oxygen is released by heating. A conductive layer may be provided below the oxide semiconductor layer.

[0020]

In the above, the channel length L of the transistor, which depends on the distance between the source electrode and the drain electrode, can be greater than or equal to 10 nm and less than or equal to 10 μm, for example, 0.1 μm to 0.5 μm. It is needless to say that the channel length L may be greater than or equal to 1 μm. The channel width W may be greater than or equal to 10 μm.

[0021]

According to one embodiment of the present invention, by providing an insulating layer from which oxygen is released by heating as a base insulating layer of an oxide semiconductor layer, a transistor which has a small off-state current, small variation in the threshold voltage, and stable electrical characteristics can be provided.

[0022]

Alternatively, according to one embodiment of the present invention, a semiconductor device which includes a transistor having favorable electrical characteristics and high reliability can be provided.

BRIEF DESCRIPTION OF DRAWINGS

[0023]

FIGS. 1A to 1C are a top view and cross-sectional views illustrating an example of a semiconductor device according to one embodiment of the present invention.

FIGS. 2A and 2B are cross-sectional views each illustrating an example of a

semiconductor device according to one embodiment of the present invention.

FIGS. 3A to 3E are cross-sectional views illustrating an example of a manufacturing process of a semiconductor device according to one embodiment of the present invention.

FIGS. 4A to 4E are cross-sectional views illustrating an example of a manufacturing process of a semiconductor device according to one embodiment of the present invention.

FIGS. 5A to 5E are cross-sectional views illustrating an example of a manufacturing process of a semiconductor device according to one embodiment of the present invention.

FIGS. 6A to 6C are diagrams each illustrating one mode of a semiconductor device according to one embodiment of the present invention.

FIG. 7 is a cross-sectional view illustrating one mode of a semiconductor device according to one embodiment of the present invention.

FIG. 8 is a cross-sectional view illustrating one mode of a semiconductor device according to one embodiment of the present invention.

FIG. 9 is a cross-sectional view illustrating one mode of a semiconductor device according to one embodiment of the present invention.

FIGS. 10A to 10F are diagrams each illustrating an electronic appliance as a semiconductor device according to one embodiment of the present invention.

FIGS. 11A and 11B are graphs each showing TDS spectra of a silicon oxide layer formed using one embodiment of the present invention.

FIG. 12 is a cross-sectional view illustrating one mode of a semiconductor device according to one embodiment of the present invention.

FIG. 13 is a graph showing drain current (Ids)-gate voltage (Vgs) measurement results of a semiconductor device manufactured using one embodiment of the present invention.

FIGS. 14A and 14B are graphs each showing Ids-Vgs measurement results before and after a BT test of a semiconductor device manufactured using one embodiment of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

[0024]

Hereinafter, embodiments of the present invention will be described in detail with reference to the drawings. Note that the present invention is not limited to the following description, and it will be easily understood by those skilled in the art that modes and details disclosed herein can be modified in various ways without departing from the spirit and the scope of the present invention. Thus, the present invention should not be construed as being limited to the following description of the embodiments. In describing structures of the present invention with reference to the drawings, the same reference numerals are used in common for the same portions in different drawings. Note that the same hatch pattern is applied to similar parts, and the similar parts are not especially denoted by reference numerals in some cases.

[0025]

Note that the ordinal numbers such as "first" and "second" in this specification are used for convenience and do not denote the order of steps or the stacking order of layers. In addition, the ordinal numbers in this specification do not denote particular names which specify the present invention.

[0026]

(Embodiment 1)

In this embodiment, one embodiment of a semiconductor device and a manufacturing method thereof will be described with reference to FIGS. 1A to 1C, FIGS. 2A and 2B, FIGS. 3A to 3E, FIGS. 4A to 4E, and FIGS. 5A to 5E.

[0027]

FIGS. 1A to 1C are a top view and cross-sectional views of a transistor 151 which is a top-gate top-contact type as an example of a semiconductor device according to one embodiment of the present invention. Here, FIG. 1A is a top view, FIG. 1B is a cross-sectional view along A-B of FIG. 1A, and FIG. 1C is a cross-sectional view along C-D of FIG. 1A. Note that in FIG. 1A, some of components of the transistor 151 (for example, a gate insulating layer 112) are omitted for brevity.

[0028]

The transistor 151 in FIGS. 1A to 1C includes an insulating layer 102, an oxide semiconductor layer 106, a source electrode 108a, a drain electrode 108b, the gate insulating layer 112, and a gate electrode 114 over a substrate 100.

[0029]

As a material of the insulating layer 102, silicon oxide, silicon oxynitride, aluminum oxide, a mixed material of any of them, or the like may be used. Alternatively, the insulating layer 102 may be formed using a stacked layer of the above material and silicon oxide, silicon nitride, silicon oxynitride, silicon nitride oxide, aluminum oxide, aluminum nitride, a mixed material of any of them, or the like. For example, when the insulating layer 102 has a stacked-layer structure of a silicon nitride layer, a silicon nitride oxide layer, an aluminum oxide layer, or an aluminum nitride layer, and a silicon oxide layer, entry of moisture and hydrogen from the substrate 100 or the like to the transistor 151 can be prevented. In the case where the insulating layer 102 is formed to have a stacked-layer structure, an oxide layer of silicon oxide, silicon oxynitride, aluminum oxide, a mixed material of any of them, or the like is preferably formed on a side where the insulating layer 102 is in contact with the oxide semiconductor layer 106. Note that the insulating layer 102 functions as a base layer of the transistor 151. The insulating layer 102 is an insulating layer from which oxygen is released by heating. "Releasing oxygen by heating" means that the released amount of O_2 is greater than or equal to $1 \times 10^{18}/cm^3$, preferably greater than or equal to $3 \times 10^{20}/cm^3$ in TDS analysis.

[0030]

As a material used for the oxide semiconductor layer, a four-component metal oxide material such as an In-Sn-Ga-Zn-O-based material; a three-component metal oxide material such as an In-Ga-Zn-O-based material, an In-Sn-Zn-O-based material, an In-Al-Zn-O-based material, a Sn-Ga-Zn-O-based material, an Al-Ga-Zn-O-based material, or a Sn-Al-Zn-O-based material; a two-component metal oxide material such as an In-Zn-O-based material, a Sn-Zn-O-based material, an Al-Zn-O-based material, a Zn-Mg-O-based material, a Sn-Mg-O-based material, an In-Mg-O-based material, or an In-Ga-O-based material; an In-O-based material; a Sn-O-based material; a Zn-O-based material; or the like can be used. In addition, any of the above materials may contain silicon oxide. Here, for example, an In-Ga-Zn-O-based material means an oxide layer containing indium (In), gallium (Ga), and zinc (Zn), and there is no particular limitation on the composition ratio thereof. Further, the In-Ga-Zn-O-based material may contain

an element other than In, Ga, and Zn. As an example, in the case where an In-Zn-O-based material is used, any of the following is employed: In/Zn is greater than or equal to 0.5 and less than or equal to 50 in an atomic ratio, preferably In/Zn is greater than or equal to 1 and less than or equal to 20 in an atomic ratio, or more preferably In/Zn is greater than or equal to 1.5 and less than or equal to 15 in an atomic ratio. When the atomic ratio of Zn is in the above range, the field effect mobility of the transistor can be improved. Here, when the atomic ratio of the compound is In:Zn:O = X:Y:Z, the relation of $Z > 1.5X + Y$ is preferably satisfied.

[0031]

For the oxide semiconductor layer, a thin film using a material represented by the chemical formula, $InMO_3(ZnO)_m$ ($m > 0$), can be used. Here, M represents one or more metal elements selected from Ga, Al, Mn, and Co. For example, M can be Ga, Ga and Al, Ga and Mn, Ga and Co, or the like.

[0032]

An interface state between the insulating layer 102 and the oxide semiconductor layer 106 and oxygen deficiency in the oxide semiconductor layer 106 can be reduced. By the above reduction in the interface state, the fluctuation in threshold voltage before and after a BT test can be reduced.

[0033]

The gate insulating layer 112 can have a structure similar to that of the insulating layer 102, and is preferably an insulating layer from which oxygen is released by heating. Note that a material having a high dielectric constant, such as hafnium oxide or aluminum oxide, may be used for the gate insulating layer 112 considering the function of the gate insulating layer of the transistor. Alternatively, a stacked layer of silicon oxide, silicon oxynitride, or silicon nitride and a material having a high dielectric constant, such as hafnium oxide or aluminum oxide, may be used considering a gate withstand voltage and a state of an interface of the oxide semiconductor layer.

[0034]

A protective insulating layer may further be provided over the transistor 151. The protective insulating layer can have a structure similar to that of the insulating layer 102. In order to electrically connect the source electrode 108a or the drain electrode

108b and a wiring, an opening may be formed in the insulating layer 102, the gate insulating layer 112, and the like. A second gate electrode may further be provided below the oxide semiconductor layer 106. Note that it is not always necessary but preferable to process the oxide semiconductor layer 106 into an island shape.

[0035]

FIGS. 2A and 2B illustrate cross-sectional structures of transistors having different structures from that of the transistor 151.

[0036]

A transistor 152 in FIG. 2A is the same as the transistor 151 in that it includes the insulating layer 102, the oxide semiconductor layer 106, the source electrode 108a, the drain electrode 108b, the gate insulating layer 112, and the gate electrode 114. The differences between the transistor 152 and the transistor 151 are the positions where the oxide semiconductor layer 106 is connected to the source electrode 108a and the drain electrode 108b. That is, in the transistor 152, the source electrode 108a and the drain electrode 108b are in contact with bottom portions of the oxide semiconductor layer 106. The other components are similar to those of the transistor 151 in FIGS. 1A to 1C.

[0037]

The transistor 153 in FIG. 2B is the same as the transistor 151 and the transistor 152 in that it includes the insulating layer 102, the gate insulating layer 112, the gate electrode 114, the source electrode 108a, and the drain electrode 108b. The transistor 153 is different from the transistor 151 and the transistor 152 in that a channel region 126, a source region 122a, and a drain region 122b are formed in the oxide semiconductor layer in the same plane. The source region 122a and the drain region 122b are connected to the source electrode 108a and the drain electrode 108b, respectively, with a protective insulating layer 124 interposed therebetween. Note that in FIG. 2B, the gate insulating layer 112 is provided only under the gate electrode 114; however, one embodiment of the present invention is not limited thereto. For example, the gate insulating layer 112 may be provided to cover the oxide semiconductor layer including the channel region 126, the source region 122a, and the drain region 122b.

[0038]

Examples of a manufacturing process of the transistor in FIGS. 1A to 1C will be described below with reference to FIGS. 3A to 3E and FIGS. 4A to 4E.

[0039]

To begin with, an example of a manufacturing process of the transistor 151 in FIGS. 1A to 1C will be described with reference to FIGS. 3A to 3E.

[0040]

First, the insulating layer 102 is formed over the substrate 100 (see FIG. 3A). The insulating layer 102 is an insulating layer from which oxygen is released by heating.

[0041]

There is no particular limitation on the property of a material and the like of the substrate 100 as long as the material has heat resistance enough to withstand at least heat treatment to be performed later. For example, a glass substrate, a ceramic substrate, a quartz substrate, a sapphire substrate, or the like can be used as the substrate 100. Alternatively, a single crystal semiconductor substrate or a polycrystalline semiconductor substrate made of silicon, silicon carbide, or the like, a compound semiconductor substrate made of silicon germanium or the like, an SOI substrate, or the like may be used as the substrate 100. Still alternatively, any of these substrates further provided with a semiconductor element may be used as the substrate 100.

[0042]

A flexible substrate may be used as the substrate 100. In that case, a transistor is formed directly on the flexible substrate. Note that as a method for forming a transistor over a flexible substrate, there is also a method in which, after a non-flexible substrate is used as the substrate 100 and a transistor is formed thereover, the transistor is separated from the substrate and transferred to a flexible substrate. In that case, a separation layer is preferably provided between the substrate 100 and the transistor.

[0043]

As a formation method of the insulating layer 102, a plasma CVD method or a sputtering method can be employed, for example. The insulating layer from which oxygen is released by heating is preferably formed by a sputtering method. As a material of the insulating layer 102, silicon oxide, silicon oxynitride, aluminum oxide, a mixed material of any of them, or the like may be used. Alternatively, the insulating layer 102 may be formed using a stacked layer of the above material and silicon oxide, silicon nitride, silicon oxynitride, silicon nitride oxide, aluminum oxide, aluminum

nitride, a mixed material of any of them, or the like. In the case where the insulating layer 102 is formed to have a stacked-layer structure, an oxide layer of silicon oxide, silicon oxynitride, aluminum oxide, a mixed material of any of them, or the like is preferably formed on a side where the insulating layer 102 is in contact with the oxide semiconductor layer 106. The total thickness of the insulating layer 102 is preferably 20 nm or more, more preferably 100 nm or more. When the thick insulating layer 102 is formed, the amount of oxygen released from the insulating layer 102 can be increased.

[0044]

In order to form the insulating layer from which oxygen is released by heating by a sputtering method, in the case where oxygen or a mixed gas of oxygen and a rare gas (such as helium, neon, argon, krypton, or xenon) is used as a film formation gas, the proportion of oxygen is preferably set higher. For example, the concentration of oxygen in the whole gas is preferably set to be higher than or equal to 6 % and lower than 100 %.

[0045]

For example, a silicon oxide film is formed by an RF sputtering method under the following conditions: quartz (preferably synthetic quartz) is used as a target; the substrate temperature is higher than or equal to 30 °C and lower than or equal to 450 °C (preferably higher than or equal to 70 °C and lower than or equal to 200 °C); the distance between the substrate and the target (the T-S distance) is greater than or equal to 20 mm and less than or equal to 400 mm (preferably greater than or equal to 40 mm and less than or equal to 200 mm); the pressure is higher than or equal to 0.1 Pa and lower than or equal to 4 Pa (preferably higher than or equal to 0.2 Pa and lower than or equal to 1.2 Pa); the high-frequency power is higher than or equal to 0.5 kW and lower than or equal to 12 kW (preferably higher than or equal to 1 kW and lower than or equal to 5 kW); and the proportion of $O_2/(O_2 + Ar)$ in the film formation gas is higher than or equal to 1 % and lower than or equal to 100 % (preferably higher than or equal to 6 % and lower than or equal to 100 %). Note that a silicon target may be used as the target instead of the quartz (preferably synthetic quartz) target. As the film formation gas, oxygen or a mixed gas of oxygen and argon is used.

[0046]

Next, an oxide semiconductor layer is formed over the insulating layer 102 and then is processed to form the oxide semiconductor layer 106 having an island shape (see FIG. 3B).

[0047]

For example, the oxide semiconductor layer can be formed by a sputtering method, a vacuum evaporation method, a pulse laser deposition method, a CVD method, or the like. The thickness of the oxide semiconductor layer is preferably greater than or equal to 3 nm and less than or equal to 50 nm. This is because when the oxide semiconductor layer is too thick (e.g., 100 nm or more), there is a possibility that the short channel effect has a large influence and the transistor with a small size is normally on. Here, "normally on" means a state where a channel exists without applying voltage to a gate electrode and current flows through the transistor. Note that the insulating layer 102 and the oxide semiconductor layer are preferably formed successively without exposure to the air.

[0048]

For example, the oxide semiconductor layer is formed by a sputtering method using an In-Ga-Zn-O-based oxide target.

[0049]

As the In-Ga-Zn-O-based oxide target, for example, an oxide target having a composition ratio of In_2O_3:Ga_2O_3:ZnO = 1:1:1 [molar ratio] can be used. Note that it is not necessary to limit the material and the composition ratio of the target to the above. For example, an oxide target having a composition ratio of In_2O_3:Ga_2O_3:ZnO = 1:1:2 [molar ratio] can be used.

[0050]

The relative density of the oxide target is higher than or equal to 90 % and lower than or equal to 100 %, preferably higher than or equal to 95 % and lower than or equal to 99.9 %. This is because, with the use of the oxide target with a high relative density, the dense oxide semiconductor layer can be formed.

[0051]

The film formation may be performed in a rare gas atmosphere, an oxygen

atmosphere, a mixed atmosphere containing a rare gas and oxygen, or the like. Moreover, it is preferably an atmosphere using a high-purity gas in which impurities such as hydrogen, water, a hydroxyl group, and hydride are sufficiently removed so that entry of hydrogen, water, a hydroxyl group, and hydride into the oxide semiconductor layer can be prevented.

[0052]

For example, the oxide semiconductor layer can be formed as follows.

[0053]

An example of the film formation conditions is as follows: the distance between the substrate and the target is 60 mm; the pressure is 0.4 Pa; the direct-current (DC) power is 0.5 kW; and the film formation atmosphere is a mixed atmosphere containing argon and oxygen (the proportion of the oxygen flow is 33 %). Note that a pulse DC sputtering method is preferable because powder substances (also referred to as particles or dust) generated in film formation can be reduced and the film thickness can be uniform.

[0054]

In this case, when the substrate temperature is higher than or equal to 100 °C and lower than or equal to 450 °C, preferably higher than or equal to 150 °C and lower than or equal to 250 °C, oxygen is released from the insulating layer 102, whereby oxygen deficiency in the oxide semiconductor layer and an interface state between the insulating layer 102 and the oxide semiconductor layer can be reduced.

[0055]

Note that before the oxide semiconductor layer 106 is formed by a sputtering method, a substance attached to a surface where the oxide semiconductor layer is to be formed (e.g., a surface of the insulating layer 102) may be removed by reverse sputtering in which a rare gas is introduced and plasma is generated. Here, the reverse sputtering is a method by which ions collide with a surface to be processed so that the surface is modified, in contrast to normal sputtering by which ions collide with a sputtering target. An example of a method for making ions collide with a surface to be processed is a method in which high-frequency voltage is applied to the surface side in an argon atmosphere so that plasma is generated near an object to be processed. Note

that an atmosphere of nitrogen, helium, oxygen, or the like may be used instead of an argon atmosphere.

[0056]

The oxide semiconductor layer 106 can be processed by etching after a mask having a desired shape is formed over the oxide semiconductor layer. The mask can be formed by a method such as photolithography. Alternatively, the mask may be formed by an ink-jet method or the like.

[0057]

For the etching of the oxide semiconductor layer, either wet etching or dry etching may be employed. It is needless to say that both of them may be employed in combination.

[0058]

After that, heat treatment (first heat treatment) is preferably performed on the oxide semiconductor layer. By the first heat treatment, excessive hydrogen (including water and a hydroxyl group) in the oxide semiconductor layer can be removed and a structure of the oxide semiconductor layer can be ordered. The temperature of the first heat treatment is higher than or equal to 100 °C and lower than or equal to 650 °C or lower than the strain point of the substrate, preferably higher than or equal to 250 °C and lower than or equal to 600 °C. The atmosphere of the first heat treatment is an oxidizing gas atmosphere or an inert gas atmosphere.

[0059]

Note that an inert gas atmosphere is preferably an atmosphere that contains nitrogen or a rare gas as its main component and does not contain water, hydrogen, and the like. For example, the purity of nitrogen or a rare gas such as helium, neon, or argon introduced into a heat treatment apparatus is set to 6N (99.9999 %) or more, preferably 7N (99.99999 %) or more (i.e., the impurity concentration is 1 ppm or lower, preferably 0.1 ppm or lower). The inert gas atmosphere is an atmosphere that contains an inert gas as its main component and contains a reactive gas of 10 ppm or lower.

[0060]

Note that the oxidizing gas is oxygen, ozone, nitrous oxide, or the like, and it is preferable that the oxidizing gas does not contain water, hydrogen, and the like. For

example, the purity of oxygen, ozone, or nitrous oxide introduced into a heat treatment apparatus is set to 6N (99.9999 %) or higher, preferably 7N (99.99999 %) or higher (i.e., the impurity concentration is 1 ppm or lower, preferably 0.1 ppm or lower). As the oxidizing gas atmosphere, an atmosphere in which an oxidizing gas is mixed with an inert gas may be used, and the oxidizing gas of at least 10 ppm is contained.

[0061]

By the first heat treatment, oxygen is released from the insulating layer 102, whereby the oxygen deficiency in the oxide semiconductor layer 106 and the interface state between the insulating layer 102 and the oxide semiconductor layer 106 can be reduced. By the above reduction in the interface state, the fluctuation in threshold voltage before and after a BT test can be reduced. Further, in general, it is known that the oxygen deficiency in the oxide semiconductor layer becomes donors and the source for generating electrons which are carriers. By the generation of electrons in the oxide semiconductor layer 106, the threshold voltage of the transistor 151 shifts to a negative direction, so that the transistor 151 tends to be normally on. By embedding the oxygen deficiency in the oxide semiconductor layer 106, the shift of the threshold voltage in a negative direction can be suppressed.

[0062]

The heat treatment can be performed in such a manner that, for example, an object to be processed is introduced into an electric furnace in which a resistance heating element or the like is used and heated at 350 °C in a nitrogen atmosphere for an hour. During the heat treatment, the oxide semiconductor layer is not exposed to the air to prevent the entry of water and hydrogen.

[0063]

Note that a heat treatment apparatus is not limited to an electric furnace, and may include a device for heating an object to be processed by heat conduction or heat radiation from a medium such as a heated gas. For example, a rapid thermal anneal (RTA) apparatus such as a gas rapid thermal anneal (GRTA) apparatus or a lamp rapid thermal anneal (LRTA) apparatus can be used. An LRTA apparatus is an apparatus for heating an object to be processed by radiation of light (electromagnetic waves) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon

arc lamp, a high pressure sodium lamp, or a high pressure mercury lamp. A GRTA apparatus is an apparatus for heat treatment using a high temperature gas. As the high temperature gas, used is an inert gas which does not react with an object to be processed in heat treatment, such as nitrogen or a rare gas like argon.

[0064]

For example, as the first heat treatment, GRTA treatment may be performed as follows. The object to be processed is put in an inert gas atmosphere that has been heated, heated for several minutes, and then taken out of the inert gas atmosphere. GRTA treatment enables high-temperature heat treatment in a short time. Moreover, GRTA treatment can be employed even when the temperature exceeds the upper temperature limit of the object. Note that the inert gas atmosphere may be switched to an atmosphere containing an oxidizing gas during the treatment. This is because by performing the first heat treatment in an atmosphere containing the oxidizing gas, oxygen deficiency in the oxide semiconductor layer 106 can be embedded and defect levels in an energy gap due to oxygen deficiency can be reduced.

[0065]

The above heat treatment (first heat treatment) can be referred to as dehydration treatment, dehydrogenation treatment, or the like because of its advantageous effect of removing hydrogen, water, and the like. In addition, the above heat treatment can also be referred to as treatment for supplying oxygen because of its advantageous effect of supplying oxygen from the insulating layer, a heat treatment atmosphere, or the like. The dehydration treatment, dehydrogenation treatment, or treatment for supplying oxygen can be performed at the timing, for example, after the oxide semiconductor layer is processed to have an island shape. Such dehydration treatment, dehydrogenation treatment, or treatment for supplying oxygen may be performed once or plural times.

[0066]

Note that the case is described here in which after the oxide semiconductor layer 106 is processed to have an island shape, the first heat treatment is performed; however, one embodiment of the present invention is not limited thereto. The oxide semiconductor layer 106 may be processed after the first heat treatment.

[0067]

Next, a conductive layer for forming the source electrode and the drain electrode (including a wiring formed in the same layer as the source electrode and the drain electrode) is formed over the insulating layer 102 and the oxide semiconductor layer 106 and processed to form the source electrode 108a and the drain electrode 108b (see FIG. 3C). The channel length L of the transistor depends on the minimum distance between the edges of the source electrode 108a and the drain electrode 108b which are formed here.

[0068]

As the conductive layer used for the source electrode 108a and the drain electrode 108b, for example, a metal layer containing an element selected from Al, Cr, Cu, Ta, Ti, Mo, and W, or a metal nitride layer containing any of the above elements as its component (e.g., a titanium nitride layer, a molybdenum nitride layer, or a tungsten nitride layer) can be used. A high-melting-point metal layer of Ti, Mo, W, or the like or a metal nitride layer of any of these elements (a titanium nitride layer, a molybdenum nitride layer, or a tungsten nitride layer) may be stacked on one of or both a bottom side and a top side of a low-melting point and low-resistance metal layer of Al, Cu, or the like.

[0069]

Alternatively, the conductive layer used for the source electrode 108a and the drain electrode 108b may be formed using a conductive metal oxide. As the conductive metal oxide, an indium oxide (In_2O_3 or the like), a tin oxide (SnO_2 or the like), a zinc oxide (ZnO or the like), an indium oxide-tin oxide alloy (In_2O_3-SnO_2 or the like, which is abbreviated to ITO), an indium oxide-zinc oxide alloy (In_2O_3-ZnO or the like), or any of these metal oxide materials containing a silicon oxide can be used.

[0070]

The conductive layer can be processed by etching with the use of a resist mask. Ultraviolet, a KrF laser light, an ArF laser light, or the like is preferably used for light exposure for forming a resist mask for the etching.

[0071]

In the case where light exposure is performed so that the channel length L is less than 25 nm, the light exposure at the time of forming the resist mask is preferably performed using, for example, extreme ultraviolet having an extremely short

wavelength of several nanometers to several tens of nanometers. In the light exposure using extreme ultraviolet, the resolution is high and the focus depth is large. Thus, the channel length L of the transistor formed later can be reduced, whereby the operation speed of a circuit can be increased.

[0072]

Etching may be performed with the use of a resist mask formed using a so-called multi-tone mask. A resist mask formed using a multi-tone mask has a plurality of thicknesses and can be further changed in shape by ashing; thus, such a resist mask can be used in a plurality of etching steps for different patterns. Therefore, a resist mask for at least two kinds of patterns can be formed using a multi-tone mask, resulting in simplification of the process.

[0073]

Note that in etching of the conductive layer, part of the oxide semiconductor layer 106 is etched, so that the oxide semiconductor layer having a groove (a recessed portion) is formed in some cases.

[0074]

After that, by plasma treatment using a gas such as oxygen, ozone, or nitrous oxide, a surface of an exposed portion of the oxide semiconductor layer 106 may be oxidized and oxygen deficiency may be embedded. In the case where plasma treatment is performed, the gate insulating layer 112 which is to be in contact with part of the oxide semiconductor layer 106 is preferably formed without being exposed to the air, following the plasma treatment.

[0075]

Next, the gate insulating layer 112 is formed so as to cover the source electrode 108a and the drain electrode 108b and to be in contact with part of the oxide semiconductor layer 106 (see FIG. 3D).

[0076]

The gate insulating layer 112 can have a structure similar to that of the insulating layer 102. Note that a material having a high dielectric constant, such as hafnium oxide or aluminum oxide, may be used for the gate insulating layer 112 considering the function of the gate insulating layer of the transistor. Alternatively, a stacked layer of silicon oxide, silicon oxynitride, or silicon nitride and a material having

a high dielectric constant, such as hafnium oxide or aluminum oxide, may be used considering a gate withstand voltage and a state of an interface of the oxide semiconductor layer. The total thickness of the gate insulating layer 112 is preferably greater than or equal to 1 nm and less than or equal to 300 nm, more preferably greater than or equal to 5 nm and less than or equal to 50 nm. The larger the thickness of the gate insulating layer is, the more easily a short channel effect occurs; thus, the threshold voltage tends to shift to a negative direction. In addition, it is found that when the thickness of the gate insulating layer is less than or equal to 5 nm, leakage due to a tunnel current is increased.

[0077]

Second heat treatment is preferably performed after the gate insulating layer 112 is formed. The second heat treatment is performed at a temperature of higher than or equal to 250 °C and lower than or equal to 700 °C, preferably higher than or equal to 350 °C and lower than or equal to 600 °C or lower than the strain point of the substrate.

[0078]

The second heat treatment may be performed in an atmosphere of an oxidizing gas or an inert gas. Note that it is preferable that water, hydrogen, and the like be not contained in the atmosphere of an oxidizing gas or an inert gas. Further, the purity of the gas introduced into a heat treatment apparatus is preferably 6N (99.9999 %) or higher, more preferably 7N (99.99999 %) or higher (that is, the impurity concentration is 1 ppm or lower, preferably 0.1 ppm or lower).

[0079]

The second heat treatment is performed while the oxide semiconductor layer 106 and the gate insulating layer 112 are in contact with each other. Thus, oxygen which is one of main components of the oxide semiconductor can be supplied from the gate insulating layer 112 containing oxygen to the oxide semiconductor layer 106. Accordingly, oxygen deficiency in the oxide semiconductor layer 106 and the interface state between the oxide semiconductor layer and the gate insulating layer 112 can be reduced. At the same time, defects in the gate insulating layer 112 can also be reduced.

[0080]

Note that there is no particular limitation on the timing of the second heat treatment as long as it is after the gate insulating layer 112 is formed. For example, the second heat treatment may be performed after the gate electrode 114 is formed.

[0081]

Then, the gate electrode 114 is formed (see FIG. 3E). The gate electrode 114 can be formed using a metal material such as molybdenum, titanium, tantalum, tungsten, aluminum, copper, neodymium, or scandium, nitride of any of these metal materials, or an alloy material which contains any of these metal materials as its main component. Note that the gate electrode 114 may have a single-layer structure or a stacked-layer structure.

[0082]

Through the above process, the transistor 151 is formed.

[0083]

Next, an example of a manufacturing process of the transistor 152 in FIG. 2A will be described with reference to FIGS. 4A to 4E.

[0084]

First, the insulating layer 102 is formed over the substrate 100 (see FIG. 4A). As the insulating layer 102 of the transistor 151, the insulating layer 102 is an insulating layer from which oxygen is released by heating.

[0085]

Next, a conductive layer for forming the source electrode and the drain electrode (including a wiring formed in the same layer as the source electrode and the drain electrode) is formed over the insulating layer 102 and processed to form the source electrode 108a and the drain electrode 108b (see FIG. 4B).

[0086]

Next, an oxide semiconductor layer is formed over the insulating layer 102 so as to be connected to the source electrode 108a and the drain electrode 108b and then is processed to form the oxide semiconductor layer 106 having an island shape (see FIG. 4C). After that, first heat treatment similar to that performed on the transistor 151 may be performed.

[0087]

Next, the gate insulating layer 112 is formed so as to be in contact with the

oxide semiconductor layer 106 and part of the source electrode 108a and the drain electrode 108b and cover the source electrode 108a, the drain electrode 108b, and the oxide semiconductor layer 106 (see FIG. 4D). After that, second heat treatment similar to that performed on the transistor 151 may be performed.

[0088]

Then, the gate electrode 114 is formed (see FIG. 4E).

[0089]

Through the above-described process, the transistor 152 is formed.

[0090]

When charge is trapped at the interface of the oxide semiconductor layer, the threshold voltage of the transistor shifts. For example, when positive charge is trapped on the back channel side, the threshold voltage of the transistor shifts in a negative direction. As one of factors of such charge trapping, the model where cations (or atoms which are sources of the cations) travel and are trapped can be supposed. In one embodiment of the present invention, the interface states between the oxide semiconductor layer and the insulating layer 102 and between the oxide semiconductor layer and the gate insulating layer 112 are reduced by the insulating layer from which oxygen is released by heating, so that it is possible to reduce charge trapping which may be caused in the above model; therefore, the shift of the threshold voltage of the transistor can be suppressed.

[0091]

An example of a manufacturing process of the transistor 153 in FIG. 2B will be described with reference to FIGS. 5A to 5E.

[0092]

First, the insulating layer 102 is formed over the substrate 100 (see FIG. 5A). The insulating layer 102 is an insulating layer from which oxygen is released by heating.

[0093]

Next, an oxide semiconductor layer is formed over the insulating layer 102 and processed to form the oxide semiconductor layer 106 having an island shape (see FIG. 5B). After that, first heat treatment similar to that performed on the transistor 151 may be performed.

[0094]

Next, the gate insulating layer 112 and the gate electrode 114 are formed and processed to have similar patterns by photolithography (see FIG. 5C). At this time, the gate electrode 114 may be processed and then the gate insulating layer 112 may be processed using the gate electrode 114 as a mask. After that, second heat treatment similar to that performed on the transistor 151 may be performed.

[0095]

Next, the resistance of the oxide semiconductor layer 106 is reduced using the gate electrode 114 as a mask, so that the source region 122a and the drain region 122b are formed. A region under the gate electrode where the resistance is not reduced becomes the channel region 126 (see FIG. 5D). As a method for reducing the resistance, argon plasma treatment, hydrogen plasma treatment, ammonia plasma treatment, and the like can be given. At this time, the channel length L of the transistor is determined by the width of the gate electrode. By patterning using the gate electrode as the mask in this manner, the source region and the drain region do not overlap with the gate electrode and parasitic capacitance is not generated; therefore, the operation speed of the transistor can be increased.

[0096]

Next, the protective insulating layer 124 is formed and an opening is provided in a region of the protective insulating layer 124, which is overlapped with the source region 122a and the drain region 122b. A conductive layer for forming the source electrode and the drain electrode (including a wiring formed in the same layer as the source and drain electrodes) is formed and processed to form the source electrode 108a and the drain electrode 108b (see FIG. 5E).

[0097]

Through the above process, the transistor 153 is formed.

[0098]

Thus, a semiconductor device including an oxide semiconductor and having stable electrical characteristics can be provided. Therefore, a semiconductor device with high reliability can be provided.

[0099]

The structures, the methods, and the like described in this embodiment can be

combined as appropriate with any of the structures, the methods, and the like described in the other embodiments.

[0100]

(Embodiment 2)

A semiconductor device (also referred to as a display device) having a display function can be manufactured using the transistor an example of which is described in Embodiment 1. Some or all driver circuits including the transistors can be formed over a substrate where a pixel portion is formed, whereby a system-on-panel can be obtained.

[0101]

In FIG. 6A, a sealant 205 is provided to surround a pixel portion 202 provided over a first substrate 201, and the pixel portion 202 is sealed with the sealant 205 and a second substrate 206. In FIG. 6A, a scan line driver circuit 204 and a signal line driver circuit 203 each are formed using a single crystal semiconductor layer or a polycrystalline semiconductor layer over a substrate prepared separately, and mounted in a region different from the region surrounded by the sealant 205 over the first substrate 201. Various signals and potentials are supplied to the signal line driver circuit 203 and the scan line driver circuit 204 each of which is separately formed, and the pixel portion 202, from flexible printed circuits (FPCs) 218a and 218b.

[0102]

In FIGS. 6B and 6C, the sealant 205 is provided to surround the pixel portion 202 and the scan line driver circuit 204 which are provided over the first substrate 201. The second substrate 206 is provided over the pixel portion 202 and the scan line driver circuit 204. Thus, the pixel portion 202 and the scan line driver circuit 204 are sealed together with a display element, by the first substrate 201, the sealant 205, and the second substrate 206. In FIGS. 6B and 6C, the signal line driver circuit 203 is formed using a single crystal semiconductor layer or a polycrystalline semiconductor layer over a substrate prepared separately, and mounted in a region different from the region surrounded by the sealant 205 over the first substrate 201. In FIGS. 6B and 6C, various signals and potentials are supplied to the signal line driver circuit 203 which is separately formed, the scan line driver circuit 204, and the pixel portion 202, from an FPC 218.

[0103]

Although FIGS. 6B and 6C each show the example in which the signal line driver circuit 203 is formed separately and mounted on the first substrate 201, the present invention is not limited to this structure. The scan line driver circuit may be separately formed and then mounted, or only part of the signal line driver circuit or part of the scan line driver circuit may be separately formed and then mounted.

[0104]

Note that a method for connecting a separately formed driver circuit is not particularly limited, and a chip on glass (COG) method, a wire bonding method, a tape automated bonding (TAB) method, or the like can be used. FIG. 6A shows an example in which the signal line driver circuit 203 and the scan line driver circuit 204 are mounted by a COG method. FIG. 6B shows an example in which the signal line driver circuit 203 is mounted by a COG method. FIG. 6C shows an example in which the signal line driver circuit 203 is mounted by a TAB method.

[0105]

The display device includes in its category a panel in which a display element is sealed, and a module in which an IC such as a controller is mounted on the panel.

[0106]

Note that a display device in this specification means an image display device, a display device, or a light source (including a lighting device). The display device also includes the following modules in its category: a module to which a connector such as an FPC, a TAB tape, or a TCP is attached; a module having a TAB tape or a TCP at the tip of which a printed wiring board is provided; and a module in which an IC is directly mounted on a display element by a COG method.

[0107]

The pixel portion and the scan line driver circuit provided over the first substrate include a plurality of transistors and any of the transistors, the examples of which are described in Embodiment 1, can be applied.

[0108]

As the display element provided in the display device, a liquid crystal element (also referred to as a liquid crystal display element) or a light-emitting element (also referred to as a light-emitting display element) can be used. The light-emitting

element includes, in its category, an element whose luminance is controlled by a current or voltage, and specifically includes, in its category, an inorganic electroluminescent (EL) element, an organic EL element, and the like. Furthermore, a display medium whose contrast is changed by an electric effect, such as electronic ink, can be used.

[0109]

One embodiment of the semiconductor device is described with reference to FIG. 7, FIG. 8, and FIG. 9. FIG. 7, FIG. 8, and FIG. 9 correspond to cross-sectional views taken along line M-N in FIG. 6B.

[0110]

As illustrated in FIG. 7, FIG. 8, and FIG. 9, the semiconductor device includes a connection terminal electrode 215 and a terminal electrode 216. The connection terminal electrode 215 and the terminal electrode 216 are electrically connected to a terminal included in the FPC 218 through an anisotropic conductive layer 219.

[0111]

The connection terminal electrode 215 is formed of the same conductive layer as a first electrode layer 230. The terminal electrode 216 is formed of the same conductive layer as a source electrode and a drain electrode of transistors 210 and 211.

[0112]

Each of the pixel portion 202 and the scan line driver circuit 204 provided over the first substrate 201 includes a plurality of transistors. In FIG. 7, FIG. 8, and FIG. 9, the transistor 210 included in the pixel portion 202 and the transistor 211 included in the scan line driver circuit 204 are shown as an example.

[0113]

In this embodiment, any of the transistors described in Embodiment 1 can be applied to the transistors 210 and 211. Fluctuation in the electrical characteristics of the transistors 210 and 211 is suppressed and the transistors 210 and 211 are electrically stable. As described above, a semiconductor device with high reliability as the semiconductor devices in this embodiment in FIG. 7, FIG. 8, and FIG. 9 can be obtained.

[0114]

The transistor 210 provided in the pixel portion 202 is electrically connected to the display element to form a display panel. A variety of display elements can be used as the display element as long as display can be performed.

[0115]

An example of a liquid crystal display device using a liquid crystal element as a display element is illustrated in FIG. 7. In FIG. 7, a liquid crystal element 213 is a display element including the first electrode layer 230, a second electrode layer 231, and a liquid crystal layer 208. Note that insulating layers 232 and 233 serving as alignment layers are provided so that the liquid crystal layer 208 is interposed therebetween. The second electrode layer 231 is formed on the second substrate 206 side. The first electrode layer 230 and the second electrode layer 231 are stacked with the liquid crystal layer 208 interposed therebetween.

[0116]

A spacer 235 is a columnar spacer obtained by selective etching of an insulating layer and is provided in order to control the thickness (a cell gap) of the liquid crystal layer 208. Alternatively, a spherical spacer may be used.

[0117]

In the case where a liquid crystal element is used as the display element, a thermotropic liquid crystal, a low-molecular liquid crystal, a high-molecular liquid crystal, a polymer dispersed liquid crystal, a ferroelectric liquid crystal, an anti-ferroelectric liquid crystal, or the like can be used. Such a liquid crystal material exhibits a cholesteric phase, a smectic phase, a cubic phase, a chiral nematic phase, an isotropic phase, or the like depending on conditions.

[0118]

Alternatively, a liquid crystal exhibiting a blue phase for which an alignment layer is unnecessary may be used. A blue phase is one of liquid crystal phases generated just before a cholesteric phase changes into an isotropic phase while temperature of cholesteric liquid crystal is increased. Since the blue phase appears only in a narrow temperature range, a liquid crystal composition in which a chiral material is mixed is used for the liquid crystal layer in order to improve the temperature range. The liquid crystal composition which includes a liquid crystal exhibiting a blue phase and a chiral agent has a short response time of 1 msec or less, has optical isotropy, which makes the alignment process unneeded, and has a small viewing angle dependence. In addition, since an alignment layer does not need to be provided and rubbing treatment is unnecessary, electrostatic discharge damage caused by the rubbing

treatment can be prevented and defects and damage of the liquid crystal display device can be reduced in the manufacturing process. Thus, productivity of the liquid crystal display device can be increased.

[0119]

The specific resistivity of the liquid crystal material is 1×10^9 Ω·cm or more, preferably 1×10^{11} Ω·cm or more, more preferably 1×10^{12} Ω·cm or more. Note that the specific resistivity in this specification is measured at 20 °C.

[0120]

The size of a storage capacitor provided in the liquid crystal display device is set considering the leakage current of the transistor provided in the pixel portion or the like so that charge can be held for a predetermined period. Since the transistor including a high-purity oxide semiconductor layer is used, a storage capacitor having capacitance which is 1/3 or less, preferably 1/5 or less with respect to a liquid crystal capacitance of each pixel is sufficient to be provided.

[0121]

In the transistor used in this embodiment, which uses a highly-purified oxide semiconductor layer, the off-state current can be made small. Therefore, an electrical signal such as an image signal can be held for a long period, and a writing interval can be set long when the power is on. Consequently, frequency of refresh operation can be reduced, which leads to an effect of suppressing power consumption.

[0122]

The field-effect mobility of the transistor including a highly-purified oxide semiconductor layer used in this embodiment can be high, whereby high-speed operation is possible. Thus, by using the transistor in a pixel portion of the liquid crystal display device, a high-quality image can be provided. In addition, since the transistors can be separately provided in a driver circuit portion and a pixel portion over one substrate, the number of components of the liquid crystal display device can be reduced.

[0123]

For the liquid crystal display device, a twisted nematic (TN) mode, an in-plane-switching (IPS) mode, a fringe field switching (FFS) mode, an axially

symmetric aligned micro-cell (ASM) mode, an optical compensated birefringence (OCB) mode, a ferroelectric liquid crystal (FLC) mode, an antiferroelectric liquid crystal (AFLC) mode, or the like can be used.

[0124]

A normally black liquid crystal display device such as a transmissive liquid crystal display device utilizing a vertical alignment (VA) mode is preferable. The vertical alignment mode is one of methods of controlling alignment of liquid crystal molecules of a liquid crystal display panel. The vertical alignment mode is a mode in which liquid crystal molecules are aligned vertically to a panel surface when voltage is not applied. Some examples are given as the vertical alignment mode. For example, a multi-domain vertical alignment (MVA) mode, a patterned vertical alignment (PVA) mode, an ASV mode, and the like can be given. Moreover, it is possible to use a method called domain multiplication or multi-domain design, in which a pixel is divided into some regions (subpixels) and molecules are aligned in different directions in their respective regions.

[0125]

In the display device, a black matrix (a light-blocking layer), an optical member (an optical substrate) such as a polarizing member, a retardation member, or an anti-reflection member, and the like are provided as appropriate. For example, circular polarization may be employed by using a polarizing substrate and a retardation substrate. In addition, a backlight, a side light, or the like may be used as a light source.

[0126]

In addition, with the use of a plurality of light-emitting diodes (LEDs) as a backlight, a time-division display method (a field-sequential driving method) can be employed. With the field-sequential driving method, color display can be performed without using a color filter.

[0127]

As a display method in the pixel portion, a progressive method, an interlace method, or the like can be employed. Color elements controlled in a pixel at the time of color display are not limited to three colors: R, G, and B (R, G, and B correspond to red, green, and blue respectively). For example, R, G, B, and W (W corresponds to white), or R, G, B, and one or more of yellow, cyan, magenta, and the like can be used.

The sizes of display regions may be different between respective dots of color elements. Note that the present invention is not limited to the application to a display device for color display but can also be applied to a display device for monochrome display.

[0128]

Alternatively, as the display element included in the display device, a light-emitting element utilizing an EL element can be used.

[0129]

In an organic EL element, by application of voltage to a light-emitting element, electrons and holes are separately injected from a pair of electrodes into a layer containing a light-emitting organic compound, and current flows. The carriers (electrons and holes) are recombined, and thus the light-emitting organic compound is excited. The light-emitting organic compound returns to a ground state from the excited state, thereby emitting light. Owing to such a mechanism, such a light-emitting element is referred to as a current-excitation light-emitting element.

[0130]

The inorganic EL elements are classified according to their element structures into a dispersion-type inorganic EL element and a thin-film inorganic EL element. A dispersion-type inorganic EL element has a light-emitting layer where particles of a light-emitting material are dispersed in a binder, and its light emission mechanism is donor-acceptor recombination type light emission that utilizes a donor level and an acceptor level. A thin-film inorganic EL element has a structure where a light-emitting layer is sandwiched between dielectric layers, which are further sandwiched between electrodes, and its light emission mechanism is localized type light emission that utilizes inner-shell electron transition of metal ions. Note that an example of an organic EL element as a light-emitting element is described here.

[0131]

In order to extract light emitted from the light-emitting element, it is acceptable as long as at least one of a pair of electrodes is transparent. Then a transistor and a light-emitting element are formed over a substrate. The light-emitting element can have any of the following structure: a top emission structure in which light is extracted through the surface opposite to the substrate; a bottom emission structure in which light is extracted through the surface on the substrate side; or a dual emission structure in

which light is extracted through the surface opposite to the substrate and the surface on the substrate side.

[0132]

An example of a light-emitting device using a light-emitting element as a display element is illustrated in FIG. 8. A light-emitting element 243 which is a display element is electrically connected to the transistor 210 provided in the pixel portion 202. The structure of the light-emitting element 243 is not limited to the stacked-layer structure including the first electrode layer 230, an electroluminescent layer 241, and the second electrode layer 231, which is illustrated in FIG. 8. The structure of the light-emitting element 243 can be changed as appropriate depending on a direction in which light is extracted from the light-emitting element 243, or the like.

[0133]

A partition wall 240 can be formed using an organic insulating material or an inorganic insulating material. It is particularly preferable that the partition wall 240 be formed using a photosensitive resin material to have an opening portion over the first electrode layer 230 so that a sidewall of the opening portion is formed as a tilted surface with continuous curvature.

[0134]

The electroluminescent layer 241 may be formed with either a single layer or a stacked layer of a plurality of layers.

[0135]

A protective layer may be formed over the second electrode layer 231 and the partition wall 240 in order to prevent entry of oxygen, hydrogen, moisture, carbon dioxide, or the like into the light-emitting element 243. As the protective layer, a silicon nitride layer, a silicon nitride oxide layer, a diamond-like carbon (DLC) layer, an aluminum oxide layer, an aluminum nitride layer, or the like can be formed. In a space sealed with the first substrate 201, the second substrate 206, and the sealant 205, a filler 244 is provided and tightly sealed. It is preferable that the light-emitting element be packaged (sealed) with a protective film (such as a laminate film or an ultraviolet curable resin film) or a cover material with high air-tightness and little degasification so that the light-emitting element is not exposed to the outside air, in this manner.

[0136]

As the filler 244, an ultraviolet curable resin or a thermosetting resin can be used as well as an inert gas such as nitrogen or argon, and polyvinyl chloride (PVC), acrylic, polyimide, an epoxy resin, a silicone resin, polyvinyl butyral (PVB), ethylene vinyl acetate (EVA), or the like can be used. For example, nitrogen may be used for the filler.

[0137]

If needed, an optical film, such as a polarizing plate, a circularly polarizing plate (including an elliptically polarizing plate), a retardation plate (a quarter-wave plate or a half-wave plate), or a color filter, may be provided as appropriate on a light-emitting surface of the light-emitting element. Further, the polarizing plate or the circularly polarizing plate may be provided with an anti-reflection layer. For example, anti-glare treatment by which reflected light can be diffused by projections and depressions on the surface so as to reduce the glare can be performed.

[0138]

An electronic paper in which electronic ink is driven can be provided as the display device. The electronic paper is also called an electrophoretic display device (electrophoretic display) and has advantages in that it has the same level of readability as regular paper, it has less power consumption than other display devices, and it can be set to have a thin and light form.

[0139]

An electrophoretic display device can have various modes. An electrophoretic display device contains a plurality of microcapsules dispersed in a solvent or a solute, each microcapsule containing first particles which are positively charged and second particles which are negatively charged. By applying an electric field to the microcapsules, the particles in the microcapsules move in opposite directions to each other and only the color of the particles gathering on one side is displayed. Note that the first particles and the second particles each contain pigment and do not move without an electric field. Moreover, the first particles and the second particles have different colors (which may be colorless).

[0140]

Thus, an electrophoretic display device is a display that utilizes a so-called dielectrophoretic effect by which a substance having a high dielectric constant moves to

a high-electric field region.

[0141]

A solution in which the above microcapsules are dispersed in a solvent is referred to as electronic ink. This electronic ink can be printed on a surface of glass, plastic, cloth, paper, or the like. Furthermore, by using a color filter or particles that have a pigment, color display can also be achieved.

[0142]

Note that the first particles and the second particles in the microcapsules may each be formed of a single material selected from a conductive material, an insulating material, a semiconductor material, a magnetic material, a liquid crystal material, a ferroelectric material, an electroluminescent material, an electrochromic material, and a magnetophoretic material, or formed of a composite material of any of these.

[0143]

As the electronic paper, a display device using a twisting ball display method can be used. The twisting ball display method refers to a method in which spherical particles each colored in white and black are arranged between a first electrode layer and a second electrode layer which are electrode layers used for a display element, and a potential difference is generated between the first electrode layer and the second electrode layer to control orientation of the spherical particles, so that display is performed.

[0144]

FIG. 9 shows an active matrix electronic paper as one embodiment of a semiconductor device. The electronic paper in FIG. 9 is an example of a display device using a twisting ball display method.

[0145]

Between the first electrode layer 230 connected to the transistor 210 and the second electrode layer 231 provided on the second substrate 206, spherical particles 253 each of which includes a black region 255a, a white region 255b, and a cavity 252 around the regions which is filled with liquid, are provided. A space around the spherical particles 253 is filled with a filler 254 such as a resin. The second electrode layer 231 corresponds to a common electrode (counter electrode). The second electrode layer 231 is electrically connected to a common potential line.

[0146]

Note that in FIG. 7, FIG. 8, and FIG. 9, a flexible substrate as well as a glass substrate can be used as the first substrate 201 and the second substrate 206. For example, a plastic substrate having light-transmitting properties can be used. For plastic, a fiberglass-reinforced plastics (FRP) plate, a polyvinyl fluoride (PVF) film, a polyester film, or an acrylic resin film can be used. A sheet with a structure in which an aluminum foil is sandwiched between PVF films or polyester films can also be used.

[0147]

An insulating layer 221 can be formed using an organic insulating material or an inorganic insulating material. Note that an organic insulating material having heat resistance, such as an acrylic resin, a polyimide, a benzocyclobutene-based resin, a polyamide, or an epoxy resin is preferably used as a planarizing insulating layer. Other than such organic insulating materials, it is possible to use a low-dielectric constant material (a low-k material), a siloxane-based resin, phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), or the like. The insulating layer 221 may be formed by stacking a plurality of insulating layers formed of these materials.

[0148]

There is no particular limitation on the method for forming the insulating layer 221, and the insulating layer 221 can be formed, depending on a material thereof, by a sputtering method, a spin coating method, a dipping method, a spray coating method, a droplet discharging method (e.g., an ink jet method, a screen printing method, or an offset printing method), a roll coating method, a curtain coating method, a knife coating method, or the like.

[0149]

The display device performs display by transmitting light from a light source or a display element. Thus, the substrates and the thin films such as insulating layers and conductive layers provided in the pixel portion where light is transmitted have light-transmitting properties with respect to light in the visible-light wavelength range.

[0150]

The first electrode layer 230 and the second electrode layer 231 (each of which may be called a pixel electrode layer, a common electrode layer, a counter electrode layer, or the like) for applying voltage to the display element may have

light-transmitting properties or light-reflecting properties, which depends on the direction in which light is extracted, the position where the electrode layer is provided, and the pattern structure of the electrode layer.

[0151]

A light-transmitting conductive material such as indium oxide containing tungsten oxide, indium zinc oxide containing tungsten oxide, indium oxide containing titanium oxide, indium tin oxide containing titanium oxide, indium tin oxide (hereinafter referred to as ITO), indium zinc oxide, or indium tin oxide to which silicon oxide is added, can be used for the first electrode layer 230 and the second electrode layer 231.

[0152]

The first electrode layer 230 and the second electrode layer 231 can be formed using one kind or plural kinds selected from metal such as tungsten (W), molybdenum (Mo), zirconium (Zr), hafnium (Hf), vanadium (V), niobium (Nb), tantalum (Ta), chromium (Cr), cobalt (Co), nickel (Ni), titanium (Ti), platinum (Pt), aluminum (Al), copper (Cu), or silver (Ag); an alloy thereof; and a nitride thereof.

[0153]

A conductive composition containing a conductive high molecule (also referred to as a conductive polymer) can be used for the first electrode layer 230 and the second electrode layer 231. As the conductive high molecule, a so-called π-electron conjugated conductive polymer can be used. For example, polyaniline or a derivative thereof, polypyrrole or a derivative thereof, polythiophene or a derivative thereof, and a copolymer of two or more of aniline, pyrrole, and thiophene or a derivative thereof can be given.

[0154]

Since the transistor is easily broken due to static electricity or the like, a protective circuit for protecting the driver circuit is preferably provided. The protective circuit is preferably formed using a nonlinear element.

[0155]

As described above, by using any of the transistors in Embodiment 1, a semiconductor device with high reliability can be provided. Note that the transistors described in Embodiment 1 can be applied to not only semiconductor devices having

the display functions described above but also semiconductor devices having a variety of functions, such as a power device which is mounted on a power supply circuit, a semiconductor integrated circuit such as an LSI, and a semiconductor device having an image sensor function of reading information of an object.

[0156]

The structures, the methods, and the like described in this embodiment can be combined as appropriate with any of the structures, the methods, and the like described in the other embodiments.

[0157]

(Embodiment 3)

A semiconductor device which is one embodiment of the present invention can be applied to a variety of electronic appliances (including game machines). Examples of electronic appliances are a television set (also referred to as a television or a television receiver), a monitor of a computer or the like, a camera such as a digital camera or a digital video camera, a digital photo frame, a mobile phone handset (also referred to as a mobile phone or a mobile phone device), a portable game machine, a portable information terminal, an audio reproducing device, a large-sized game machine such as a pachinko machine, and the like. Examples of electronic appliances each including the semiconductor device described in the above embodiment are described.

[0158]

FIG. 10A illustrates a laptop personal computer, which includes a main body 301, a housing 302, a display portion 303, a keyboard 304, and the like. By applying the semiconductor device described in Embodiment 1 or 2, the laptop personal computer can have high reliability.

[0159]

FIG. 10B illustrates a portable information terminal (PDA) which includes a display portion 313, an external interface 315, an operation button 314, and the like in a main body 311. A stylus 312 is included as an accessory for operation. By applying the semiconductor device described in Embodiment 1 or 2, the portable information terminal (PDA) can have higher reliability.

[0160]

FIG. 10C illustrates an example of an e-book reader. For example, an e-book

reader 320 includes two housings, a housing 321 and a housing 322. The housing 321 and the housing 322 are combined with a hinge 325 so that the e-book reader 320 can be opened and closed with the hinge 325 as an axis. With such a structure, the e-book reader 320 can operate like a paper book.

[0161]

A display portion 323 and a display portion 324 are incorporated in the housing 321 and the housing 322, respectively. The display portion 323 and the display portion 324 may display one image or different images. When the display portion 323 and the display portion 324 display different images, for example, text can be displayed on a display portion on the right side (the display portion 323 in FIG. 10C) and graphics can be displayed on a display portion on the left side (the display portion 324 in FIG. 10C). By applying the semiconductor device described in Embodiment 1 or 2, the e-book reader 320 can have high reliability.

[0162]

FIG. 10C illustrates an example in which the housing 321 is provided with an operation portion and the like. For example, the housing 321 is provided with a power switch 326, operation keys 327, a speaker 328, and the like. With the operation key 327, pages can be turned. Note that a keyboard, a pointing device, or the like may also be provided on the surface of the housing, on which the display portion is provided. Furthermore, an external connection terminal (an earphone terminal, a USB terminal, or the like), a recording medium insertion portion, and the like may be provided on the back surface or the side surface of the housing. Moreover, the e-book reader 320 may have a function of an electronic dictionary.

[0163]

The e-book reader 320 may have a configuration capable of wirelessly transmitting and receiving data. Through wireless communication, desired book data or the like can be purchased and downloaded from an e-book server.

[0164]

FIG. 10D illustrates a mobile phone, which includes two housings, a housing 330 and a housing 331. The housing 331 includes a display panel 332, a speaker 333, a microphone 334, a pointing device 336, a camera lens 337, an external connection terminal 338, and the like. In addition, the housing 330 includes a solar cell 340

having a function of charge of the portable information terminal, an external memory slot 341, and the like. Further, an antenna is incorporated in the housing 331. By applying the semiconductor device described in Embodiment 1 or 2, the mobile phone can have high reliability.

[0165]

Further, the display panel 332 is provided with a touch panel. A plurality of operation keys 335 which are displayed as images is illustrated by dashed lines in FIG. 10D. Note that a boosting circuit by which a voltage output from the solar cell 340 is increased to be sufficiently high for each circuit is also included.

[0166]

In the display panel 332, the display orientation can be changed as appropriate depending on a usage pattern. Further, the mobile phone is provided with the camera lens 337 on the same surface as the display panel 332, and thus it can be used as a video phone. The speaker 333 and the microphone 334 can be used for videophone calls, recording and playing sound, and the like as well as voice calls. Moreover, the housings 330 and 331 in a state where they are opened as illustrated in FIG. 10D can be slid so that one overlaps the other; therefore, the size of the mobile phone can be reduced, which makes the mobile phone suitable for being carried.

[0167]

The external connection terminal 338 can be connected to an AC adapter and various types of cables such as a USB cable, and charging and data communication with a personal computer are possible. Moreover, a larger amount of data can be saved and moved by inserting a recording medium to the external memory slot 341.

[0168]

Further, in addition to the above functions, an infrared communication function, a television reception function, or the like may be provided.

[0169]

FIG. 10E illustrates a digital video camera which includes a main body 351, a display portion (A) 357, an eyepiece 353, an operation switch 354, a display portion (B) 355, a battery 356, and the like. By applying the semiconductor device described in Embodiment 1 or 2, the digital video camera can have high reliability.

[0170]

FIG. 10F illustrates an example of a television set. In a television set 360, a display portion 363 is incorporated in a housing 361. The display portion 363 can display images. Here, the housing 361 is supported by a stand 365. By applying the semiconductor device described in Embodiment 1 or 2, the television set 360 can have high reliability.

[0171]

The television set 360 can be operated by an operation switch of the housing 361 or a separate remote controller. Further, the remote controller may be provided with a display portion for displaying data output from the remote controller.

[0172]

Note that the television set 360 is provided with a receiver, a modem, and the like. With the use of the receiver, general television broadcasting can be received. Furthermore, when the television set is connected to a communication network with or without wires via the modem, one-way (from a sender to a receiver) or two-way (between a sender and a receiver or between receivers) information communication can be performed.

[0173]

The structures, the methods, and the like described in this embodiment can be combined as appropriate with any of the structures, the methods, and the like described in the other embodiments.

[Example 1]

[0174]

In this example, a silicon oxide layer formed using one embodiment of the present invention is described.

[0175]

First, as a sample, a silicon oxide layer was formed over a glass substrate by the method described in Embodiment 1. In this example, a 100-nm-thick silicon oxide layer was formed over a 0.7-mm-thick glass substrate.

[0176]

Other formation conditions of the silicon oxide layer were as follows.

· Film formation method: RF sputtering method

· Target: synthesized quartz target

· Film formation gas: Ar (40 sccm), O_2 (10 sccm)

· Electric power: 1.5 kW (13.56 MHz)

· Pressure: 0.4 Pa

· T–S distance: 60 mm

· Substrate temperature: 100 °C

[0177]

After the silicon oxide layer was formed, the substrate was divided into 1 cm square and degassing yield obtained by TDS analysis was examined. A thermal desorption spectroscopy apparatus manufactured by ESCO Ltd., EMD–WA1000S/W was used for the TDS analysis. Note that TDS analysis is an analysis method in which a sample is heated in a vacuum case and a gas component generated from the sample when the temperature of the sample is increased is detected by a quadrupole mass analyzer. Detected gas components are distinguished from each other by the value of m/z (mass/charge)

[0178]

Results of TDS analysis of manufactured samples are shown in FIGS. 11A and 11B.

[0179]

FIG. 11A shows TDS spectra when the value of m/z is 16. Here, a thick line 401 indicates a spectrum of a sample after a film formation was performed (as–depo sample) and a thin line 403 indicates a spectrum of a sample on which heat treatment was performed at 250 °C in a nitrogen atmosphere for an hour after the film formation. As examples of a component in which the value of m/z is 16, O, CH_4, and the like can be given. The as–depo sample has a peak when the substrate temperature is 200 °C to 300 °C; however, a similar spectrum was not observed in the sample on which heat treatment was performed at 250 °C in a nitrogen atmosphere for an hour. FIG. 11B shows TDS spectra when the value of m/z is 32. Here, a thick line 405 indicates a spectrum of an as–depo sample and a thin line 407 indicates a spectrum of a sample on which heat treatment was performed at 250 °C in a nitrogen atmosphere for an hour after the film formation. As examples of a component in which the value of m/z is 32,

O_2, CH_3OH, and the like can be given. The as-depo sample has a peak when the substrate surface temperature is 200 °C to 350 °C; however, the similar spectrum was not observed in the sample on which heat treatment was performed at 250 °C for an hour. According to the above results, oxygen are released from the as-depo samples.

[0180]

The released amount of oxygen converted to O_2 was $3 \times 10^{20}/cm^3$ with the use of the TDS spectra of the samples manufactured in this example in the case where it was assumed that components in which the value of m/z was 16 were all O and components in which the value of m/z was 32 were all O_2. Although not shown in the graphs, when the percentage of $O_2/(O_2+Ar)$ in the film formation was 50 %, the released amount of oxygen converted to O_2 was $5 \times 10^{20}/cm^3$.

[Example 2]

[0181]

In this example, a transistor formed using one embodiment of the present invention is described.

[0182]

FIG. 12 illustrates a structure of the transistor of this example.

[0183]

The transistor in FIG. 12 includes an insulating layer 502 provided over a substrate 500, an oxide semiconductor layer 506, a source electrode 508a and a drain electrode 508b, a gate insulating layer 512 provided over the source electrode 508a and the drain electrode 508b, a gate electrode 514 provided over the gate insulating layer 512, a protective insulating layer 516 provided over the gate electrode 514, and a source wiring 518a and a drain wiring 518b connected to the source electrode 508a and the drain electrode 508b, respectively, with the protective insulating layer 516 interposed therebetween.

[0184]

In this example, a 0.7-mm-thick glass substrate was used as the substrate 500, a 300-nm-thick silicon oxide layer was formed as the insulating layer 502, a 30-nm-thick In-Ga-Zn-O-based non-single-crystal layer was formed as the oxide semiconductor layer 506, a 100-nm-thick tungsten layer was formed as the source electrode 508a and

the drain electrode 508b, a 20-nm-thick silicon oxynitride layer was formed as the gate insulating layer 512, a stack of a 30-nm-thick tantalum nitride layer and a 370-nm-thick tungsten layer was formed as the gate electrode 514, a 300-nm-thick silicon oxide layer was formed as the protective insulating layer 516, and a stack of a 50-nm-thick titanium layer, a 100-nm-thick aluminum layer, and a 5-nm-thick titanium layer was formed as the source wiring 518a and the drain wiring 518b.

[0185]

In the transistor of this example, an insulating layer from which oxygen is released by heating was used as the insulating layer 502 which is a base layer, whereby fluctuation in the threshold voltage and fluctuation in the threshold voltage after a BT test were reduced. In this example, a silicon oxide layer was used as the insulating layer from which oxygen is released by heating.

[0186]

Other formation conditions of the silicon oxide layer were as follows.

· Film formation method: RF sputtering method

· Target: synthesized quartz target

· Film formation gas: Ar (25 sccm), O_2 (25 sccm)

· Electric power: 1.5 kW (13.56 MHz)

· Pressure: 0.4 Pa

· T–S distance: 60 mm

· Substrate temperature: 100 °C

[0187]

The formation conditions of the oxide semiconductor layer 506 in the transistor of this example were as follows.

· Film formation method: DC sputtering method

· Target: In-Ga-Zn-O (In_2O_3:Ga_2O_3:ZnO = 1:1:2 [molar ratio]) target

· Film formation gas: Ar (30 sccm), O_2 (15 sccm)

· Electric power: 0.5 kW (DC)

· Pressure: 0.4 Pa

· T–S distance: 60 mm

· Substrate temperature: 200 °C

[0188]

After the oxide semiconductor layer 506 was formed, heat treatment was performed at 350 °C in a nitrogen atmosphere for an hour using a resistance heating furnace.

[0189]

FIG. 13 shows drain current (Ids)-gate voltage (Vgs) measurement results in the transistor of this example. Note that the measurement was performed at 25 points on a substrate surface. The measurement results are overlapped with each other in FIG. 13. The channel length L is 2 μm, and the channel width W is 50 μm. Note that the voltage Vds between the source electrode and the drain electrode of the transistor was set to 3 V.

[0190]

According to FIG. 13, it was found that there was no variation in the substrate surface of the transistor of this example. Note that the average threshold voltage of the 25 points was 0.27 V.

[0191]

Next, the BT test in this example is described. The transistor on which the BT test is performed has a channel length L of 3 μm and a channel width W of 50 μm. In this example, first, the substrate temperature was set to 25 °C and the voltage Vds of the source electrode and the drain electrode was set to 3 V to perform the Ids-Vgs measurement of the transistor.

[0192]

Next, the substrate stage temperature was set to 150 °C, and the source electrode and the drain electrode of the transistor were set to 0 V and 0.1 V, respectively. Then, a negative voltage was applied to the gate electrode so that electric-field intensity applied to the gate insulating layer was 2 MV/cm, and the gate electrode was kept for an hour. Next, the voltage of the gate electrode was set to 0 V. After that, the substrate temperature was set to 25 °C and the voltage Vds of the source electrode and the drain electrode was set to 3 V to perform the Ids-Vgs measurement of the transistor. FIG. 14A shows the Ids-Vgs measurement results before and after the BT test.

[0193]

In FIG. 14A, a thin line 522 shows the Ids-Vgs measurement results before the BT test, and a thick line 524 shows the Ids-Vgs measurement results after the BT test. It is found that the threshold voltage fluctuates in a negative direction by 0.07 V after the BT test, as compared to the measurement results before the BT test.

[0194]

In a similar manner, another transistor for measurement was prepared, and the substrate temperature was set to 25 °C and the voltage Vds of the source electrode and the drain electrode was set to 3 V to perform the Ids-Vgs measurement of the transistor. The channel length L of the transistor is 3 μm, and the channel width W thereof is 50 μm.

[0195]

Next, the substrate stage temperature was set to 150 °C, and the source electrode and the drain electrode of the transistor were set to 0 V and 0.1 V, respectively. Then, a positive voltage was applied to the gate electrode so that electric-field intensity applied to the gate insulating layer was 2 MV/cm, and the gate electrode was kept for an hour. Next, the voltage of the gate electrode was set to 0 V. After that, the substrate temperature was set to 25 °C and the voltage Vds of the source electrode and the drain electrode was set to 3 V to perform the Ids-Vgs measurement of the transistor. FIG. 14B shows the Ids-Vgs measurement results before and after the BT test.

[0196]

In FIG. 14B, a thin line 532 shows the Ids-Vgs measurement results before the BT test, and a thick line 534 shows the Ids-Vgs measurement results after the BT test. It is found that the threshold voltage fluctuates in a positive direction by 0.19 V after the BT test, as compared to the measurement results before the BT test.

[0197]

As described above, it is found that the transistor of this example has small variation in the threshold voltage of the substrate surface and small fluctuation in the threshold voltage between before and after a BT test.

This application is based on Japanese Patent Application serial no. 2010-116952 filed with Japan Patent Office on May 21, 2010, the entire contents of

which are hereby incorporated by reference.

CLAIMS

1. A semiconductor device comprising:

an insulating layer configured to release oxygen by heating;

an oxide semiconductor layer over and in contact with the insulating layer;

a source electrode and a drain electrode over the oxide semiconductor layer, and electrically connected to the oxide semiconductor layer;

a gate insulating layer over the source electrode and the drain electrode; and

a gate electrode over the gate insulating layer,

wherein a part of the gate insulating layer is in contact with the oxide semiconductor layer; and

2. A semiconductor device comprising:

an insulating layer configured to release oxygen by heating;

a source electrode and a drain electrode provided over the insulating layer;

an oxide semiconductor layer electrically connected to the source electrode and the drain electrode;

a gate insulating layer provided over the oxide semiconductor layer; and

a gate electrode over the gate insulating layer,

wherein a part of the oxide semiconductor layer is in contact with the insulating layer.

3. The semiconductor device according to claim 1, wherein the insulating layer comprises any of silicon oxide, silicon oxynitride, aluminum oxide, and hafnium oxide.

4. The semiconductor device according to claim 2, wherein the insulating layer comprises any of silicon oxide, silicon oxynitride, aluminum oxide, and hafnium oxide.

5. The semiconductor device according to claim 1, wherein a released amount of oxygen molecules of the insulating layer is greater than or equal to $1 \times 10^{18}/cm^3$ in thermal desorption spectroscopy.

6. The semiconductor device according to claim 1, wherein a released amount

of oxygen molecules of the insulating layer is greater than or equal to $1 \times 10^{18}/cm^3$ in thermal desorption spectroscopy.

7. The semiconductor device according to claim 1,

wherein the oxide semiconductor layer comprises a channel region, and a source region and a drain region,

wherein a resistance of the oxide semiconductor layer is reduced, and

wherein the source region and the drain region are connected to the source electrode and the drain electrode, respectively.

8. The semiconductor device according to claim 2,

wherein the oxide semiconductor layer comprises a channel region, and a source region and a drain region,

wherein a resistance of the oxide semiconductor layer is reduced, and

wherein the source region and the drain region are connected to the source electrode and the drain electrode, respectively.

9. A method of manufacturing a semiconductor device comprising the steps of:

forming an insulating layer configured to release oxygen by heating, over a substrate;

forming an oxide semiconductor layer over and in contact with the insulating layer;

forming a source electrode and a drain electrode electrically connected to the oxide semiconductor layer;

forming a gate insulating layer over the source electrode and the drain electrode, and

forming a gate electrode over the gate insulating layer,

wherein a part of the gate insulating layer is in contact with the oxide semiconductor layer.

10. A method of manufacturing a semiconductor device comprising the steps of:

forming an insulating layer configured to release oxygen by heating, over a substrate;

forming a source electrode and a drain electrode over the insulating layer;

forming an oxide semiconductor layer electrically connected to the source electrode and the drain electrode;

forming a gate insulating layer over the oxide semiconductor layer; and

forming a gate electrode over the gate insulating layer,

wherein a part of the oxide semiconductor layer is in contact with the insulating layer.

11. The method of manufacturing a semiconductor device according to claim 9, wherein a channel region is formed in a portion of the oxide semiconductor layer overlapped with the gate electrode at the same time of a formation of a source region and a drain region by performing treatment for reducing resistance of the oxide semiconductor layer using the gate electrode as a mask.

12. The method of manufacturing a semiconductor device according to claim 10, wherein a channel region is formed in a portion of the oxide semiconductor layer overlapped with the gate electrode at the same time of a formation of a source region and a drain region by performing treatment for reducing resistance of the oxide semiconductor layer using the gate electrode as a mask.

13. The method of manufacturing a semiconductor device according to claim 9, wherein the insulating layer is formed by a sputtering method or a plasma CVD method.

14. The method of manufacturing a semiconductor device according to claim 10, wherein the insulating layer is formed by a sputtering method or a plasma CVD method.

15. The method of manufacturing a semiconductor device according to claim 9, wherein the insulating layer is formed using an oxygen gas or a mixed gas of oxygen

and argon by a sputtering method.

16. The method of manufacturing a semiconductor device according to claim 10, wherein the insulating layer is formed using an oxygen gas or a mixed gas of oxygen and argon by a sputtering method.

17. The method of manufacturing a semiconductor device according to claim 9, wherein the oxide semiconductor layer is formed by a sputtering method.

18. The method of manufacturing a semiconductor device according to claim 10, wherein the oxide semiconductor layer is formed by a sputtering method.

19. The method of manufacturing a semiconductor device according to claim 9, wherein a substrate temperature is higher than or equal to 100 °C and lower than or equal to 450 °C when the oxide semiconductor layer is formed.

20. The method of manufacturing a semiconductor device according to claim 10, wherein a substrate temperature is higher than or equal to 100 °C and lower than or equal to 450 °C when the oxide semiconductor layer is formed.

21. The method of manufacturing a semiconductor device according to claim 9, wherein heat treatment is performed at a temperature of higher than or equal to 100 °C and lower than or equal to 450 °C after the oxide semiconductor layer is formed.

22. The method of manufacturing a semiconductor device according to claim 10, wherein heat treatment is performed at a temperature of higher than or equal to 100 °C and lower than or equal to 450 °C after the oxide semiconductor layer is formed.

FIG. 1A

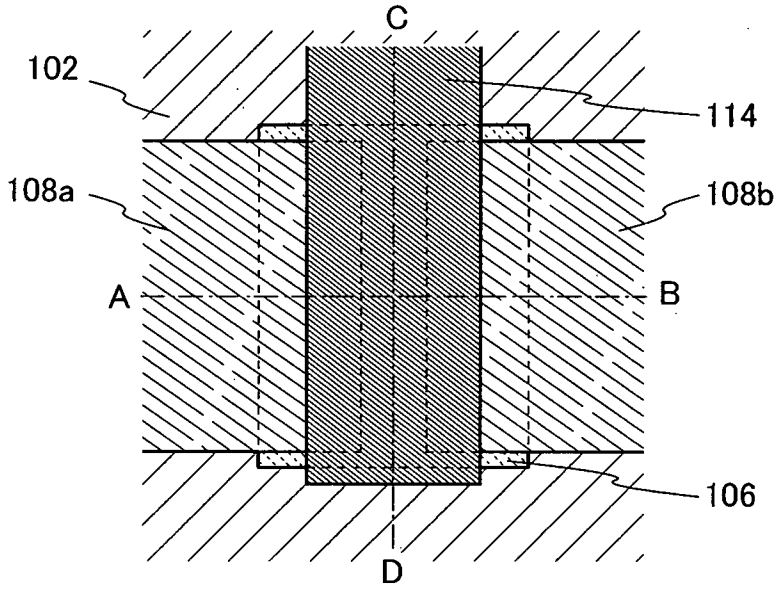

FIG. 1B

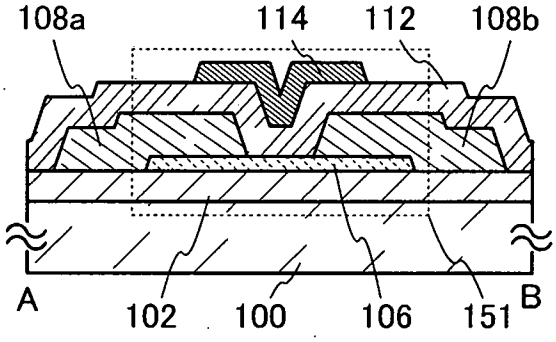

FIG. 1C

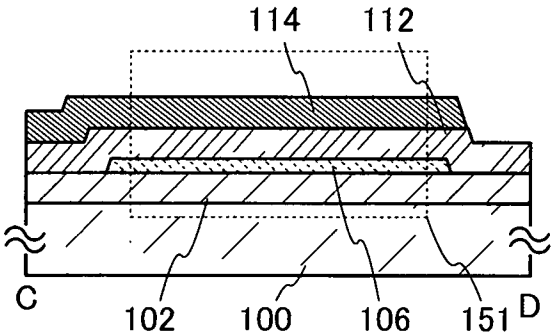

FIG. 2A

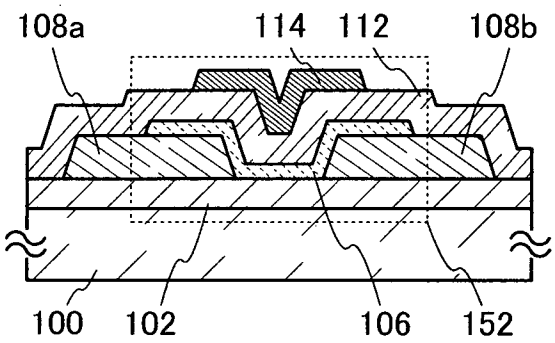
108a
114
112
108b
100
102
106
152

FIG. 2B

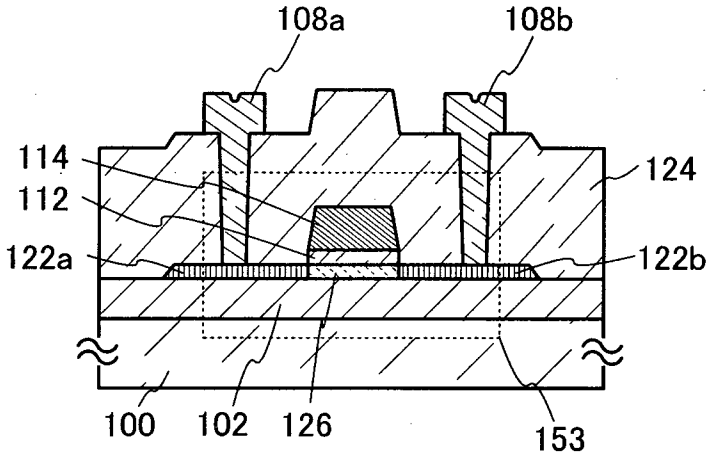
108a
108b
114
112
122a
124
122b
100
102
126
153

FIG. 3A

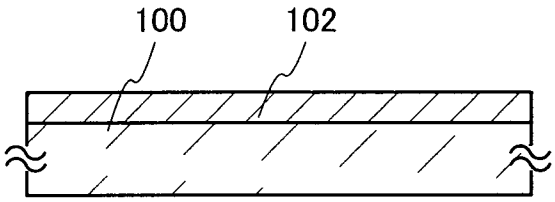

FIG. 3B

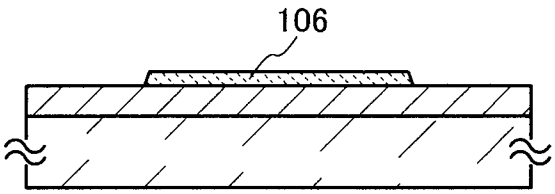

FIG. 3C

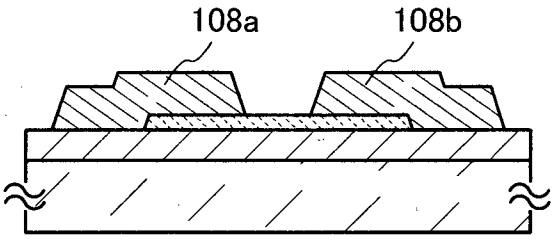

FIG. 3D

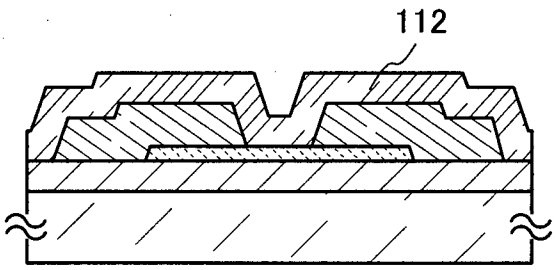

FIG. 3E

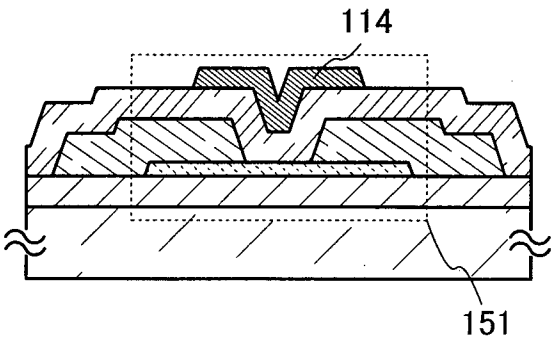

FIG. 4A

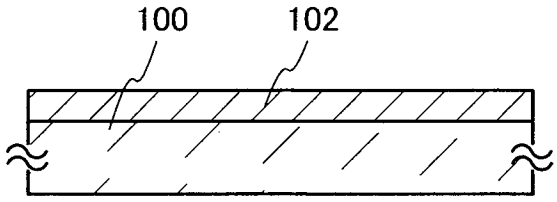

FIG. 4B

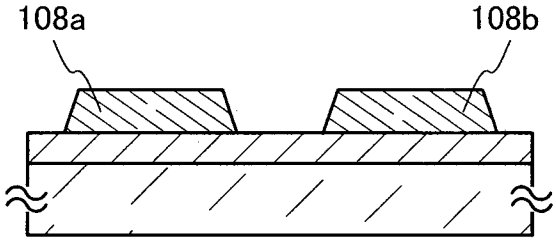

FIG. 4C

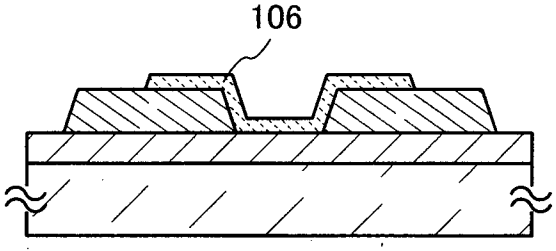

FIG. 4D

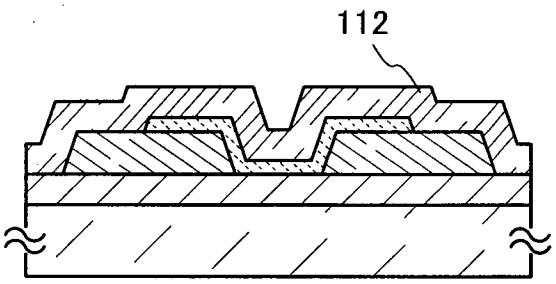

FIG. 4E

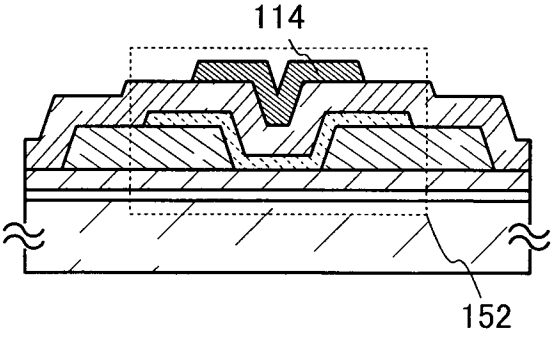

FIG. 5A

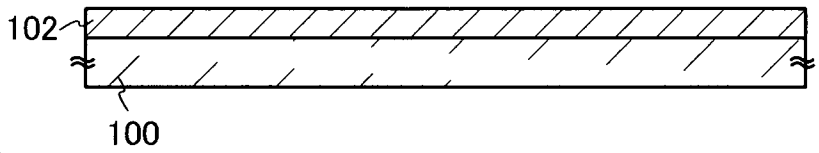

FIG. 5B

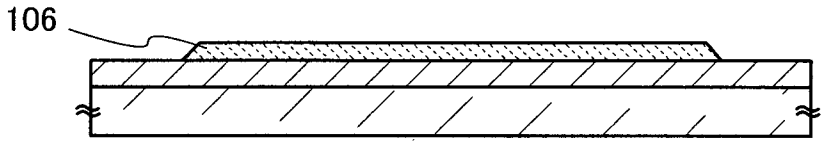

FIG. 5C

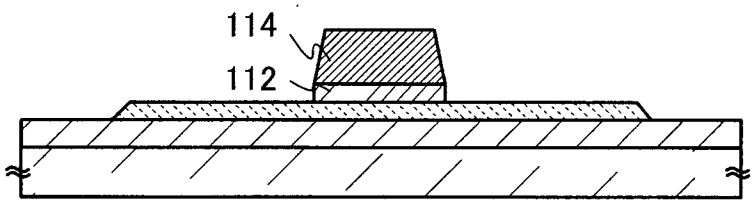

FIG. 5D

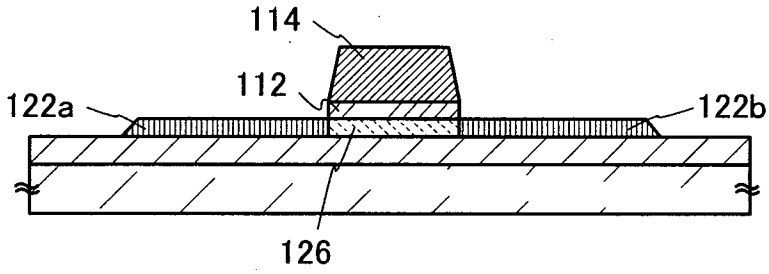

FIG. 5E

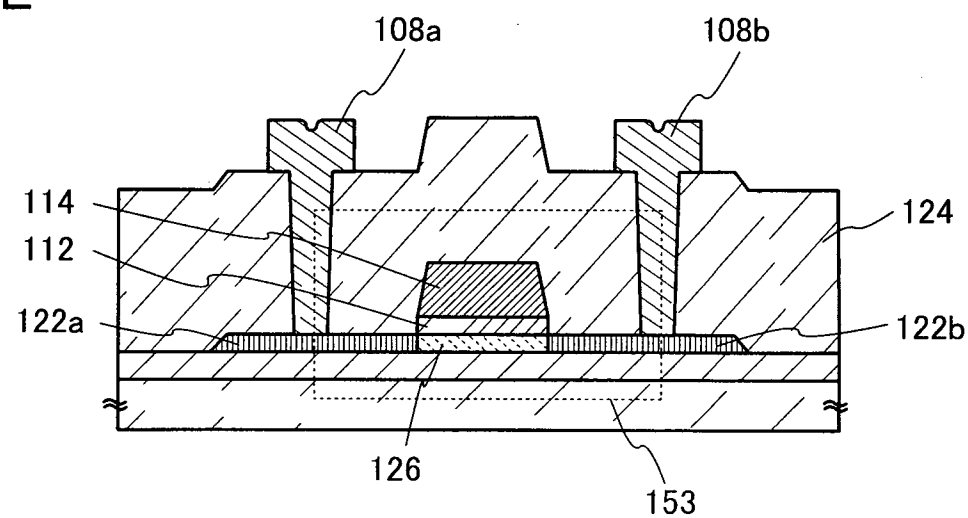

FIG. 6A

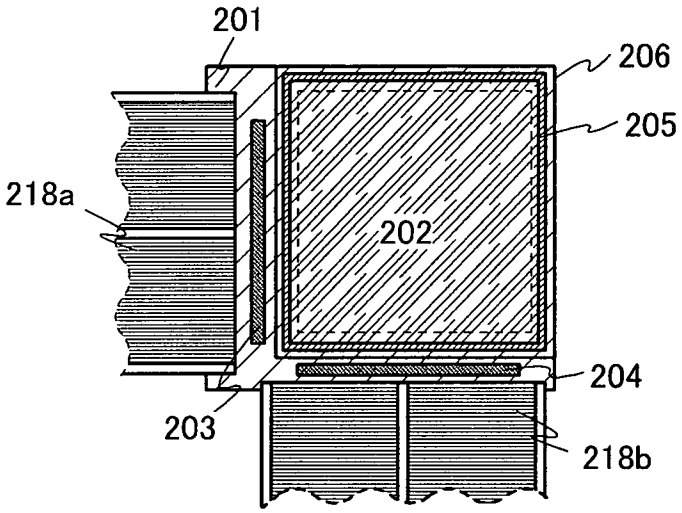

FIG. 6B

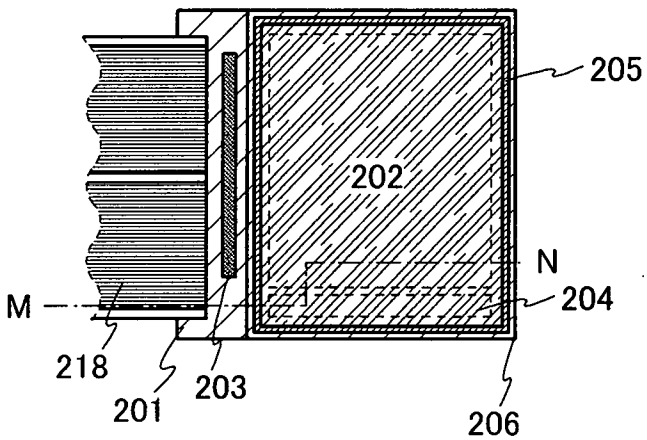

FIG. 6C

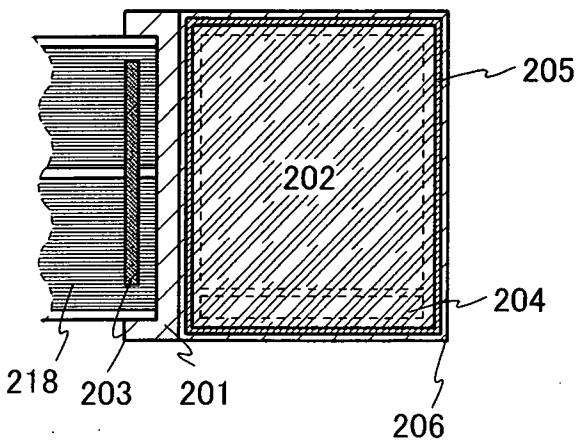

FIG. 7

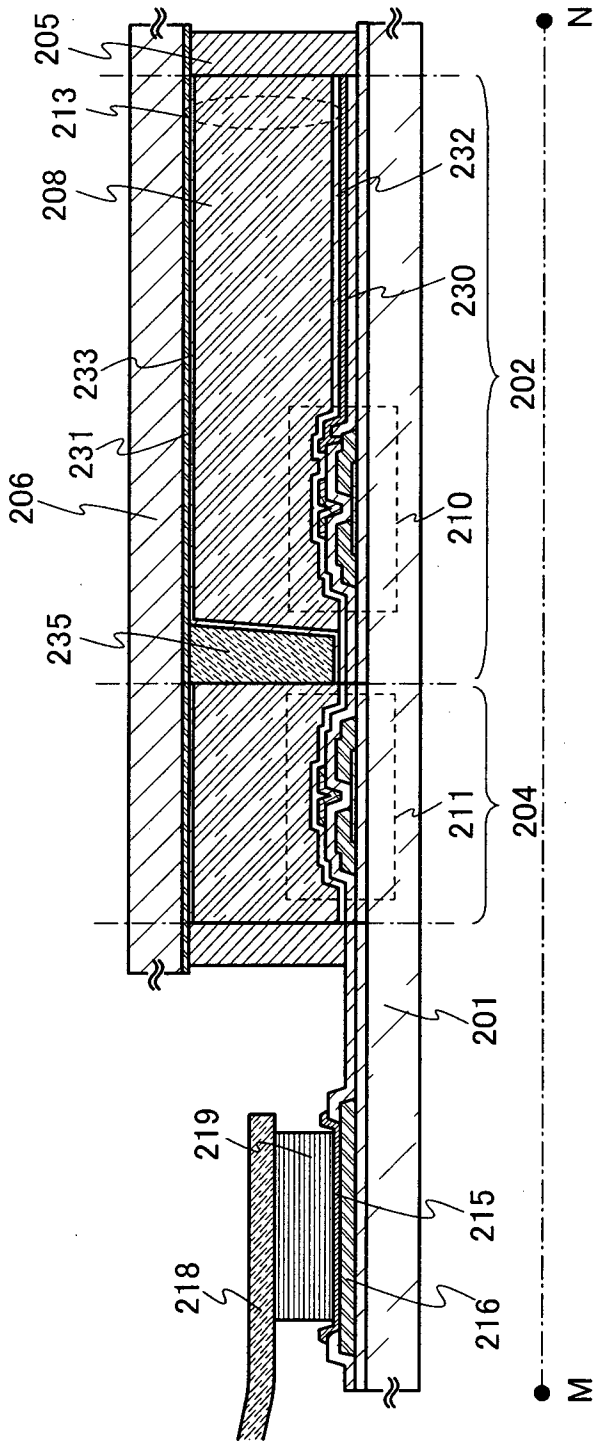
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FIG. 8

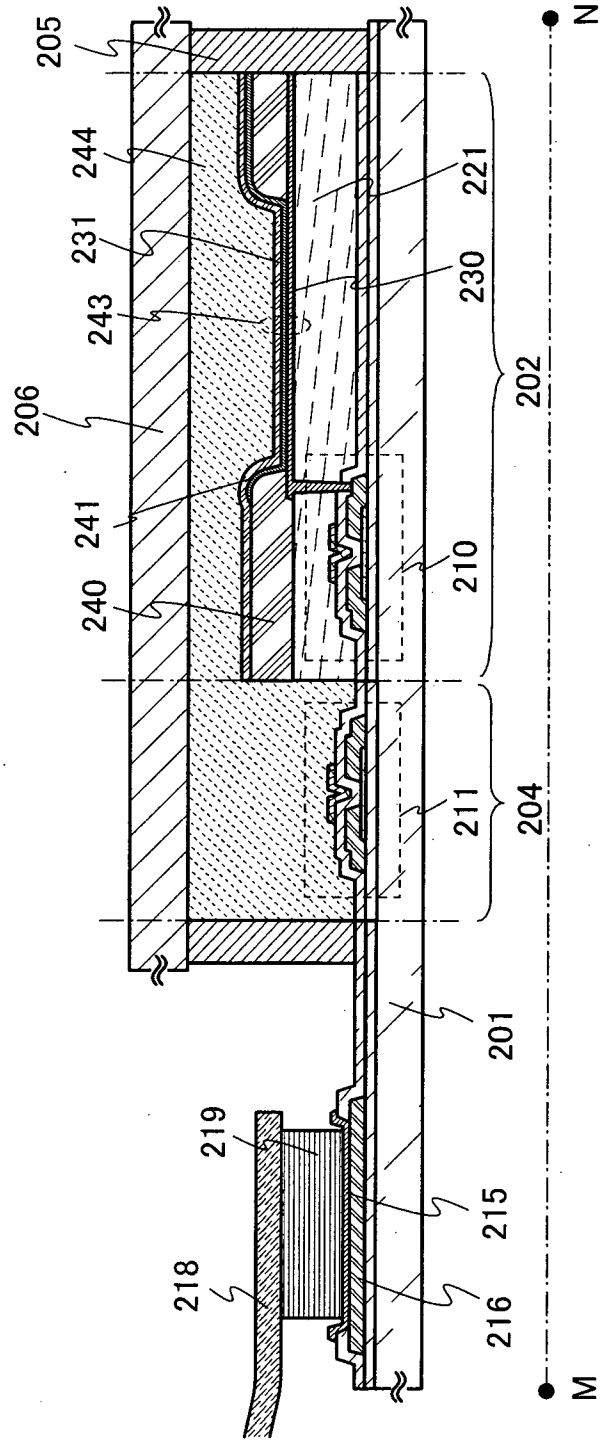
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FIG. 9

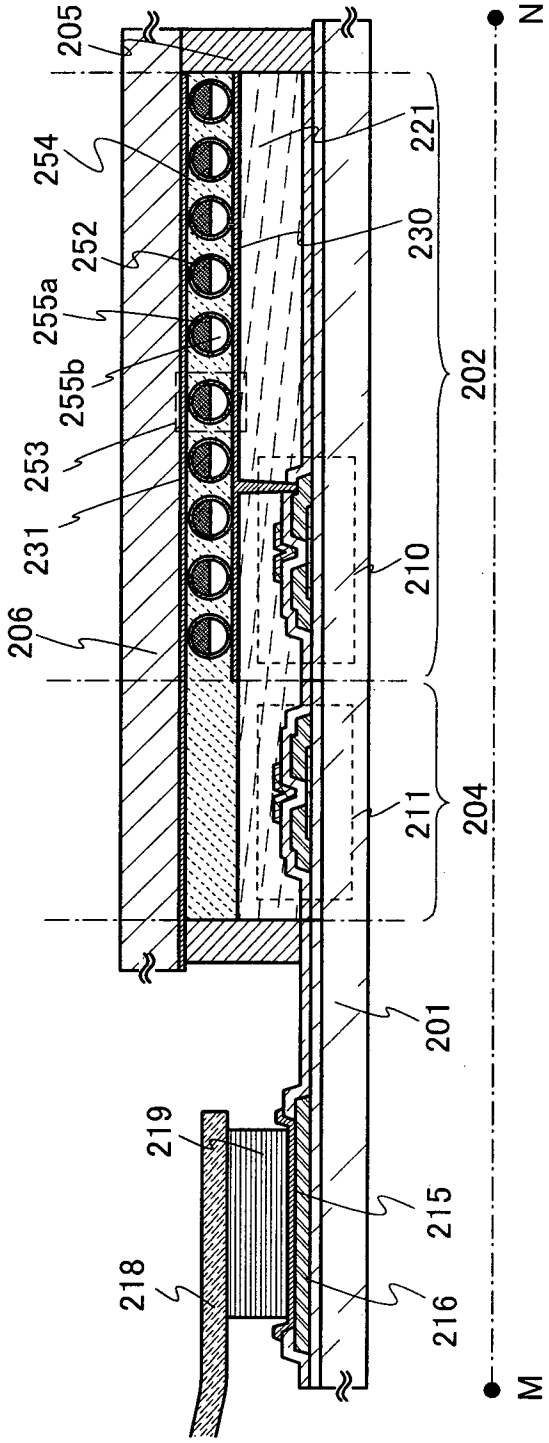
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FIG. 10A

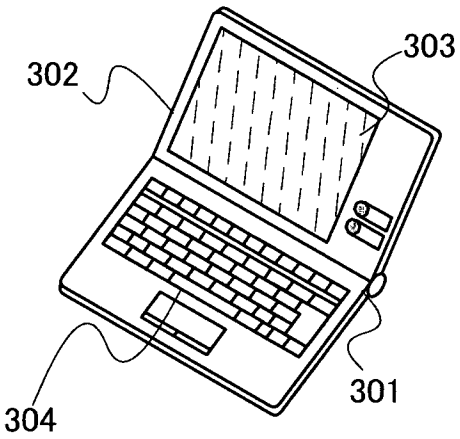


FIG. 10B

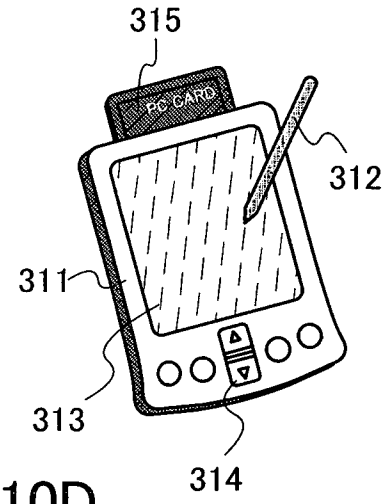


FIG. 10C

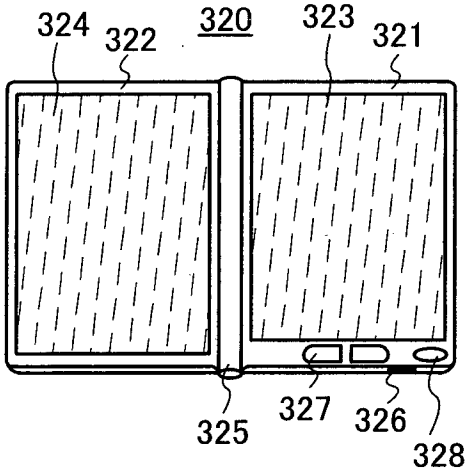


FIG. 10D

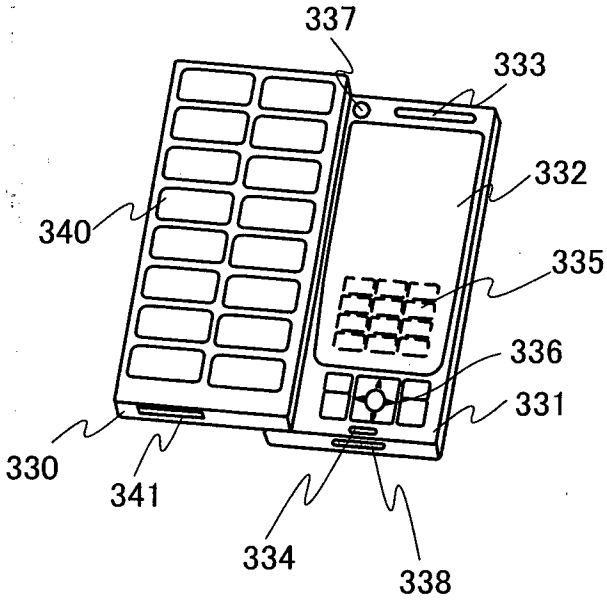


FIG. 10E

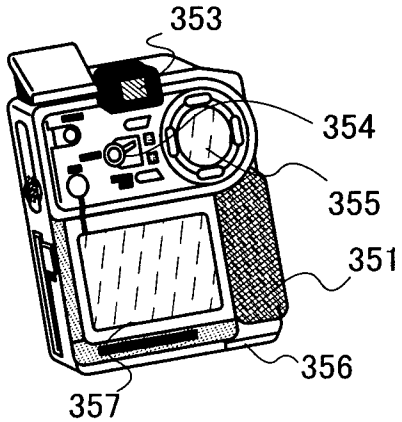


FIG. 10F

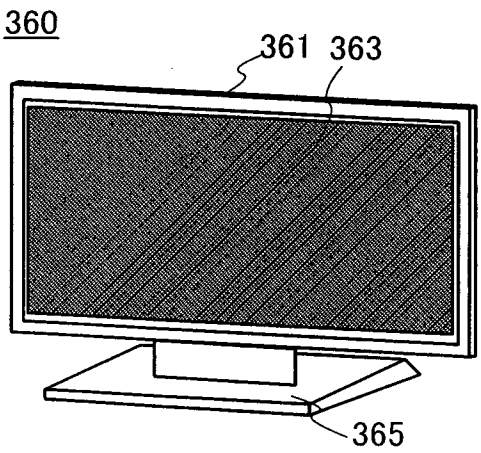


FIG. 11A

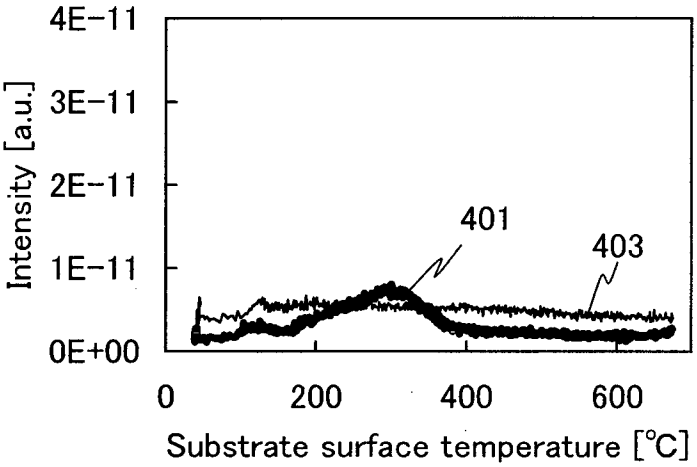


FIG. 11B

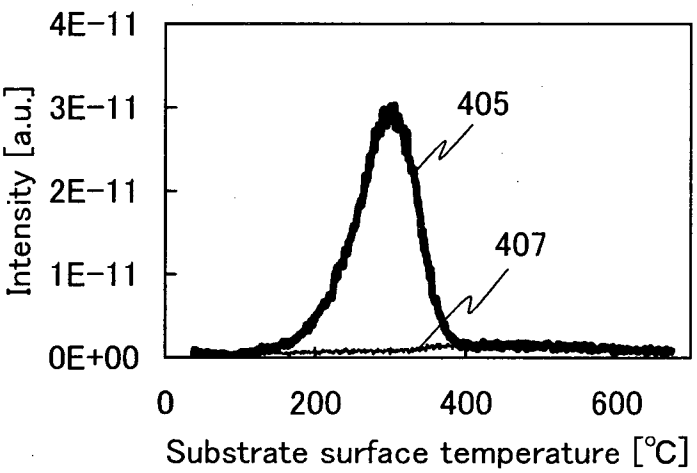


FIG. 12

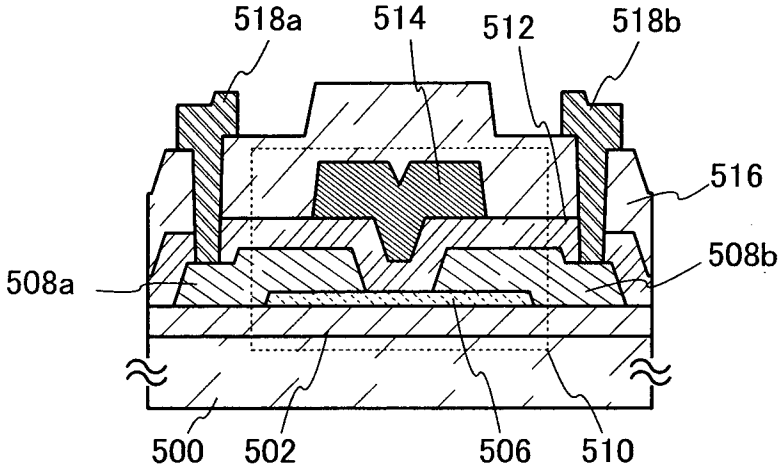


FIG. 13

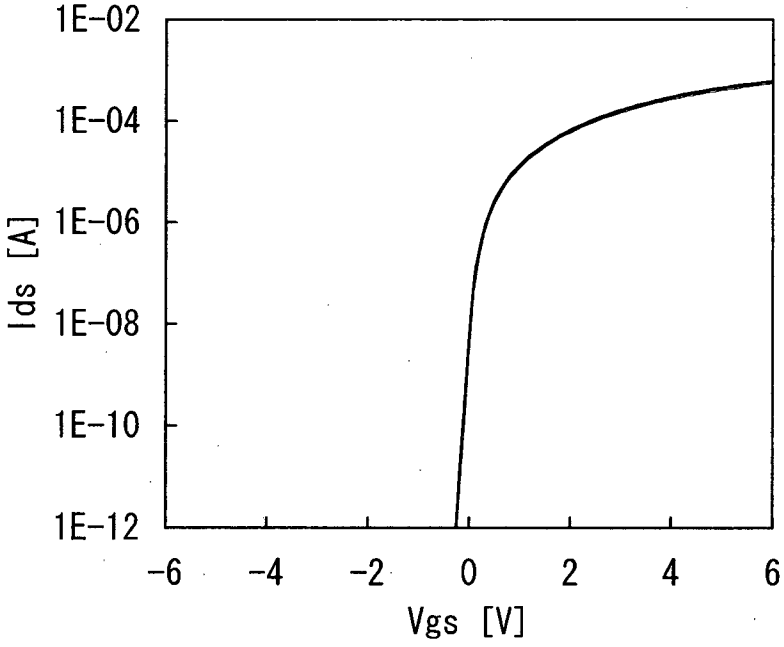


FIG. 14A

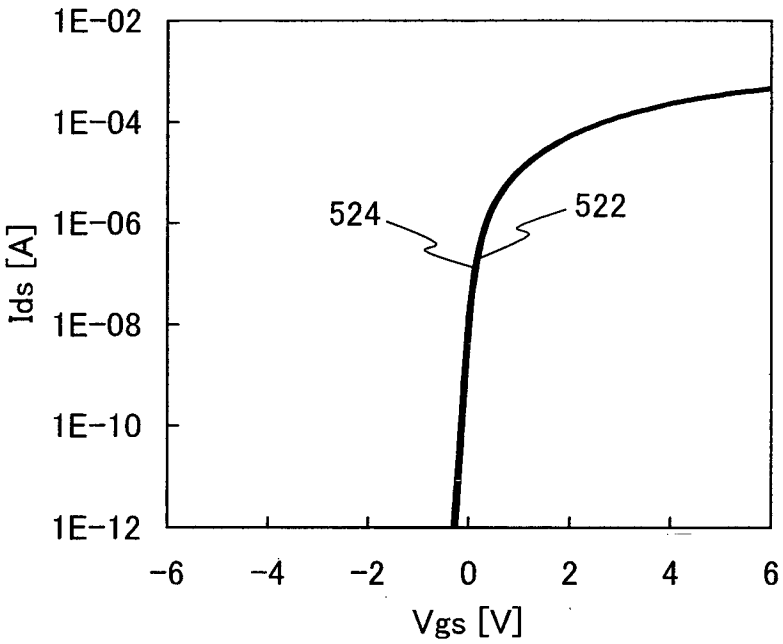
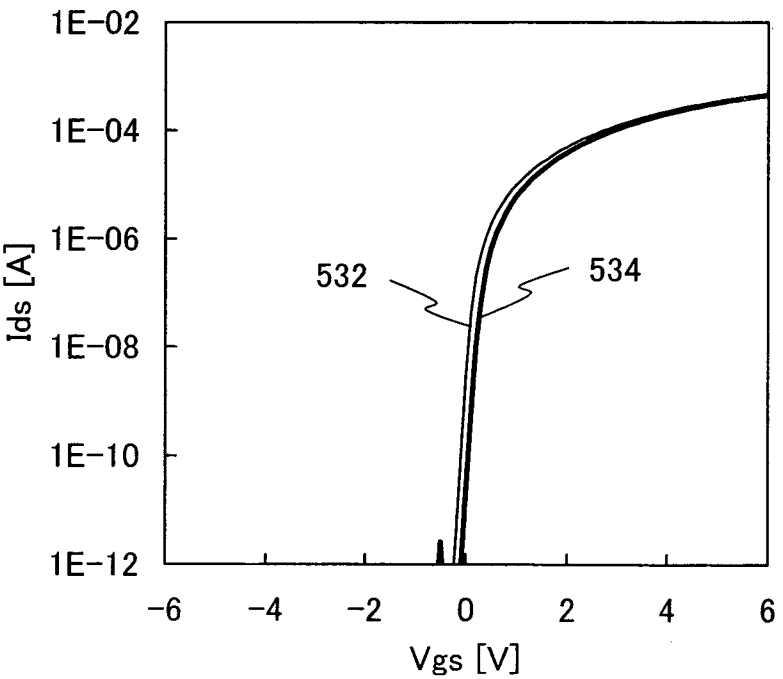


FIG. 14B



EXPLANATION OF REFERENCE

100: substrate, 102: insulating layer, 106: oxide semiconductor layer, 108a: source electrode, 108b: drain electrode, 112: gate insulating layer, 114: gate electrode, 122a: source region, 122b: drain region, 124: protective insulating layer, 126: channel region, 151: transistor, 152: transistor, 153: transistor, 201: first substrate, 202: pixel portion, 203: signal line driver circuit, 204: scan line driver circuit, 205: sealant, 206: second substrate, 208: liquid crystal layer, 210: transistor, 211: transistor, 213: liquid crystal element, 215: connection terminal electrode, 216: terminal electrode, 218: FPC, 218a: FPC, 218b: FPC, 219: anisotropic conductive layer, 221: insulating layer, 230: first electrode layer, 231: second electrode layer, 232: insulating layer, 233: insulating layer, 235: spacer, 240: partition wall, 241: electroluminescent layer, 243: light-emitting element, 244: filler, 252: cavity, 253: spherical particle, 254: filler, 255a: black region, 255b: white region, 301: main body, 302: housing, 303: display portion, 304: keyboard, 311: main body, 312: stylus, 313: display portion, 314: operation button, 315: external interface, 320: e-book reader, 321: housing, 322: housing, 323: display portion, 324: display portion, 325: hinge, 326: power switch, 327: operation key, 328: speaker, 330: housing, 331: housing, 332: display panel, 333: speaker, 334: microphone, 335: operation key, 336: pointing device, 337: camera lens, 338: external connection terminal, 340: solar cell, 341: external memory slot, 351: main body, 353: eyepiece, 354: operation switch, 355: display portion (B), 356: battery, 357: display portion (A), 360: television set, 361: housing, 363: display portion, 365: stand, 401: thick line, 403: thin line, 405: thick line, 407: thin line, 500: substrate, 502: insulating layer, 506: oxide semiconductor layer, 508a: source electrode, 508b: drain electrode, 512: gate insulating layer, 514: gate electrode, 516: protective insulating layer, 518a: source wiring, 518b: drain wiring, 522: thin line, 524: thick line, 532: thin line, and 534: thick line.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2011/060682

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H01L29/786, G02F1/1368, G09F9/30, H01L21/316, H01L21/336, H01L51/50, H05B33/14

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2011
Registered utility model specifications of Japan 1996-2011
Published registered utility model applications of Japan 1994-2011

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2009-065012 A (KONICA MINOLTA HOLDINGS, INC.) 2009.03.26, Paragraphs 0084-0128 (No Family)	1-4,9,10
A	JP 2009-278115 A (SAMSUNG ELECTRONICS CO., LTD.) 2009.11.26, Paragraphs 0025-0032 & EP 2120267 A1 & KR 10-2009-0119666 A	1-4,9,10

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29.07.2011	09.08.2011

Name and mailing address of the ISA/JP	Authorized officer
Japan Patent Office 3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan	KAZUNARI TANADA Telephone No. +81-3-3581-1101 Ext. 3462

4M 9361

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2011/060682

CLASSIFICATION OF SUBJECT MATTER
H01L29/786(2006.01)i, G02F1/1368(2006.01)i, G09F9/30(2006.01)i,
H01L21/316(2006.01)i, H01L21/336(2006.01)i, H01L51/50(2006.01)i,
H05B33/14(2006.01)i

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2011/060682

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
D1: JP 2009-065012 A (KONICA MINOLTA HOLDINGS, INC.) 2009.03.26,Paragraphs 0084-0128 (No Family)
D1 discloses a semiconductor device comprising: an insulating layer configured to release oxygen by heating; an oxide semiconductor layer over and in contact with the insulating layer; a source electrode and a drain electrode over the oxide semiconductor layer, and electrically connected to the oxide semiconductor layer; a gate insulating layer over the source electrode and the drain electrode; and a gate electrode over the gate insulating layer, wherein a part of the gate insulating layer is in contact with the oxide semiconductor layer. Therefore, claims 1-4, 9, 10 lacks novelty over D1, and involves no special technical features. Thus, there are 9 inventions in the claims of this application.

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☑ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-4,9,10

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
☐ No protest accompanied the payment of additional search fees.