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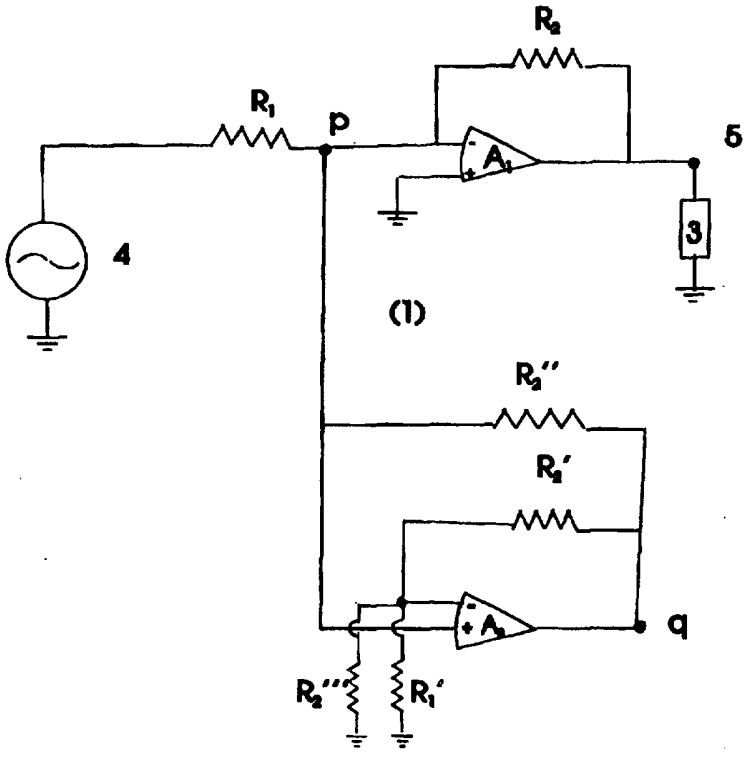
(57) Abstract

An amplifier structure with reduced distortion which is simple and easy to operate comprises a main or power amplifier circuit and a subsidiary circuit. The output from the power circuit is considered as comprising the ideal or undistorted voltage and an error voltage which produces distortion, the subsidiary circuit generates a compensation voltage substantially the same as the error voltage, when this compensation voltage is combined with the output from the main amplifier circuit the distortion is substantially reduced or eliminated.



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Point Feedback

The present invention relates to an amplifier with reduced distortion in the output signal, more particularly it relates to an amplifier circuit in which the distortion normally present is reduced.

Techniques which have been used for distortion compensation include feedforward, predistortion and negative feedback. Feedback is commonly used in a wide range of applications but it can have disadvantages in its actual applications. For example gain in the amplifier to be linearised falls proportionally to the return difference of the feedback loop and this means a compromise of linear performance at the expense of a minor gain which can be unacceptable. Known feedback circuits to overcome this and instability and other problems are complex and often have only a limited success.

We have now devised an amplifier structure which is simple to implement and which reduces distortion.

According to the invention there is provided an amplifier structure which comprises a main amplifier circuit and a subsidiary amplifier circuit, the subsidiary amplifier circuit being able to generate a compensation voltage (as herein defined) which corresponds substantially to the error voltage (as herein defined) of the main circuit the compensation voltage being able to be combined with the error voltage so that when this compensation voltage is inverted and combined with the output of the amplifier, distortion in the main amplifier output is substantially reduced.

The invention also comprises a method of reducing distortion in an amplifier circuit which comprises generating a compensation voltage (as herein defined) and combining the inverted compensation voltage with the output of the amplifier to reduce distortion in the main amplifier circuit.

The error voltage is defined as that part of an output signal which is due to distortion. The output from an amplifier can be considered as consisting of the ideal voltage (which is the undistorted signal required) plus the error voltage (which is defined as the variation introduced by distortion in the circuit). This is true for all

waveforms and amplifiers. By generating a voltage equivalent to this error voltage and inverting this generated voltage the error voltage can be cancelled out leaving the ideal voltage.

The compensation voltage is defined as the voltage generated in the subsidiary circuit which corresponds to the error voltage.

In order to generate the compensation voltage, the subsidiary amplifier circuit can have performance characteristics substantially the same as that of the main amplifier circuit and the input signal is fed into this subsidiary amplifier circuit from a position on the main amplifier circuit at which the ideal voltage is balanced off. This signal will correspond to or be equivalent to an attenuated error voltage and it is then passed through the subsidiary amplifier circuit to compensate for the attenuation so that when it is fed back into the main amplifier circuit it is inverted and combined with the output of the main amplifier It is clear that combining this inverted compensation voltage with the output from the main amplifier circuit will substantially compensate for the error voltage in the output signal and thus reduce the distortion.

The values of the resistors in the in the subsidiary amplifier circuit can be substantially the same as those in the main circuit (although they will have different power ratings) so that the performance characteristics of the circuits are substantially similar. The resistors in the subsidiary circuit have substantially no power currents flowing through them so the values do not depend on the power of the output. They depend principally on the gain of the overall circuit and the characteristics of the operational amplifier.

As the signal fed to the subsidiary amplifier circuit comes from the main amplifier circuit, the input to the subsidiary amplifier circuit will vary as the error voltage varies so that the compensation voltage will correspond closely to the error voltage A circuit diagram illustrating the circuit of the invention is shown in figure 1 of the drawings where R_1, R_2, R1`, R2`, R_2``, R_2```, are resistors. R_1 and R_1` can be of the same value and $R_2$, $R_2$`, and R2`` can be of the same value. Referring to this drawing the main amplifier circuit is shown generally at (1) and can be a conventional operational power amplifier circuit.

The input signal is generated at 4 and the load is at the output at 5. At the point p the ideal voltage can be shown to balance off, so the voltage at point p, which goes to subsidiary amplifier circuit 2 is the error voltage, which will be attenuated by a factor of R_1/R_2. The subsidiary amplifier circuit (2) will amplify the attenuated error voltage so that it becomes the compensation voltage and this is fed back into the main amplifier circuit via R_2''' where it will be inverted and combined with the output at the point 5. The gain in the subsidiary amplifier 2 should be substantially the same as the gain in the main amplifier circuit 1 so the error voltage is substantially reduced by the compensation voltage.

This result arises as, in the absence of the subsidiary circuit, the output voltage at 5, V_O, can be considered as comprising two components V_C, the ideal voltage plus V_E the error voltage. With an input signal V_I and no error voltage, V_O equals V_I x R_2/R_1. At the point p the ideal voltage V_C balances off and so can be ignored at this point. The signal passing to circuit 2 has a value which is V_E attenuated by a factor of $R_1/(R_1+R_2)$..

At the point q in the subsidiary circuit a voltage is generated which is V_E' which substantially has the same value as V_E and is the compensation voltage, this is fed back to point p and is then inverted at A_1 so as to neutralise the error voltage V_E.

The performance characteristics of the subsidiary circuit can be made similar to those of the main amplifier circuit by having the components forming each circuit the same or by having components in each circuit which have corresponding values.

It is a feature of the circuit of the invention that it is stable, as the amplifier in the subsidiary amplifier circuit only operates on the error voltage and so the Nyquist stability criterion does not apply.

In the circuit of the present invention only one power amplifier is required as the main amplifier circuit, the subsidiary amplifier circuit only has very small power e.g. of the order less than 50 milliwatts and can be less than 10 milliwatts. The amplifier in the subsidiary amplifier circuit is preferably a differential amplifier. This enables

an amplifier to be used in the subsidiary amplifier circuit which can be of low power and, at the signal levels obtained, slew rate is of little consequence and so the amplifier can be chosen accordingly.

Preferably the output is earthed on one side and so the load can also be earthed on one side. This is of particular advantage in cascade voltage amplifiers since this enables the amplifiers to be simply interconnected.

The circuit of the present invention provides a cheap simple method of neutralising distortions in an amplifier circuit which avoids the need for complex and costly circuitry and components.

Example

A demonstration circuit was set out as in figure 2, the resistances are expressed as one thousand ohms i.e. 10k is ten thousand ohms. The main or power circuit is shown generally at 1 and the subsidiary circuit is shown generally at 2. At 7 a voltage can be fed in which represents an error voltage. The earthed 100k and 10k resistors in the subsidiary circuit corresponding to R_2``` and R_1` in fig. 1 are equivalent to one resistor of (100k x 10k)/(100k+10k).

In operation the subsidiary circuit was not connected at the point p, and a signal at 1kHz was generated at 4 and an error signal was fed in at 7 of a different frequency this gave an error signal at the output 5. When amplifier circuit 2 was connected into the circuit the error was greatly diminished. In order to measure the reduction in error, the error signal alone was fed into the circuit and gave a wave pattern of peak to peak voltage of 1.3 volts. The circuit 2 was connected in and the peak to peak voltage was reduced to 0.1 volts giving a reduction of 13:1.

Claims

1. An amplifier structure which comprises a main amplifier circuit and a subsidiary amplifier circuit, the subsidiary amplifier circuit being able to generate a compensation voltage (as herein defined) which corresponds substantially to the error voltage (as herein defined) of the main circuit, the compensation voltage, after inversion, being able to be combined with the error voltage so that when this compensation voltage is inverted and combined with the output of the amplifier distortion in the main amplifier output is substantially reduced.

2. An amplifier structure as claimed in claim 1 in which the amplifier in the subsidiary amplifier circuit is a differential amplifier.

3. An amplifier structure as claimed in claim 2 in which the amplifier in the main amplifier circuit is a power amplifier.

4. An amplifier structure as claimed in any one of claims 1 to 3 in which the gain in the subsidiary amplifier circuit is substantially the same as the reciprocal of the gain in the main amplifier circuit.

5. An amplifier structure as claimed in any one of claims 1 to 4 in which the compensation voltage is generated by taking a signal from a point in the main amplifier circuit where the ideal voltage (as herein defined) is balanced off so as to obtain an attenuated error voltage, which attenuated error voltage is amplified in the subsidiary amplifier circuit to obtain a compensation voltage which is substantially the same as the error voltage, which compensation voltage is fed into the main amplifier circuit and inverted so that it substantially nullifies the error voltage to produce an output with reduced distortion.

6. An amplifier structure as described with reference to figure 1 of the drawings.

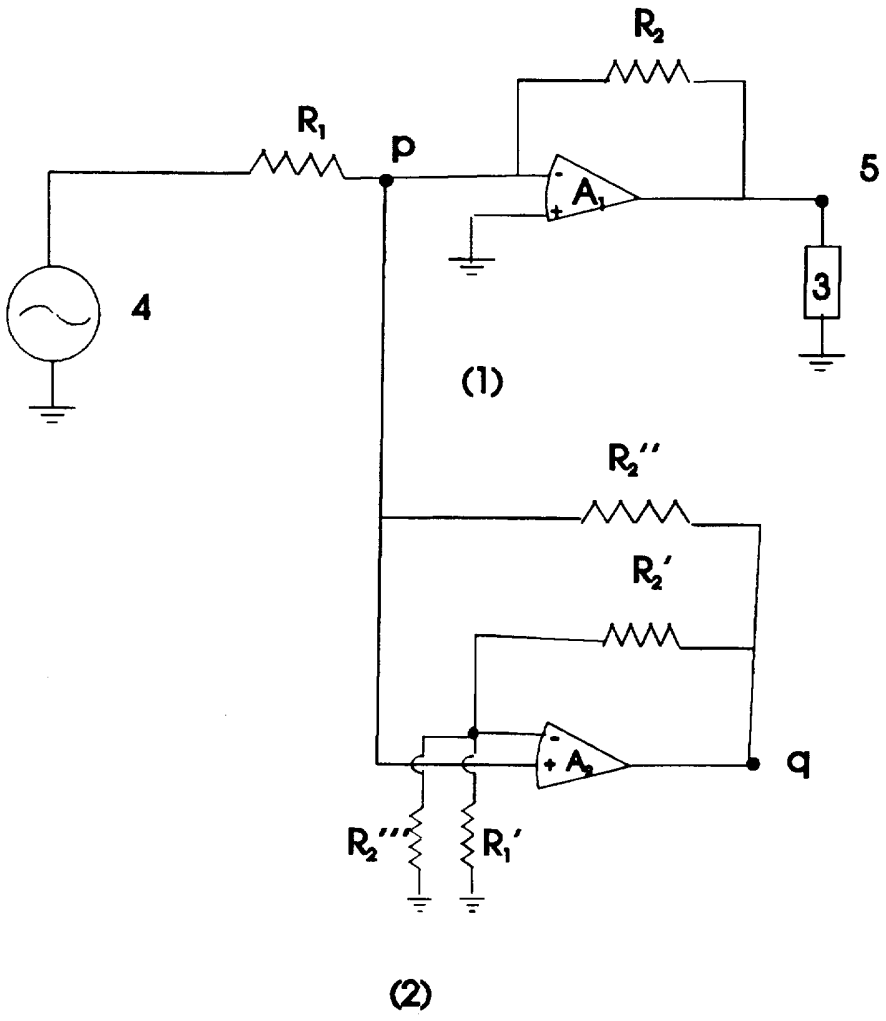

Fig. 1

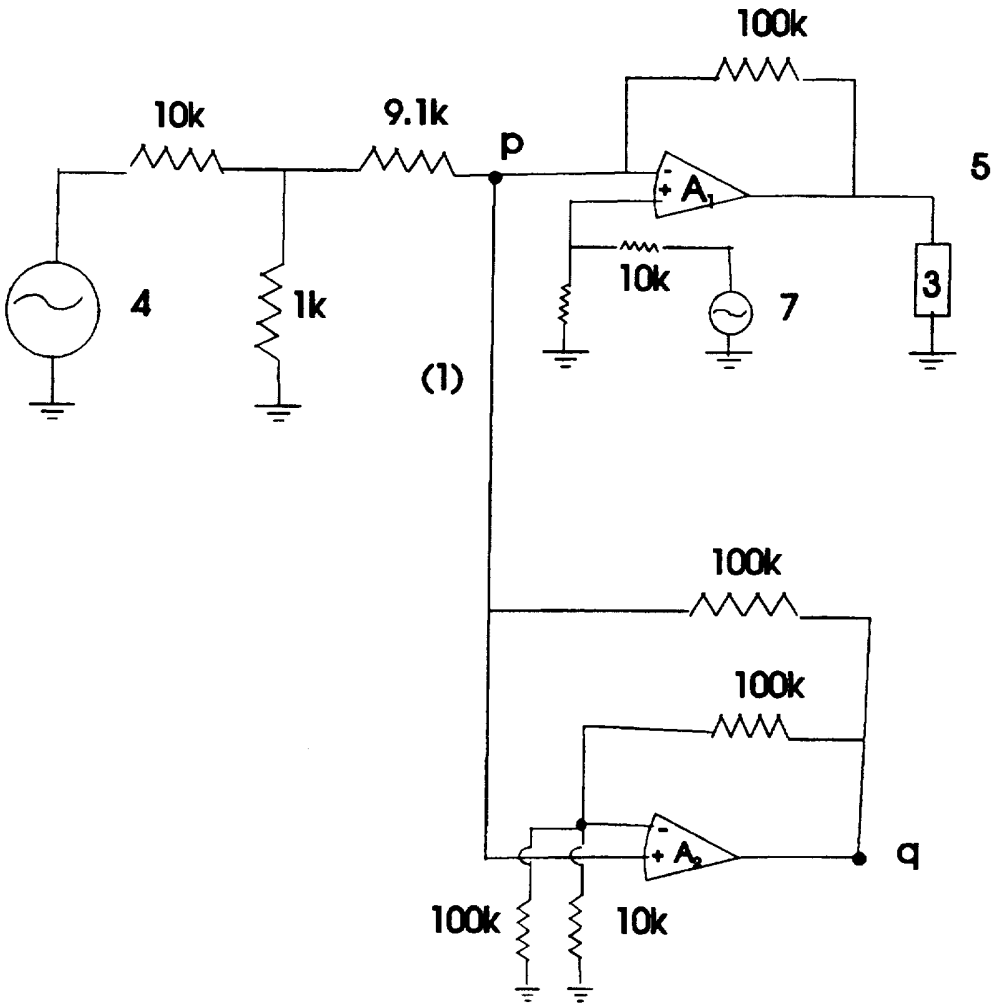

Fig. 2

INTERNATIONAL SEARCH REPORT

Int ional Application No
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A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H03F3/45

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 215 317 A (TRAYNOR ROBERT J) 29 July 1980 see the whole document ---	1-4
A	US 4 207 536 A (LEWIS PAUL H) 10 June 1980 see abstract; figure 1 -----	5

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Information on patent family members

Int ional Application No
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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4215317 A	29-07-80	NONE	
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