

(51) International Patent Classification:
H03J 7/04 (2006.01)(21) International Application Number:
PCT/US2013/053372(22) International Filing Date:
2 August 2013 (02.08.2013)

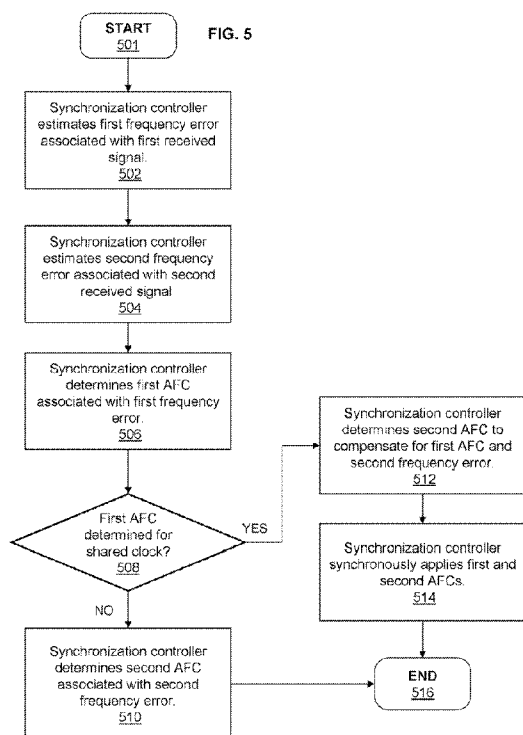
(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
13/589,503 20 August 2012 (20.08.2012) US(71) Applicant: **MOTOROLA MOBILITY LLC** [US/US];
600 North US Highway 45, Libertyville, Illinois 60048
(US).(72) Inventors: **KLOMSDORF, Armin W.**; 2800 N.
Lakeshore Drive, #2710, Chicago, IL 60657 (US). **AL-**
BERTH, JR., William P.; 2715 Cyrstal Way, Prairie
Grove, Illinois 60012 (US). **BLACK, Gregory R.**; 715 S.
Sussex Circle, Vernon Hills, Illinois 60061 (US).(74) Agents: **ANOLICK, Simon B.** et al.; 600 North US High-
way 45, Libertyville, IL 60048 (US).(81) Designated States (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY,
BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM,
DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,
HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KN, KP, KR,
KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME,
MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ,
OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC,
SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN,
TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.(84) Designated States (unless otherwise indicated, for every
kind of regional protection available): ARIPO (BW, GH,
GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ,
UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ,
TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK,
EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV,
MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM,
TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW,
KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: METHOD FOR AUTOMATIC FREQUENCY CORRECTION IN A MULTI-CARRIER COMMUNICATIONS
DEVICE

(57) Abstract: A method and system provides an automatic frequency correction (AFC) within a wireless communication device. A synchronization controller estimates first and second frequency errors respectively associated with a first received signal corresponding to a first receiver path and a second received signal corresponding to a second receiver path. The synchronization controller determines a value and a type of target clock of a first AFC associated with the first frequency error. If the first AFC is not generated to target a shared clock such as a reference clock, the synchronization controller generates a second AFC to compensate for the second frequency error. However, if it is determined that the first AFC targets a shared clock, the synchronization controller generates the second AFC to compensate for the first AFC and the second frequency error. The synchronization controller synchronously applies the first and second AFCs to the relevant clocks.

**METHOD FOR AUTOMATIC FREQUENCY CORRECTION IN A MULTI-CARRIER
COMMUNICATIONS DEVICE**

BACKGROUND

1. Technical Field

[0001] The present disclosure relates in general to wireless communication devices and in particular to frequency correction in wireless communication devices.

2. Description of the Related Art

[0002] Carrier aggregation (CA) increases device throughput and improves network load leveling performance for a wireless communication device. A wireless communication device operating in a CA mode utilizes at least two receivers and/or at least two transmitters. Frequency error values may differ between two corresponding carriers based on a number of factors including cell tower-to-carrier mapping and handover, carrier frequency and Doppler rate. Separate automatic frequency corrections (AFCs) corresponding to two reference and/or system clock domains can be used to respectively compensate for the different frequency error values. Although two reference and/or system clock domains corresponding to separate AFCs can be used, it is more desirable to share the reference/system clock and minimize the number of phase locked loops utilized, especially for single radio frequency (RF) transceiver implementations.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] The described embodiments are to be read in conjunction with the accompanying drawings, wherein:

[0004] **FIG. 1** is a block diagram illustrating an example wireless communication device within which the various features of the described embodiments can be advantageously implemented, according to one embodiment;

[0005] **FIG. 2A** provides a block diagram representation of a transceiver module having a pair of receiver paths and a synchronization module, according to one embodiment;

[0006] **FIG. 2B** provides another block diagram representation of a transceiver module having a pair of receiver paths and a synchronization module, according to one embodiment;

[0007] **FIG. 3** is a block diagram illustrating an embodiment of a transceiver module comprising two signal processing branches showing the various clock components and/or signals from a synchronization module which provides synchronization for carrier aggregation, according to one embodiment;

[0008] **FIG. 4** is a table that provides information about a maximum correction rate and a maximum correction limit for a number of clocks within transceiver **130**, according to one embodiment; and

[0009] **FIG. 5** is a flow chart illustrating one embodiment of a method for providing an automatic frequency correction (AFC) within a wireless communication device, according to one embodiment; and

[0010] **FIG. 6** is a flow chart illustrating one embodiment of a method for determining whether a shared clock is a candidate clock to which a first AFC can be applied, according to one embodiment.

DETAILED DESCRIPTION

[0011] The illustrative embodiments provide a method and system for providing an automatic frequency correction (AFC) within a wireless communication device. A synchronization controller estimates first and second frequency errors respectively associated with a first received signal corresponding to a first receiver path and a second received signal corresponding to a second receiver path. The synchronization controller determines a value and a type of target clock of a first AFC associated with the first frequency error. If the first AFC is not generated to target a shared clock such as a reference clock, the synchronization controller generates a second AFC to compensate for the second frequency error. However, if the first AFC is determined to target a shared clock such as the reference clock, the synchronization controller generates the second AFC to compensate for the first AFC and the second frequency error. The synchronization controller synchronously applies the first and second AFCs to the relevant clocks.

[0012] In the following detailed description of exemplary embodiments of the disclosure, specific exemplary embodiments in which the various aspects of the disclosure may be practiced are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, architectural, programmatic, mechanical, electrical and other changes may be made without departing from the spirit or scope of the present disclosure. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present disclosure is defined by the appended claims and equivalents thereof.

[0013] Within the descriptions of the different views of the figures, similar elements are provided similar names and reference numerals as those of the previous figure(s). The specific numerals assigned to the elements are provided solely to aid in the description and are not meant to imply any limitations (structural or functional or otherwise) on the described embodiment.

[0014] It is understood that the use of specific component, device and/or parameter names, such as those of the executing utility, logic, and/or firmware described herein, are for example only and not meant to imply any limitations on the described embodiments. The embodiments may thus be described with different nomenclature and/or terminology utilized to describe the components, devices, parameters, methods and/or functions herein, without limitation.

References to any specific protocol or proprietary name in describing one or more elements, features or concepts of the embodiments are provided solely as examples of one implementation, and such references do not limit the extension of the claimed embodiments to embodiments in which different element, feature, protocol, or concept names are utilized. Thus, each term utilized herein is to be given its broadest interpretation given the context in which that terms is utilized.

[0015] As further described below, implementation of the functional features of the disclosure described herein is provided within processing devices and/or structures and can involve use of a combination of hardware, firmware, as well as several software-level constructs (e.g., program code and/or program instructions and/or pseudo-code) that execute to provide a specific utility for the device or a specific functional logic. The presented figures illustrate both hardware components and software and/or logic components.

[0016] Those of ordinary skill in the art will appreciate that the hardware components and basic configurations depicted in the figures may vary. The illustrative components are not intended to be exhaustive, but rather are representative to highlight essential components that are utilized to implement aspects of the described embodiments. For example, other devices/components may be used in addition to or in place of the hardware and/or firmware depicted. The depicted example is not meant to imply architectural or other limitations with respect to the presently described embodiments and/or the general invention.

[0017] The description of the illustrative embodiments can be read in conjunction with the accompanying figures. It will be appreciated that for simplicity and clarity of illustration, elements illustrated in the figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements are exaggerated relative to other elements. Embodiments incorporating teachings of the present disclosure are shown and described with respect to the figures presented herein.

[0018] With specific reference now to **FIG. 1**, there is depicted a block diagram of an example wireless communication device **100**, within which the functional aspects of the described embodiments may be implemented. Wireless communication device **100** represents a device that is adapted to transmit and receive electromagnetic signals over an air interface via uplink and/or downlink channels between the wireless communication device **100** and communication network equipment (e.g., base-stations **145**, **147**) utilizing a plurality of different communication

standards, such as Global System for Mobile Communications (GSM) Code Division Multiple Access (CDMA), Orthogonal Frequency Division Multiple Access (OFDMA), and similar systems. In addition, wireless communication device **100** is able to utilize a number of communication standards such as carrier aggregation and simultaneous voice and LTE (SVLTE). In one or more embodiments, the wireless communication device can be a mobile cellular device/phone or smartphone, or laptop, netbook or tablet computing device, or other types of communications devices. Wireless communication device **100** comprises processor **105** and interface circuitry **125**, which are connected to memory component **110** via signal bus **102**. Interface circuitry **125** includes digital signal processor (DSP) **128**. Wireless communication device **100** also includes a transceiver module **130** for sending and receiving communication signals. In at least some embodiments, the sending and receiving of communication signals occur wirelessly and are facilitated by one or more antennas **140** and **142** coupled to the transceiver module **130**. The number of antennas can vary from device to device, ranging from a single antenna to two or more antennas, and the presentation within wireless communication device **100** of two antennas **140**, **142** is merely for illustration.

[0019] Wireless communication device **100** is able to wirelessly communicate to base-stations **145** and **147** via antenna **140** and/or antenna **142**. Base stations **145**, **147** can be any one of a number of different types of network stations and/or antennas associated with the infrastructure of the wireless network and configured to support uplink and downlink communication via one or more of the wireless communication protocols, as known by those skilled in the art.

[0020] Transceiver module **130** comprises baseband modem integrated circuit (BBIC) **133** and radio frequency integrated circuit (RFIC) **132**. Transceiver module **130** comprises a memory or storage system **150**, synchronization controller **160** and first and second receiver paths **202A**, **202B** and **222A**, **222B**. First and second receiver paths **202A**, **202B** and **222A**, **222B** comprise a number of components shown in **FIGs. 2A** and **2B**. Synchronization controller **160** is communicatively coupled to both first and second receiver paths **202A**, **202B** and **222A**, **222B**. In one embodiment, transceiver module **130** also includes local processor **155**, which can be described as a digital signal processor (DSP). According to one aspect of the disclosure, local memory/storage **150** includes therein firmware, such as Antenna Frequency Correction (AFC) utility **167**, which supports the various processing functions of transceiver module **130**. The structural makeup of transceiver module **130** is described in greater detail in **FIGs. 2A** and **2B**.

[0021] In addition to the above described hardware components of wireless communication device **100**, various features of the invention may be completed or supported via software (or firmware) code and/or logic stored within at least one of memory **110** and local memory **150**, and respectively executed by DSP **128**, Processor **105**, or local processor **155** of transceiver module **130**. Thus, for example, illustrated within memory **110** are a number of software/firmware/logic components/modules, including current correction count and rate data **114**, applications **116** and AFC utility **167**.

[0022] The various components within wireless communication device **100** can be electrically and/or communicatively coupled together as illustrated in **FIG. 1**. As utilized herein, the term “communicatively coupled” means that information signals are transmissible through various interconnections between the components. The interconnections between the components can be direct interconnections that include conductive transmission media, or may be indirect interconnections that include one or more intermediate electrical components. Although certain direct interconnections are illustrated in **FIG. 1**, it is to be understood that more, fewer or different interconnections may be present in other embodiments.

[0023] **FIG. 2A** provides a block diagram representation of a transceiver module having a pair of receiver paths and a synchronization module, according to one embodiment. Transceiver module **130** comprises first receiver path **202A** and second receiver path **222A**. Each receiver path (**202A**, **222A**) comprises (a) RF signal processing stages of RFIC **132** and (b) baseband and intermediate frequency (IF) signal processing stages of BBIC **133**. In addition, transceiver module **130** comprises synchronization module **240** and frequency error estimator **260** which is coupled to synchronization module **240**. Also included within transceiver module **130** is reference clock **246**.

[0024] First receiver path **202A** comprises down-converter **206**, first RF local oscillator (LO) **242** and analog to digital (A/D) converter **208**. Down-converter **206** is communicatively coupled to both first RF LO **242** and analog to digital (A/D) converter **208**. Down-converter **206**, first RF LO **242** and analog to digital (A/D) converter **208** are located within RFIC **132**. Illustrated along first receiver path **202A** within BBIC **133** are de-rotation component **210** and OFDM time-frequency converter module **212**, which comprises filter **214**. Additional components of BBIC **133** which are also illustrated along first receiver path **202A** include detector **216** and decoder **218**. Antenna **140** is communicatively coupled to first receiver path **202A**.

[0025] Second receiver path **222A** comprises down-converter **226**, second RF LO **244** and analog to digital (A/D) converter **228**. Down-converter **226** is communicatively coupled to both second RF LO **244** and analog to digital (A/D) converter **228**. Down-converter **226**, second RF LO **244** and analog to digital (A/D) converter **228** are located within RFIC **132**. Illustrated along second receiver path **222A** and within BBIC **133** are de-rotation component **230** and OFDM time-to-frequency converter module **232**, which comprises filter **234**. Additional components of BBIC **133** which are also illustrated along second receiver path **222A** include detector **236**, and decoder **238**. Antenna **142** is communicatively coupled to second receiver path **222A**.

[0026] As illustrated, frequency error estimator **260** is coupled to first and second receiver paths **202A** and **222A**, and in particular to output ports of detectors **216**, **236**. However, one skilled in the art is aware that frequency error estimator **260** can be coupled at any one of various alternate locations in order to generate frequency error estimates.

[0027] Synchronization module **240** comprises system clock **248**, which is coupled to reference clock **246**, and from which the various LOs are able to generate the respective synchronization signals. Also illustrated within synchronization module **240** is synchronization controller **160**. In one embodiment, synchronization controller **160** is respectively coupled to each of first RF LO **242**, second RF LO **244**, and system clock **248** in order to receive, adjust and/or distribute the various synchronization signals accordingly. Several inputs **265** which can include correction count and correction rate data **114** are received by synchronization module **240**, and in particular, by synchronization controller **160**. In one embodiment, in response to obtaining frequency error estimates, synchronization controller **160** is able to apply automatic frequency corrections (AFCs) to the respective clocks and/or oscillators, as illustrated within **FIG. 3**.

[0028] **FIG. 2A** provides a first implementation of transceiver **130** in which synchronization controller **160** is coupled to de-rotation components **210** and **230** within a respective receiver path. **FIG. 2B** provides a second implementation of transceiver **130** in which synchronization controller **160** is coupled to digital low IF mixer LOs **252** and **254** within a respective receiver path. The calculation of AFC values and selection of corresponding AFC target types are described in further detail within the description of **FIG. 3**.

[0029] **FIG. 2B** provides another block diagram representation of a transceiver module having a pair of receiver paths and a synchronization module, according to one embodiment. Transceiver module **130** comprises first receiver path **202B** and second receiver path **222B**. In addition,

transceiver module **130** comprises synchronization module **240** and frequency error estimator **260** which is coupled to synchronization module **240**. Also included within transceiver module **130** is reference clock **246**. Similar to the implementation of **FIG. 2A**, in **FIG. 2B**, each receiver path (**202A**, **202B** and **222A**, **222B**) comprises (a) RF signal processing stages of RFIC **132** and (b) baseband and intermediate frequency (IF) signal processing stages of BBIC **133**. Between the implementations of **FIGs. 2A** and **2B**, the RF signal processing stages of RFIC **132** provide similar components. However, the baseband and intermediate frequency (IF) signal processing stages of BBIC **133** provide different components between the implementations of **FIGs. 2A** and **2B**.

[0030] First receiver path **202B** comprises down-converter **206**, first RF LO **242** and analog to digital (A/D) converter **208**. Down-converter **206** is communicatively coupled to both first RF LO **242** and analog to digital (A/D) converter **208**. Down-converter **206**, first RF LO **242** and analog to digital (A/D) converter **208** are located within RFIC **132**. Illustrated along first receiver path **202B** within BBIC **133** are digital low IF mixer LO **252** and digital low IF mixer **253** which is coupled to digital low IF mixer LO **252**. Within first receiver path **202B**, BBIC **133** also comprises OFDM time-to-frequency converter module **212**, which comprises filter **214**. Additional components of BBIC **133** which are also illustrated along first receiver path **202B** include detector **216** and decoder **218**. Antenna **140** is communicatively coupled to first receiver path **202B**.

[0031] Second receiver path **222B** comprises down-converter **226**, second RF LO **244** and analog to digital (A/D) converter **228**. Down-converter **226** is communicatively coupled to both second RF LO **244** and analog to digital (A/D) converter **228**. Down-converter **226**, second RF LO **244** and analog to digital (A/D) converter **228** are located within RFIC **132**. Illustrated along second receiver path **222B** within BBIC **133** are digital low IF mixer LO **254** and digital low IF mixer **255** which is coupled to digital low IF mixer LO **254**. Within second receiver path **222B**, BBIC **133** also comprises OFDM time-frequency converter module **232**, which comprises filter **234**. Additional components of BBIC **133** which are also illustrated along second receiver path **222B** include detector **236**, and decoder **238**. Antenna **142** is communicatively coupled to second receiver path **222B**.

[0032] As illustrated, frequency error estimator **260** is coupled to first and second receiver paths **202B** and **222B**, and in particular to output ports of detectors **216**, **236**. However, one skilled in

the art is aware that frequency error estimator **260** can be coupled at any one of various alternate locations in order to generate frequency error estimates.

[0033] Synchronization module **240** comprises system clock **248**, which is coupled to reference clock **246**, and from which the various LOs are able to generate the respective synchronization signals. Also illustrated within synchronization module **240** is synchronization controller **160**. In one embodiment, synchronization controller **160** is respectively coupled to each of first RF LO **242**, second RF LO **244**, and system clock **248** in order to receive, adjust and/or distribute the various synchronization signals accordingly. Several inputs **265** which can include correction count and correction rate data **114** are received by synchronization module **240**, and in particular, by synchronization controller **160**.

[0034] FIG. 3 is a block diagram illustrating an embodiment of a transceiver module comprising two signal processing branches showing the various clock components and/or signals from the synchronization module that provide synchronization for carrier aggregation, according to one embodiment. Transceiver module **130** comprises first receiver path **302** and second receiver path **322**. First receiver path **302** comprises a down-converter and analog to digital (A/D) converter (not shown), a first RF LO **342**, and first digital low IF mixer LO **352**. In one embodiment, first receiver path **302** also comprises a digital de-rotation component **355**. Also illustrated in first receiver path **302** is a first AFC signal illustrated as AFC#1 **349**. AFC#1 **349** is also shown in a second instance connecting to reference clock **346**. Although AFC#1 **349** is illustrated as targeting first RF LO **342** and reference clock **346**, the illustration is intended to depict two options for a target of a first AFC.

[0035] Second receiver path **322** comprises a down-converter and analog to digital (A/D) converter (not shown), a second RF LO **344**, and first digital low IF mixer LO **354**. In one embodiment, second receiver path **322** also comprises a digital de-rotation component **356**. Also illustrated in second receiver path **322** is a second AFC signal illustrated as AFC#2 **351**. Transceiver module **130** comprises reference clock **346** and system clock **348**. Antenna **340** is communicatively coupled to both first receiver path **302** and second receiver path **322**.

[0036] In first receiver path **302**, first RF LO **342** provides synchronization within RFIC **132** (FIG. 1) for a received RF signal provided by a first carrier. First digital low IF mixer LO **352** provides synchronization within BBIC **133** for at least one of a baseband signal and an IF signal

provided by the first carrier. The baseband signal and the IF signal provided by the first carrier are down-converted signals corresponding to the received RF signal provided by the first carrier.

[0037] Similarly, in second receiver path **322**, second RF LO **344** provides synchronization within RFIC **132** for a received RF signal provided by a second carrier. Second digital low IF mixer LO **354** provides synchronization within BBIC **133** for at least one of a baseband signal and an IF signal provided by the second carrier. The baseband signal and the IF signal provided by the second carrier are down-converted signals corresponding to the received RF signal provided by the second carrier.

[0038] Synchronization controller **160** estimates (a) a first frequency error between the first received RF signal and a shared synchronization signal provided by reference clock **346** and (b) a second frequency error between a second received RF signal and the shared synchronization signal. The first frequency error and the second frequency error are respectively affected by at least one of: (a) a mapping of specific carrier frequencies to a particular cell tower associated with a respective received signal; (b) a change to the mapping of specific carrier frequencies associated with a handover procedure; and (c) a Doppler rate corresponding to a respective received signal. For example, a first received signal received from a first base-station **145** and which corresponds to first receiver path **202A**, **202B** may exhibit a different Doppler rate compared to the Doppler rate exhibited by a second received signal received from a second base-station **147** and which corresponds to second receiver path **222A**, **222B**.

[0039] Synchronization controller **160** determines a first AFC for the first frequency error. In particular, synchronization controller **160** determines a value and a type (i.e., a target clock type) for the first AFC. In addition, synchronization controller **160** determines a second AFC based on (a) values corresponding to the second frequency error and (b) the first AFC determined. Synchronization controller **160** synchronously applies (a) the determined first AFC to compensate for the first frequency error and (b) the second AFC determined using the second frequency error.

[0040] Synchronization controller **160** selects a type of the first AFC that provides at least one of: (a) an adjustment to a shared synchronization signal; (b) an adjustment to an exclusively local synchronization signal; and (c) a de-rotation of a first carrier signal corresponding to the first received signal. The shared synchronization signal is one of (a) a shared reference clock signal and (b) a shared system clock signal. The exclusively local synchronization signal is one of (a)

an unshared RF local oscillator signal and (b) a digital low intermediate frequency (IF) mixer LO signal corresponding to a respective received signal. In response to selecting the type of the first AFC that provides an adjustment to at least the shared synchronization signal, synchronization controller **160** calculates a second AFC using values corresponding to (a) the second frequency error and (b) the adjustment to the at least the shared synchronization signal provided by the first AFC. In response to not selecting the type of the first AFC that provides an adjustment to at least the shared synchronization signal, synchronization controller **160** calculates the second AFC utilizing values corresponding to the second frequency error. In this case, the second AFC is not calculated based on an adjustment associated with the first AFC.

[0041] In general, synchronization controller **160** applies the second AFC as at least one of (i) an adjustment to an exclusively local synchronization signal for the second received signal and (ii) a de-rotation of a second carrier signal corresponding to the second received signal. Furthermore, synchronization controller **160** selects a type of a first AFC to apply from among: (a) a first type that provides an adjustment to the shared reference clock signal; (b) a second type that provides an adjustment to a first radio frequency (RF) local oscillator (LO); (c) a third type that provides a de-rotation of a first carrier signal corresponding to the first received signal; and (d) a fourth type that provides an adjustment to a digital low intermediate frequency (IF) mixer LO corresponding to the first received signal.

[0042] In general, an AFC is applied to a single target. However, synchronization controller **160** is able to apply at least two partial corrections corresponding to a single AFC, as is explained within the description of table **400** of FIG. 4.

[0043] FIG. 4 is a table that provides information about a maximum correction rate and a maximum correction limit for a number of clocks within transceiver **130**, according to one embodiment. Table **400** provides clock or synchronization source IDs in a first column and, in a second column, tolerance level of specific applications dependent on the clock for timing and/or synchronization, which applications are sensitive to changes in a corresponding clock signal. An AFC applied to a shared reference or system clock may be restricted to a maximum correction rate and/or maximum correction limit if the reference clock is also shared with an application that is particularly intolerant of frequency or phase changes (e.g. GPS).

[0044] In addition, table **400** provides, in a third column, a maximum correction rate that controls a rate at which adjustments are applied to a corresponding clock while the application is

running. In a fourth column, table **400** provides a maximum correction limit for a number of instances that adjustments (e.g., AFC#1) can be applied to a corresponding clock while the application is running. Additionally, table **400** provides, in a fifth column, a value for the number of dependent receiver paths impacted by changes to a corresponding clock signal. In one embodiment, table **400** is stored in local memory **150**.

[0045] Synchronization controller **160** establishes at least one of a maximum correction rate and a maximum correction limit associated with the shared reference clock signal, which is associated with a specific tolerance level of an application for frequency changes and phase changes. The specific tolerance level is used to establish at least one of the maximum correction rate and the maximum correction limit associated with the shared reference clock signal.

[0046] Synchronization controller **160** applies a first correction that does not cause a violation of the at least one of the maximum correction rate and the maximum correction limit to the shared reference clock signal. The first correction is one of (a) the first AFC and (b) a partial correction corresponding to the first AFC. Synchronization controller **160** selects the type of AFC to apply based on at least one of: (a) the maximum correction rate; (b) the maximum correction limit; (c) a complexity associated with an adjustment; and (d) a number of further adjustments that are triggered by selection of a particular type of AFC.

[0047] Referring specifically to table **400**, first row **402** of table **400** provides information to guide an AFC of a reference clock. “App1” is identified as an application that is sensitive to adjustments and/or AFCs applied to the reference clock. In particular, tolerance level “c” is a value that provides a quantitative measure of the sensitivity of App1 to adjustments to the reference clock. First row **402** also provides specific values, “rate1” for maximum correction rate and “limit1” for maximum correction limit. These values are both used to guide changes to the reference clock when App1 is running. In addition, first row **402** indicates that two receiver paths are affected by changes to the reference clock.

[0048] Second row **404** also provides information that synchronization controller **160** uses to determine whether to apply an AFC to a reference clock. However, the information is provided for a different “sensitive” application “App2” that has a different tolerance level, “d”. A “sensitive” application is described herein as an application having a tolerance level (to changes

to the reference clock) that is less than a pre-determined threshold minimum level. Third row **406** provides information to determine whether to apply an AFC to a system clock. Fourth row **408** provides information to determine whether to apply an AFC to a shared clock identified in table **400** as “shared clock”. Synchronization controller **160** is able to utilize information retrieved from second row **404**, third row **406** and fourth row **408** similarly to the manner in which synchronization controller **160** is able to utilize the information in first row **402**.

[0049] In one embodiment, synchronization controller **160** determines whether to apply a first AFC to the reference clock by determining whether any application identified within the corresponding rows of a second column of table **400** (i.e., any application that is particularly sensitive to changes to the reference clock) is running. In response to determining that at least one of the applications (e.g., App1) that is particularly sensitive to changes to the reference clock is executing, synchronization controller **160** retrieves a current count of the number of AFCs to the reference clock while the at least one application is running. In addition, synchronization controller **160** retrieves a correction rate that provides an updated value for the rate at which AFCs are applied to the reference clock while the at least one application is running. Synchronization controller **160** compares the retrieved values for maximum correction rate and maximum correction limit and respectively compares these retrieved values to the current count of the number of AFCs applied to the reference clock and the current correction rate. As a result, synchronization controller **160** determines whether there is at least one application with corresponding current count and/or correction rate values that equal the maximum correction rate and maximum correction limit values. In one embodiment, if synchronization controller **160** determines that there is at least one application with corresponding current count and/or correction rate values that equal the maximum correction rate and maximum correction limit values retrieved from table **400**, synchronization controller **160** does not apply an AFC to the reference clock and selects another type of AFC to apply. However, if synchronization controller **160** determines that there is no application with corresponding current count and/or correction rate values that equal the maximum correction rate and maximum correction limit values retrieved from table **400**, synchronization controller **160** applies the AFC to the reference clock and updates the current count and correction rate.

[0050] In another embodiment, if the current count and correction rate values are both less than the maximum correction rate and maximum correction limit values, and if all the receiver paths that are affected by changes to the reference clock are actively propagating received signals, synchronization controller **160** is able to apply an AFC to the reference clock if the number of actively propagating receiver paths is less than a threshold number of receiver paths affected by AFCs to the reference clock. Synchronization controller **160** uses the threshold number of receiver paths affected by AFCs to the reference clock to avoid and/or minimize a complexity associated with providing compensation within a number of second AFCs corresponding to the receiver paths that can be affected.

[0051] In one embodiment, table **400** includes information for maximum phase change and/or maximum frequency change. Synchronization controller **160** utilizes the maximum allowed phase change and/or maximum allowed frequency change to determine the maximum level of adjustment that is allowed by any single AFC applied to a shared clock such as the reference clock when a respective application is running. As a result, synchronization controller **160** is able to perform partial AFCs. In particular, synchronization controller **160** can perform a first partial correction (i.e., a correction that is less than a complete AFC) to the reference clock up to a specified maximum allowed phase change and a remainder of the complete AFC can be performed using another partial AFC on a clock which provides synchronization for a corresponding received signal and is not utilized by the respective application.

[0052] **FIGs. 5 and 6** are flow charts illustrating an embodiment of the method by which the above processes of the illustrative embodiments can be implemented. Specifically, **FIG. 5** illustrates one embodiment of a method for providing automatic frequency corrections within a wireless communication device. **FIG. 6** illustrates one embodiment of a method for determining whether a shared clock such as reference clock **246** is a candidate clock to which a first AFC can be applied. Although the method illustrated by **FIGs. 5 and 6** may be described with reference to components and functionality illustrated by and described in reference to **FIGs. 1-4**, it should be understood that this is merely for convenience and alternative components and/or configurations thereof can be employed when implementing the method. Certain portions of the methods may be completed by AFC utility **167** executing on one or more processors (processor **105** or DSP **128**) within wireless communication device **100** (**FIG. 1**), or local processor **155** or synchronization controller **160** of transceiver module **130** (**FIG. 1 and 2**). The executed

processes then control specific operations of or on transceiver module **130**. For simplicity in describing the method, all method processes are described from the perspective of transceiver module **130** and specifically synchronization controller **160**.

[0053] The method of **FIG. 5** begins at initiator block **501** and proceeds to block **502** at which synchronization controller **160** estimates a first frequency error associated with a first received signal corresponding to a first receiver path. At block **504**, synchronization controller **160** estimates a second frequency error associated with a second received signal corresponding to a second receiver path. At block **506**, synchronization controller **160** determines a first AFC associated with the first frequency error. At decision block **508**, synchronization controller **160** determines whether the first AFC is determined to target a shared clock such as reference clock **246**. If at decision block **508**, synchronization controller **160** determines that the first AFC is not determined to target a shared clock such as reference clock **246**, synchronization controller **160** determines/generated the second AFC to compensate for the second frequency error, as shown at block **510**. However, if at decision block **508**, synchronization controller **160** determines that the first AFC is determined to target a shared clock such as reference clock **246**, synchronization controller **160** generates the second AFC to compensate for the first AFC and the second frequency error, as shown at block **512**. At block **514**, synchronization controller **160** synchronously applies the first and second AFCs to the relevant clocks. The process ends at block **516**.

[0054] The method of **FIG. 6** begins at initiator block **601** and proceeds to decision block **602** at which synchronization controller **160** determines whether an application having less than a threshold minimum tolerance level to changes in a corresponding clock signal is running. An application having less than the threshold minimum tolerance level is described herein as a “sensitive” application. Synchronization controller **160** determines whether an application having less than a threshold minimum tolerance level is running in order to initiate a process to determine whether a shared clock such as reference clock **246** is a candidate clock to which a first AFC can be applied. If at decision block **602**, synchronization controller **160** determines that no application having less than the threshold minimum tolerance level is running, synchronization controller **160** determines that the reference clock is a candidate clock to which the first AFC can be applied, as shown at block **618**. However, if at decision block **602**,

synchronization controller **160** determines that at least one application having less than the threshold minimum tolerance level is running, synchronization controller **160** retrieves the current correction count and correction rate data, as shown at block **604**. At block **606**, synchronization controller **160** retrieves the maximum correction limit and correction rate data. At block **608**, synchronization controller **160** respectively compares the current correction count and current correction rate with the maximum correction limit and the maximum correction rate.

[0055] At decision block **610**, synchronization controller **160** determines whether at least one of the current correction count and the current correction rate respectively equals the maximum correction limit and the maximum correction rate, for at least one currently executing application. If at decision block **610**, synchronization controller **160** determines that there is at least one currently executing application for which at least one of the current correction count and the current correction rate respectively equals the maximum correction limit and the maximum correction rate, synchronization controller **160** determines that the reference clock is not a candidate clock to which the first AFC can be applied, as shown at block **612**. However, if at decision block **610**, synchronization controller **160** determines that there is no currently executing application for which at least one of the current correction count and the current correction rate respectively equals the maximum correction limit and the maximum correction rate, synchronization controller **160** determines whether the phase change corresponding to the first AFC exceeds the maximum phase change that can be tolerated by at least one “sensitive application”, as shown at block **614**. If at decision block **614**, synchronization controller **160** determines that the phase change corresponding to the first AFC exceeds the maximum phase change that can be tolerated by at least one “sensitive application”, synchronization controller **160** determines that the reference clock is not a candidate clock to which the first AFC can be applied, as shown at block **612**. However, if at decision block **614**, synchronization controller **160** determines that the phase change corresponding to the first AFC does not exceed the maximum phase change that can be tolerated by at least one “sensitive application”, synchronization controller **160** determines that the reference clock is a candidate clock to which the first AFC can be applied, as shown at block **618**. The process ends at block **620**.

[0056] The flowchart and block diagrams in the various figures presented and described herein illustrate the architecture, functionality, and operation of possible implementations of systems, methods and computer program products according to various embodiments of the present

disclosure. In this regard, each block in the flowcharts or block diagrams may represent a module, segment, or portion of code, which comprises one or more executable instructions for implementing the specified logical function(s). It should also be noted that, in some alternative implementations, the functions noted in the block may occur out of the order noted in the figures. For example, two blocks shown in succession may, in fact, be executed substantially concurrently, or the blocks may sometimes be executed in the reverse order, depending upon the functionality involved. Thus, while the method processes are described and illustrated in a particular sequence, use of a specific sequence of processes is not meant to imply any limitations on the disclosure. Changes may be made with regards to the sequence of processes without departing from the spirit or scope of the present disclosure. Use of a particular sequence is therefore, not to be taken in a limiting sense, and the scope of the present disclosure extends to the appended claims and equivalents thereof.

[0057] In some implementations, certain processes of the methods are combined, performed simultaneously or in a different order, or perhaps omitted, without deviating from the spirit and scope of the disclosure. It will also be noted that each block of the block diagrams and/or flowchart illustration, and combinations of blocks in the block diagrams and/or flowchart illustration, can be implemented by special purpose hardware-based systems that perform the specified functions or acts, or combinations of special purpose hardware and computer instructions.

[0058] While the disclosure has been described with reference to exemplary embodiments, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted for elements thereof without departing from the scope of the disclosure. In addition, many modifications may be made to adapt a particular system, device or component thereof to the teachings of the disclosure without departing from the essential scope thereof. Therefore, it is intended that the disclosure not be limited to the particular embodiments disclosed for carrying out this disclosure, but that the disclosure will include all embodiments falling within the scope of the appended claims. Moreover, the use of the terms first, second, etc. do not denote any order or importance, but rather the terms first, second, etc. are used to distinguish one element from another.

[0059] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the disclosure. As used herein, the singular forms "a", "an"

and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0060] The corresponding structures, materials, acts, and equivalents of all means or step plus function elements in the claims below are intended to include any structure, material, or act for performing the function in combination with other claimed elements as specifically claimed. The description of the present disclosure has been presented for purposes of illustration and description, but is not intended to be exhaustive or limited to the disclosure in the form disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the disclosure. The embodiment was chosen and described in order to best explain the principles of the disclosure and the practical application, and to enable others of ordinary skill in the art to understand the disclosure for various embodiments with various modifications as are suited to the particular use contemplated.

CLAIMS

What is claimed is:

1. A method for providing automatic frequency correction (AFC) in a wireless communication device having at least two transceivers, the method comprising:

estimating a first frequency error between a first received signal corresponding to a first transceiver and a shared reference clock signal;

estimating a second frequency error between a second received signal corresponding to a second transceiver and the shared reference clock signal;

determining a first AFC for the first frequency error;

determining a second AFC based on (a) values corresponding to the second frequency error and (b) the first AFC determined; and

synchronously applying (a) the determined first AFC to compensate for the first frequency error and (b) the second AFC determined using the second frequency error.

2. The method of Claim 1, wherein said determining the first AFC further comprises:

selecting a type of the first AFC that provides at least one of: (a) an adjustment to a shared synchronization signal; (b) an adjustment to an exclusively local synchronization signal; and (c) a de-rotation of a first carrier signal corresponding to the first received signal;

in response to selecting the type of the first AFC that provides an adjustment to at least the shared synchronization signal, calculating a second AFC using values corresponding to (a) the second frequency error and (b) the adjustment to the at least the shared synchronization signal provided by the first AFC; and

in response to not selecting the type that provides an adjustment to the shared synchronization signal, calculating the second AFC utilizing values corresponding to the second frequency error, wherein the second AFC is not calculated based on an adjustment associated with the first AFC.

3. The method of Claim 2, wherein said synchronously applying further comprises:
applying the second AFC as at least one of (i) an adjustment to an exclusively local synchronization signal for the second received signal and (ii) a de-rotation of a second carrier signal corresponding to the second received signal.
4. The method of Claim 3, wherein:
the shared synchronization signal is one of (a) a shared reference clock signal and (b) a shared system clock signal;
the exclusively local synchronization signal is one of (a) an unshared RF local oscillator signal and (b) a digital low intermediate frequency (IF) mixer LO signal corresponding to a respective received signal.
5. The method of Claim 1, further comprising:
establishing at least one of a maximum correction rate and a maximum correction limit associated with the shared reference clock signal, wherein the shared reference clock signal is utilized by an application associated with a specific tolerance level for frequency changes and phase changes, and the specific tolerance level is used to establish at least one of the maximum correction rate and the maximum correction limit associated with the shared reference clock signal; and
applying a first correction that does not cause a violation of the at least one of the maximum correction rate and the maximum correction limit to the shared reference clock signal, wherein the first correction is one of (a) the first AFC; and (b) a partial correction corresponding to the first AFC.
6. The method of Claim 5, further comprising:
selecting the type of AFC to apply based on at least one of: (a) the maximum correction rate; (b) the maximum correction limit; (c) a complexity associated with an adjustment; and (d) a number of further adjustments that are triggered by selection of a particular type of AFC; and
wherein the type of AFC is one of: (a) a first type that provides an adjustment to the shared reference clock signal; (b) a second type that provides an adjustment to a first radio frequency (RF) local oscillator (LO); (c) a third type that provides a de-rotation of a first carrier

signal corresponding to the first received signal; and (d) a fourth type that provides an adjustment to a digital low intermediate frequency (IF) mixer LO corresponding to the first received signal.

7. The method of Claim 1, wherein:

the first frequency error and the second frequency error are respectively affected by at least one of: (a) a mapping of specific carrier frequencies to a particular cell tower associated with a respective received signal; (b) a change to the mapping of specific carrier frequencies associated with a handover procedure; and (c) a Doppler rate corresponding to a respective received signal.

8. A transceiver integrated circuit (IC) comprising:

at least two transceivers;

a shared reference clock utilized for signal detection at a first transceiver and a second transceiver;

a frequency error estimator that estimates: (a) a first frequency error between a first received signal corresponding to a first transceiver and the shared reference clock signal; and (b) a second frequency error between a second received signal corresponding to a second transceiver and the shared reference clock signal; and

an automatic frequency correction (AFC) module that:

determines a first AFC for the first frequency error;

determines a second AFC based on (a) values corresponding to the second frequency error and (b) the first AFC determined; and

synchronously applies (a) the determined first AFC to compensate for the first frequency error; and (b) the second AFC determined using the second frequency error.

9. The transceiver IC of Claim 8, wherein the AFC module:

selects a type of the first AFC that provides at least one of: (a) an adjustment to a shared synchronization signal; (b) an adjustment to an exclusively local synchronization signal; and (c) a de-rotation of a first carrier signal corresponding to the first received signal;

in response to selecting the type of the first AFC that provides an adjustment to at least the shared synchronization signal, calculating a second AFC using values corresponding to (a) the second frequency error and (b) the adjustment to the at least the shared synchronization signal provided by the first AFC; and

in response to not selecting the type that provides an adjustment to the shared synchronization signal, calculating the second AFC using values corresponding to the second frequency error, wherein the second AFC is not calculated based on an adjustment associated with the first AFC.

10. The transceiver IC of Claim 9, wherein the AFC module:

applies the second AFC as at least one of (i) an adjustment to an exclusively local synchronization signal for the second received signal; and (ii) a de-rotation of a second carrier signal corresponding to the second received signal.

11. The transceiver IC of Claim 10, wherein:

the shared synchronization signal is one of a shared reference clock signal and (b) a shared system clock signal;

the exclusively local synchronization signal is one of (a) an unshared RF local oscillator signal and (b) a digital low intermediate frequency (IF) mixer LO signal corresponding to a respective received signal.

12. The transceiver IC of Claim 8, wherein the AFC module:

establishes at least one of a maximum correction rate and a maximum correction limit associated with the shared reference clock signal, wherein the shared reference clock signal is utilized by an application associated with a specific tolerance level for frequency changes and phase changes, and the specific tolerance level is used to establish at least one of the maximum correction rate and the maximum correction limit associated with the shared reference clock signal; and

applies a first correction that does not cause a violation of the at least one of the maximum correction rate and the maximum correction limit to the shared reference clock signal,

wherein the first correction is one of (a) the first AFC; and (b) a partial correction corresponding to the first AFC.

13. The transceiver IC of Claim 12, wherein the AFC module:

selects the type of AFC to apply based on at least one of: (a) the maximum correction rate; (b) the maximum correction limit; (c) a complexity associated with an adjustment; and (d) a number further adjustments that are triggered by selection of a particular type of AFC; and

wherein the type of AFC is one of: (a) a first type that provides an adjustment to the shared reference clock signal; (b) a second type that provides an adjustment to a first radio frequency (RF) local oscillator (LO); (c) a third type that provides a de-rotation of a first carrier signal corresponding to the first received signal; and (d) a fourth type that provides an adjustment to a digital low intermediate frequency (IF) mixer LO corresponding to the first received signal.

14. The transceiver IC of Claim 8, wherein:

the first frequency error and the second frequency error are respectively affected by at least one of: (a) a mapping of specific carrier frequencies to a particular cell tower associated with a respective received signal; (b) a change to the mapping of specific carrier frequencies associated with a handover procedure; and (c) a Doppler rate corresponding to a respective received signal.

15. A wireless communication device having a transceiver integrated circuit (IC) coupled to at least one antenna and which includes:

at least one processor;

at least two transceivers;

a shared reference clock utilized for signal reception at a first transceiver and a second transceiver;

a frequency error estimator that estimates: (a) a first frequency error between a first received signal corresponding to a first transceiver and a shared reference clock signal; and (b) a second frequency error between a second received signal corresponding to a second transceiver and the shared reference clock signal; and

an automatic frequency correction (AFC) module that:

determines a first AFC for the first frequency error;

determines a second AFC based on (a) values corresponding to the second frequency error and (b) the first AFC determined; and

synchronously applies (a) the determined first AFC to compensate for the first frequency error; and (b) the second AFC determined using the second frequency error.

16. The wireless communication device of Claim 15, wherein the AFC module:

selects a type of the first AFC that provides at least one of: (a) an adjustment to a shared synchronization signal; (b) an adjustment to an exclusively local synchronization signal; and (c) a de-rotation of a first carrier signal corresponding to the first received signal;

in response to selecting the type that provides an adjustment to at least the shared synchronization signal, calculating a second AFC using values corresponding to (a) the second frequency error and (b) the adjustment to the at least the shared synchronization signal provided by the first AFC;

in response to not selecting the type that provides an adjustment to the shared synchronization signal, calculating the second AFC using values corresponding to the second frequency error, wherein the second AFC is not calculated based on an adjustment associated with the first AFC; and

applies the second AFC as at least one of (i) an adjustment to an exclusively local synchronization signal for the second received signal; and (ii) a de-rotation of a second carrier signal corresponding to the second received signal.

17. The wireless communication device of Claim 16, wherein:

the shared synchronization signal is one of (a) a shared reference clock signal and (b) a shared system clock signal;

the exclusively local synchronization signal is one of (a) an unshared RF local oscillator signal and (b) a digital low intermediate frequency (IF) mixer LO signal corresponding to a respective received signal.

18. The wireless communication device of Claim 15, wherein the AFC module:

establishes at least one of a maximum correction rate and a maximum correction limit associated with the shared reference clock signal, wherein the shared reference clock signal is utilized by an application associated with a specific tolerance level for frequency changes and phase changes, and the specific tolerance level is used to establish at least one of the maximum correction rate and the maximum correction limit associated with the shared reference clock signal; and

applies a first correction that does not cause a violation of the at least one of the maximum correction rate and the maximum correction limit to the shared reference clock signal, wherein the first correction is one of (a) the first AFC; and (b) a partial correction corresponding to the first AFC.

19. The wireless communication device of Claim 18, wherein the AFC module:

selects the type of AFC to apply based on at least one of: (a) the maximum correction rate; (b) the maximum correction limit; (c) a complexity associated with an adjustment; and (d) a number of further adjustments that are triggered by selection of a particular type of AFC; and

wherein the type of AFC is one of: (a) a first type that provides an adjustment to the shared reference clock signal; (b) a second type that provides an adjustment to a first radio frequency (RF) local oscillator (LO); (c) a third type that provides a de-rotation of a first carrier signal corresponding to the first received signal; and (d) a fourth type that provides an adjustment to a digital low intermediate frequency (IF) mixer LO corresponding to the first received signal.

20. The wireless communication device of Claim 15, wherein:

the first frequency error and the second frequency error are respectively affected by at least one of: (a) a mapping of specific carrier frequencies to a particular cell tower associated with a respective received signal; (b) a change to the mapping of specific carrier frequencies associated with a handover procedure; and (c) a Doppler rate corresponding to a respective received signal.

FIG. 1

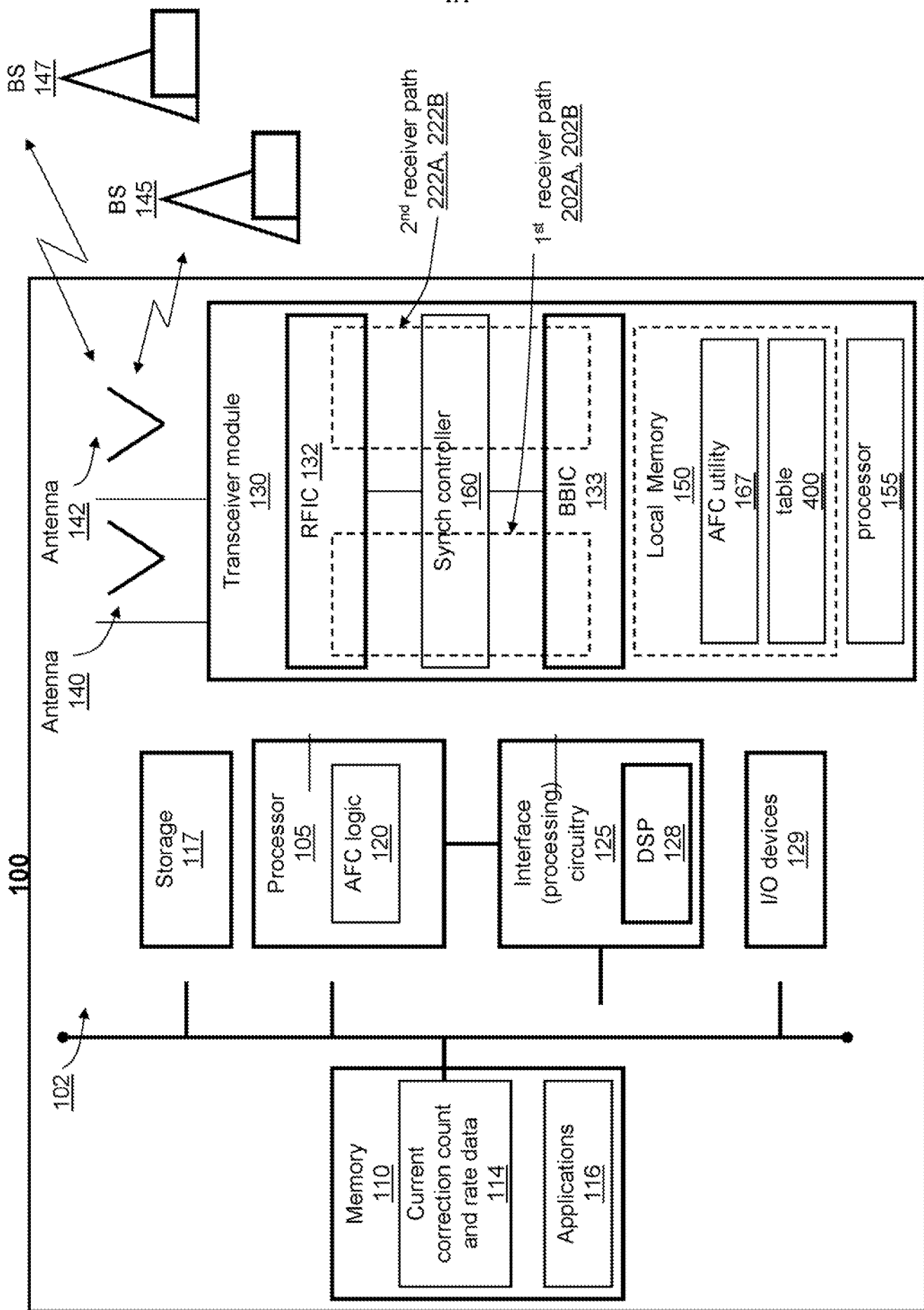


FIG. 2A

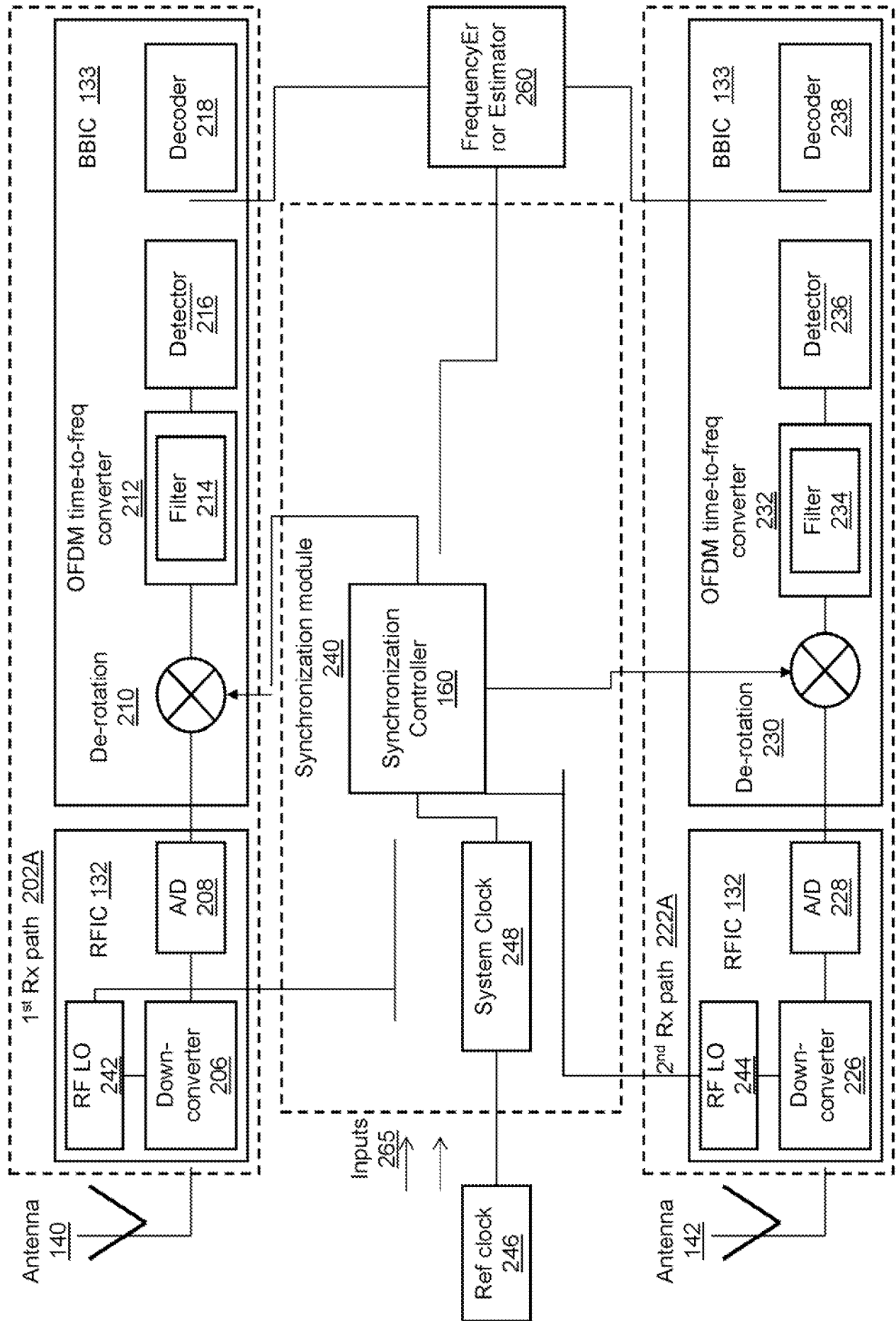


FIG. 2B

130

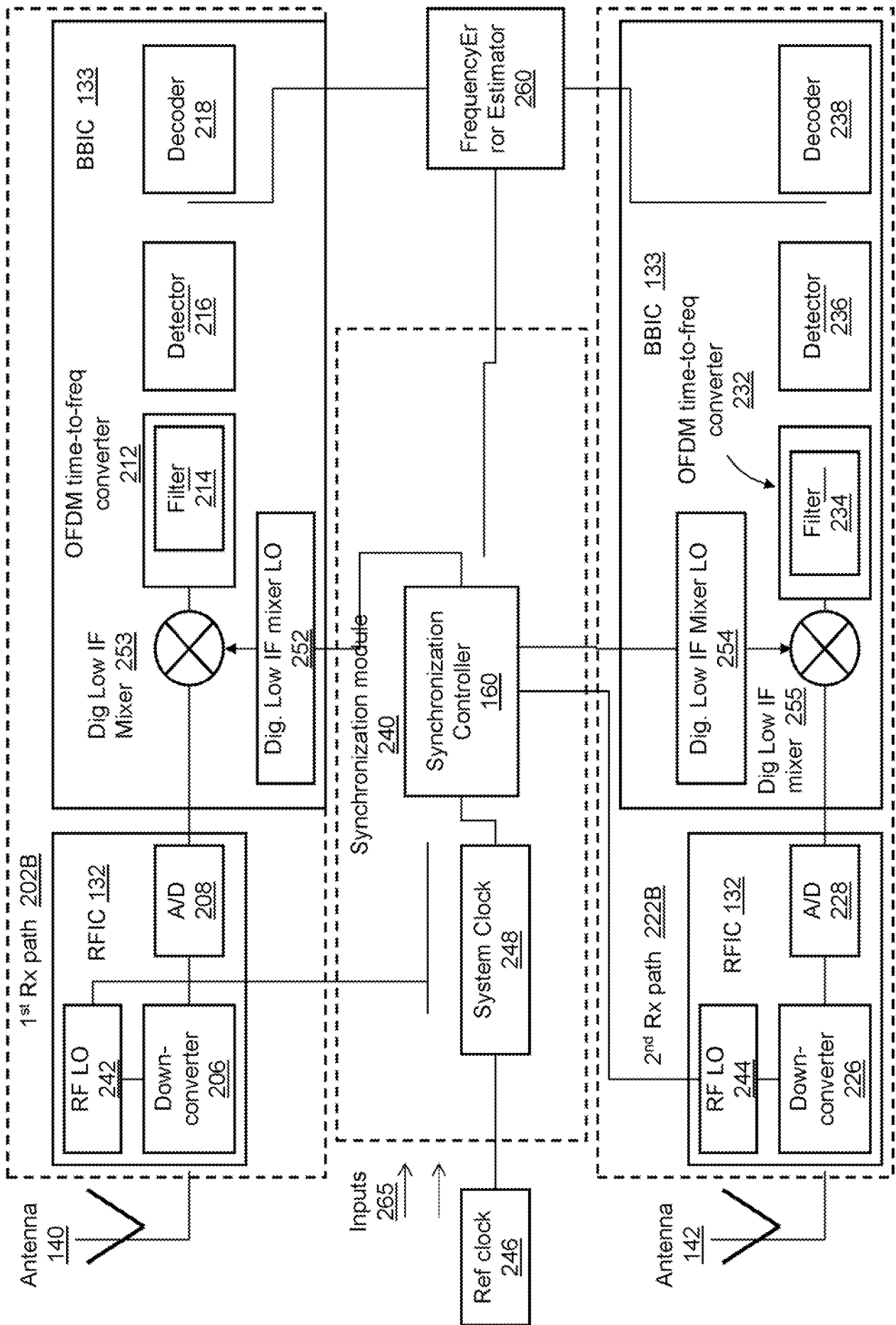


FIG. 3

130

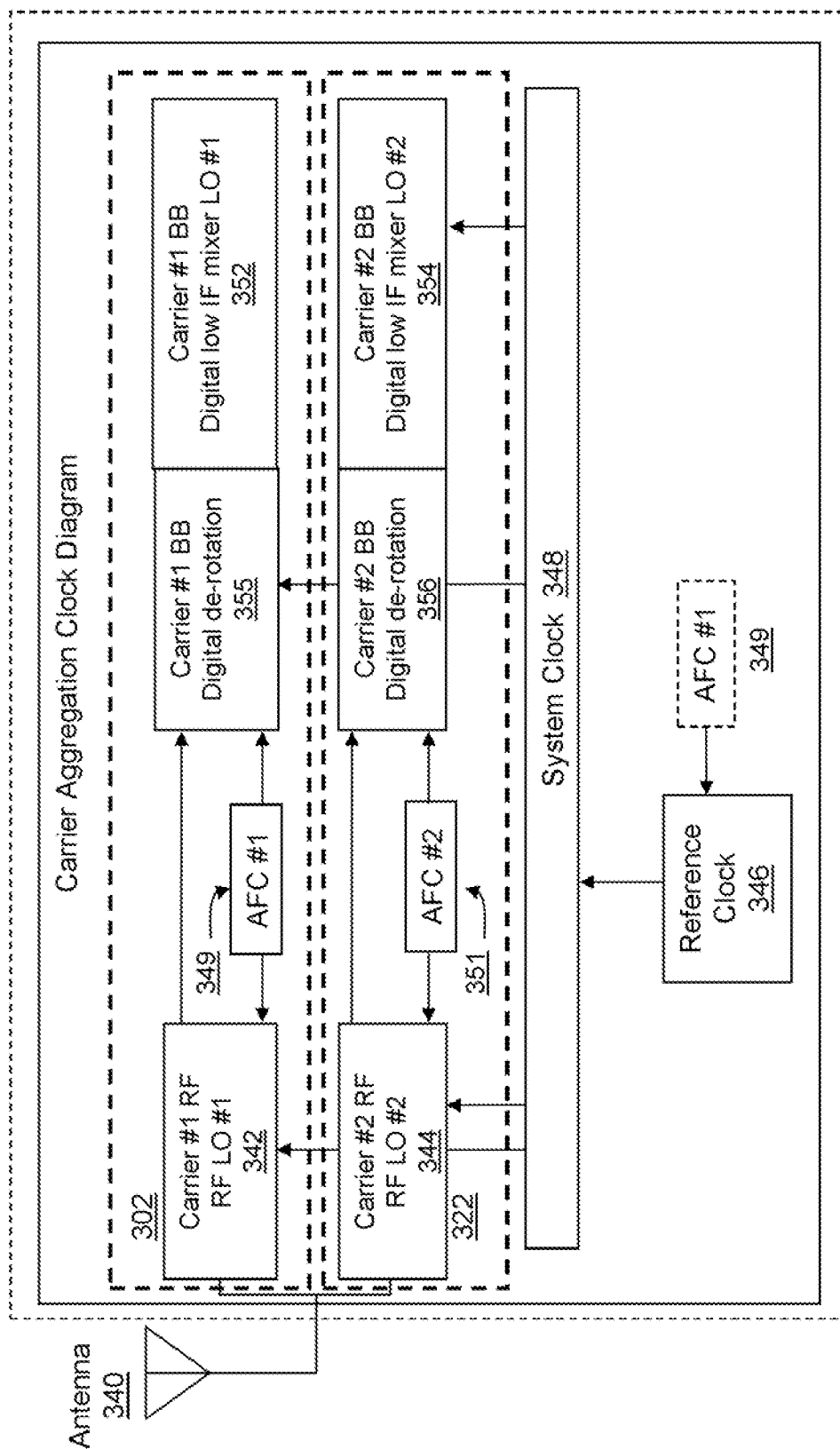


FIG. 4

400

Clock or synchronization source ID	Tolerance level for dependent applications sensitive to changes in synchronization signal	Maximum correction rate	Maximum correction limit	Number of receiver paths impacted
Reference Clock <u>402</u>	App 1: tolerance level c	rate 1	Limit 1	2
Reference Clock <u>404</u>	App 2: tolerance level d	rate 2	Limit 3	2
System Clock <u>406</u>	App 3: tolerance level a	rate 3	Limit 2	2
Shared Clock <u>408</u>	App 4: tolerance level e	rate 2	Limit 2	2
.....				

FIG. 5

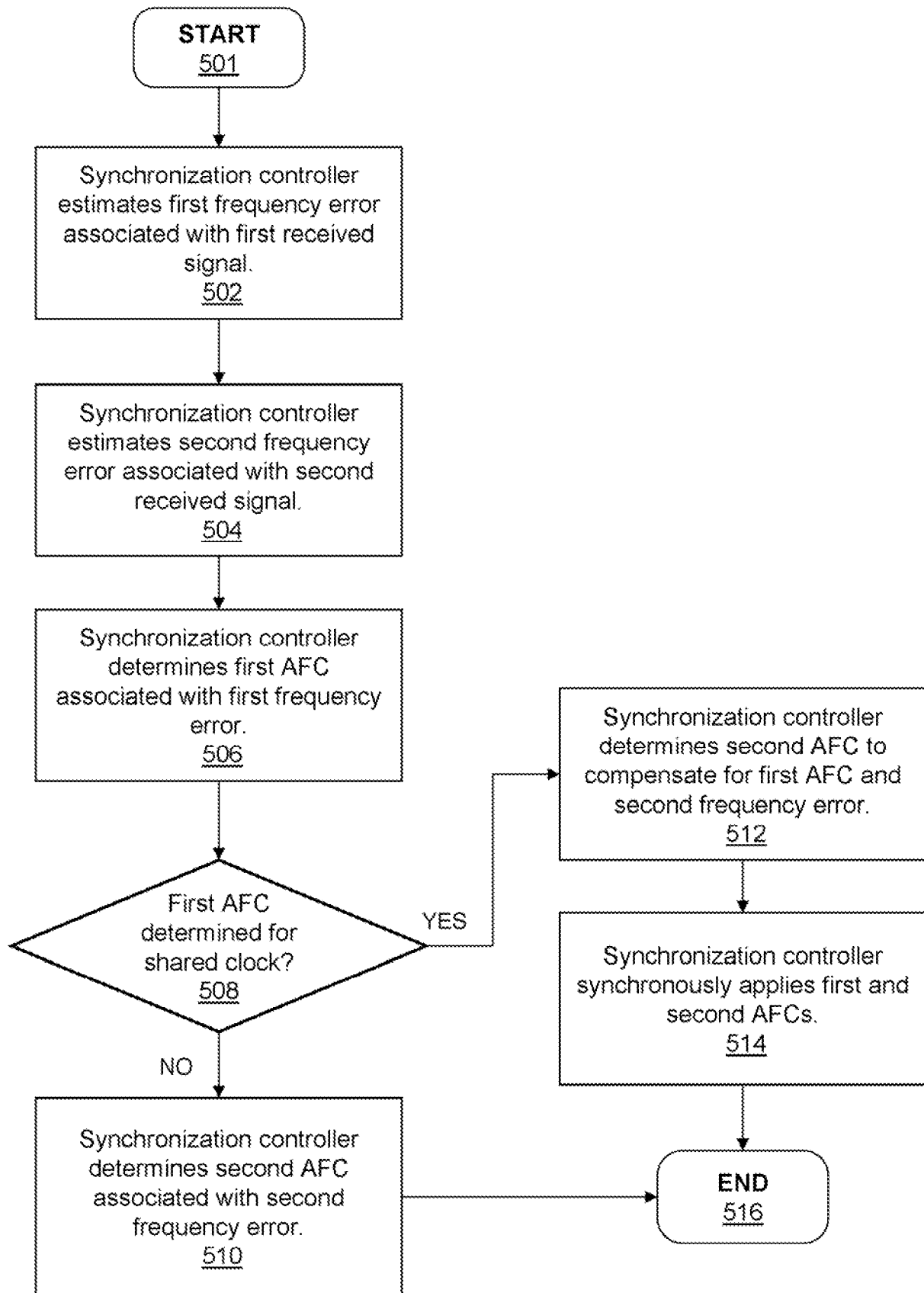
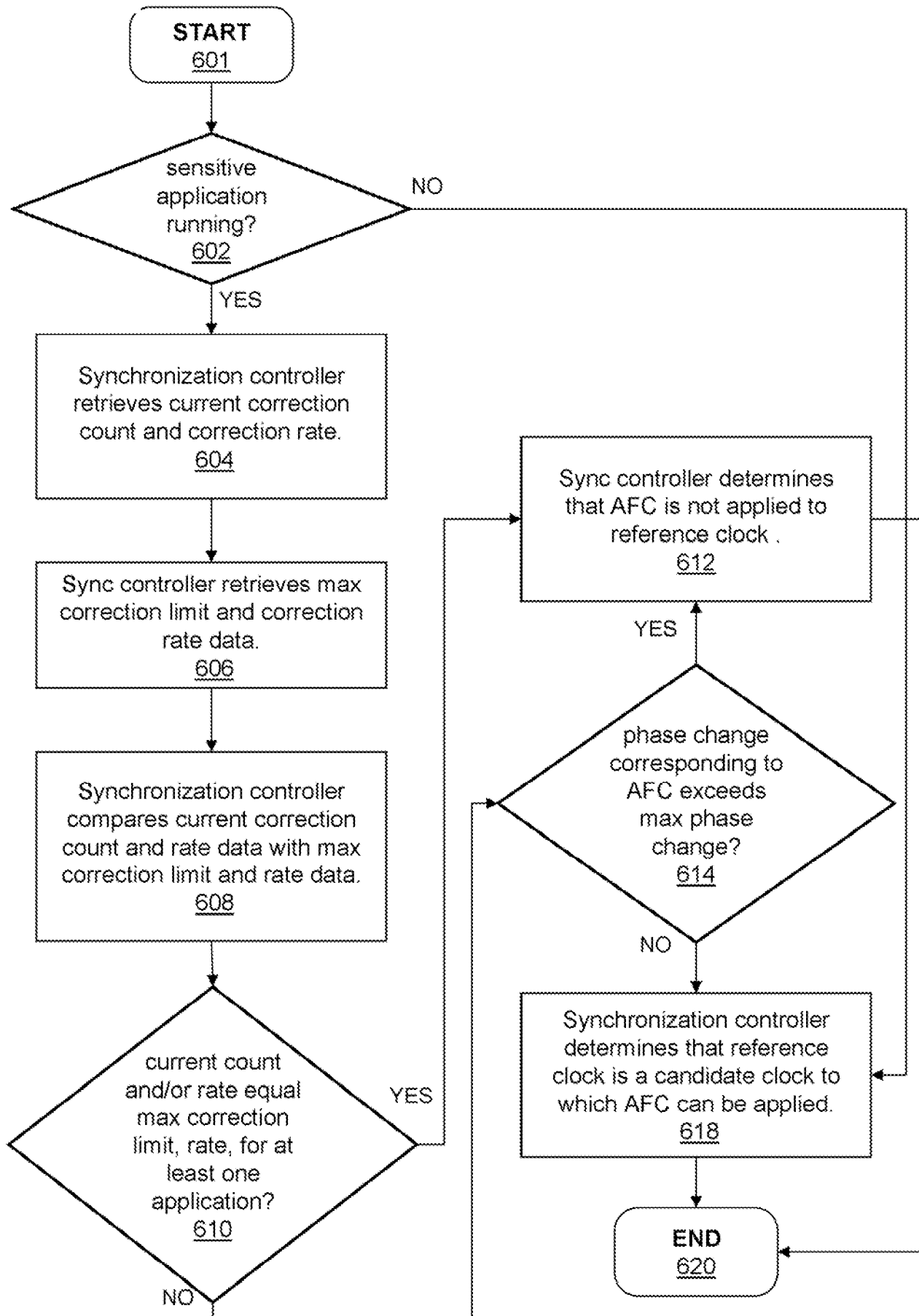


FIG. 6



INTERNATIONAL SEARCH REPORT

International application No

PCT/US2013/053372

A. CLASSIFICATION OF SUBJECT MATTER
 INV. H03J7/04
 ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
 H03J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009/258628 A1 (LINDOFF BENGT [SE] ET AL) 15 October 2009 (2009-10-15) paragraphs [0027] - [0028]; figure 3 paragraph [0030] paragraph [0032] - paragraph [0033] paragraph [0039] -----	1,8,15
X	US 2012/207010 A1 (EGAWA HIROYUKI [JP] ET AL) 16 August 2012 (2012-08-16) paragraph [0051] - paragraph [0064]; figures 5,7 paragraph [0079] - paragraph [0087] -----	1,8,15
A	US 2003/214436 A1 (VOOR THOMAS E [US] ET AL) 20 November 2003 (2003-11-20) paragraph [0013] - paragraph [0023]; figure 1 ----- -/-	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

14 November 2013

Date of mailing of the international search report

22/11/2013

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
 NL - 2280 HV Rijswijk
 Tel. (+31-70) 340-2040,
 Fax: (+31-70) 340-3016

Authorized officer

Peeters, Mark

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2013/053372

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 2004/055543 A1 (QUALCOMM INC [US]) 1 July 2004 (2004-07-01) paragraph [0065] - paragraph [0066]; figure 4 -----	1-20
A	US 2009/088085 A1 (NILSSON MAGNUS [SE] ET AL) 2 April 2009 (2009-04-02) paragraph [0028] - paragraph [0029]; figure 3 -----	1-20

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2013/053372

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2009258628 A1	15-10-2009	EP 2286561 A2	23-02-2011
		JP 2011522452 A	28-07-2011
		US 2009258628 A1	15-10-2009
		WO 2009127357 A2	22-10-2009
US 2012207010 A1	16-08-2012	JP 2012169812 A	06-09-2012
		US 2012207010 A1	16-08-2012
US 2003214436 A1	20-11-2003	AU 2003229308 A1	02-12-2003
		AU 2003233548 A1	02-12-2003
		CN 1653351 A	10-08-2005
		CN 1729405 A	01-02-2006
		EP 1508055 A1	23-02-2005
		EP 1512026 A2	09-03-2005
		JP 4373326 B2	25-11-2009
		JP 2005526256 A	02-09-2005
		JP 2006506832 A	23-02-2006
		US 2003214432 A1	20-11-2003
		US 2003214436 A1	20-11-2003
		WO 03098258 A1	27-11-2003
		WO 03098817 A2	27-11-2003
WO 2004055543 A1	01-07-2004	AU 2003296943 A1	09-07-2004
		CA 2509527 A1	01-07-2004
		HK 1084733 A1	26-03-2010
		HK 1139463 A1	31-05-2013
		JP 4851186 B2	11-01-2012
		JP 2006510034 A	23-03-2006
		KR 20050085628 A	29-08-2005
		KR 20110023919 A	08-03-2011
		US 2004130484 A1	08-07-2004
		WO 2004055543 A1	01-07-2004
US 2009088085 A1	02-04-2009	AR 068602 A1	18-11-2009
		CN 101889393 A	17-11-2010
		EP 2201682 A1	30-06-2010
		JP 5291108 B2	18-09-2013
		JP 2010541353 A	24-12-2010
		JP 2013168990 A	29-08-2013
		RU 2010117398 A	10-11-2011
		US 2009088085 A1	02-04-2009
		WO 2009043757 A1	09-04-2009