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(54) **Title:** METHOD FOR STORING CALIBRATION DATA OF A DEVICE INTERFACE IN A TEST SYSTEM, DEVICE INTERFACE, TEST SYSTEM, AND COMPUTER PROGRAM

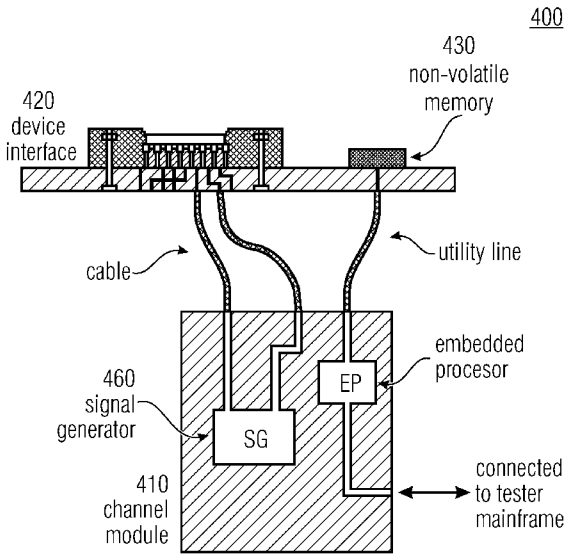


Fig. 4

(57) **Abstract:** A test system is described for testing one or more devices under test comprising one or more channel modules and a device interface. Therein at least information of a first part of the calibration data is stored on a non-volatile memory associated with the one or more channel modules, and at least information of a second part of the calibration data is stored on a non-volatile memory associated with the device interface. Corresponding method and computer programs are also described.

WO 2021/244751 A1

Method for storing calibration data of a device interface in a test system, device interface, test system, and computer program

Technical Field

Embodiments according to the present invention are related to a method for storing calibration data for a device interface in a test system. A test system can also be called automated test equipment.

Further embodiments according to the present invention are related to a test system comprising one or more channel modules and a device interface.

Further embodiments according to the invention are related to a device interface for a test system.

Further embodiments according to the invention are related to respective computer programs.

Embodiments according to the invention are related to storing calibration data for using a test system in different parts.

Background of the Invention

In the following, an introduction into some conventional solutions will be provided.

Automated test equipment (ATE) is any apparatus that performs tests on a device, known as the device under test (DUT), using automation to quickly perform measurements and evaluate the test results. An ATE can be a simple computer-controlled digital multimeter, or a complicated system containing dozens of complex test instruments – real or simulated electronic test equipment – capable of automatically testing and diagnosing faults in sophisticated electronic packaged parts or on wafer testing, including system on chips and integrated circuits. The DUT is connected to the ATE via a DUT interface, or simply device interface.

Structural tests enable systematic test coverage of individual structures, so-called cells, implementing the complex functions of a digital block within an System on a Chip, SOC. Structural test includes a variety of test methods including, but not limited to Memory built-in self-test, BIST, Logic BIST (pattern generated on-chip) and Scan Test (pattern externally

provided). Individual tests are combined to test blocks: e.g. scan test is hierarchically applied to blocks (serially or in parallel).

Advanced structural test methodologies apply a combination of externally provided test data (stimulus from Automated Test Equipment, ATE) and on-chip device for testing, DFT, that expands externally provided test data, so-called seeds, into scan chains. Test results are compacted and compressed into a reduced amount of test data provided to the primary input-output interface, IO, of a SOC. This data is called received data and is compared by the ATE with expected data. The received data can also be masked by the ATE.

The DFT, also sometimes called design for testing or design for testability typically consists of integrated circuit design techniques that add testability features to a hardware product design or device, i.e. the DUT. The added features make it easier to develop and apply tests to the DUT.

The following refers to Scan Test as general representation of structural test as described above.

In order to get valid results from a device-under-test on the device interface, the device interface needs to be calibrated, such that the individual transmission path from a signal generator, SG, to a device-under-test, which is located on the device interface, does not lead to additional unwanted changes of the test results for the device-under-test. In other words, the transmission path of the signal must be compensated in order to improve the test results.

Fig. 1 shows prior art details of a test system, and in particular the transmission path. Therein the channel module 100 comprises a signal generator, SG, 110, which via a transmission path, for example cable 120, sends a signal to the device-under-test on the DUT interface 130.

Although Fig. 1 shows a test system, where a channel module generates a signal to be sent to the device-under-test. Similarly, but not depicted, the transmission path from the device-under-test to a signal receiver on a channel module, can be compensated in a test system, where a channel module receives data from the device-under-test.

Fig. 2 shows a device interface 210, a test head 220, and a tester mainframe 230, which can, in one exemplary arrangement constitute the entire test system. In the prior art, the complete calibration data is stored, for example, in the tester mainframe.

However, there are challenges to cost-effectively scaling scan tests with the increasing complexity of SOCs enabled by new fabrication processes.

One challenge is the escalating amount of test data that needs to be stored on the ATE. Another challenge is the escalating test times to feed the test data through the SOC IO. Also, the increasing on-chip complexity is challenging the distribution of test data to blocks-under-test and to create the required clock signals.

In addition, quality and reliability expectations of complex SOCs require structural tests when the SOC is deployed in the end-application: e.g. in automobile or communication infrastructure system.

Conventionally, the calibration data includes only propagation delay information of every transmission path. However, with the recent high-speed interfaces, where transmission path frequencies can be well over 5GHz, frequency characteristic information of the transmission paths should also be included in the calibration information in order to compensate for the loss on the transmission paths.

In view of this situation, there is a desire for a concept which provides for an improved compromise between data to be stored, processing speed and quality and reliability of tests when testing devices under test with an automated test equipment.

Summary of the Invention

The present invention effects an improved storage of calibration data, reduction of calibration time and enables improved testing for high speed digital interfaces.

An embodiment according to the present invention is a method for storing calibration data for a device interface in a test system. Such a system comprises one or more channel modules and a device interface.

The method comprises storing at least information of a first part of the calibration data on a non-volatile memory associated with the one or more channel modules, and storing at least information of a second part of the calibration data on a non-volatile memory associated with the device interface.

It has been found beneficial, if the calibration data is split into two parts, such that each part, the channel modules and the device interface, which can be separated from each other, are calibrated individually, therefore, each part has its own calibration data, which can be stored separately. So, if for example, the device interface is exchanged, the system put together thereby, does not have to be calibrated as a whole, but the calibration data for each part is known before, by calibration in the factory, and the calibration data for both parts can be combined.

In a preferred embodiment, the method can further comprise storing at least information of a third part of the calibration data on a non-volatile memory, associated with an attachment, which is located between the one or more channel modules and the device interface.

It has been found beneficial, that in test systems, where an attachment is located between the channel modules and the device interface, the attachment connecting the device interface to the remainder of the test system, that the attachment is calibrated individually. Thereby a replacement of the attachment does not require re-calibration of the test system.

In a preferred embodiment of the method, the respective information of the first, second and/or third part of the calibration data can be a memory address and an identification code of the associated one or more channel modules, device, and attachment, respectively, and wherein the method further comprises storing the calibration data in a storage device at the memory address.

It has been found beneficial, that the non-volatile memory stores as the information of the calibration data only a memory address, and the actual calibration data is stored in a storage device at this memory address. Thereby the non-volatile memory on the respective part can be reduced in size.

A further embodiment according to the present invention is a test system comprising one or more channel modules and a device interface, wherein at least information of a first part of the calibration data is stored on a non-volatile memory associated with the one or more channel modules, and at least information of a second part of the calibration data is stored on a non-volatile memory associated with the device interface.

A further embodiment according to the present invention is a device interface for a test system, the test system further comprising one or more channel modules, wherein at least information of a first part of the calibration data is stored on a non-volatile memory associated with the one

or more channel modules, and at least information of a second part of the calibration data is stored on a non-volatile memory associated with the device interface.

In a preferred embodiment, the test system in both above apparatus embodiments can further comprise an attachment located between the one or more channel modules and the device interface, wherein at least information of a third part of the calibration data, corresponding to the attachment, is stored on a non-volatile memory associated with the attachment.

In a preferred embodiment, in the test system of both above apparatus embodiments the respective information of the first, second and/or third part of the calibration data can be a memory address and an identification code of the associated one or more channel modules, device, and attachment, respectively, and the calibration data can be stored in a storage device at the memory address.

For the both apparatus embodiments, the same considerations apply as for the method embodiment.

The following features apply to all above embodiments.

In a preferred embodiment, the first part of the calibration data can be data corresponding to the one or more channel modules. The second part of the calibration data can be data corresponding to the device interface. The third part of the calibration data can be data corresponding to the attachment.

It has been found beneficial if each channel module and/or device interface and/or attachment is calibrated individually, such that a replacement does not require a re-calibration.

In a preferred embodiment, the device interface can be a high-speed digital interface.

It has been found beneficial, as stated above, that the invention is particularly useful for high-speed interfaces, where the transmission path frequencies can be well over 5GHz.

In a preferred embodiment, the calibration data can contain information of frequency characteristics of components for transmitting signals from the one or more channel modules to the device.

It has been found beneficial, that the frequency characteristics are included in the calibration data, such that loss can be compensated.

In a preferred embodiment, the calibration data can comprise at least two filters, the filters describing the frequency characteristics.

It has been found beneficial, that the frequency characteristics are included in the calibration data in the form of filters.

In a preferred embodiment, the first part of the calibration data can a first filter, and the second part of the calibration data can be a second filter. The third part of the calibration data can be a third filter.

It has been found beneficial, that the filters can be different from each other, enabling a more efficient storing of the frequency characteristics.

In a preferred embodiment, the filters can be compensation filters.

It has been found useful, that the filters are compensation filters, thereby enabling an easier inclusion of the frequency characteristic in the calibration data.

In a preferred embodiment, the calibration data can comprise transmissions functions describing the frequency characteristics.

It has been found beneficial for the efficiency of the calibration data storing, that the frequency characteristics are described as transmission functions.

In a preferred embodiment, the calibration data can comprise one or more of tap coefficients of digital filters, Fourier series, and/or a two-port network model.

It has been found beneficial for the storing of the calibration data, if the calibration data comprises tap coefficients of digital filters, Fourier series, and/or a two-port network model.

In a preferred embodiment, each calibration data can be unified by convolution for a time domain, multiplication for a frequency domain, and/or cascaded two-port networks for two-port networks.

It has been found beneficial for the storing efficiency of the calibration data, if the calibration data is unified, for example, by convolution for a time domain, multiplication for a frequency domain, and/or cascaded two-port networks for two-port networks.

In a preferred embodiment, the non-volatile memory associated with the one or more channel modules can be on the respective channel modules. The non-volatile memory associated with the device interface can be on the device interface. And/or the non-volatile memory associated with the attachment can be on the attachment.

It has been found beneficial, that the non-volatile memory storing the calibration data of a part, i.e. a channel module, a device interface and/or an attachment is location on the respective part.

In a preferred embodiment, any of the information can be stored in encrypted form.

It has been found beneficial that the stored information is stored encrypted. Thereby the security can be increased.

In a preferred embodiment, the one or more channel modules can comprise a signal generator or signal receiver.

It has been found beneficial, if the signal generator and/or receiver that is used for the testing by the test system, is located on the channel modules. Thereby the testing can be further optimized.

In a preferred embodiment, the device can be a calibration module for calibrating the test system.

It has been found beneficial, that a special calibration module (or calibration device) can be used on the device interface. With such an arrangement, calibration of the channel modules and the device interface can be facilitated.

All embodiments are based on the same considerations as the above-described method for storing calibration data. However, it should be noted that all embodiments can be supplemented by any of the features, functionalities and details described herein, in particular the above described features. Moreover, every embodiment can be supplemented by the

features, functionalities, and details described herein, both individually and taken in combination.

A further embodiment according to the invention is a computer program for performing the method described herein, when the computer program runs on a computer.

Brief Description of the Figures

Embodiments according to the present invention will subsequently be described taking reference to the enclosed figures in which:

Fig. 1 shows a schematic diagram of an automated test equipment according to prior art;

Fig. 2 shows a schematic diagram of an automated test equipment according to prior art;

Fig. 3 shows a block schematic diagram of an information structure according to an embodiment of the present invention;

Fig. 4 shows a block schematic diagram of an automated test equipment according to an embodiment of the present invention;

Fig. 5 shows a block schematic diagram of an information structure according to another embodiment of the present invention;

Fig. 6 shows a block schematic diagram of an automated test equipment according to another embodiment of the present invention;

Fig. 7 shows a block schematic diagram of an information structure according to another embodiment of the present invention;

Fig. 8 shows a block schematic diagram of an automated test equipment according to another embodiment of the present invention; and

Fig. 9 shows a flow chart of a method according to an embodiment of the present invention.

In the figures, similar reference signs denote similar elements and features.

Detailed Description of the Embodiments

Generally, an automated test equipment, or test system 400, 600, 800 according to an embodiment of the present invention is for testing one or more devices under test, DUTs, which are connected to the test system via a device interface 420.

The DUTs are tested, e.g. by providing them with test data, and receiving from them test results in various ways. Testing a device under test requires data transmission in both directions between the test system and the DUTs. Some of these transmissions are transmitted via the device interface.

The data can provide the DUTs with test data, test signals, or test programs, and the data can be the data that the test system receives, or a processed version thereof, i.e. the data provided to the DUTs is data on the basis of the data. Alternatively, the data can also represent expected signals or expected results from the device under test which the DUTs return to the test system after the test. This data can also be the expect data or require processing in the test system, such that the expect data is data on the basis of the data received by the test system.

Any combination of the above is also possible, since the data that is provided to the one or more DUTs can be a combination of the options detailed above.

Fig. 3 shows a block schematic diagram of an information structure 300 according to an embodiment of the present invention. It represents the information of the calibration data. In Fig. 3 this it consists of two parts, namely a first part 310 and a second part 320.

Fig. 4 shows a block schematic diagram of an automated test equipment, or test system, 400 according to an embodiment of the present invention. The test system 400 comprises one or more channel modules 410 and a device interface 420. The device interface 420 serves to connect to a device, which is the device-under-test, which is tested by the test system 400. Alternatively, the device interface can be used to connect a calibration module (not shown) for calibration purposes.

The test system can comprise multiple channel modules 410, although only one is depicted in the figures. A skilled person can easily adapt the invention to other channel modules as well.

The first part 310 of the calibration data 300 is stored on a non-volatile memory 430. As will be discussed later-on, the non-volatile memory can be located on different parts. In Fig. 4 it is

located on the device interface. It could very well be located on one or more of the channel modules 410, as well as the later introduced attachment 470, if it is present. The non-volatile memory 430 is associated with the one or more channel modules 410. Further the second part 320 of the calibration data 300 is stored on a non-volatile memory 430 associated with the device-under-test interface 420.

The first part 310 of the calibration data can be data corresponding to the one or more channel modules 410. This means that the first part is describing calibration information relating to the respective channel module. The second part 320 of the calibration data can be data corresponding to the device-under-test interface 420. This means that the second part is describing calibration information relating to the device interface.

The device-under-test interface 420 can be a high-speed digital interface, for devices-under-test with high-speed capabilities.

The calibration data can further contain information of frequency characteristics of components for transmitting signals from the one or more channel modules 410 to the device-under-test. Clearly, the invention is similar applicable for the other direction, i.e. for signals transmitted from the device-under-test to the channel modules 410. In the first case the channel module can comprise a signal generator 460, as can be seen in Figs. 4 and 6, and in the second case the channel modules 410 can comprise a signal receiver 465, as can be seen in Fig. 8. Although the respective figures show different arrangements of the embodiments of the present invention, the channel modules 410 can comprise either a signal generator 460 and/or a signal receiver 465 in any combination of features, i.e. in any embodiment.

The calibration data can comprise at least two filters, the filters describing the frequency characteristics, wherein, for example, the first part 310 of the calibration data is a first filter, and the second part 320 of the calibration data is a second filter. Although the first part and the second part can be the same filter, if applicable.

As an example, the first filter only contains information that refers to the channel modules, and the second filter only contains information regarding the device interface. The required information, i.e. the calibration data can be measured in the factory, where the channel module, the device interface, i.e. the test system, is manufactured, before it is shipped to customers.

Each component can for example be measured by an equipment such as network analyzer or oscilloscope, and the obtained frequency response is transferred to appropriate parameter and

stored into a corresponding non-volatile memory. This means the calibration data is originally an individual data that belongs to each component.

The filters can, as one possibility, be so-called compensation filters. The calibration data can further comprise transmissions functions, which describe the frequency characteristics of the individual parts of the test system 400. As further examples, the calibration data can contain tap coefficients of digital filters, Fourier series, and/or a two-port network model. All these are used to describe the calibration information of a respective part of the test system 400.

The calibration data, or the parts of it, can also be unified. Such a unification can, for example, be based on a convolution for a time domain, a multiplication for a frequency domain, and/or cascaded two-port networks for two-port networks.

In summary, as shown in Fig.3, the calibration data 300 is divided into two parts. The first part 310 of the calibration data can for example be a compensation filter corresponding, for example, to the channel module 410. This can also include the cable shown in Figs. 4, 6, and 8. The second part 320 of the calibration data can for example be a compensation filter corresponding to the device interface 420, for example.

Generally, the part of the calibration data, i.e. for example the filters are descriptions of frequency characteristics of the components that compose the signal path or paths from the signal generator 460 to the device-under-test, or from the device-under-test to the signal receiver 465 as shown later.

The frequency characteristic may be stored as a form of transmission function instead of compensation filter because they are mathematically equivalent information but reciprocal.

The information may have a form of, tap coefficients of digital filters, Fourier series and/or a two-port network model.

Each of the data parts, for example filters, can be unified by means of, convolution if the filters are described in time domain, multiplication if the filters are described in frequency domain, or cascaded two-port networks if the filters are described as two-port networks.

The information of for example the second part 320 of the calibration data, i.e. for example a filter, is stored in the non-volatile memory 430 on the device interface as shown in Fig.4.

Fig. 6 shows a block schematic diagram of an automated test equipment according to another embodiment of the present invention. As pointed out above, in Fig. 6, more non-volatile memories 430, 440, and 450 can be seen. The same as described for test system 400 is in general applicable to the test system 600. In Fig. 6 it is thereby indicated that each part of the test system 600, i.e. the channel module 410, the device interface 420 and the attachment 470 can comprise its own non-volatile memory, 430, 440, and 450, respectively. Thereby the respective calibration data can be stored on the actual part of the test system it belongs to.

Corresponding Fig. 5 shows a block schematic diagram of an information structure according to another embodiment of the present invention.

As shown in Fig.5, the calibration data can be divided into more than two parts. For example, they can be divided into three parts, corresponding to device interface 420, attachment 470, and channel module 410.

In this embodiment, it is shown that the non-volatile memory 440 associated with the one or more channel modules 410 can be located on the respective channel modules. The non-volatile memory 430 associated with the device-under-test interface 420 can be located on the device interface.

The test system 600 can further comprise an attachment 470, which can be located between the one or more channel modules 410 and the device interface 420. The calibration data can then contain a third part 330 of the calibration data, which corresponds to the attachment. This third part 330 can then be stored on a non-volatile memory 430, 440, 450 associated with the attachment. Again, this non-volatile memory can be located on the attachment 470 itself, but also on one or more of the channel modules 410 or the device interface 420.

Fig. 7 shows a block schematic diagram of an information structure according to another embodiment of the present invention, and Fig. 8 shows a block schematic diagram of an automated test equipment according to another embodiment of the present invention.

In this embodiment, it is shown that in the test system 800, the one or more channel modules 410 can comprise not only a signal generator 460, as shown in Figs. 4 and 6, but also a signal receiver 465. As stated before, the combination of these, i.e. generator 460 and receiver 465 is possible in each of the embodiments of the invention.

Thus, the invention is also applicable to the receiver signal path, where one or more of the channel modules 410 comprises a signal receiver 465.

Further, not shown, the device can be a calibration module for calibrating the test system 400, 600, 800. Thus, the invention is also applicable to the case where the device under test is replaced by a calibration module that calibrate the test system itself.

Further it is noted that also for all embodiments, the respective information of the first 310, second 320 and/or third 330 part of the calibration data can also refer only to a memory address and an identification code of the associated device. The associated device again is one or more channel modules 410, the device interface 420, or the attachment 470.

The calibration data can then be stored in a storage device at the memory address. This storage device can be located in the tester mainframe, or in any other accessible memory location. This memory location can be accessible via wired or wireless connection by one of the known techniques.

The memory address describes the actual location of the calibration data. Since therefore only the address is stored in the respective non-volatile memory (one of 430, 440, and 450), storage size can be reduced.

The memory for which the address is stored in the non-volatile memory (one of 430, 440, and 450), can be a part of or connected to the test system, or the tester mainframe. In case it is connected to the test system or tester mainframe, this connection can be realized by any wired or wireless data connection.

In other words, the non-volatile memory (one of 430, 440, and 450) may only have an identification information (ID) and the information part (for example filter information) may be stored in other storage space such as an external server via a network.

One embodiment refers directly and solely to the device interface 420 as described above, which is an individual part of the test system, which can contain its own calibration data thereby. The device interface 420, however, it is noted, can be modified also by the important points and aspects described here. These can also either be used individually or in combination and can be introduced into the device interface 420 described herein, both individually and in combination.

Fig. 9 shows a flow chart of a method according to an embodiment of the present invention.

Method 900 is a method for storing calibration data for a device interface in a test system 400, 600, 800 as described above. The method comprises storing 910 at least information of a first part of the calibration data on a non-volatile memory associated with the one or more channel modules, and storing 920 at least information of a second part of the calibration data on a non-volatile memory associated with the device interface.

Further optional steps of the method 900 are indicated in Fig. 9 by dotted lines.
If the test system 400, 600, 800 comprises an attachment 470, the method 900 can further comprise storing 930 at least information of a third part of the calibration data, corresponding to the attachment, on a non-volatile memory associated with the attachment.

Also, as with all embodiments possible, the stored information may be encrypted.

Also, with the respective information of the first, second and/or third part of the calibration data being a memory address and an identification code of the associated one or more channel modules, device interface, and attachment, respectively, the method 900 can further comprise storing 940 the calibration data in a storage device at the memory address.

This method is based on the same considerations as the above-described test system. However, it should be noted that the method can be supplemented by any of the features, functionalities and details described herein, also with respect to the test system. Moreover, the method can be supplemented by the features, functionalities, and details of the test system, both individually and taken in combination.

An embodiment according to the invention creates a computer program for performing the method described herein, when the computer program runs on a computer.

With this invention, the calibration data, i.e. filter information, can be included in its components itself. This feature improves portability of calibration data. Further, the total data, i.e. of the filter, can be generated by relatively small computation costs. And finally, the test system nor any of its components, needs re-calibration when the components are changed.

Conclusions

To conclude, the embodiments described herein can optionally be supplemented by any of the important points or aspects described here. However, it is noted that the important points and aspects described here can either be used individually or in combination and can be introduced into any of the embodiments described herein, both individually and in combination.

Implementation Alternatives

Although some aspects have been described in the context of an apparatus, it is clear that these aspects also represent a description of the corresponding method, where a block or device corresponds to a method step or a feature of a method step. Analogously, aspects described in the context of a method step also represent a description of a corresponding block or item or feature of a corresponding apparatus. Some or all of the method steps may be executed by (or using) a hardware apparatus, like for example, a microprocessor, a programmable computer or an electronic circuit. In some embodiments, one or more of the most important method steps may be executed by such an apparatus.

Depending on certain implementation requirements, embodiments of the invention can be implemented in hardware or in software. The implementation can be performed using a digital storage medium, for example a floppy disk, a DVD, a Blu-Ray, a CD, a ROM, a PROM, an EPROM, an EEPROM or a FLASH memory, having electronically readable control signals stored thereon, which cooperate (or are capable of cooperating) with a programmable computer system such that the respective method is performed. Therefore, the digital storage medium may be computer readable.

Some embodiments according to the invention comprise a data carrier having electronically readable control signals, which are capable of cooperating with a programmable computer system, such that one of the methods described herein is performed.

Generally, embodiments of the present invention can be implemented as a computer program product with a program code, the program code being operative for performing one of the methods when the computer program product runs on a computer. The program code may for example be stored on a machine readable carrier.

Other embodiments comprise the computer program for performing one of the methods described herein, stored on a machine readable carrier.

In other words, an embodiment of the inventive method is, therefore, a computer program having a program code for performing one of the methods described herein, when the computer program runs on a computer.

A further embodiment of the inventive methods is, therefore, a data carrier (or a digital storage medium, or a computer-readable medium) comprising, recorded thereon, the computer program for performing one of the methods described herein. The data carrier, the digital storage medium or the recorded medium are typically tangible and/or non–transitionary.

A further embodiment of the inventive method is, therefore, a data stream or a sequence of signals representing the computer program for performing one of the methods described herein. The data stream or the sequence of signals may for example be configured to be transferred via a data communication connection, for example via the Internet.

A further embodiment comprises a processing means, for example a computer, or a programmable logic device, configured to or adapted to perform one of the methods described herein.

A further embodiment comprises a computer having installed thereon the computer program for performing one of the methods described herein.

A further embodiment according to the invention comprises an apparatus or a system configured to transfer (for example, electronically or optically) a computer program for performing one of the methods described herein to a receiver. The receiver may, for example, be a computer, a mobile device, a memory device or the like. The apparatus or system may, for example, comprise a file server for transferring the computer program to the receiver.

In some embodiments, a programmable logic device (for example a field programmable gate array) may be used to perform some or all of the functionalities of the methods described herein. In some embodiments, a field programmable gate array may cooperate with a microprocessor in order to perform one of the methods described herein. Generally, the methods are preferably performed by any hardware apparatus.

The apparatuses described herein may be implemented using a hardware apparatus, or using a computer, or using a combination of a hardware apparatus and a computer.

The apparatuses described herein, or any components of the apparatus described herein, may be implemented at least partially in hardware and/or in software.

The methods described herein may be performed using a hardware apparatus, or using a computer, or using a combination of a hardware apparatus and a computer.

The methods described herein, or any components of the apparatus described herein, may be performed at least partially by hardware and/or by software.

The above described embodiments are merely illustrative for the principles of the present invention. It is understood that modifications and variations of the arrangements and the details described herein will be apparent to others skilled in the art. It is the intent, therefore, to be limited only by the scope of the impending patent claims and not by the specific details presented by way of description and explanation of the embodiments herein.

Claims

1. A method (900) for storing calibration data for a device interface in a test system, the system comprising one or more channel modules and a device interface, the method comprising:
   storing (910) at least information of a first part of the calibration data on a non-volatile memory associated with the one or more channel modules, and
   storing (920) at least information of a second part of the calibration data on a non-volatile memory associated with the device interface.

2. Method according to claim 1, wherein the first part of the calibration data is data corresponding to the one or more channel modules.

3. Method according to any one of claims 1 to 2, wherein the second part of the calibration data is data corresponding to the device interface.

4. Method according to any one of claims 1 to 3, wherein the device interface is a high-speed digital interface.

5. Method according to any one of claims 1 to 4, wherein the calibration data contains information of frequency characteristics of components for transmitting signals from the one or more channel modules to the device.

6. Method according to any one of claims 1 to 5, wherein the calibration data comprises at least two filters, the filters describing the frequency characteristics.

7. Method according to claim 6, wherein the first part of the calibration data is a first filter, and the second part of the calibration data is a second filter.

8. Method according to any one of claims 6 to 7, wherein the filters are compensation filters.

9. Method according to any one of claims 1 to 8, wherein the calibration data comprises transmissions functions, the transmission functions describing the frequency characteristics.

10. Method according to any one of claims 1 to 9, wherein the calibration data comprises one or more of

tap coefficients of digital filters,
Fourier series, and/or
a two-port network model.

11. Method according to any one of claims 1 to 10, wherein each calibration data is unified by
convolution for a time domain,
multiplication for a frequency domain, and/or
cascaded two-port networks for two-port networks.

12. Method according to any one of claims 1 to 11, wherein the non-volatile memory associated with the one or more channel modules is on the respective channel modules.

13. Method according to any one of claims 1 to 12, wherein the non-volatile memory associated with the device interface is on the device interface.

14. Method according to any one of claims 1 to 13, further comprising
storing (930) at least information of a third part of the calibration data, corresponding to the attachment, on a non-volatile memory associated with an attachment, which is located between the one or more channel modules and the device interface.

15. Method according to claim 14, wherein the non-volatile memory associated with the attachment is on the attachment.

16. Method according to any one of claims 1 to 15, wherein storing any information is storing the information encrypted.

17. Method according to any one of claims 1 to 16, wherein the one or more channel modules comprise a signal generator or signal receiver.

18. Method according to any one of claims 1 to 17, wherein the device is a calibration module for calibrating the test system.

19. Method according to any one of claims 1 to 18, wherein the respective information of the first, second and/or third part of the calibration data is a memory address and an identification code of the associated one or more channel modules, device interface, and

attachment, respectively, and wherein the method further comprises storing (940) the calibration data in a storage device at the memory address.

20. A computer program for a processing device, comprising software code portions for performing the steps of any one of claims 1 to 19, when the program is run on the processing device.

21. The computer program according to claim 20, comprising a computer-readable medium on which the software code portions are stored, wherein the program is directly loadable into an internal memory of the processing device.

22. A test system (400, 600, 800) comprising one or more channel modules (410) and a device interface (420), wherein:
at least information of a first part (310) of calibration data (300) is stored on a non-volatile memory (440) associated with the one or more channel modules (410), and
at least information of a second part (320) of the calibration data (300) is stored on a non-volatile memory (430) associated with the device interface (420).

23. Test system (400, 600, 800) according to claim 22, wherein the first part (310) of the calibration data is data corresponding to the one or more channel modules (410).

24. Test system (400, 600, 800) according to any one of claims 22 to 23, wherein the second part (320) of the calibration data is data corresponding to the device interface (420).

25. Test system (400, 600, 800) according to any one of claims 22 to 24, wherein the device interface (420) is a high-speed digital interface.

26. Test system (400, 600, 800) according to any one of claims 22 to 25, wherein the calibration data contains information of frequency characteristics of components for transmitting signals from the one or more channel modules (410) to the device.

27. Test system (400, 600, 800) according to any one of claims 22 to 26, wherein the calibration data comprises at least two filters, the filters describing the frequency characteristics.

28. Test system (400, 600, 800) according to claim 27, wherein the first part (310) of the calibration data is a first filter, and the second part (320) of the calibration data is a second filter.

29. Test system (400, 600, 800) according to any one of claims 27 to 28, wherein the filters are compensation filters.

30. Test system (400, 600, 800) according to any one of claims 22 to 29, wherein the calibration data comprises transmissions functions, the transmission functions describing the frequency characteristics.

31. Test system (400, 600, 800) according to any one of claims 22 to 30, wherein the calibration data comprises one or more of
tap coefficients of digital filters,
Fourier series, and/or
a two-port network model.

32. Test system (400, 600, 800) according to any one of claims 22 to 31, wherein each calibration data is unified by
convolution for a time domain,
multiplication for a frequency domain, and/or
cascaded two-port networks for two-port networks.

33. Test system (400, 600, 800) according to any one of claims 22 to 32, wherein the non-volatile memory (440) associated with the one or more channel modules (410) is on the respective channel modules (410).

34. Test system (400, 600, 800) according to any one of claims 22 to 33, wherein the non-volatile memory (430) associated with the device interface (420) is on the device interface (420).

35. Test system (400, 600, 800) according to any one of claims 22 to 34, further comprising an attachment (470) located between the one or more channel modules (410) and the device interface (420), wherein
at least information of a third part (330) of the calibration data, corresponding to the attachment, is stored on a non-volatile memory (430, 440, 450) associated with the attachment (470).

36. Test system (400, 600, 800) according to claim 35, wherein the non-volatile memory (450) associated with the attachment is on the attachment (470).

37. Test system (400, 600, 800) according to any one of claims 22 to 36, wherein any information is stored encrypted.

38. Test system (400, 600, 800) according to any one of claims 22 to 37, wherein the one or more channel modules (410) comprise a signal generator (460) or signal receiver (465).

39. Test system (400, 600, 800) according to any one of claims 22 to 38, wherein the device is a calibration module for calibrating the test system (400, 600, 800).

40. Test system (400, 600, 800) according to any one of claims 22 to 39, wherein the respective information of the first (310), second (320) and/or third (330) part of the calibration data is a memory address and an identification code of the associated one or more channel modules (410), device interface (420), and attachment (470), respectively, and wherein the calibration data is stored in a storage device at the memory address.

41. A device interface (420) for a test system (400, 600, 800), the test system (400, 600, 800) further comprising one or more channel modules, wherein:
at least information of a second part (320) of the calibration data (300) is stored on a non-volatile memory (430) associated with the device interface (420).

42. Device interface (420) according to claim 41, wherein the first part (310) of the calibration data is data corresponding to the one or more channel modules (410).

43. Device interface (420) according to any one of claims 41 to 42, wherein the second part (320) of the calibration data is data corresponding to the device interface (420).

44. Device interface (420) according to any one of claims 41 to 43, wherein the device interface (420) is a high-speed digital interface.

45. Device interface (420) according to any one of claims 41 to 44, wherein the calibration data contains information of frequency characteristics of components for transmitting signals from the one or more channel modules (410) to the device.

46. Device interface (420) according to any one of claims 41 to 45, wherein the calibration data comprises at least two filters, the filters describing the frequency characteristics.

47. Device interface (420) according to claim 46, wherein the first part (310) of the calibration data is a first filter, and the second part (320) of the calibration data is a second filter.

48. Device interface (420) according to any one of claims 46 to 47, wherein the filters are compensation filters.

49. Device interface (420) according to any one of claims 41 to 48, wherein the calibration data comprises transmissions functions, the transmission functions describing the frequency characteristics.

50. Device interface (420) according to any one of claims 41 to 49, wherein the calibration data comprises one or more of

tap coefficients of digital filters,

Fourier series, and/or

a two-port network model.

51. Device interface (420) according to any one of claims 41 to 50, wherein each calibration data is unified by

convolution for a time domain,

multiplication for a frequency domain, and/or

cascaded two-port networks for two-port networks.

52. Device interface (420) according to any one of claims 41 to 51, wherein the non-volatile memory (430) associated with the device interface (420) is on the device interface (420).

53. Device interface (420) according to any one of claims 41 to 52, the test system (400, 600, 800) further comprising an attachment (470) located between the one or more channel modules (410) and the device interface (420), wherein

at least information of a third part (330) of the calibration data, corresponding to the attachment, is stored on a non-volatile memory (430, 450) associated with the attachment (470).

54. Device interface (420) according to claim 53, wherein the non-volatile memory (450) associated with the attachment is on the attachment (470).

55. Device interface (420) according to any one of claims 41 to 54, wherein any information is stored encrypted.

56. Device interface (420) according to any one of claims 41 to 55, wherein the device is a calibration module for calibrating the test system (400, 600, 800).

57. Device interface (420) according to any one of claims 41 to 56, wherein the respective information of the first (310), second (320) and/or third (330) part of the calibration data is a memory address and an identification code of the associated one or more channel modules (410), device interface (420), and attachment (470), respectively, and wherein the calibration data is stored in a storage device at the memory address.

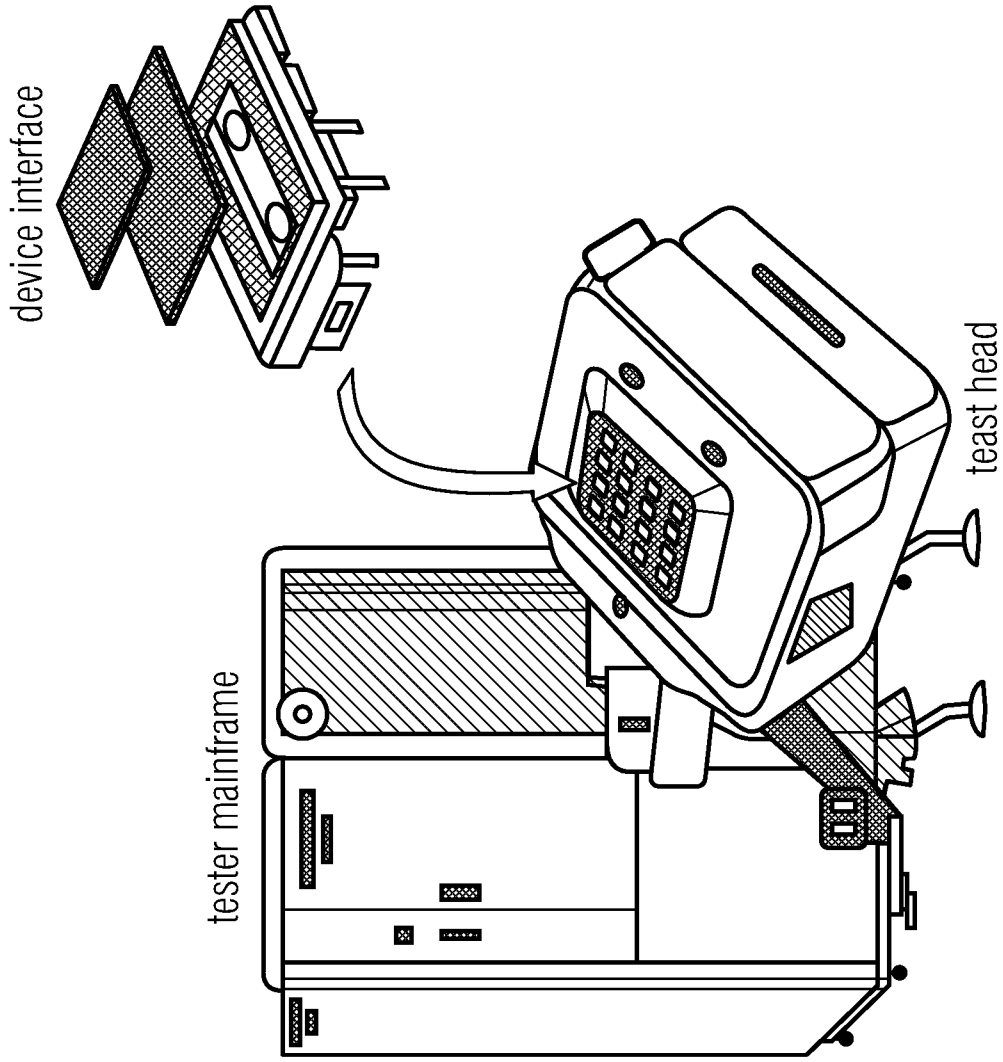

device interface
teast head
tester mainframe

Fig. 2

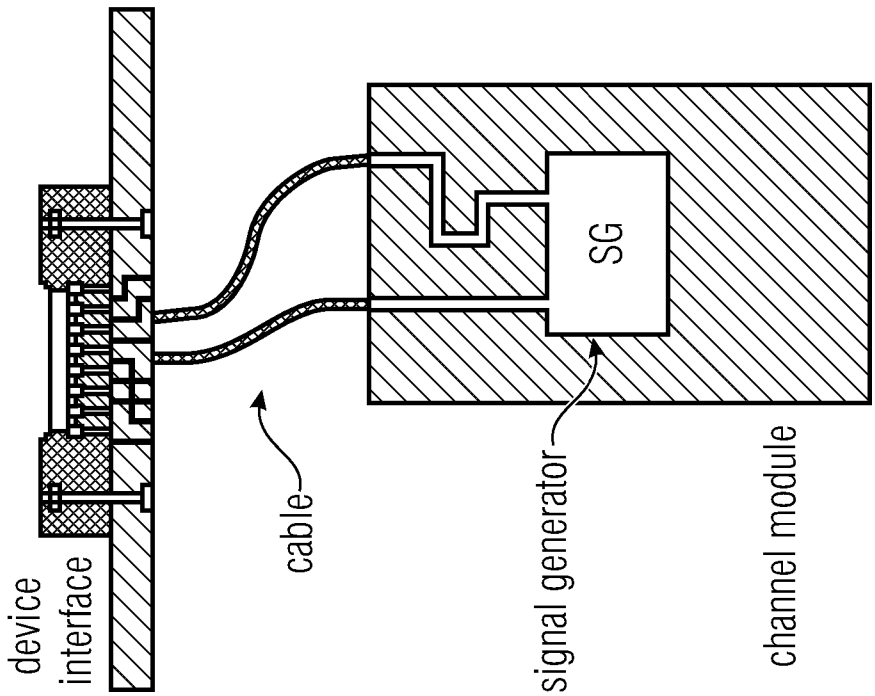
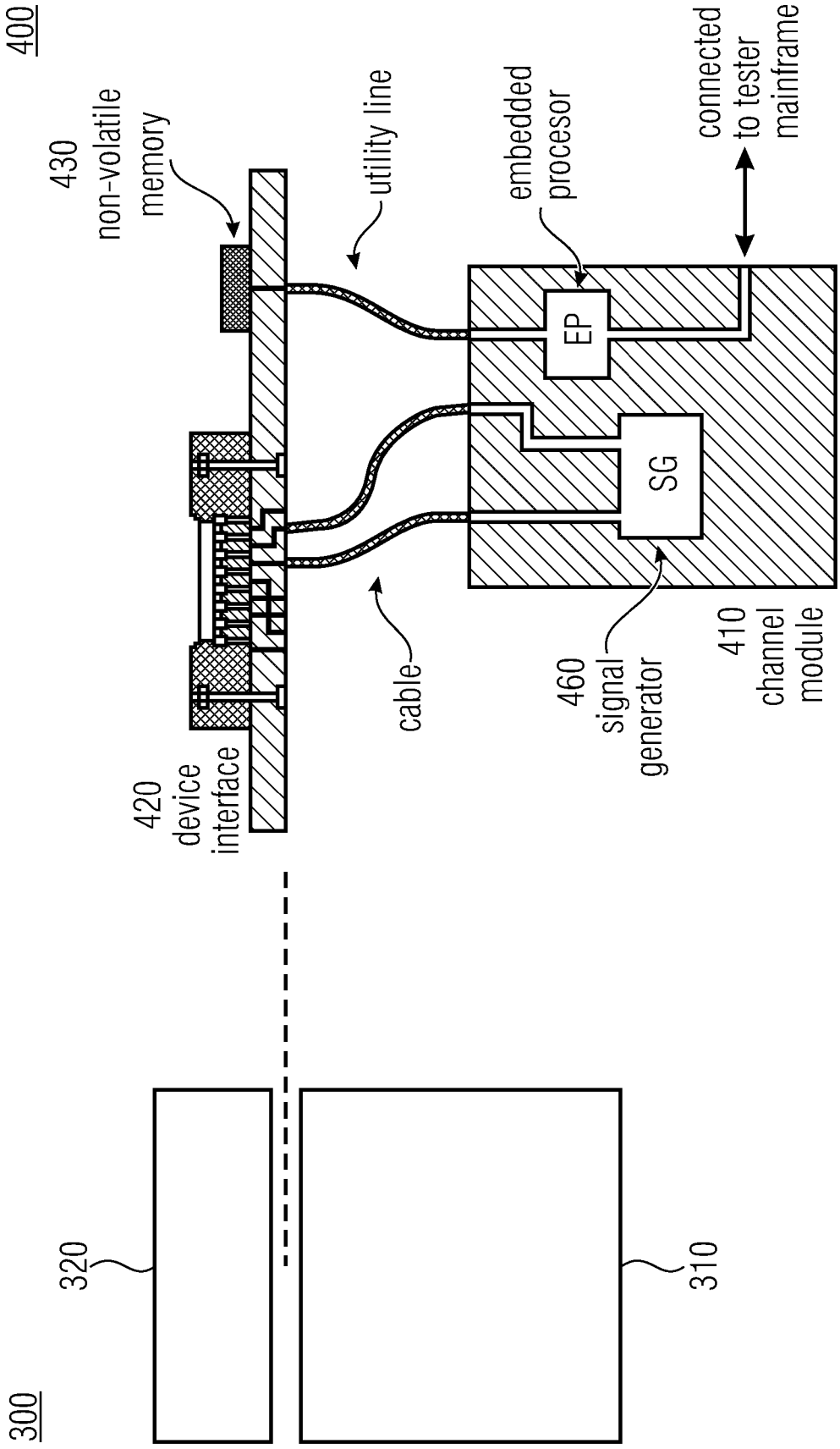

SG
device interface
cable
signal generator
channel module

Fig. 1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procesor
connected
to tester
mainframe
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SG
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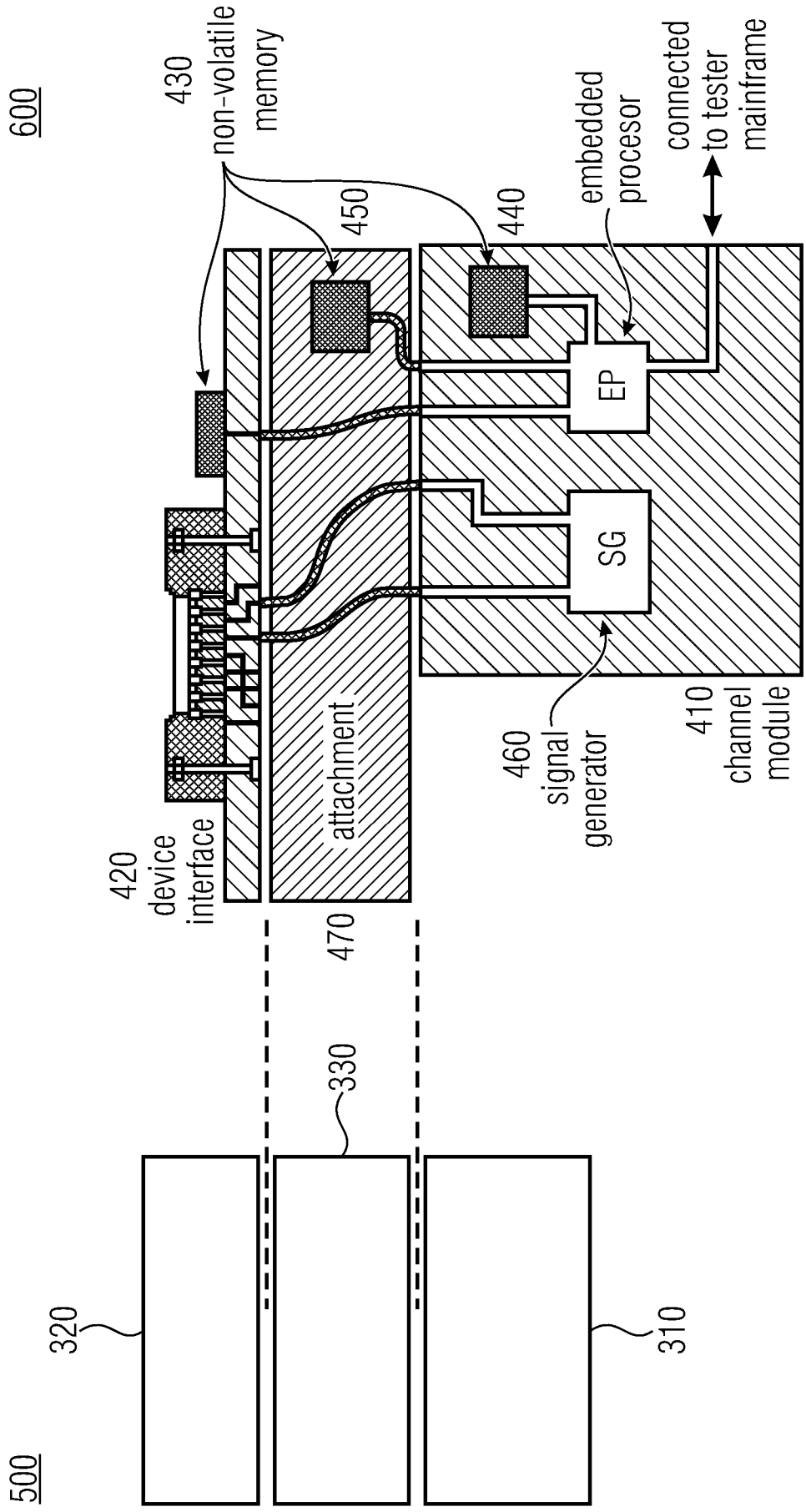
device
interface
cable
460
signal
generator
410
channel
module
300
320
310

Fig. 4

Fig. 3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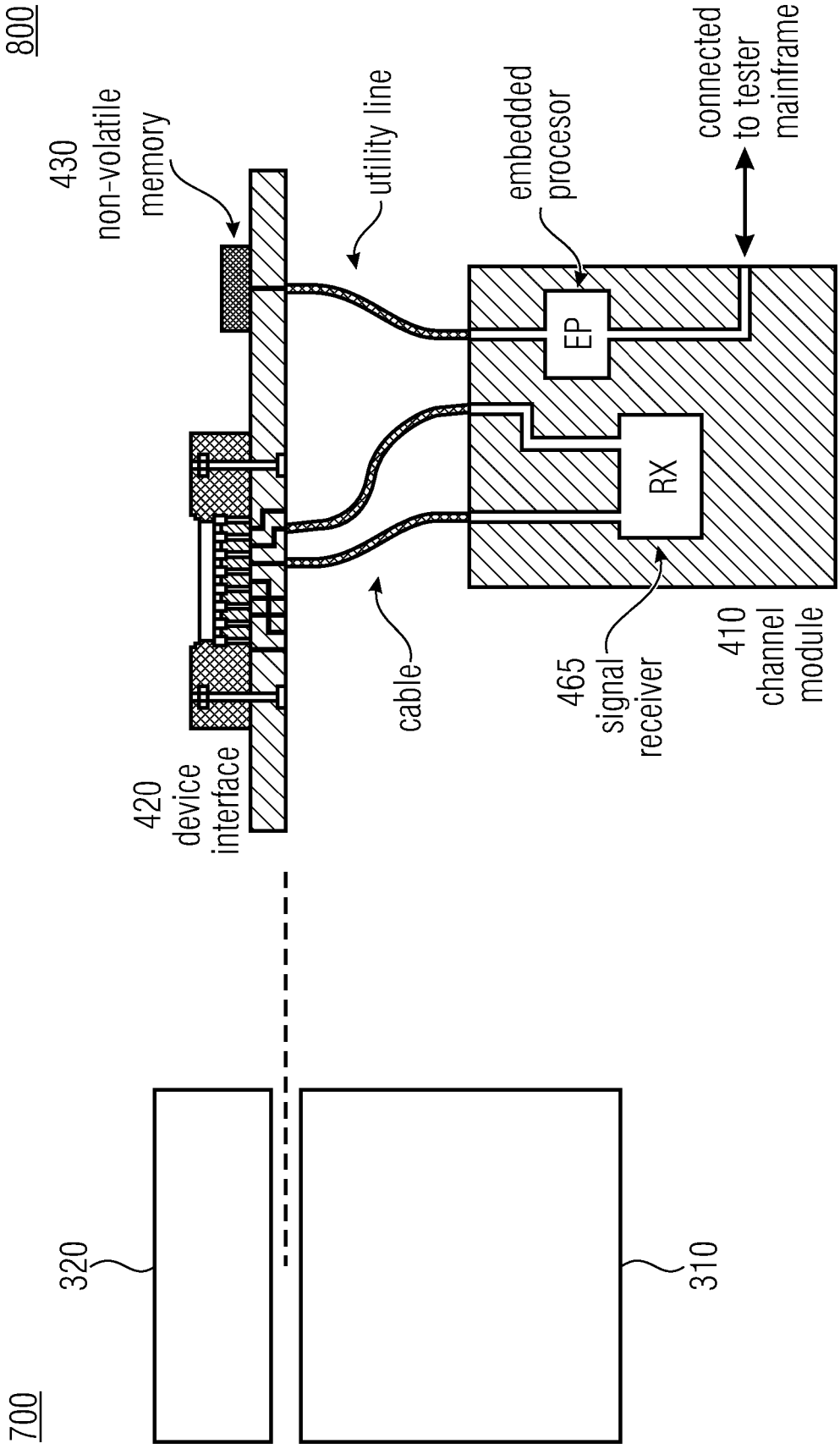
memory
450
440
embedded
procesor
connected
to tester
mainframe
EP
SG
420
device
interface
attachment
470
460
signal
generator
410
channel
module
330
320
310
500

Fig. 5

Fig. 6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non-volatile
memory
utility line
embedded
procesor
connected
to tester
mainframe
EP
RX
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device
interface
cable
465
signal
receiver
410
channel
module
700
320
310

Fig. 8

Fig. 7

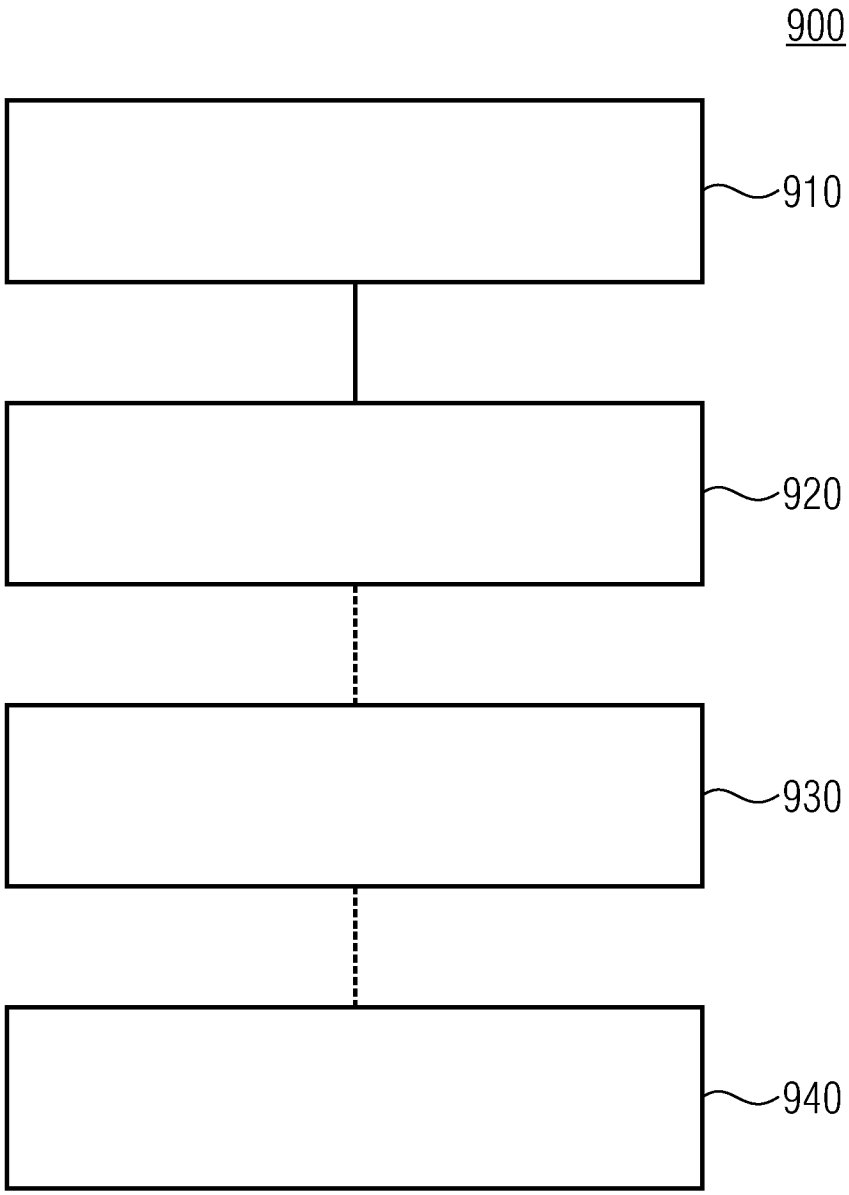

Fig. 9

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2020/065564

A. CLASSIFICATION OF SUBJECT MATTER
INV. G01R31/319
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2003/110427 A1 (RAJSUMAN ROCHIT [US] ET AL) 12 June 2003 (2003-06-12) abstract; claims 1-29; figures 1-12 paragraph [0015] - paragraph [0025] paragraph [0038] - paragraph [0089] -----	1-57
X	US 2004/186675 A1 (LARSON DOUGLAS [US] ET AL) 23 September 2004 (2004-09-23) abstract; claims 1-36; figures 1-15 paragraph [0009] - paragraph [0015] paragraph [0033] - paragraph [0073] -----	1-57
X	US 2004/181731 A1 (RAJSUMAN ROCHIT [US] ET AL) 16 September 2004 (2004-09-16) abstract; claims 1-8; figures 1-14 paragraph [0019] - paragraph [0030] paragraph [0045] - paragraph [0100] -----	1-57
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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 February 2021	23/02/2021

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Nadal, Rafael

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INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2020/065564

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 923 098 A (OLSON DONALD R [US]) 13 July 1999 (1999-07-13) abstract; claims 1-6; figures 1-4 column 1, line 45 - column 2, line 30 column 2, line 50 - column 4, line 26 -----	1-57
X	US 5 629 880 A (NEGISHI TOSHIYUKI [JP]) 13 May 1997 (1997-05-13) abstract; claims 1-6; figures 1-9I column 3, line 27 - column 4, line 11 column 4, line 41 - column 8, line 50 -----	1-57

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2020/065564

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