Abstract: A device that includes a core and a wrapper. The wrapper includes at least one shared wrapper cell that is shared by a group of core pins that belong to a single clock domain. A method for designing a wrapper. The method includes receiving design information representative of a design of a core, locating a group of mutually independent core pins that belong to a single clock domain; and designing a shared wrapped cell that is shared by the group of core pins.
DEVICE AND METHOD FOR TESTING A DEVICE

FIELD OF THE INVENTION
The present invention relates to methods for testing devices, methods for designing wrappers and a device having test capabilities.

BACKGROUND OF THE INVENTION
The complexity of integrated circuits forced designers to use various testing procedures and architectures.

During the last couple of years a group of companies developed what is now known as the IEEE P1500 scalable architecture for testing embedded cores. In a nutshell, the P1500 defines an integrated circuit architecture that is based upon wrappers that wrap cores (these re-usable cores are also referred to as Intellectual Property). The development of the P1500 was intended to ease the testing procedures of multiple core integrated circuits and simplify the re-use of previously developed cores.

The following two articles, also being incorporated herein by reference, also describe P1500 compliant wrappers: "Design of reconfigurable access wrappers for embedded core based SOC test", S. Kpranne, Proceedings of the international symposium on quality electronic design (ISQED'02), 2002 IEEE; and "IEEE P1500-compliant test wrapper design for hierarchical cores", A. Sehgal, S.K. Goel, E. J. Marinissen, K. Chakrabarty, ICT international test conference, 2004 IEEE.

FIG. 1 illustrates a prior art P1500 compliant integrated circuit 8. For simplicity of explanation FIG. 1 illustrates only a single core 9, but those of skill in the art will appreciate that a P1500 compliant integrated circuit usually includes multiple cores that can be arranged in a hierarchical manner.

Integrated circuit 8 includes core 9 that is wrapped by wrapper 11. Core 9 has many core pins. Each core pin is connected to one wrapper cell. It is noted that two wrapper cells can be required per core pin if the wrapper is required to enable at speed testing of core 9.

The wrapper cells 12 are also connected to each other in order to form a wrapper boundary register. In addition, wrapper 11 includes a wrapper serial input 12, a wrapper serial output (WSO) 13, a wrapper instruction register (WIR) 17, a wrapper bypass register 15, and test access mechanism (TAM) 16 that is connected to wrapper 11.

Many modern cores include a large number of pins. Allocating one or even two wrapper cells per each core pin is area consuming, as well as complicates the design of the wrapper.
There is a need to provide an efficient wrapper, efficient method for designing wrappers and an efficient method for testing devices.

SUMMARY OF THE PRESENT INVENTION
Method for testing a device, method for designing a wrapper and a device having test capabilities as described in the accompanying claims.

BRIEF DESCRIPTION OF THE DRAWINGS
The present invention will be understood and appreciated more fully from the following detailed description of embodiments thereof taken in conjunction with the accompanying drawings in which:

FIG. 1 is a schematic diagram of a prior art P1500 compliant integrated circuit;
FIG. 2 illustrates a device according to an embodiment of the invention;
FIG. 3 illustrates a shared wrapper cell according to an embodiment of the invention;
FIG. 4 illustrates multiple shared wrapper cells and additional circuits of a core, according to an embodiment of the invention;
FIG. 5 is a timing diagram illustrating various clock signals that are provided to shared wrapper cells, according to an embodiment of the invention;
FIG. 6 is a flow chart of a method for testing a device, according to an embodiment of the invention;
FIG. 7 is a flow chart of a method for designing a wrapper, according to an embodiment of the invention; and
FIG. 8 illustrates a shared wrapper cell according to an embodiment of the invention.
DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Embodiments of the present invention illustrated in the accompanying drawings provide a device that includes a core and a wrapper that includes at least one shared wrapper cell that is shared by a group of core pins that belong to a single clock domain. Typically, an integrated circuit that includes multiple clock domains may include one or more shared wrapper cells per clock domain.

Embodiments of the present invention illustrated in the accompanying drawings provide a method for testing a device. The method includes determining whether to operate an integrated circuit in a test mode or in a non-test mode, and connecting a group of core pins (that belong to a single clock domain) to a shared wrapper cell during a test mode.

Embodiments of the present invention illustrated in the accompanying drawings provide a method for designing a wrapper. The method includes receiving information representative of a design of a core; locating a group of mutually independent core pins that belong to a single clock domain; and designing a shared wrapped cell that is shared by the group of core pins.

The integrated circuit 10 is conveniently a part of a device 10' such as but not limited to a mobile phone, a music player, a laptop computer, a desktop processor, a base station, and the like. Device 10' can include multiple integrated circuits such as integrated circuit 10. Device 10' can also be an integrated circuit.

FIG. 2 illustrates an integrated circuit 10 according to an embodiment of the invention.

For simplicity of explanation integrated circuit 10 is illustrated as including a single core 20 and as including a single clock domain. It is noted that this is
not necessarily so and in many cases a single integrated circuit includes multiple cores. Each core can have its own wrapper. In addition many integrated circuits may include multiple clock domains. Conveniently each clock domain includes one or more shared wrapper cells.

Core 20 includes many pins. A pin includes any type of connector or connection that allows signals to enter the core 20 and/or to be outputted from the core 20.

Core 20 is surrounded by wrapper 30. Wrapper 30 includes multiple wrapper cells, various registers and the like. A wrapper such as 30 can include a large number and even a very large number of shared wrapper cells. The inventors tested a circuit that includes more than two hundred shared wrapper cells.

Wrapper 30 includes one or more shared wrapper cells such as shared wrapper cells 40_i, 40_j, 40_k, and 40_l. It is noted that wrapper 30 can include a single wrapper cell, and can include multiple wrapper cells.

A shared wrapper cell is a wrapper cell that can be connected in parallel to a group of core pins, during a certain test mode of the integrated circuit. In other modes, such as a normal (non-test) mode, the shared wrapper cell can be transparent - it receives multiple signals and outputs these multiple signals to the core pins.

By using shared wrapper cells the number of wrapper cells as well as the area of the wrapper can be decreased and even dramatically decreased. The inventors achieved a 1:3 area ratio between a wrapper that was based upon shared wrapper cells and a wrapper that included non-shared test wrapper cells.

Sharing a single wrapper cell by a group of core pins can theoretically limit the testability of the core,
as the same test signal is applied to this group of core pins. The inventors found that by selecting group of pins that include mutually independent pins this theoretical limitation does not influence (or does not substantially influence) the testability of the core. In addition, the size of the group of core pins can be adjusted to further reduce any possible testing limitation. Mutually independent pins can be pins that can convey signals that are not dependent upon each other. Mutually independent core pins are pins that are not forced by certain logical connections, to convey signals that differ from each other. Typical dependent core pins are core pins that convey instructions while typical independent core pins convey data, as the constrains imposed upon the values of data that is conveyed over data buses during test modes can be more relaxed.

The inventors compared between a first wrapper that includes non-shared wrapper cells and a second wrapper that included shared wrappers cells. The size of the shared wrapper cells was eight meaning that each wrapper cell is connected to eight core pins. The core included 21,000 flip-flops and was completely scanable (all the flip-flops of the core were connected to form one or more core scan chains).

TABLE 1 compares between the characteristics of both wrappers:

<table>
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<th>Characteristic</th>
<th>First wrapper (non-shared)</th>
<th>Second wrapper (shared)</th>
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<tbody>
<tr>
<td>Number of wrapper cells</td>
<td>1824</td>
<td>235</td>
</tr>
<tr>
<td>Number of wrapper flip-flops</td>
<td>3648</td>
<td>235</td>
</tr>
<tr>
<td>Wrapper scan chain</td>
<td>912</td>
<td>59</td>
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A size of a wrapper cell indicates the number of core pins that are connected to the wrapper cell. The size of different shared wrapper cells can be the same or can differ from each other. For example, shared wrapper cell 40_k can have fewer outputs than shared wrapper cell 40_j.

Referring back to FIG. 2, shared wrapper cell 40_k is shared by a group 60 of core pins that belong to a single clock domain. It is noted that the number of pins that belongs to group 60 exceeds one. The inventors used groups of eight core pins. It is noted that other sized groups can be used.

The shared wrapper cell 40_k is also connected to other wrapper cells. FIG. 4 illustrates a chain of four shared wrapper cells 40_i – 40_l. It is noted that shared wrapper cells can be connected to non-shared wrapper cells and that the chain of wrapper cells is closed such as to form a loop of wrapper cells, for transition testing.

FIG. 3 illustrates a shared wrapper cell 40_k according to an embodiment of the invention.
Shared wrapper cell 40_k includes: (i) multiple \( (N) \) inputs \((46(1)-46(N))\) collectively denoted 46, wherein \( N \) is a positive integer that defines the size of the share wrapper cell 40_k, (ii) multiple \( (N) \) outputs \((42(1)-42(N))\) collectively denoted 42, (iii) multiple \( (N) \) output multiplexers \((49(1)-49(N))\), adapted to select between test signal and between an input signal, (iv) wrapper cell flip-flop 44, (v) isolate mode multiplexer 47, (vi) test signal selection multiplexer 41, and (vii) launch multiplexer 43.

Assuming that \( n \) is an index that ranges between 1 and \( N \) then the \( 46(n) \) input is connected to an \( n'\)th input \((41(n))\) of the test signal selection multiplexer 41, and to a first input \((49(n,1))\) of output multiplexer 49(n).

Inputs \( 41(1)-41(N) \) of test signal multiplexer 41 are connected to inputs \( 46(1)-46(N) \). The control input \( 41(c) \) of test signal multiplexer 41 is connected to control circuit 80 of FIG. 4.

The output \( 41(o) \) of test signal selection multiplexer 41 is connected to a first input \( 43(1) \) of launch multiplexer 43. The second input \( 43(2) \) of the launch multiplexer 43 is connected to an output of a wrapper flip flop that belongs to a previous shared wrapper cell 40_j.

The output \( 43(4) \) of launch multiplexer 43 is connected to input \( 44(1) \) of wrapper flip-flop 44. Launch multiplexer 43 can send to the wrapper flip-flop 44 either a selected test signal or a signal from a previous wrapper flip-flip. The signal from the previous wrapper flip-flop can be provided to core 20 during a transition test (also referred to as an ac-speed test) of core 20.

Conveniently, a launch vector serially propagates through a chain of wrapper flip-flops. During a
transition test the wrapper flip-flops output in parallel the launch vector, and the response of the core (or usually various circuits within the core) is sampled and later on outputted from the core 20.

A first input 47(1) of isolate mode multiplexer 47 is connected to an output 44(3) of wrapper flip-flop 44. A second input 47(2) is connected to an isolate mode signal provider (illustrated as Ground 39). The output 47(4) of isolate mode multiplexer 47 is connected to second inputs 49(1,2) - 49(N,2) of output multiplexers 49(I) - 49(N).

Each output multiplexer 49(n) includes two inputs 49(n,1) and 49(n,2), one control input 49(n,3) and one output 49(n,4). The first input 49(n,1) of output multiplexer 49(n) is connected to the n'th input 46(n), while the output 49(n,4) of output multiplexer 49(n) is connected to an n'th core pin of group 60. Outputs (46(1) - 46(N)) are collected to multiple input pins (60(1) - 60(N)) that belong to a group 60 of core pins.

Second inputs 49(1,2) - 49(N,2) of output multiplexers 49(1) - 49(N) are connected to the output 47(4) of isolate mode multiplexer 47.

The n'th output 42(n) of shared wrapper cell 40 can provide to core pin 60(n): (i) an input signal from a corresponding input (46(n)) of shared wrapper cell 40_k, during a non-test mode of integrated circuit 10; (ii) an isolate signal from isolate mode multiplexer 47, during an isolate mode; or (iii) a test signal, provided from wrapper cell flip-flop 44. It is noted that the test signal as well as the isolate signal are provided in parallel to all outputs 42(1) - 42(N).

Multiplexers 41, 43, 47 and 49(1) - 49(N) are controlled by control signals that are generated by a
controller 80 (illustrated in FIG. 4). At least part of the controller 80 can be included within wrapper 30.

Controller 80 sends the following control signals: (i) select test signal 81, (ii) isolate mode signal 82, and (iii) operational mode signal 83. Select test signal 81 is provided to test signal selection multiplexer 41 in order to select which input out of inputs 46(1)-46(N) shall provide a selected test signal to wrapper flip-flop 44. Isolate test mode 82 is provided to isolate mode multiplexer 47 in order to select whether to provide an isolate mode signal to output multiplexers 49(1)-49(N) or to provide a test signal to these output multiplexers. Optionally, the isolate mode is also provided to launch multiplexer 43 so that it selects the output of the previous wrapper flip-flop during at speed test. Operational mode signal 83 is provided to each of the output multiplexers.

Those of skill in the art will appreciate that the wrapper flip-flop can be a part of a scan chain. Such a scan chain can include flip-flops of wrapper cells but this is not necessarily so. For simplicity of explanation the additional logic (usually an additional multiplexer) required for connecting the wrapper flip-flop to another flip-flop that belongs to the scan chain (if that other flip-flop differs from the wrapper flip-flops of wrapper cells 40_j and 40_l) is not illustrated.

FIG. 8 illustrates a shared wrapper cell 40_j according to an embodiment of the invention.

Shared wrapper cell 40_j is conveniently used as an output shared wrapper cell that is connected to outputs of a core while shared wrapper cell 40_k is conveniently used as an input shared wrapper cell that is connected to inputs of a core.
Shared wrapper cell 40_j differs from shared wrapper cell 40_k by not having an isolate mode multiplexer 47, by controlling its output multiplexers by isolate mode signal 82 instead of controlling its output multiplexers by a operational mode signal 83, and by providing an inverted isolate mode signal (instead of providing an isolate mode signal) to its launch multiplexer.

Shared wrapper cell 40_j includes: (i) multiple (N) inputs (46' (I)- 46' (N)) collectively denoted 46', wherein N is a positive integer that defines the size of the share wrapper cell 40_j, (ii) multiple (N) outputs (42' (I)- 42' (N)) collectively denoted 42', (iii) multiple (N) output multiplexers (49' (I)- 49' (N)), adapted to select between test signal and between an input signal, (iv) wrapper cell flip-flop 44', (v) test signal selection multiplexer 41', and (vi) launch multiplexer 43'.

Due to the absence of isolate mode multiplexer 47 the output 44' (3) of wrapper flip-flop 44 is connected to the second inputs 49' (1,2)- 49' (N, 2) of output multiplexers 49'.

The multiple (N) inputs (46' (I)- 46' (N)) are collected to multiple output pins (60' (I)- 60' (N)) of core 60, collectively denoted 60'.

FIG. 4 illustrates multiple shared wrapper cells 40_i - 40_l and additional circuits of core 20, according to an embodiment of the invention.

Shared wrapper cells 40_i and 40_k are connected to input pins of core 20 while shared wrapper cells 40_j and 40_l are connected to output pins of core 20. These four shared wrapper cells are connected in serial to each other such as to form a closed loop. All shared wrapper
cells receive the same select test signal \('\) from controller 80.

Shared wrapper cells 40\_i and 40\_k, as well as additional wrapper cells (not shown) are used to serially propagate a launch vector. The launch vector can be provided to these wrapper cells via a wrapper serial input (WPI).

Shared wrapper cells 40\_i and 40\_k are connected to circuits 21\(\_i\) and 21\(\_j\) of core. Circuits 21\(\_i\) and 21\(\_j\) are also connected to sampling circuit 22\(\_i\) and 22\(\_j\). Sampling circuits 22\(\_i\) and 22\(\_j\) can be a part of scan chain 22.

During an at-speed test the shared wrapper cell 40\_i sends to circuits 21\(\_i\) and 21\(\_j\) a launch vector. The response of circuits 21\(\_i\) and 21\(\_j\) to the launch vector is sampled by sampling circuit 22\(\_i\) and 22\(\_j\). This response vector can be later outputted from core 20 in various manners, for example by using a scan chain 22 that includes sampling circuits 22\(\_i\) and 22\(\_j\).

Typically, core 20 receives a very fast clock signal (CLK\_core 91), while the shared wrapper cells 40 receives a much slower clock (CLK\_wrapper 92). The transition test is enabled by synchronizing both clocks, so that during a launch cycle both clock signal transient substantially simultaneously. This is not necessarily so. For example, the frequency of the clock provided to the shared wrapper cells can equal the frequency of the clock provided to core 20, as illustrated by the dashed waveform denoted CLK\_wrapper 92'.

FIG. 5 is a timing diagram illustrating various clock signals that are provided to shared wrapper cells 40\_i and 40\_k, according to an embodiment of the invention.
If the input shared wrapper cells include R shared wrapper cells then during R cycles of CLK_wrapper 92 the launch vector serially propagates through these shared wrappers of the chain. At the (R+1)'th cycle of CLK_wrapper 92 the launch vector is provided to core 20 and especially to various tested circuits such as 21 (1) and 21 (3).

The (R+1)'th cycle of CLK_wrapper 92 starts when a Q'th cycle of CLK_core 91 starts. At the (Q+1)'th clock cycle of CLK_core 91 the response of core 20 is sampled.

FIG. 6 is a flow chart of method 100 for testing a device, according to an embodiment of the invention.

Method 100 starts by stage 110 of determining the operational mode of a core. Conveniently, the core can operate in a non-test mode, in an isolate mode and in a test mode.

If non-test mode is selected stage 110 is followed by stage 112 of operating in a non-test mode during which the wrapper cell is transparent. Referring to the example set in previous figures, the signals that arrive to inputs 46(1)- 46(N) are provided, via output multiplexers 49(1) - 49(N) to outputs 42(1)- 42(N).

If an isolate mode is selected then stage 110 is followed by stage 114 of operating in an isolate mode.

During this mode input shared wrapper cells provide isolate mode signals (such as ground) to the core, thus isolating the core from inputs signals provided to the inputs of the shared wrapper cell.

If test mode is selected then stage 110 is followed by stages 140-150. Stage 130 includes allowing group of core pins that belong to a single clock domain to receive a test signal from a shared wrapper cell during a test mode.
Stage 140 includes selecting the test signal out of multiple signals provided to multiple inputs of the shared wrapper cell.

Stage 150 includes providing, during the test mode, the same test signal to all the core pins that belong to the group of core pins. Conveniently, stage 150 includes connecting all the core pins that belong to the group of core pins to a wrapper cell flip-flop within the shared wrapper cell.

Stage 150 can be followed by stage 110 or stage 160. Stage 160 includes providing a launch vector to serially connected wrapper flip-flops of shared wrapper cells.

Stage 160 is followed by stage 170 of sending in parallel the launch vector to multiple core pins that are connected to the serially connected wrapper flip-flops.

Stage 170 is followed by stage 180 of sampling a response of multiple components of the core to the launch vector.

FIG. 7 is a flow chart of method 200 for designing a wrapper, according to an embodiment of the invention.

Method 200 starts by stage 210 of receiving design information representative of a design of a core.

Stage 210 is followed by stage 220 of receiving group size indication. This can indicate allowable sizes of groups of core pins that share shared wrapper cells. The previous drawings illustrated an N sized shared wrapper cell 40_k.

Stage 220 is followed by stage 230 of locating a group of mutually independent core pins that belong to a single clock domain. Conveniently, stage 230 is responsive to the group size information. It is noted that a typical integrated circuit includes many groups of
mutually independent core pins. These can be data conveying core pins but this is not necessarily so.

According to an embodiment of the invention the user or designer can provide group size information, the method can locate one or more groups in response to the design information, and if the size of the group does not match the group size then another iteration of the locating stage can be executed. Alternatively the user or designer can be requested to alter the size group information.

Stage 230 is followed by stage 250 of designing a shared wrapper cell that is shared by the group of core pins. Conveniently, the designing includes designing the wrapper cell such as to be transparent during a normal mode. Such a shared wrapper cell can have substantially the same structure of shared wrapper cell 40_k.

Stage 250 is followed by stage 260 of defining a sequence of wrapper flip-flops wherein at least one wrapper flip-flop can operate as a launch element for an adjacent wrapper filp-flop. A launch element is an element that propagates a launch vector to another launce element.

Referring to the example provided in FIG. 3, the shared wrapper cells may include shared wrapper cells 40_i and 40_k. These shared wrapper cells include wrapper flip-flops that are serially connected to each other by circuits such as launch multiplexer 43.

In order to enable at speed tests, the wrapper flip-flops should be designed to propagate a launch vector and to provide the launch vector to various circuits within core 20 during a launch cycle.

The clock signal provided to the wrapper flip flops should be synchronized with the clock signal that is
provided to the circuits within core 20 that are tested during the at speed test.

Variations, modifications, and other implementations of what is described herein will occur to those of ordinary skill in the art without departing from the spirit and the scope of the invention as claimed. Accordingly, the invention is to be defined not by the preceding illustrative description but instead by the spirit and scope of the following claims.
WE CLAIM

1. A device (10') that comprises a core (20); wherein the device (10') is characterized by comprising a wrapper (30) that comprises at least one shared wrapper cell (40_k) that is shared by a group (60) of core pins that belong to a single clock domain.

2. The device (10') according to claim 1 wherein the shared wrapper cell (40_k) comprises a group (42) of wrapper cell outputs that are coupled to the group (50) of core pins; wherein during a test mode all the outputs of the group (60) of core pins receive the same test signal.

3. The device (10') according to claim 2 wherein the shared wrapper cell (40_k) comprises a wrapper cell flip-flop (44) that is coupled to the group (42) of wrapper cell outputs during the test mode.

4. The device (10') according to any claim of claims 2-3 wherein the shared wrapper cell (40_k) comprises a group (46) of wrapper cell inputs, and an input selection circuit (48) adapted to select, out of multiple input signals provided to the shared wrapper cell (40_k) the test signal.

5. The device (10') according to any claim of claims 1-4 wherein each wrapper cell comprises a wrapper cell flip-flops and wherein the wrapper cell flip-flops are serially coupled to each other; wherein at least one wrapper flip-flop functions as a launch element for an adjacent wrapper flip-flop.

6. The device (10') according to any claim of claims 1-5 wherein the core pins that belong to the group (60) of core pins are mutually independent.
7. The device (10') according to any claim of claims 1-6 wherein the core pins that belong to the group (60) of core pins convey data signals during a non-test mode of the integrated circuit.

8. The device (10') according to any claim of claims 1-7 wherein the wrapper (30) comprises at least one shared wrapper cell (40_k) and at least one non-shared wrapper cell (40').

9. The device (10') according to any claim of claims 1-8 wherein the wrapper (30) comprises a first shared wrapper cell (40_k) and a second shared wrapper cell (40'), wherein the first shared wrapper cell (40_k) has fewer output pins than the second shared wrapper cell (40').

10. A method (100) for testing a device, the method (100) comprises determining (110) an operational mode of a core; wherein the method (100) is characterized by allowing (130) a group of core pins that belong to a single clock domain to receive a test signal from a shared wrapper cell during a test mode.

11. The method (100) according to claim 10 further comprising providing (150), during a test mode, the same test signal to all the core pins that belong to the group of core pins.

12. The method (100) according to claim 11 wherein the providing (150) comprises coupling all the core pins that belong to the group of core pins to a wrapper cell flip-flop within the shared wrapper cell.

13. The method (100) according to any claim of claims 11-12 wherein the providing (150) is preceded by selecting (140) the test signal out of multiple signals provided to multiple inputs of the shared wrapper cell.
14. The method (100) according to any claim of claims 11-13 further comprising providing (160) a launch vector to serially coupled wrapper flip-flops of wrapper cells, and sending (170) in parallel the launch vector to multiple core pins coupled to the serially coupled wrapper flip-flops; and sampling (180) a response of multiple components of the core to the launch vector.

15. The method (100) according to any claim of claims 11-14 further comprising defining (105) a group of core pins that are mutually independent.

16. A method (200) for designing a wrapper; the method (200) comprises receiving (210) information representative of a design of a core; the method (200) is characterized by comprising: locating (230) a group of mutually independent core pins that belong to a single clock domain; designing (250) a shared wrapped cell that is shared by the group of core pins.

17. The method (200) according to claim 16 further comprising receiving (220) group size indication, and wherein the locating (230) is responsive to the group size information.

18. The method (200) according to any claim out of claims 16-17 wherein the designing (250) further comprises designing the wrapper cell such as to be transparent during a normal mode.

19. The method (200) according to any claim out of claims 16-18 further comprising defining (260) multiple wrapper cells that comprise multiple wrapper flip-flops; wherein the wrapper flip-flop of different wrapper cells are serially coupled to each other; wherein at least one wrapper flip-flop functions as a launch element for an adjacent wrapper flip-flop.
TEST MODE

determining in what mode to operate the integrated circuit 110

NON-TEST MODE

allowing group of core pins that belong to a single clock domain to receive a test signal from a shared wrapper cell during a test mode 130

selecting the test signal out of multiple signals provided to multiple inputs of the shared wrapper cell 140

providing, during the test mode, the same test signal to all the core pins that belong to the group of core pins 150

Operating in non-test mode 112

Operating in isolate mode 114

providing a launch vector to serially coupled wrapper flip-flops of wrapper cells 160

sending in parallel the launch vector to multiple core pins coupled to the serially coupled wrapper flip-flops 170

sampling a response of multiple components of the core to the launch vector 180

FIG. 6
receiving design information representative of a design of a core.

locating a group of mutually independent core pins that belong to a single clock domain.

designing a shared wrapper cell that is shared by the group of core pins.

defining multiple wrapper cells that include multiple wrapper flip-flops.
A. CLASSIFICATION OF SUBJECT MATTER
INV. G01R 31/3185

According to International Patent Classification (IPC) or both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and where practical, search terms used)
EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
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<tr>
<th>Category</th>
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<th>Relevant to claim No</th>
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Further documents are listed in the continuation of Box C

See patent family annex

- Special categories of cited documents
- 'A' document defining the general state of the art which is not considered to be of particular relevance
- 'E' earlier document but published on or after the international filing date
- 'L' document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- 'O' document referring to an oral disclosure, use, exhibition or other means
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- 'X' document of particular relevance, the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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Date of the actual completion of the international search
17 November 2006

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