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(54) **Title**: RESISTIVE ION SENSING DEVICE

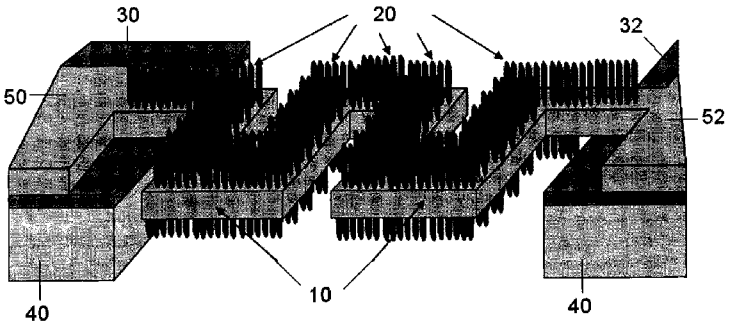

Figure 1

(57) **Abstract**: A sensor device and method of fabrication based on a change in electrical resistance comprising: a resistor structure having two ends; a plurality of 5 nanostructures attached to at least a portion of said resistor structure; a pair of contact pads, each contact pad located at each said end of the resistor structure; a substrate supporting each said end of the resistor structure; and an insulating layer sandwiched between said substrate and each said end of the resistor structure. The resistor structure between each said contact pad comprises either a long wire shaped in a serpentine fashion to cover a larger area or a plurality of wires running parallel to each other. In operation, an electrical current is maintained along the said resistor structure and the said nanostructures upon detecting receptive ions, changes the resistance of the said resistor structure, said change in resistance measurable by an external measuring means.

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RESISTIVE ION SENSING DEVICE

FIELD OF INVENTION

The present invention relates to a device for sensing ions based on a change in electrical resistance.

BACKGROUND OF INVENTION

Chemical gas detection has many applications in agriculture, environmental monitoring, biomedical and industrial processes. With the emergence of nanotechnology, new sensing materials have been developed, thus allowing passive type devices such as resistors to be used as a chemical sensing platform. Chemical sensors are attracting tremendous interest due to their widespread applications in industry, environmental monitoring, space exploration, biomedicine, and pharmaceutics. Gas sensors with high sensitivity and selectivity are required for leakage detections of explosive gases such as hydrogen, and for real-time detections of toxic or pathogenic gases in industries. There is also a strong demand for the ability to monitor and control our ambient environment, especially with the increasing concern of the globe warming. Micro sensors fabricated by MEMS technology have the advantages of small size, high performance, low cost and easy mass-production. With the emergence of nanotechnology, new sensing materials have been developed, thus allowing passive type devices such as micro-resistors to be used as a chemical sensing platform. However, at present such devices are more 2-dimensional with nanostructures and nano-materials incorporated only on the device surface utilising less than 50% of the total device area. Hence there is a limited area for ion detection resulting in lower or limited device sensitivity and performance.

What is desirable is a device that utilises a larger portion of the device surface area.

SUMMARY OF INVENTION

The present invention aims at providing a device that fully utilises its surface area by forming receptive nanostructures at all sides of a resistive structure.

This invention relates to a sensor device based on a change in electrical resistance comprising: a resistor structure having two ends; a plurality of nanostructures attached to at least a portion of said resistor structure; a pair of contact pads, each contact pad located at each said end of the resistor structure; a substrate supporting each said end of the resistor structure; and an insulating layer sandwiched between said substrate and each said end of the resistor structure. The resistor structure between each said contact pad comprises either a long wire shaped in a serpentine fashion to cover a larger area or a plurality of wires running parallel to each other. In operation, an electrical current is maintained along the said resistor structure and the said nanostructures upon detecting receptive ions, changes the resistance of the said resistor structure, said change in resistance measurable by an external measuring means. The nanostructures are either nanotubes or nanowires selected from a group consisting and not limited to carbon nanotubes, silicon nanowires, tungsten nanowires, tungsten oxide nanowires, zinc oxide nanowires, indium oxide nanowires, tin oxide nanowires, gold nanowires or a combination thereof. The nanostructures may be either uni-directional or multi-directional.

This invention also relates to a method of fabricating a sensor device comprising the steps of:

a) depositing insulating layers onto a front and a back side of a silicon substrate, the insulating layers are any or a combination of: silicon dioxide or silicon nitride deposited by physical or chemical vapour deposition; or silicon dioxide grown by a thermal oxidation method;

b) etching the said back side insulating layer done using either Tetrafluoromethane (CF_4) and Trifluoromethane (CHF_3) plasma or in a hydrofluoric acid (HF) based chemical solution;

c) depositing a first metal catalyst layer on the said front side insulating layer by physical or chemical vapour deposition (PVD or CVD) and made from any or a combination of: gold (Au), cobalt (Co), iron (Fe), nickel (Ni), indium (In) and copper (Cu);

d) depositing a conductive layer on the said first metal catalyst layer by PVD or CVD and made from any or a combination of: gold (Au), platinum (Pt), nickel (Ni), tungsten (W), cobalt (Co) and copper (Cu);

e) depositing a second metal catalyst layer on top of the said conductive layer by physical or chemical vapour deposition (PVD or CVD) and made from any or a combination of: gold (Au), cobalt (Co), iron (Fe), nickel (Ni), indium (In) and copper (Cu);

f) etching the said first metal catalyst layer, conductive layer and second metal catalyst layer simultaneously to form resistor and contact pad areas with Argon (Ar) plasma or in a wet chemical solution using an inductively coupled plasma reactive ion etching (ICP-RIE) method with sulphur hexafluoride (SF_6) based plasma, or with a wet chemical etchant of potassium hydroxide (KOH) or Tetramethylammonium Hydroxide (TMAH);

g) removing the said second metal catalyst layer from the said contact pad areas using buffered hydrofluoric acid (HF);

h) etching the said silicon substrate from the bottom to form an opening beneath the said front side insulating layer;

i) removing the said front side insulating layer from a resistor region, said resistor region located between the said contact pads; and

j) growing of nanostructures at the said resistor region from the exposed metal catalyst areas using a method selected from the group consisting of chemical vapour deposition (CVD), metalorganic chemical vapour deposition (MOCVD), plasma enhanced chemical vapour deposition (PECVD), hot wire chemical vapour deposition (HWCVD), atomic layer deposition (ALD), electrochemical deposition, solution chemical deposition or combinations thereof.

This invention also relates to a method of fabricating a sensor device comprising the steps of:

a) depositing insulating layers onto a front and a back side of a silicon substrate;
b) etching the said back side insulating layer;
c) depositing and etching a first metal catalyst layer on the said front side insulating layer;
d) depositing and etching a conductive layer on the said first metal catalyst layer;
e) depositing and etching a second metal catalyst layer on top of the said conductive layer;
f) etching the said silicon substrate from the bottom to form an opening beneath the said front side insulating layer;
g) removing the said front side insulating layer from a resistor region, said resistor region located between the said contact pads; and
h) growing of nanostructures at the said resistor region from the exposed metal catalyst areas.

This invention also relates to method of fabricating a sensor device comprising the steps of:

a) depositing a first metal catalyst layer on a substrate;
b) depositing a conductive layer on the said first metal catalyst layer;
c) depositing a second metal catalyst layer on top of the said conductive layer;
d) etching the said first metal catalyst layer, conductive layer and second metal catalyst layer simultaneously to form resistor and contact pad areas;
e) removing the said second metal catalyst layer from the said contact pad areas;
f) depositing and etching a backside masking material to be use as a mask during glass etching;
g) etching the said substrate from the bottom to form an opening beneath a resistor region, said resistor region located between the said contact pads;

h) growing of nanostructures at the said resistor region from the exposed metal catalyst areas.

The metal catalysts are deposited by physical or chemical vapour deposition (PVD or CVD) and made from any or a combination of: gold (Au), cobalt (Co), iron (Fe), nickel (Ni), indium (In) and copper (Cu). The conductive layer (704) is deposited by PVD or CVD and made from any or a combination of: gold (Au), platinum (Pt), nickel (Ni), tungsten (W), cobalt (Co) and copper (Cu). The said etching of the said first metal catalyst layer (703), conductive layer (704) and second metal catalyst layer simultaneously is done with Argon (Ar) plasma or in a wet chemical solution. The said backside masking material is selected from a group consisting and not limited to polymers, silicon, chrome (Cr), molybdenum (Mo), gold (Au) and silver (Ag). The said substrate is done using hydrofluoric acid (HF) or combination with inductively couple plasma reactive ion etching (ICP-RIE) method with octafluorocyclobutane (C_4F_8) plasma. The said growing of nanostructures at the said resistor region is done using a method selected from the group consisting of chemical vapour deposition (CVD), metalorganic chemical vapour deposition (MOCVD), plasma enhanced chemical vapour deposition (PECVD), hot wire chemical vapour deposition (HWCVD), atomic layer deposition (ALD), electrochemical deposition, solution chemical deposition or combinations thereof.

This invention also relates to method of fabricating a sensor device comprising the steps of:

a) depositing and etching a first metal catalyst layer on a glass substrate;
b) depositing and etching a conductive layer on the said first metal catalyst layer;
c) depositing and etching a second metal catalyst layer on top of the said conductive layer;
d) depositing and etching a backside masking material to be used as a mask during glass etching;

e) etching the glass substrate from the bottom to form an opening beneath a resistor region, said resistor region located between the said contact pads; and

f) growing of nanostructures at the said resistor region from the exposed metal catalyst areas.

The metal catalysts are deposited by physical or chemical vapour deposition (PVD or CVD) and made from any or a combination of: gold (Au), cobalt (Co), iron (Fe), nickel (Ni), indium (In) and copper (Cu). The said conductive layer is deposited by PVD or CVD and made from any or a combination of: gold (Au), platinum (Pt), nickel (Ni), tungsten (W), cobalt (Co) and copper (Cu). The said etching of the said first metal catalyst layer, conductive layer and second metal catalyst layer simultaneously is done with Argon (Ar) plasma or in a wet chemical solution. The said backside masking material is selected from a group consisting and not limited to polymers, silicon, chrome (Cr), molybdenum (Mo), gold (Au) and silver (Ag). The said etching of the said substrate (40) is done using hydrofluoric acid (HF) or combination with inductively couple plasma reactive ion etching (ICP-RIE) method with octafluorocyclobutane (C_4F_8) plasma. The said growing of nanostructures at the said resistor region is done using a method selected from the group consisting of chemical vapour deposition (CVD), metalorganic chemical vapour deposition (MOCVD), plasma enhanced chemical vapour deposition (PECVD), hot wire chemical vapour deposition (HWCVD), atomic layer deposition (ALD), electrochemical deposition, solution chemical deposition or combinations thereof.

These and other objects of the present invention will become more readily apparent from the detailed description given hereinafter. However, it should be understood that the detailed description and specific examples, while indicating the preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.

BRIEF DESCRIPTION OF DRAWINGS

Figure 1 shows a view of a sensing device in an embodiment of this invention.

Figure 2a shows a plan view of an embodiment of this invention.

Figure 2b shows a plan view of an embodiment of this invention.

Figure 3 shows a process flow of an embodiment of this invention.

Figure 4 shows a process flow of an embodiment of this invention.

Figure 5a shows a cross sectional view of an embodiment of this invention.

Figure 5b shows a cross sectional view of an embodiment of this invention.

Figure 5 shows a cross sectional view of an embodiment of this invention.

Figure 6 (a) through (j) show stages in the fabrication process of an embodiment of this invention.

Figures 7 (a) through (h) show stages in the fabrication process of an embodiment of this invention.

Figures 8 (a) through (h) show stages in the fabrication process of an embodiment of this invention.

Figures 9 (a) through (f) show stages in the fabrication process of an embodiment of this invention.

DETAILED DESCRIPTION OF INVENTION

It should be noted that the following detailed description is directed to a sensing device that fully utilises its fringing field effect by incorporating a second sensing membrane on the opposite side of the interdigitated electrode to the side with the first sensing membrane and the fabrication method thereof and is not limited to any particular size or configuration but in fact a multitude of sizes and configurations within the general scope of the following description.

Referring to Figure 1, there is shown a sensor device based on a change in electrical resistance comprising: a resistor structure (10) having two ends; a plurality of nanostructures (20) attached to at least a portion of said resistor structure (10); a pair of contact pads (50, 52), each contact pad located at each said end of the resistor structure (10); a substrate (40) supporting each said end of the resistor structure (10); and an insulating layer (30, 32) sandwiched between said substrate (40) and each said end of the resistor structure (10).

Referring to Figure 2a, there is shown that a resistor region of the said resistor structure (10) between each said contact pad (50, 52) comprising a long wire shaped in a serpentine fashion (12) to cover a larger area.

Figure 2b shows another embodiment whereby a resistor region of the said resistor structure (10) between each said contact pad (50, 52) comprises or a plurality of wires (14) running parallel to each other.

In operation, an electrical current is maintained along the said resistor structure (10) and the said nanostructures (20) upon detecting receptive ions, changes the resistance of the said resistor structure, said change in resistance measurable by an external measuring means. The nanostructures (20) are either nanotubes or nanowires selected from a group consisting and not limited to carbon nanotubes,

silicon nanowires, tungsten nanowires, tungsten oxide nanowires, zinc oxide nanowires, indium oxide nanowires, tin oxide nanowires, gold nanowires or a combination thereof. The nanostructures may be either uni-directional or multi-directional.

Figure 3 shows a process flow of a multiple deposition and single etching step in an embodiment of this invention.

Figure 4 shows a process flow of a multiple deposition and multiple etching step in an embodiment of this invention.

Figures 5 (a) shows a cross sectional view of a first embodiment of this invention where the nanostructures (20) are ordered in a vertical uni-directional array (201).

Figures 5 (b) shows a cross sectional view of a first embodiment of this invention where the nanostructures (20) are ordered in a vertical uni-directional array (202).

Figures 5 (c) shows a cross sectional view of a first embodiment of this invention where the nanostructures (20) are ordered in a vertical uni-directional array (203).

Figure 6 shows a process flow in a fabrication process using a silicon substrate and a multiple deposition and single etching step comprising the steps of:

a) depositing insulating layers onto a front (700) and a back (701) side of a silicon substrate (40), the insulating layers (700, 701) are any or a combination of: silicon dioxide or silicon nitride deposited by physical or chemical vapour deposition; or silicon dioxide grown by a thermal oxidation method;
b) etching the said back side insulating layer (701) done using either Tetrafluoromethane (CF_4) and Trifluoromethane (CHF_3) plasma or in a hydrofluoric acid (HF) based chemical solution;
c) depositing a first metal catalyst layer (703) on the said front side insulating layer (700) by physical or chemical vapour deposition (PVD or CVD) and

made from any or a combination of: gold (Au), cobalt (Co), iron (Fe), nickel (Ni), indium (In) and copper (Cu);

d) depositing a conductive layer (704) on the said first metal catalyst layer (703) by PVD or CVD and made from any or a combination of: gold (Au), platinum (Pt), nickel (Ni), tungsten (W), cobalt (Co) and copper (Cu);

e) depositing a second metal catalyst layer (705) on top of the said conductive layer (704) by physical or chemical vapour deposition (PVD or CVD) and made from any or a combination of: gold (Au), cobalt (Co), iron (Fe), nickel (Ni), indium (In) and copper (Cu);

f) etching the said first metal catalyst layer (703), conductive layer (704) and second metal catalyst layer (705) simultaneously to form resistor and contact pad areas (50, 52) with Argon (Ar) plasma or in a wet chemical solution using an inductively coupled plasma reactive ion etching (ICP-RIE) method with sulphur hexafluoride (SF_6) based plasma, or with a wet chemical etchant of potassium hydroxide (KOH) or Tetramethylammonium Hydroxide (TMAH);

g) removing the said second metal catalyst layer (705) from the said contact pad areas (50, 52) using buffered hydrofluoric acid (HF);

h) etching the said silicon substrate (40) from the bottom to form an opening beneath the said front side insulating layer (700);

i) removing the said front side insulating layer (700) from a resistor region, said resistor region located between the said contact pads (50, 52); and

j) growing of nanostructures at the said resistor region from the exposed metal catalyst (703, 705) areas using a method selected from the group consisting of chemical vapour deposition (CVD), metalorganic chemical vapour deposition (MOCVD), plasma enhanced chemical vapour deposition (PECVD), hot wire chemical vapour deposition (HWCVD), atomic layer deposition (ALD), electrochemical deposition, solution chemical deposition or combinations thereof.

Figure 7 shows a process flow in a fabrication process using a silicon substrate and a multiple deposition and multiple etching step comprising the steps of:

a) depositing insulating layers onto a front (700) and a back (701) side of a silicon substrate (40);
b) etching the said back side insulating layer (701);
c) depositing and etching a first metal catalyst layer (703) on the said front side insulating layer (700);
d) depositing and etching a conductive layer (704) on the said first metal catalyst layer (703);
e) depositing and etching a second metal catalyst layer (705) on top of the said conductive layer (704);
f) etching the said silicon substrate (40) from the bottom to form an opening beneath the said front side insulating layer (700);
g) removing the said front side insulating layer (700) from a resistor region, said resistor region located between the said contact pads (50, 52); and
h) growing of nanostructures at the said resistor region from the exposed metal catalyst (703, 705) areas.

Figure 8 shows a process flow in a fabrication process using a glass substrate and a multiple deposition and single etching step comprising the steps of:

a) depositing a first metal catalyst layer (703) on a substrate (40);
b) depositing a conductive layer (704) on the said first metal catalyst layer (703);
c) depositing a second metal catalyst layer (705) on top of the said conductive layer (704);
d) etching the said first metal catalyst layer (703), conductive layer (704) and second metal catalyst layer (705) simultaneously to form resistor and contact pad areas (50, 52);
e) removing the said second metal catalyst layer (705) from the said contact pad areas (50, 52);
f) depositing and etching a backside masking material (706) to be use as a mask during glass etching;

g) etching the said substrate (40) from the bottom to form an opening beneath a resistor region, said resistor region located between the said contact pads (50, 52);

h) growing of nanostructures at the said resistor region from the exposed metal catalyst (703, 705) areas.

The metal catalysts (703, 705) are deposited by physical or chemical vapour deposition (PVD or CVD) and made from any or a combination of: gold (Au), cobalt (Co), iron (Fe), nickel (Ni), indium (In) and copper (Cu). The conductive layer (704) is deposited by PVD or CVD and made from any or a combination of: gold (Au), platinum (Pt), nickel (Ni), tungsten (W), cobalt (Co) and copper (Cu). The said etching of the said first metal catalyst layer (703), conductive layer (704) and second metal catalyst layer (705) simultaneously is done with Argon (Ar) plasma or in a wet chemical solution. The said backside masking material (706) is selected from a group consisting and not limited to polymers, silicon, chrome (Cr), molybdenum (Mo), gold (Au) and silver (Ag). The said substrate (40) is done using hydrofluoric acid (HF) or combination with inductively couple plasma reactive ion etching (ICP-RIE) method with octafluorocyclobutane (C_4F_8) plasma. The said growing of nanostructures at the said resistor region is done using a method selected from the group consisting of chemical vapour deposition (CVD), metalorganic chemical vapour deposition (MOCVD), plasma enhanced chemical vapour deposition (PECVD), hot wire chemical vapour deposition (HWCVD), atomic layer deposition (ALD), electrochemical deposition, solution chemical deposition or combinations thereof.

Figure 9 shows a process flow in a fabrication process using a glass substrate and a multiple deposition and multiple etching step comprising the steps of:

a) depositing and etching a first metal catalyst layer (703) on a glass substrate (40);

b) depositing and etching a conductive layer (704) on the said first metal catalyst layer (703);

c) depositing and etching a second metal catalyst layer (705) on top of the said conductive layer (704);

d) depositing and etching a backside masking material (706) to be used as a mask during glass etching;

e) etching the glass substrate (40) from the bottom to form an opening beneath a resistor region, said resistor region located between the said contact pads (50, 52); and

f) growing of nanostructures at the said resistor region from the exposed metal catalyst (703, 705) areas.

The metal catalysts (703, 705) are deposited by physical or chemical vapour deposition (PVD or CVD) and made from any or a combination of: gold (Au), cobalt (Co), iron (Fe), nickel (Ni), indium (In) and copper (Cu). The said conductive layer (704) is deposited by PVD or CVD and made from any or a combination of: gold (Au), platinum (Pt), nickel (Ni), tungsten (W), cobalt (Co) and copper (Cu). The said etching of the said first metal catalyst layer (703), conductive layer (704) and second metal catalyst layer (705) simultaneously is done with Argon (Ar) plasma or in a wet chemical solution. The said backside masking material (706) is selected from a group consisting and not limited to polymers, silicon, chrome (Cr), molybdenum (Mo), gold (Au) and silver (Ag). The said etching of the said substrate (40) is done using hydrofluoric acid (HF) or combination with inductively couple plasma reactive ion etching (ICP-RIE) method with octafluorocyclobutane (C_4F_8) plasma. The said growing of nanostructures at the said resistor region is done using a method selected from the group consisting of chemical vapour deposition (CVD), metalorganic chemical vapour deposition (MOCVD), plasma enhanced chemical vapour deposition (PECVD), hot wire chemical vapour deposition (HWCVD), atomic layer deposition (ALD), electrochemical deposition, solution chemical deposition or combinations thereof.

While several particularly preferred embodiments of the present invention have been described and illustrated, it should now be apparent to those skilled in the art that various changes and modifications can be made without departing from the

spirit and scope of the invention. Accordingly, the following claims are intended to embrace such changes, modifications, and areas of application that are within the spirit and scope of this invention.

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CLAIMS

1. A sensor device based on a change in electrical resistance comprising:
   a resistor structure (10) having two ends;
   a plurality of nanostructures (20) attached to at least a portion of said resistor structure (10);
   a pair of contact pads (50, 52), each contact pad located at each said end of the resistor structure (10);
   a substrate (40) supporting each said end of the resistor structure (10); and
   an insulating layer (30, 32) sandwiched between said substrate (40) and each said end of the resistor structure (10).

2. A sensor device based on a change in electrical resistance according to claim 1 wherein the said resistor structure (10) between each said contact pad (50, 52) comprises a long wire shaped in a serpentine fashion (12) to cover a larger area.

3. A sensor device based on a change in electrical resistance according to claim 1 wherein the said resistor structure (10) between each said contact pad (50, 52) comprises a plurality of wires running parallel to each other (14).

4. A sensor device based on a change in electrical resistance according to any of claims 1 to 3 wherein in operation, an electrical current is maintained along the said resistor structure (10) and the said nanostructures (20), upon detecting receptive ions, changes the resistance of the said resistor structure (10), said change in resistance measurable by an external measuring means.

5. A sensor device based on a change in electrical resistance according to any of claims 1 to 4 wherein the said nanostructures are either nanotubes or

nanowires selected from a group consisting and not limited to carbon nanotubes, silicon nanowires, tungsten nanowires, tungsten oxide nanowires, zinc oxide nanowires, indium oxide nanowires, tin oxide nanowires, gold nanowires or a combination thereof.

6. A sensor device based on a change in electrical resistance according to any of the preceding claims wherein the said nanostructures (20) may be either uni-directional (201) or multi-directional (202).

7. A method of fabricating a sensor device comprising the steps of:

a) depositing insulating layers onto a front (700) and a back (701) side of a substrate (40);

b) etching the said back side insulating layer (701);

c) depositing a first metal catalyst layer (703) on the said front side insulating layer (700);

d) depositing a conductive layer (704) on the said first metal catalyst layer (703);

e) depositing a second metal catalyst layer (705) on top of the said conductive layer (704);

f) etching the said first metal catalyst layer (703), conductive layer (704) and second metal catalyst layer (705) simultaneously to form resistor and contact pad areas (50, 52);

g) removing the said second metal catalyst layer (705) from the said contact pad areas (50, 52);

h) etching the said substrate (40) from the bottom to form an opening beneath the said front side insulating layer (700);

i) removing the said front side insulating layer (700) from a resistor region, said resistor region located between the said contact pads (50, 52); and

j) growing of nanostructures at the said resistor region from the exposed metal catalyst (703, 705) areas.

8. A method of fabricating a sensor device according to claim 7 wherein the said insulating layers (700, 701) are any or a combination of: silicon dioxide or silicon nitride deposited by physical or chemical vapour deposition; or silicon dioxide grown by a thermal oxidation method.

9. A method of fabricating a sensor device according to claim 7 or 8 wherein the said etching of the said back side insulating layer (701) is done using either Tetrafluoromethane (CF_4) and Trifluoromethane (CHF_3) plasma or in a hydrofluoric acid (HF) based chemical solution.

10. A method of fabricating a sensor device according to any of claims 7 to 9 wherein the said metal catalysts (703, 705) are deposited by physical or chemical vapour deposition (PVD or CVD) and made from any or a combination of: gold (Au), cobalt (Co), iron (Fe), nickel (Ni), indium (In) and copper (Cu).

11. A method of fabricating a sensor device according to any of claims 7 to 10 wherein the said conductive layer (704) is deposited by PVD or CVD and made from any or a combination of: gold (Au), platinum (Pt), nickel (Ni), tungsten (W), cobalt (Co) and copper (Cu).

12. A method of fabricating a sensor device according to any of claims 7 to 11 wherein the said etching of the said first metal catalyst layer (703), conductive layer (704) and second metal catalyst layer (705) simultaneously is done with Argon (Ar) plasma or in a wet chemical solution.

13. A method of fabricating a sensor device according to any of claims 7 to 12 wherein the said etching of the said substrate (40) is done using an inductively coupled plasma reactive ion etching (ICP-RIE) method with sulphur hexafluoride (SF_6) based plasma, or with a wet chemical etchant of potassium hydroxide (KOH) or Tetramethylammonium Hydroxide (TMAH).

14. A method of fabricating a sensor device according to any of claims 7 to 13 wherein the said removing the said front side insulating layer (700) from a resistor region is done using buffered hydrofluoric acid (HF).

15. A method of fabricating a sensor device according to any of claims 7 to 14 wherein the said growing of nanostructures at the said resistor region is done using a method selected from the group consisting of chemical vapour deposition (CVD), metalorganic chemical vapour deposition (MOCVD), plasma enhanced chemical vapour deposition (PECVD), hot wire chemical vapour deposition (HWCVD), atomic layer deposition (ALD), electrochemical deposition, solution chemical deposition or combinations thereof.

16. A method of fabricating a sensor device comprising the steps of:

a) depositing insulating layers onto a front (700) and a back (701) side of a substrate (40);

b) etching the said back side insulating layer (701);

c) depositing and etching a first metal catalyst layer (703) on the said front side insulating layer (700);

d) depositing and etching a conductive layer (704) on the said first metal catalyst layer (703);

e) depositing and etching a second metal catalyst layer (705) on top of the said conductive layer (704);

f) etching the said substrate (40) from the bottom to form an opening beneath the said front side insulating layer (700);

g) removing the said front side insulating layer (700) from a resistor region, said resistor region located between the said contact pads (50, 52); and

h) growing of nanostructures at the said resistor region from the exposed metal catalyst (703, 705) areas.

17. A method of fabricating a sensor device according to claim 16 wherein the said insulating layers (700, 701) are any or a combination of: silicon dioxide or silicon nitride deposited by physical or chemical vapour deposition; or silicon dioxide grown by a thermal oxidation method.

18. A method of fabricating a sensor device according to claim 16 or 17 wherein the said etching of the said back side insulating layer (701) is done using either Tetrafluoromethane (CF_4) and Trifluoromethane (CHF_3) plasma or in a hydrofluoric acid (HF) based chemical solution.

19. A method of fabricating a sensor device according to any of claims 16 to 18 wherein the said metal catalysts (703, 705) are deposited by physical or chemical vapour deposition (PVD or CVD) and made from any or a combination of: gold (Au), cobalt (Co), iron (Fe), nickel (Ni), indium (In) and copper (Cu).

20. A method of fabricating a sensor device according to any of claims 16 to 19 wherein the said conductive layer (704) is deposited by PVD or CVD and made from any or a combination of: gold (Au), platinum (Pt), nickel (Ni), tungsten (W), cobalt (Co) and copper (Cu).

21. A method of fabricating a sensor device according to any of claims 16 to 20 wherein the said etching of the said first metal catalyst layer (703), conductive layer (704) and second metal catalyst layer (705) simultaneously is done with Argon (Ar) plasma or in a wet chemical solution.

22. A method of fabricating a sensor device according to any of claims 16 to 21 wherein the said etching of the said substrate (40) is done using an inductively coupled plasma reactive ion etching (ICP-RIE) method with sulphur hexafluoride (SF_6) based plasma, or with a wet chemical etchant of potassium hydroxide (KOH) or Tetramethylammonium Hydroxide (TMAH).

23. A method of fabricating a sensor device according to any of claims 16 to 22 wherein the said removing the said front side insulating layer (700) from a resistor region is done using buffered hydrofluoric acid (HF).

24. A method of fabricating a sensor device according to any of claims 16 to 23 wherein the said growing of nanostructures at the said resistor region is done using a method selected from the group consisting of chemical vapour deposition (CVD), metalorganic chemical vapour deposition (MOCVD), plasma enhanced chemical vapour deposition (PECVD), hot wire chemical vapour deposition (HWCVD), atomic layer deposition (ALD), electrochemical deposition, solution chemical deposition or combinations thereof.

25. A method of fabricating a sensor device according to any of claims 7 to 23 wherein the said substrate is silicon.

26. A method of fabricating a sensor device comprising the steps of:

a) depositing a first metal catalyst layer (703) on a substrate (40);
b) depositing a conductive layer (704) on the said first metal catalyst layer (703);
c) depositing a second metal catalyst layer (705) on top of the said conductive layer (704);
d) etching the said first metal catalyst layer (703), conductive layer (704) and second metal catalyst layer (705) simultaneously to form resistor and contact pad areas (50, 52);
e) removing the said second metal catalyst layer (705) from the said contact pad areas (50, 52);
f) depositing and etching a backside masking material (706) to be use as a mask during glass etching
g) etching the said substrate (40) from the bottom to form an opening beneath a resistor region, said resistor region located between the said contact pads (50, 52);

h) growing of nanostructures at the said resistor region from the exposed metal catalyst (703, 705) areas.

27. A method of fabricating a sensor device according to claim 26 wherein the said metal catalysts (703, 705) are deposited by physical or chemical vapour deposition (PVD or CVD) and made from any or a combination of: gold (Au), cobalt (Co), iron (Fe), nickel (Ni), indium (In) and copper (Cu).

28. A method of fabricating a sensor device according to any of claims 26 to 27 wherein the said conductive layer (704) is deposited by PVD or CVD and made from any or a combination of: gold (Au), platinum (Pt), nickel (Ni), tungsten (W), cobalt (Co) and copper (Cu).

29. A method of fabricating a sensor device according to any of claims 26 to 28 wherein the said etching of the said first metal catalyst layer (703), conductive layer (704) and second metal catalyst layer (705) simultaneously is done with Argon (Ar) plasma or in a wet chemical solution.

30. A method of fabricating a sensor device according to any of claims 26 to 29 wherein the said backside masking material (706) is selected from a group consisting and not limited to polymers, silicon, chrome (Cr), molybdenum (Mo), gold (Au) and silver (Ag).

31. A method of fabricating a sensor device according to any of claims 26 to 30 wherein the said etching of the said substrate (40) is done using hydrofluoric acid (HF) or combination with inductively couple plasma reactive ion etching (ICP-RIE) method with octafluorocyclobutane (C_4F_8) plasma.

32. A method of fabricating a sensor device according to any of claims 26 to 31 wherein the said growing of nanostructures at the said resistor region is done using a method selected from the group consisting of chemical vapour

deposition (CVD), metalorganic chemical vapour deposition (MOCVD), plasma enhanced chemical vapour deposition (PECVD), hot wire chemical vapour deposition (HWCVD), atomic layer deposition (ALD), electrochemical deposition, solution chemical deposition or combinations thereof.

33. A method of fabricating a sensor device comprising the steps of:
    a) depositing and etching a first metal catalyst layer (703) on a substrate (40);
    b) depositing and etching a conductive layer (704) on the said first metal catalyst layer (703);
    c) depositing and etching a second metal catalyst layer (705) on top of the said conductive layer (704);
    d) depositing and etching a backside masking material (706) to be used as a mask during glass etching;
    e) etching the said substrate (40) from the bottom to form an opening beneath a resistor region, said resistor region located between the said contact pads (50, 52);
    f) growing of nanostructures at the said resistor region from the exposed metal catalyst (703, 705) areas.

34. A method of fabricating a sensor device according to claim 33 wherein the said metal catalysts (703, 705) are deposited by physical or chemical vapour deposition (PVD or CVD) and made from any or a combination of: gold (Au), cobalt (Co), iron (Fe), nickel (Ni), indium (In) and copper (Cu).

35. A method of fabricating a sensor device according to any of claims 33 to 34 wherein the said conductive layer (704) is deposited by PVD or CVD and made from any or a combination of: gold (Au), platinum (Pt), nickel (Ni), tungsten (W), cobalt (Co) and copper (Cu).

36. A method of fabricating a sensor device according to any of claims 33 to 35 wherein the said etching of the said first metal catalyst layer (703), conductive layer (704) and second metal catalyst layer (705) simultaneously is done with Argon (Ar) plasma or in a wet chemical solution.

37. A method of fabricating a sensor device according to any of claims 33 to 36 wherein the said backside masking material (706) is selected from a group consisting and not limited to polymers, silicon, chrome (Cr), molybdenum (Mo), gold (Au) and silver (Ag).

38. A method of fabricating a sensor device according to any of claims 33 to 37 wherein the said etching of the said substrate (40) is done using hydrofluoric acid (HF) or combination with inductively couple plasma reactive ion etching (ICP-RIE) method with octafluorocyclobutane (C_4F_8) plasma.

39. A method of fabricating a sensor device according to any of claims 33 to 38 wherein the said growing of nanostructures at the said resistor region is done using a method selected from the group consisting of chemical vapour deposition (CVD), metalorganic chemical vapour deposition (MOCVD), plasma enhanced chemical vapour deposition (PECVD), hot wire chemical vapour deposition (HWCVD), atomic layer deposition (ALD), electrochemical deposition, solution chemical deposition or combinations thereof.

40. A method of fabricating a sensor device according to any of claims 26 to 39 wherein the said substrate is glass.

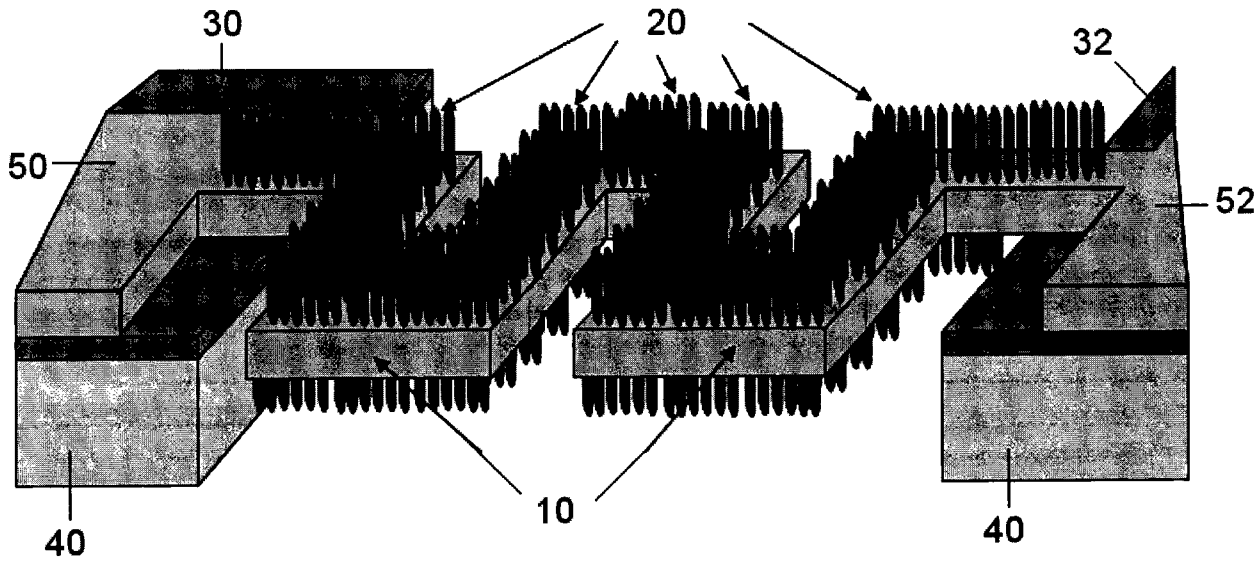

Figure 1

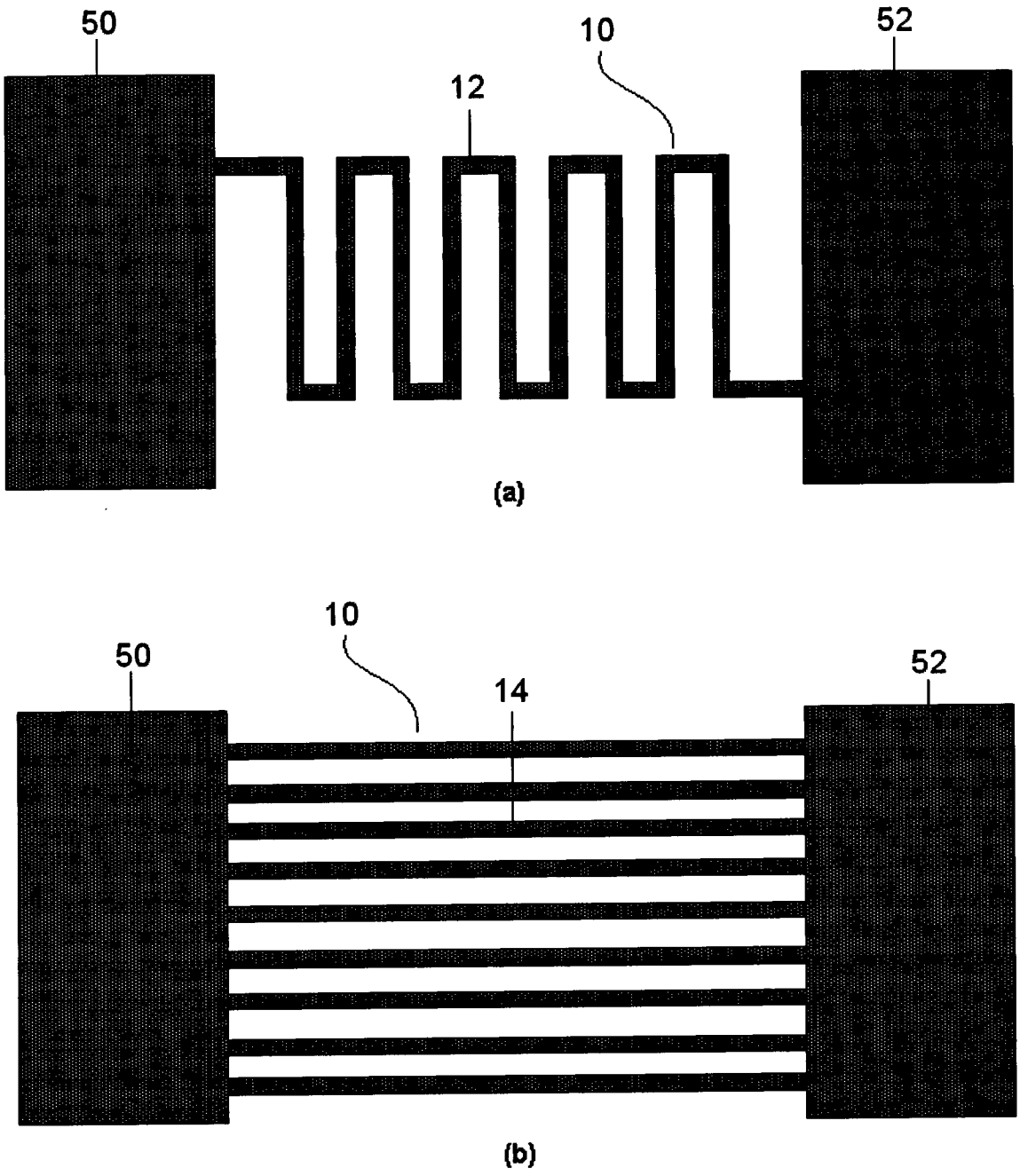

Figure 2

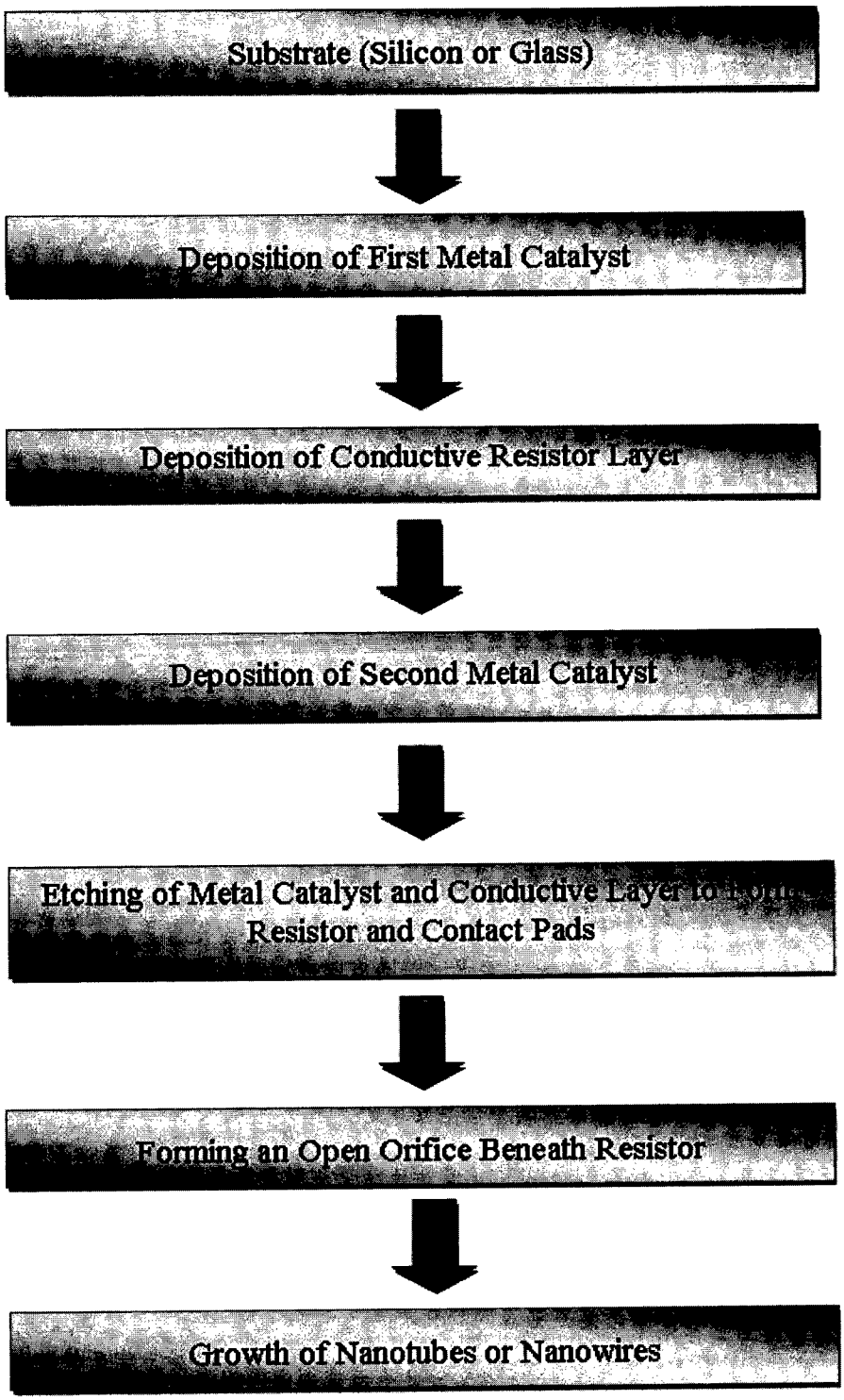
Substrate (Silicon or Glass)
Deposition of First Metal Catalyst
Deposition of Conductive Resistor Layer
Deposition of Second Metal Catalyst
Etching of Metal Catalyst and Conductive Layer to Form Resistor and Contact Pads
Forming an Open Orifice Beneath Resistor
Growth of Nanotubes or Nanowires

Figure 3

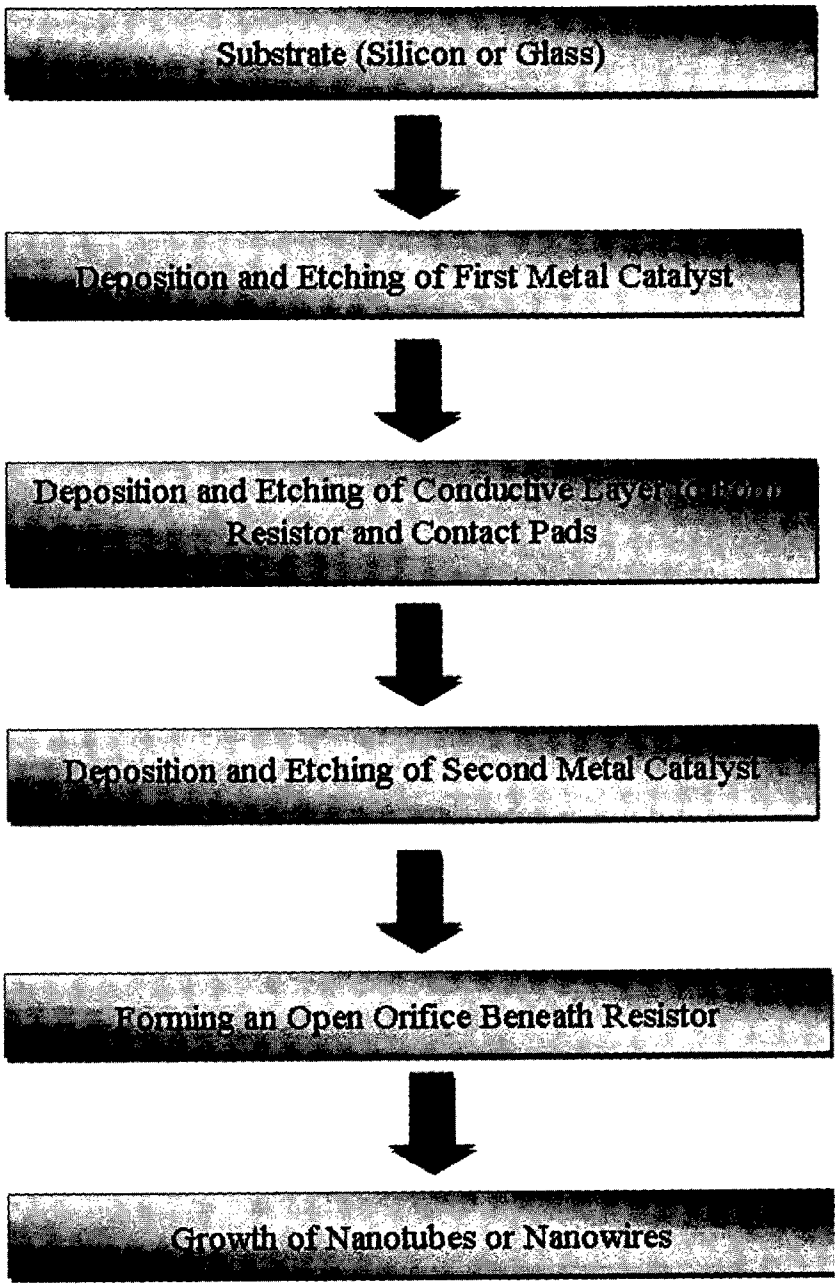
Substrate (Silicon or Glass)
Deposition and Etching of First Metal Catalyst
Deposition and Etching of Conductive Layer
Resistor and Contact Pads
Deposition and Etching of Second Metal Catalyst
Forming an Open Orifice Beneath Resistor
Growth of Nanotubes or Nanowires

Figure 4

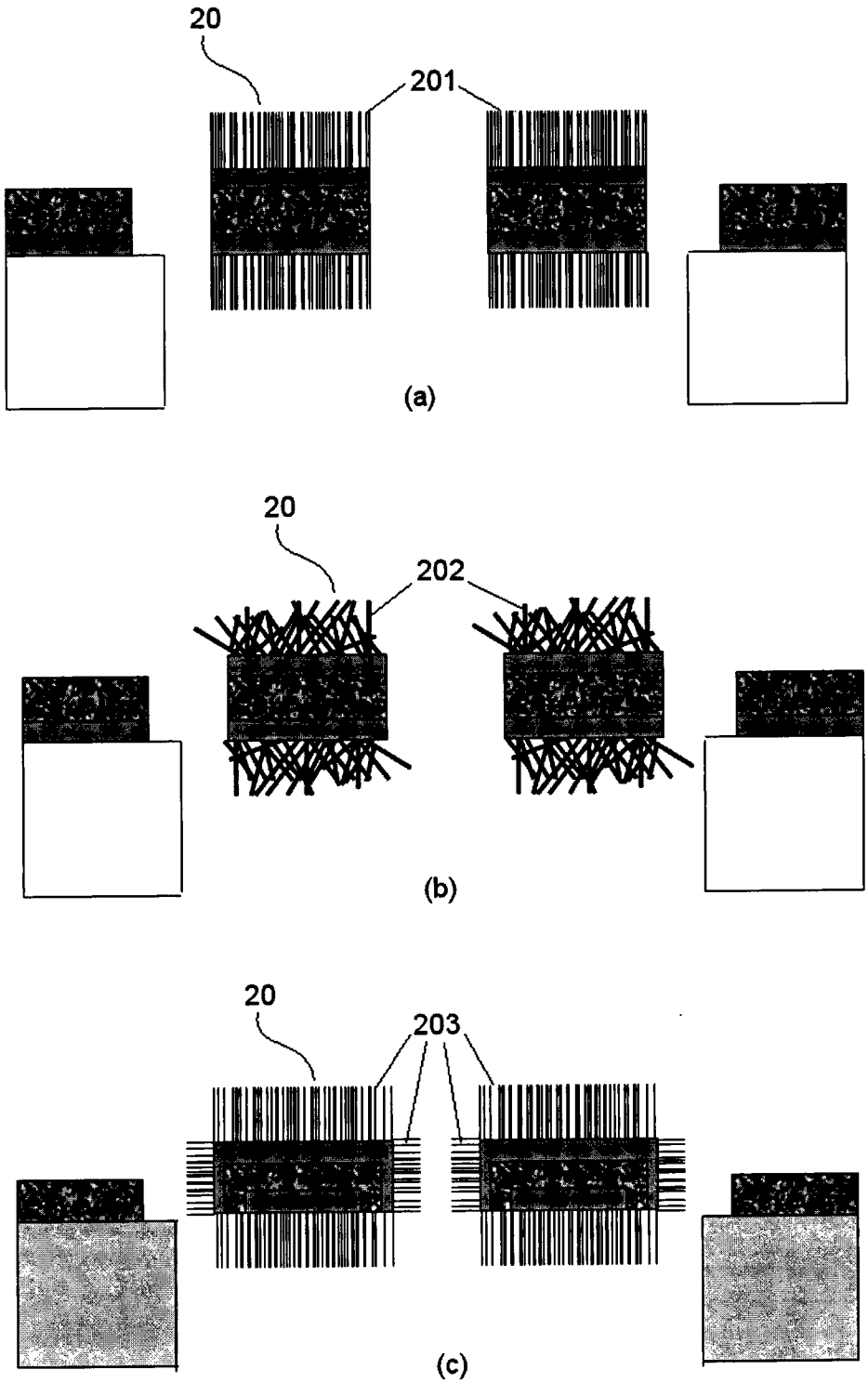

Figure 5

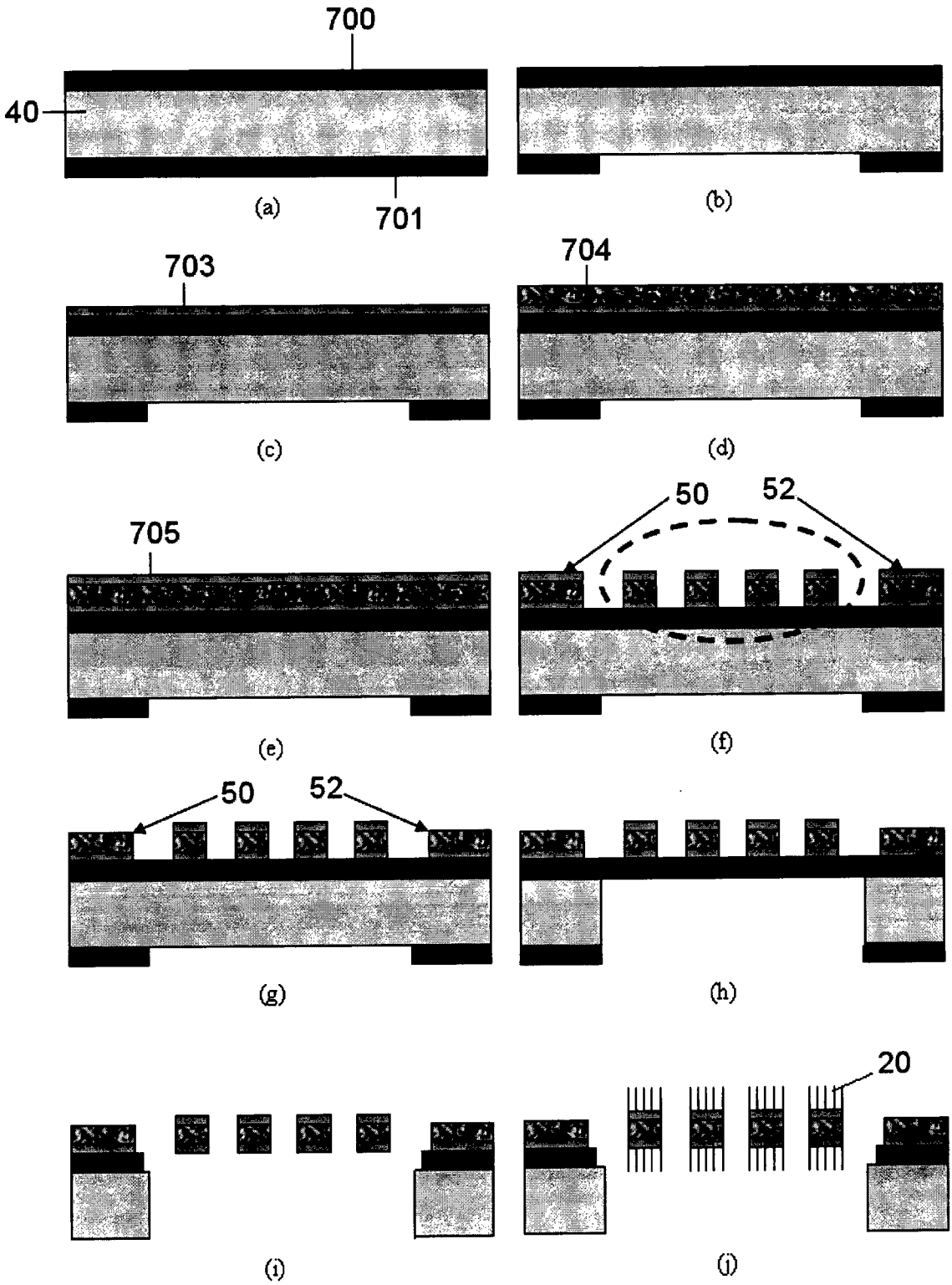

Figure 6

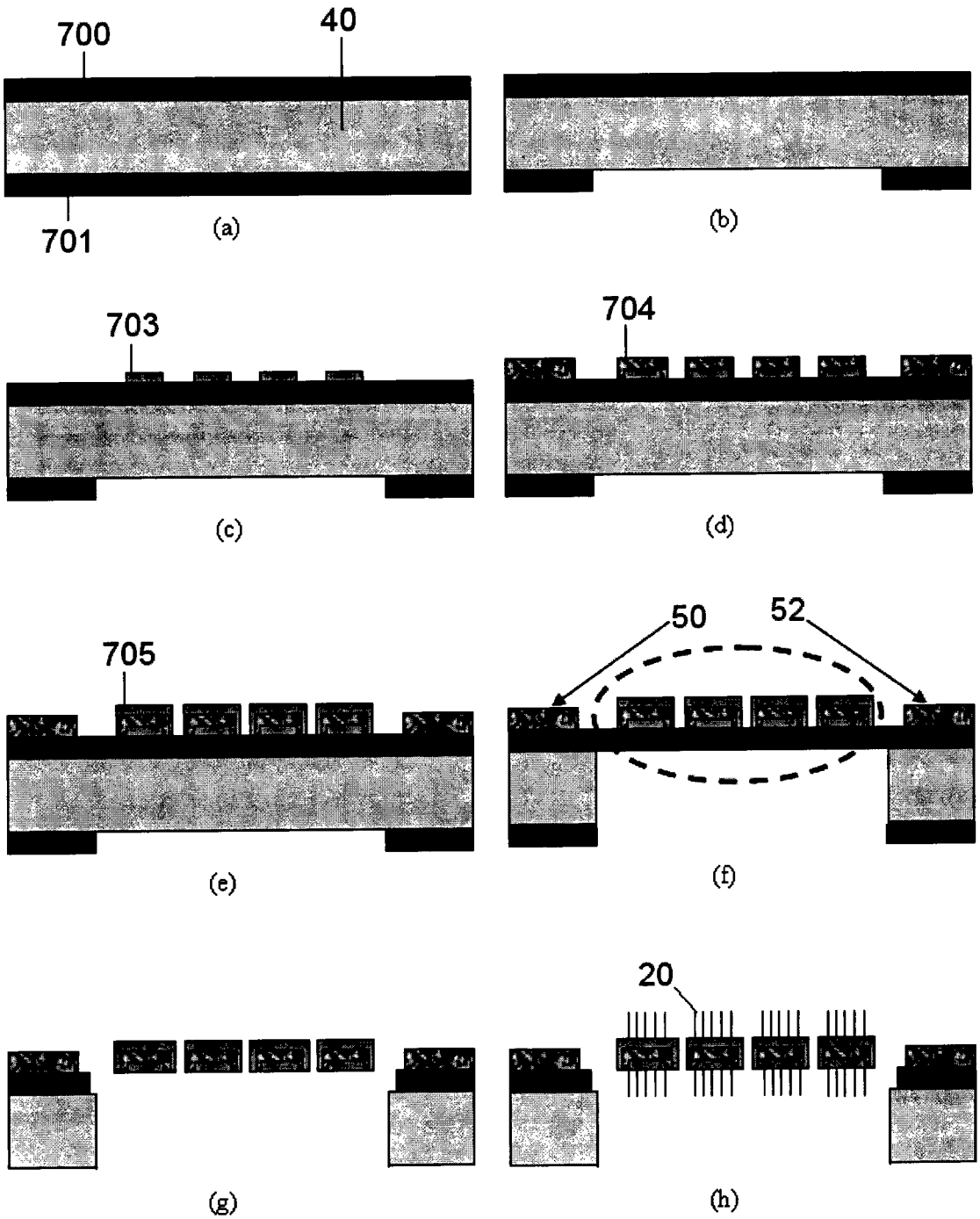

Figure 7

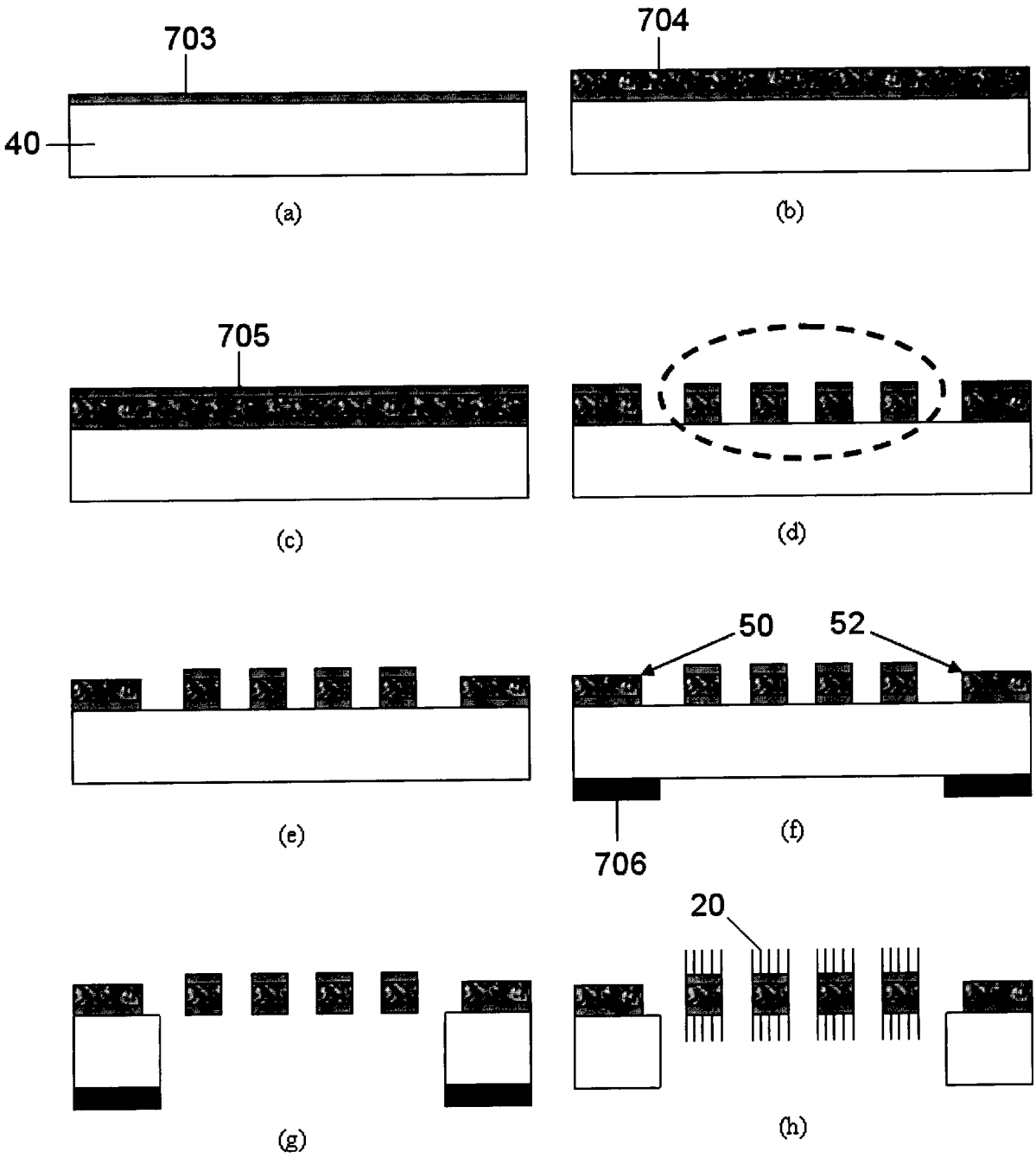

Figure 8

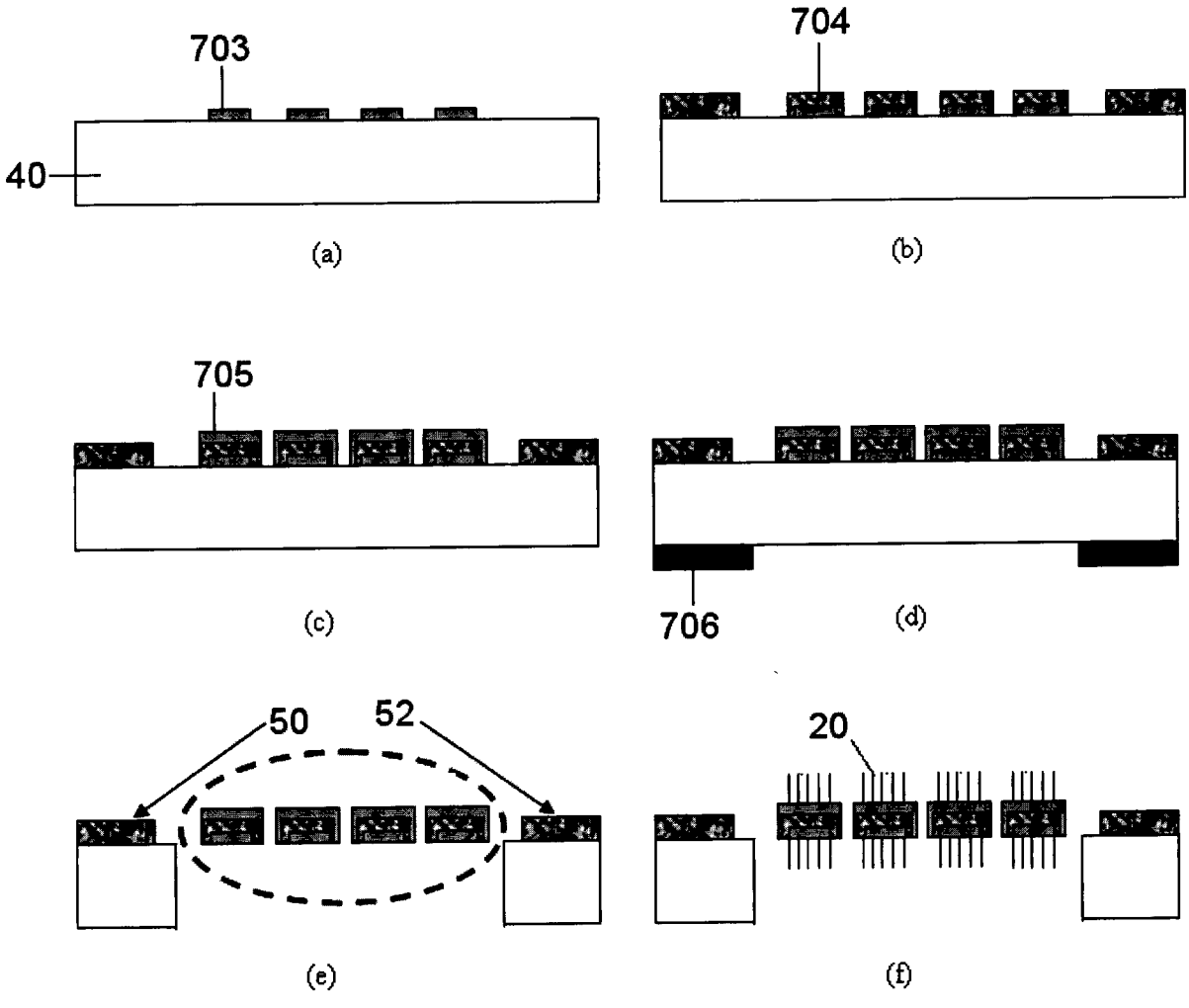

Figure 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/MY2011/000151

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl.

G01N 27/04 (2006.01) ***G01R 27/22*** (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
WPI, EPODOC: G01R 27/22, G01N27/04, resistor, cavity, contact pad, nano, tube, impedance, change, sensor, bridge, ion, field effect, plurality and similar terms

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2007/0062812 A1 (WEBER et al) 22 March 2007 See paras 29, 34, 40 , fig 2.	
A	US 2009/0151429 A1 (JUN et al) 18 June 2009 See fig 9, paras 111-116, 124, 132, 133.	
A	US 2010/0133528 A1 (MOON et al) 3 June 2010 See figs 2,3, paras 45,46,49,51,52.	

☐ Further documents are listed in the continuation of Box C ☒ See patent family annex

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
05 October 2011	19 OCTOBER 2011
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. +61 2 6283 7999	Authorized officer **SUSAN PRING** AUSTRALIAN PATENT OFFICE (ISO 9001 Quality Certified Service) Telephone No : +61 2 6283 2210

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/MY2011/000151

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
US	2007062812	DE	10347414	DE	10347415	DE	10347416
		EP	1649270	EP	1649271	GB	2407215
		IT	MI20041921	JP	2006528766	JP	2006528767
		KR	20060055524	KR	20060055525	US	2007234801
		US	7453254	US	2005122253	WO	2005012892
		WO	2005012893				
US	2009151429	KR	20090064693	US	7861575		
US	2010133528	JP	2010133926	KR	20100063608	US	7816681

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.

END OF ANNEX