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J. M. BERGEY ETAL
UNIVERSAL INTERVALOMETER

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2 Sheets-Sheet 1

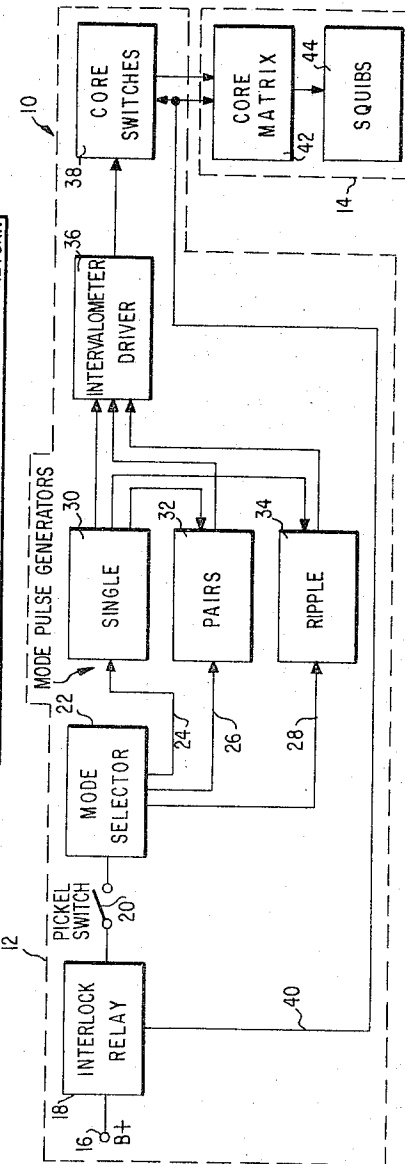
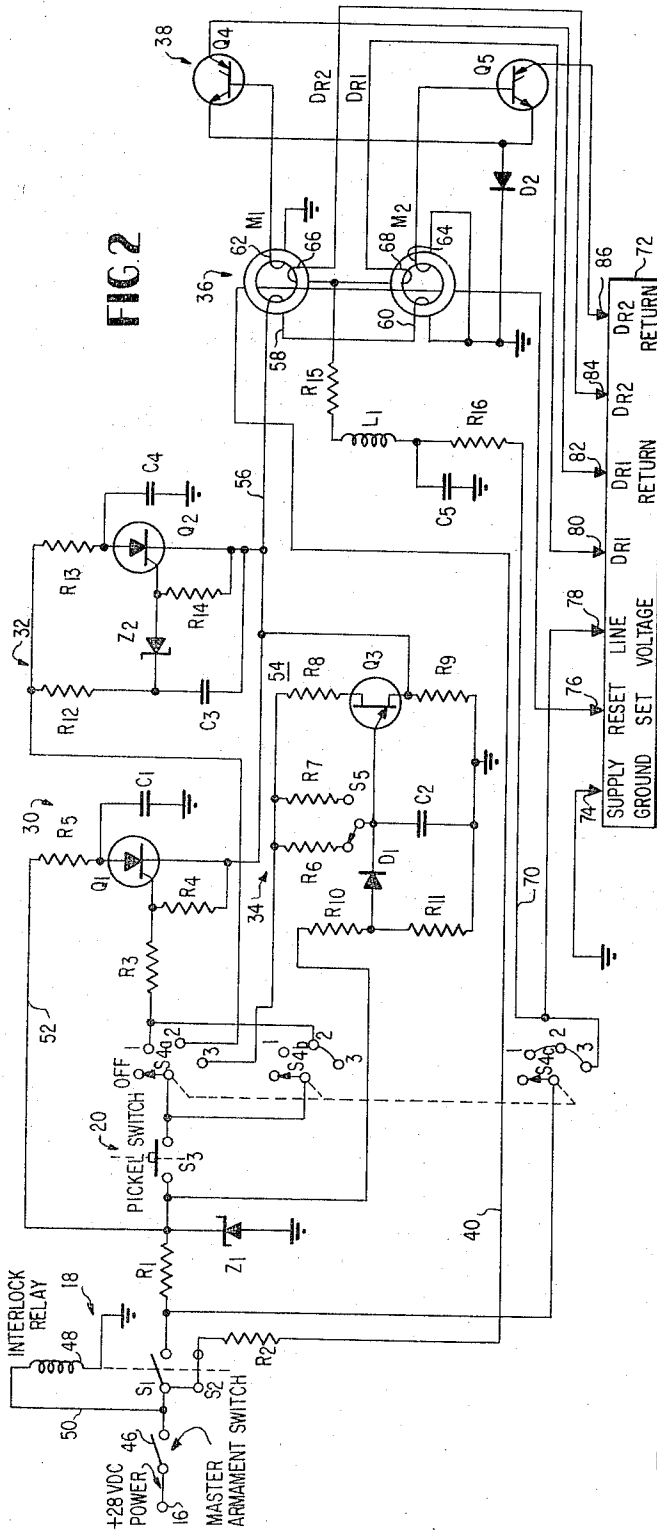


FIG. 1

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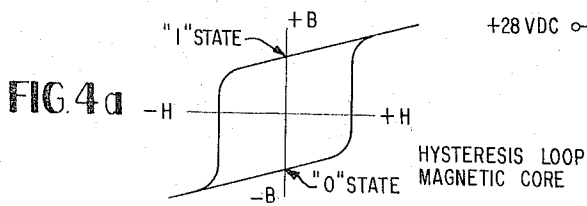
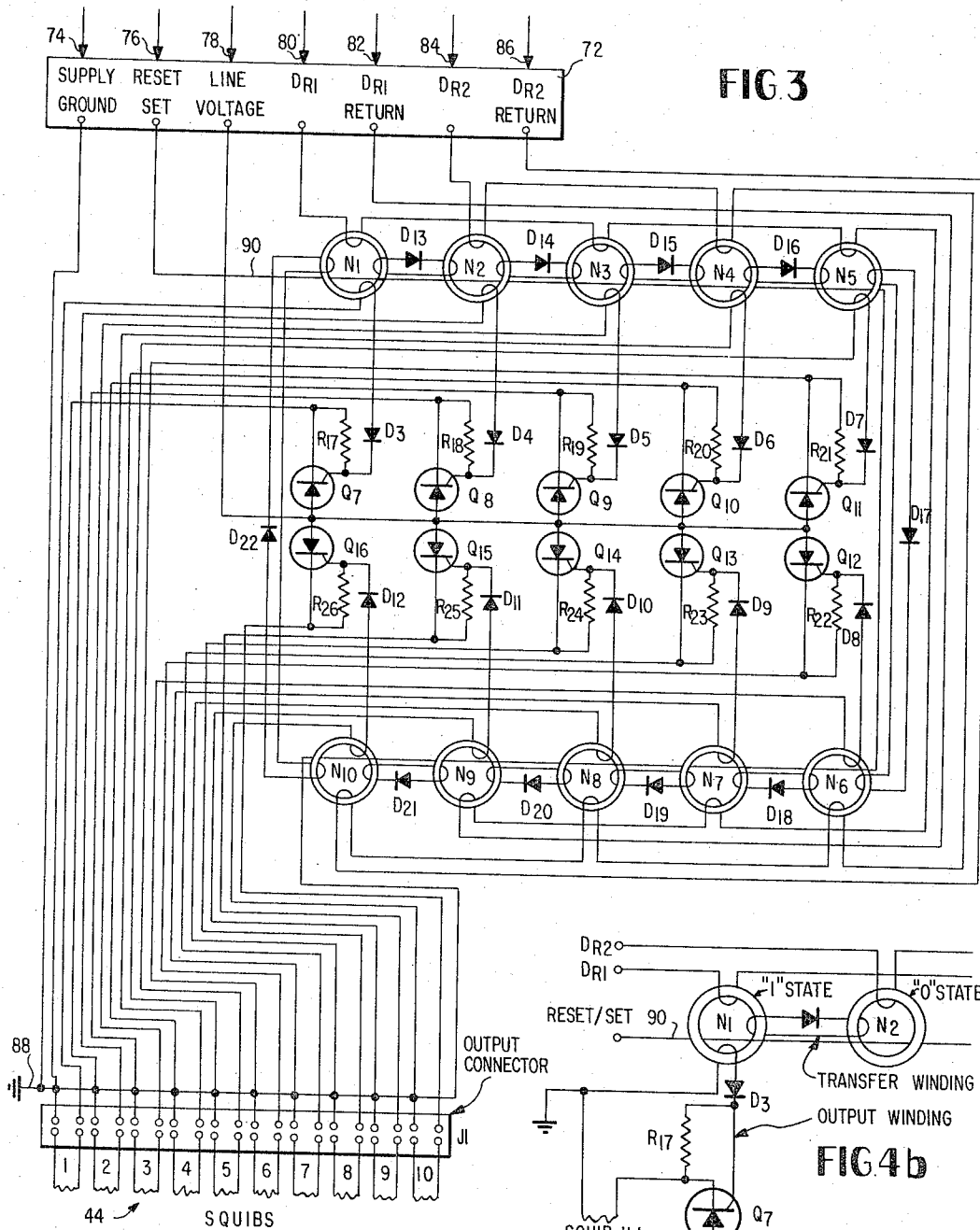
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UNIVERSAL INTERVALOMETER

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This invention relates to a novel electronic intervalometer and more specifically to a novel aircraft weapons system incorporating the intervalometer and particularly suited for multiple rocket firing.

The advent of multiple rocket firing requirements along with complex tactical situations brought forth the first intervalometers. Used in air-to-air weapons systems, the initial intervalometers were relatively simple mechanical or electro-mechanical stepping switches which responded to the pilot's command.

As aircraft speeds increased and weapons became more sophisticated, the armament delivery techniques required updating. Mechanical gadgetry provided part of the answer but the additional complexity introduced a glaring shortcoming—reliability. Pilots returning from firing missions repeatedly complained of the number of malfunctions encountered. The intervalometer was too often the cause.

The present invention provides a novel device for correcting many of the deficiencies inherent in existing intervalometers and particularly provides a device having increased reliability. The system of the present invention is a unique combination of solid state electronic components arranged to give optimum performance while operating in the rigorous aircraft environment. The lack of moving parts within the intervalometer adds factors of increased reliability without sacrificing the ruggedness required of air-to-air and air-to-ground weapons systems. The unit of the present invention is of relatively light weight and may be packaged in a small volume so as to satisfy the weight and volume load restrictions in present day aircraft. It is readily adapted to existing weapons systems and exhibits substantially increased versatility in providing the pilot with three possible firing modes, namely single, pairs and ripple firing.

It is therefore one object of the present invention to provide a novel intervalometer.

Another object of the present invention is to provide a novel weapons firing system.

Another object of the present invention is to provide an intervalometer and weapons system having only solid state electronic components.

Another object of the present invention is to provide a weapons system having increased versatility and reliability.

Another object of the present invention is to provide an intervalometer and weapons system having reduced size and weight for use in aircraft.

Another object of the present invention is to provide a weapons system having increased firing interval accuracy.

These and further objects and advantages of the invention will be more apparent upon reference to the following specification, claims and appended drawings, wherein FIGURE 1 is a block diagram of the overall weapons system of the present invention.

FIGURE 2 is a detailed circuit diagram of the aircraft cockpit portion or master mode selector of FIGURE 1.

FIGURE 3 is a detailed circuit diagram of the basic intervalometer portion of the circuit of FIGURE 1.

FIGURE 4a is typical hysteresis loop for the magnetic core devices used in the present invention, and

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FIGURE 4b illustrates the operation of the intervalometer cores.

Referring to the drawings and particularly to FIGURE 1, the overall weapons system of the present invention, generally indicated at 10, comprises a master mode selector enclosed in the dashed box 12, electrically connected to a basic intervalometer enclosed in the dashed box 14. The master mode selector portion of the weapons system is located in the aircraft cockpit. It is an integral part of the aircraft weapons system and is constructed to fit into existing armament systems with little or no change. The basic intervalometer 14 is located in the non-expendable rocket launcher or pylon normally underslung on the wing of the tactical aircraft. It receives appropriate inputs from the mode selector 12 in pulse form and through magnetic core logic circuitry converts these inputs to useable squib firing signals. Any aircraft requires only one mode selector 12 but may accommodate as many basic intervalometers 14 as required for its mission. However, for the sake of simplicity only a single basic intervalometer is shown and discussed.

As shown in FIGURE 1, the mode selector 12 includes a power supply terminal 16 feeding in interlock relay 18. The terminal 16 may be connected to the plus 28 volt D.C. power supply conventionally available in the aircraft. The output of interlock relay 18 is connected to a trigger or pickel switch 20 and to a mode selector 22. Mode selector 22 is coupled by way of leads 24, 26 and 28 to the three mode pulse generators comprising a single mode generator 30, pairs generator 32 and ripple mode generator 34. These are, in turn, coupled to an intervalometer drive 36 feeding the core switches 38. Interlock relay 18 is also connected by way of lead 40 to the core switches 38 and to the core matrix 42 forming a part of the basic intervalometer 14. The output of the core matrix fires the squibs illustrated at 44.

FIGURE 2 is a detailed circuit diagram of the master mode selector 12. Power supply terminal 16 is coupled to the interlock relay 18 through a master armament switch 46 which is manually operated. Coil 48 of interlock relay 18 as indicated by the dash line in FIGURE 2 actuates a normally open switch S_1 and a normally closed switch S_2 . Coil 48 has one side connected to ground and the other side is connected by way of lead 50 to the master armament switch and hence to the power supply terminal 16.

Output from the interlock relay is through input resistor R_1 and a zener diode Z_1 to the pickel switch 20 labeled S_3 . Zener diode Z_1 acts as a voltage regulator.

Pickel switch 20 is connected by way of manual switch S_{4a} to a single pulse mode generator 30 including a silicon controlled rectifier Q_1 . This connection is by way of terminal 1 of switch S_{4a} through resistor R_3 to the gate of SCR Q_1 . The anode of Q_1 is connected to ground by way of capacitor C_1 . Current limiting resistor R_5 also connects the anode of Q_1 by way of lead 52 to zener diode Z_1 .

Ganged with manual switch S_{4a} are additional switches S_{4b} and S_{4c} . In addition to the "off" position each section of manual switch S_4 is provided with positions labeled "1," "2" and "3" representing single mode firing, pairs mode firing, and ripple mode firing, respectively. The position of switch S_4 is manually selected by the pilot in accordance with the desired firing mode.

Terminal 2 of switch S_{4a} is connected to the pairs mode generator 32 which includes in conjunction with Q_1 a second silicon controlled rectifier Q_2 . Q_2 is similarly provided with an anode capacitor C_4 while its gate is connected to a zener diode Z_2 and to a further capacitor C_3 .

Terminal 3 of switch S_{4a} connects the pickel switch 20 to a ripple mode generator 34 which includes a unijunc-

tion relaxation oscillator generally indicated at 54. Oscillator 54 includes a unijunction transistor Q_3 and an emitter capacitor C_2 , a rectifier diode D_1 , and a pair of timing resistors R_6 and R_7 which are selected by the position of a manual switch S_5 .

The outputs of the pulse mode generators are connected by way of lead 56 to the input windings 58 and 60 respectively of a pair of drive cores labelled M_1 and M_2 . Cores M_1 and M_2 are also provided with switch windings 62 and 64 and drive windings 66 and 68 labelled DR1 and DR2 respectively. The switch windings 62 and 64 are coupled to the base of respective trigistors Q_4 and Q_5 . Lead 40 connected to the interlock relay 18 passes through the drive cores to form a reset/set winding for each of these cores as more fully explained below. A resistor R_{15} and inductor L_1 , and further resistor R_{16} connect the drive coils DR1 and DR2 by way of lead 70 to the power supply through switch S_{4c} . The trigistors Q_4 and Q_5 are connected to ground by a rectifier diode D_2 and are coupled to a cable connector 72 having seven terminals as shown in FIGURE 2. Terminal 74 is a ground terminal for the power supply, terminal 76 is the reset/set terminal for the reset/set winding passing through drive cores M_1 and M_2 , and terminal 78 is the power supply terminal. Terminals 80 and 82 are the drive and return terminals for drive coil DR1, while terminals 84 and 86 are the drive and return terminals respectively for drive coil DR2.

FIGURE 3 is a detailed circuit diagram of the basic intervalometer 14 of FIGURE 1. As shown, connector 72 is coupled to a plurality of counting cores N_1 through N_{10} . Corresponding cores actuate a plurality of silicon controlled rectifiers labelled Q_7 through Q_{16} . The output windings of the cores are coupled to the gates of the silicon controlled rectifiers through rectifier diodes D3 through D12. The transfer windings of adjacent cores are connected together by rectifier diodes D13 through D22. Each of the silicon controlled rectifiers couples the power supply to an output connector J_1 which in turn connects to the squibs 44 in FIGURE 4 labelled 1 through 10. The circuit is grounded as indicated at 88.

FIGURE 4a illustrates a typical hysteresis loop for each of the magnetic cores M_1 , M_2 and N_1 through N_{10} . The magnetic cores exhibit two stable states corresponding to the convention "1" and "0." As indicated in FIGURE 4a the "1" state is represented by the positive flux density plus B, while the "0" state is represented by the negative flux density minus B. This notation is purely arbitrary but if one state is called "1" the other state is, by convention, called "0." A particular core once set into a remanent state will remain in this state of magnetization, that is, store the information, until a magnetomotive force H of sufficient amplitude and proper polarity to magnetize the core in the opposite direction is applied to the core. The core will then switch to the opposite remanent state and remain there until further energized.

FIGURE 4b illustrates the action of two of the magnetic cores N_1 and N_2 of FIGURE 3. As illustrated, drive winding DR1 is connected to the first core N_1 , while drive winding DR2 is connected to the second core N_2 . Reset winding 90 passes through both cores. The output winding of core N_1 is connected to silicon controlled rectifier Q_7 which when turned on by the core causes the power supply to fire the squib.

DESCRIPTION OF OPERATION

The operation of the universal intervalometer of the present invention can be viewed through eight distinct phases. These are weapon loading, power-on, mode selection, firing trigger, pulse generation, drive-switching, core operation, and squib firing.

Weapon loading

The first step of operation is for the loadmaster to connect the intervalometer output connector J_1 to the mating

connector from the rocket launcher. Since certain loads can contain nineteen rockets, and since there are a maximum of only ten outputs from the output connector J_1 , the mating plug to the intervalometer output connector J_1 should have parallel squib firing.

It should be noted that no power is available to any of the sections of either the master mode selector 12 or the basic intervalometer 14 at this time. Switch S_1 of the interlock relay (see FIGURE 2) is open as is the mode selector switch S_4 , and the pickel switch S_3 . In other words, the system is in the completely safe condition during the loading operation. In the event that aircraft power is on during the loading operation, only S_1 of the open switches mentioned above will be closed. This still results in two open switches and therefore no safety compromise.

Power on

After completion of the above steps, the next event normally expected is the availability of plus 28 v. D.C. aircraft power. This is fed to the system upon the closure by the loadmaster or pilot of the master armament switch 46. The presence of plus 28 v. D.C. power results in two events. A reset/set pulse immediately travels through normally closed switch S_2 of interlock relay 18. This pulse, controlled by current limiting resistor R_2 , will set a "1" in drive core M_1 , and in intervalometer core N_1 , and a "0" in drive core M_2 , and in intervalometer cores N_2 through N_{10} (FIGURE 3). The setting of either a "1" or "0" in the cores is simply determined by the direction of the core winding.

This momentary application of power erases any previous information in the cores and is necessary regardless of eventual mode selection. The reset/set pulse is only momentary because of the second event resulting from power-on operation. This second event is the energizing of the interlock relay 18. Pulling in of the relay causes the opening of switch S_2 thus ending the reset/set pulse. It also closes switch S_1 and supplies power to the voltage regulator zener diode Z_1 , the pickel switch 20 and to switch S_4 . Power is also supplied to the anode of silicon controlled rectifier Q_1 and to capacitor C_1 and C_2 . No power is supplied to the intervalometer 14 or to any other part of the master mode selector 12 at this time.

Mode selection

The intervalometer system is now ready for the pilot to select the operational firing mode. This is accomplished by manually setting the rotary switch R_4 located on the pilot's console. Clockwise rotation of switch S_4 in FIGURE 2 will enable the selection of the single, pairs or ripple mode respectively. Switch S_4 placement connects plus 28 v. D.C. power to the intervalometer 14 and the core drive circuit comprising resistors R_{15} , R_{16} , capacitor C_5 and inductor coil L_1 in FIGURE 2.

Firing trigger

The intervalometer system is now capable of accepting the firing trigger or pickel switch actuation from the pilot. Firing occurs when the pilot manually depresses the pickel switch S_3 thereby supplying a firing signal to the desired mode generator as selected by the position of switch S_4 . This pickel switch is normally located within the pilot's control stick. In the case of radar controlled fire control systems, a signal from the fire control system can be substituted for the manual operation performed by the pilot.

Pulse generation

The object of closing pickel switch S_3 in series with switch S_4 is to present a drive pulse or drive pulses to the drive cores M_1 and M_2 shown in FIGURE 2. This is achieved by supplying power to the single pulse generator 30 for the single mode, the two pulse generator 32 for the pairs mode, or the dual frequency oscillator 54 for the ripple mode.

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The single pulse generator is activated when selector switch S_4 is placed on "single," that is, turned one step to the "1" position illustrated in FIGURE 2 and the switch S_3 closed by the pickel actuation. Plus 28 v. D.C. power is presented through resistor R_3 to resistor R_4 which provides the gate voltage to trigger the silicon controlled rectifier Q_1 . Capacitor C_1 , which had been charged to the zener voltage of diode Z_1 with the closure of switch S_1 , then discharges through Q_1 and the series resistance offered by the input windings of drive cores M_1 and M_2 . After capacitor C_1 is discharged, the series resistance of Q_1 and the drive core windings is small compared to the resistance of resistor R_5 , and the voltage at the anode of Q_1 drops to nearly zero. In effect a pulse has been delivered to the drive core windings at this time.

Releasing the pickel switch removes the gate voltage from Q_1 and the anode circuit causes conduction through Q_1 to cease. Capacitor C_1 again charges to the zener voltage and the single pulse generator is ready to deliver another pulse when the pickel switch is depressed a second time. The minimum time interval between pulses is determined by the speed in which capacitor C_1 charges to the zener voltage. This time is dependent upon the values of C_1 and R_5 and can easily be designed to be 1 millisecond or less. The time lapse between pickel actuation and the first output is between 4 to 5 microseconds.

The two pulse generator consists of the single pulse generator and a similar pulse generator with a time delay in the gate circuit of a silicon controlled rectifier. The two pulse generator is activated when selector switch S_4 is placed in the "pairs mode" (terminal 2) and the pickel switch S_3 is closed, a pulse is delivered to the drive cores as previously described. At the same time, C_4 charges through R_{13} to the zener Z_1 voltage level and C_3 begins to charge through R_{12} . When the charge on C_3 exceeds the break-down voltage of zener diode Z_2 , the gate voltage to Q_2 is established and Q_2 conducts. C_4 discharges through Q_2 thus delivering a second pulse to the drive cores. The objective of supplying two pulses to the drive cores for each pickel actuation has thus been accomplished. The delay between the two pulses is dependent on the values of R_{12} , C_3 and Z_2 . A nominal value for the delay is 10 milliseconds but this can be changed considerably if desired. The minimum delay between pulses is a function of the switching speeds of the core material.

The dual frequency oscillator 54 is activated when selector switch S_4 is placed on "ripple" position (terminal 3) and switch S_3 is closed by pickel actuation. Closure of switch S_3 causes two events to occur. First, an immediate pulse is fed to the drive cores from the single pulse generator. Secondly, power is supplied to the unijunction controlled oscillator.

The oscillator operates in the following manner: capacitor C_2 is charged at a rate determined by resistor R_6 .

When the emitter of Q_3 reaches a predetermined voltage, unijunction Q_3 conducts sending a pulse to the drive cores. After capacitor C_2 discharges, the unijunction turns off and the process is repeated. The frequency of oscillation is determined by the values of R_6 and C_2 . If select switch S_5 is set to connect R_7 to C_2 , the oscillator operation is similar to that described above with the exception of the frequency of operation. The values of R_6 and R_7 are selected to provide 10 c.p.s. and 100 c.p.s. pulses to the drive cores respectively.

The single pulse generator provides a pulse as the pickel switch is closed. The first pulse from the dual frequency oscillator will not occur until Q_3 conducts.

A difference would normally exist in the time between pickel actuation and the first pulse from the oscillator 54 and between any other two pulses from the oscillator. This is due to the fact that the capacitor C_2 initially charges from zero while for every pulse thereafter it charges from the valley point of the unijunction Q_3 . The

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voltage divider network of R_{10} and R_{11} is added to provide an initial charge on C_2 with the closing of the master armament switch. This circuit eliminates the time delay which would normally be present.

Drive switching

FIGURE 2 also depicts the drive and switching circuitry required to operate the core matrix. The drive cores M_1 and M_2 were set by the procedures described above. When a pulse arrives at core M_1 by way of winding 58 as described above, an induced pulse from winding 62 arrives at the base of trigistor Q_4 since core M_1 switches from a "1" to "0" state. This pulse causes Q_4 to conduct through diode $D2$ and completes the return circuit for drive winding $DR1$ to switch the "1" from magnetic core N_1 to N_2 . Drive winding $DR1$ at 68 also switches drive core M_2 from a "0" to a "1" state. The next pulse that arrives at the drive cores will not affect core M_1 since it is already at the "0" state but will rather switch core M_2 from a "1" to a "0" state. Core M_2 switching causes an induced pulse to arrive at the base of trigistor Q_5 from winding 64 and consequent conduction of Q_5 through diode $D2$. Drive winding $DR2$ receives a pulse and magnetic core N_2 will switch from the "1" state back to the "0" state. Simultaneously a "1" is placed by winding $DR2$ at 66 back in drive core M_1 and the drive switch process is ready to start all over.

The duration of the drive pulse is determined by the circuit components listed as resistor R_{15} , capacitor C_5 and inductor L_1 . Pulse induction between drive cores M_1 and M_2 cannot occur through the reset/set windings because of the limited number of turns of these windings and the higher energy required for the resetting event. The purpose of the drive cores, then, is to provide proper turn-on levels for the bases of trigistors Q_4 and Q_5 and to alternately supply pulses to drive windings $DR1$ and $DR2$. The trigistors assure that the "1" state is alternately switched from drive core M_1 to drive core M_2 while controlling which winding receives the power pulse from the power supply line 70.

Core operation

Magnetic cores exhibit two stable remanent states corresponding to the convention "ones" ("1") and "zeros" ("0"). Reference is made to the hysteresis loop for a magnetic core shown in FIGURE 4a. If one state is called a "1," then the other state is, by convention called a "0." A particular core once set into a remanent state, will remain in this state of magnetization—store the information—until a magnetomotive force of sufficient amplitude and proper polarity to magnetize the core in the opposite direction is applied to the core. The core will then switch to the opposite remanent state.

The cores are wound as shown in FIGURE 3 and in FIGURE 4b. There are two drive windings, $DR1$ and $DR2$, each lacing every other core. According to the previous description, core N_1 has a "1" while all the other matrix cores has a "0." This condition is initially set when the interlock relay 18 pulls in.

When the first pulse arrives through drive winding $DR1$, core N_1 is switched from a "1" to a "0" as described above. Core N_2 , the next core laced by drive winding $DR1$, cannot switch since it has a "0" set in. Switching of core N_1 induces a pulse in the transfer winding (see FIGURE 4b) and places a "1" in core N_2 .

The transfer windings each contain a diode which permits unidirectional operation only. Simultaneously a pulse is induced on the output winding shown on FIGURE 4b. This pulse is presented to the gate of silicon controlled rectifier Q_7 .

Squib firing

The output pulse to the silicon controlled rectifier Q_7 gate causes this silicon controlled rectifier to conduct. This in turn places ample current through the squib to

fire. Conduction through silicon controlled rectifier Q_1 ceases as the squib firing presents an opening to the silicon controlled rectifier-squib circuit.

The next pulse through the drive cores ends up on drive winding DR2. The identical procedure occurs on core N_2 causing squib #2 to fire. As many squibs will fire as pulses received at the drive cores. The core matrix thus acts as a solid state stepping switch. The number of steps (pulses) is determined by the master mode selection—one step for single, two steps for pairs, and all ten steps for ripple.

An additional feature is provided by the transfer winding between cores N_{10} and N_1 . When the last or tenth pulse is received, core N_1 is again placed in the "1" state and the firing cycle repeats from the beginning. This feature is incorporated so that any squib failure will receive an additional firing chance.

It is apparent from the above that the present invention provides a novel intervalometer of a very versatile and reliable construction making possible three different modes of firing at the election of the pilot. Utilization of solid state circuitry and miniature magnetic cores results in an unusually small and lightweight device. The universal intervalometer consists of two discrete packages joined by the interconnecting cabling. One of the basic intervalometers 14 is located in each rocket launcher or weapon pylon. Up to seven such packages can be installed per aircraft. Only one master mode selector package 12 is placed in each rocket equipped aircraft.

All the micro-components for the intervalometer 14 can be contained within a 2" long x 1½" wide x 1" deep rectilinear envelope. This three cubic inch volume comfortably houses thirty solid-state components, ten resistors, a printed board mounting card, a five pin connector, an eleven pin connector, and the drawn-can cover. The weight of this package is seven ounces maximum. Ample room is available for subsequent inclusion of a mounting flange compatible with end-item use and an O-ring or solder seal is provided, as required.

The master mode selector package 12 is contained in a conventional console opening in the aircraft cockpit. This package is approximately 2¾" deep. This envelope contains a relay, a mode selector switch, eight semi-conductors, two drive coils, miscellaneous resistors and capacitors (approximately twenty-one), a mounting plate, and interconnecting wiring. The weight of this package is in the neighborhood of thirteen ounces. Weight, always an important consideration in aircraft equipment, is minimized because of the miniature components employed.

The time delay between successive ignition signals is quite accurate. The unijunction controlled oscillator operates over a temperature range of from -60° F. to 165° F. and is able to hold a hundred cycle per second output, with a plus or minus 3 to 4 percent accuracy with minimum temperature compensation. The 100 c.p.s. mode will operate within plus or minus 5 percent accuracy without temperature compensation and the 10 c.p.s. mode operates without temperature compensation within 15 percent accuracy.

Potting of the electronic components plus sealing of the cover can makes the intervalometer insensitive to pressure and humidity. Complex vibration spectra and shock pulses do not seriously affect the intervalometer because of the lack of mechanical or electromechanical parts. The light weight and small size make it additionally impervious to mechanical environmental variations. The silicon controlled rectifier gates are located close to the trigger source resulting in short lead lengths, thus minimizing radio frequency interference. The power supply lines are isolated by open switches and common intervalometer grounds are preferably used and isolated from the aircraft or chassis ground. The squib grounds and intervalometer grounds are common. The diodes in the

transfer loops prevent inadvertent feedback currents from supplying gate pulses to the SCR switches.

The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The present embodiment is therefore to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than by the foregoing description and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein.

What is claimed and desired to be secured by United States Letters Patent is:

1. An intervalometer comprising a magnetic core matrix stepper switch for generating a squib firing signal for each step of said switch, a pair of drive cores for alternately providing stepping impulses to said stepper switch, a trigger switch, and a plurality of pulse generators including a single pulse generator, a pulse pair generator, and a ripple pulse generator, for energizing said drive cores in response to actuation of said trigger switch.

2. An intervalometer according to claim 1 wherein said ripple pulse generator comprises a relaxation oscillator having a unijunction transistor.

3. An intervalometer according to claim 1 including a first drive winding interlacing alternate ones of the cores of said magnetic core stepper switch, a second drive winding interlacing the remainder of the cores of said magnetic core stepper switch, each of said drive cores being interlaced by one of said drive windings, and an input winding interlacing both of said drive cores.

4. An intervalometer comprising a plurality of magnetic cores changeable between two magnetic remanent states, a first drive winding interlacing alternate ones of said cores, a second drive winding interlacing the remainder of said cores, a transfer winding coupling each core with the next adjacent core for causing a change of state in said each core to produce an opposite change of state in said adjacent core, a squib firing signal output terminal for each of said cores, a power supply terminal, a solid state switch device coupling said power supply terminal to each of said output terminals, an output winding coupling each of said cores to its respective solid state switch device whereby said change of state in each said core activates said respective switch device, first and second drive cores interlaced by said first and second drive windings respectively, an input winding interlacing both of said drive cores, means for setting said first drive core in a first magnetic remanent state and said second drive core in a second remanent state, and means for supplying pulses to said input winding to produce corresponding output pulses alternately on said drive windings.

5. An intervalometer comprising a plurality of magnetic cores changeable between two magnetic remanent states, a first drive winding interlacing alternate ones of said cores, a second drive winding interlacing the remainder of said cores, a transfer winding coupling each core with the next adjacent core for causing a change of state in said each core to produce an opposite change of state in said adjacent core, a squib firing signal output terminal for each of said cores, a power supply terminal, a solid state switch device coupling said power supply terminal to each of said output terminals, an output winding coupling each of said cores to its respective solid state switch device whereby said change of state in each said core activates said respective switch device, first and second drive cores interlaced by said first and second drive windings respectively, an input winding interlacing both of said drive cores, means for setting said first drive core in a first magnetic remanent state and said second drive core in a second remanent state, and means for supplying pulses to said input winding to produce corresponding output pulses alternately on said drive windings, said pulse supplying means including a picket switch, single pulse generator

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means and multiple pulse generator means, and a mode selector switch for selectively coupling either of said pulse generator means between said pickel switch and said drive core input winding.

6. An intervalometer according to claim 5 including first and second trigistors, a switch winding on each of said drive cores coupled to the base of a respective trigistor, means coupling the emitter-base circuit of said first trigistor in series with said first drive winding, and means coupling the emitter-base circuit of said second trigistor in series with said second drive winding.

7. A weapons system comprising a plurality of magnetic cores changeable between two magnetic remanent states, a first drive winding interlacing alternate ones of said cores, a second drive winding interlacing the remainder of said cores, a transfer winding coupling each core with the next adjacent core for causing a change of state in said each core to produce an opposite change of state in said adjacent core, a squib firing signal output terminal for each of said cores, a power supply terminal, a solid state switch device coupling said power supply terminal to each of said output terminals, an output winding coupling each of said cores to its respective solid state switch device whereby said change of state in each said core activates said respective switch device, a rocket firing squib coupled to each of said output terminals, first and second drive cores interlaced by said first and second drive windings respectively, an input winding interlacing both of said drive cores, means for setting said first drive core in a first magnetic remanent state and said second drive core in a second remanent state, and means for supplying pulses to said input winding to produce corresponding output pulses alternately on said drive windings, said pulse supplying means comprising a pickel switch, a single pulse generator, a double pulse generator, and an oscillator pulse generator, means coupling the output of each

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of said generators to said drive core input winding, and a mode selector switch for selectively coupling said pickel switch to the input of one of said pulse generators.

8. A weapons system according to claim 7 wherein said single and double pulse generators each include a silicon controlled rectifier, and said oscillator pulse generator includes a variable frequency unijunction transistor oscillator.

9. A weapons system according to claim 8 including an interlock relay between said power supply terminal and said pickel switch, and zener diode voltage regulator means coupled to said power supply terminal.

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