



- (51) **International Patent Classification:**
H01L 27/108 (2006.01) *H01L 21/8242* (2006.01)
- (21) **International Application Number:**
PCT/US2012/022195
- (22) **International Filing Date:**
23 January 2012 (23.01.2012)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**
13/011,946 24 January 2011 (24.01.2011) US
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(81) **Designated States** (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE,

[Continued on next page]

- (54) **Title:** PULSE METHOD OF OXIDIZING SIDEWALL DIELECTRICS FOR HIGH CAPACITANCE APPLICATIONS

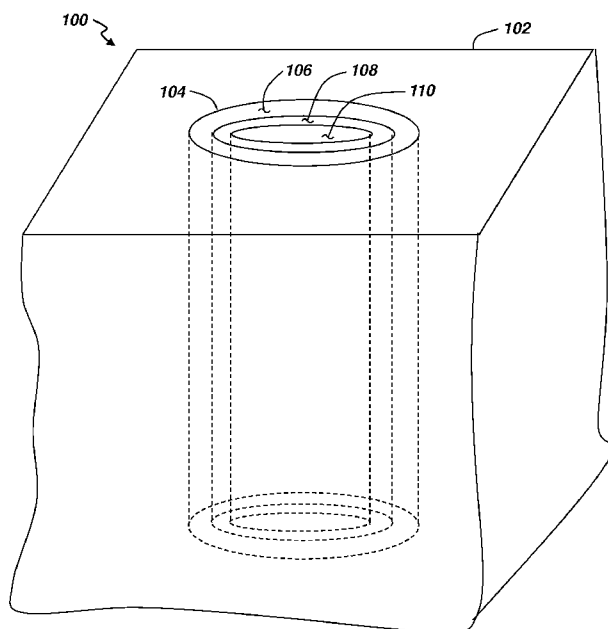


FIG. 1

(57) **Abstract:** The present invention provides systems, methods and apparatus for manufacturing a memory cell. The invention includes forming a feature having sidewalls in a first dielectric material; forming a first conductive material on the sidewalls of the feature; depositing a layer of a second dielectric material on the conductive material; and exposing the second dielectric material to oxidizing species and ultraviolet light to oxidize the second dielectric material. Numerous additional aspects are disclosed.



DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT,
LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE,
SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA,
GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *without international search report and to be republished
upon receipt of that report (Rule 48.2(g))*

**PULSE METHOD OF OXIDIZING SIDEWALL DIELECTRICS FOR
HIGH CAPACITANCE APPLICATIONS**

FIELD OF THE INVENTION

5 **[0001]** The present invention relates to data storage memories, and more particularly to methods and apparatus for increasing the capacitance of memory cells.

BACKGROUND

10 **[0002]** The design goal of reducing the size and power consumption of memory devices, including dynamic random access memory (DRAM) devices, is enabled by the emerging technologies that enable feature size reduction. However, as memory designs are scaled down to create higher density memories,
15 issues may arise that interfere with the operation of the devices. Thus, improved methods, apparatus, and systems that allow reliable operation of higher density memories are desirable.

20 **SUMMARY**

[0003] In some embodiments, the present invention provides a method of manufacturing a memory cell. The method includes forming a feature having sidewalls in a first dielectric material; forming a first conductive material on the sidewalls
25 of the feature; depositing a layer of a second dielectric material on the conductive material; and exposing the second dielectric material to oxidizing species and ultraviolet light to oxidize the second dielectric material.

[0004] In some other embodiments, the present invention provides another method of manufacturing a memory cell. The method includes forming a feature having sidewalls in a first dielectric material; forming a first conductive material on the sidewalls of the feature; depositing a layer of a second dielectric material on the conductive material; and exposing the second dielectric material to O₂, ultraviolet light, and heat to oxidize the second dielectric material.

[0005] In yet other embodiments, the present invention provides a memory cell. The memory cell includes a feature formed in a first dielectric material, the feature including sidewalls; a first conductive material formed on the sidewalls of the feature; and a layer of a second dielectric material deposited on the conductive material. The second dielectric material is oxidized by exposure to oxidizing species and ultraviolet light.

[0006] In still yet other embodiments, the present invention provides a memory cell that includes a feature formed in a first dielectric material, the feature having sidewalls; a first conductive material formed on the sidewalls of the feature; and a layer of a second dielectric material deposited on the conductive material. The second dielectric material is oxidized by exposure to O₂, ultraviolet light, and heat.

[0007] In a further embodiment, the present invention provides a memory that includes a plurality of features formed in a first dielectric material, the features each having sidewalls; a first conductive material formed on the sidewalls of the features; and a layer of a second dielectric material

deposited on the conductive material. The second dielectric material is oxidized by exposure to oxidizing species and ultraviolet light.

[0008] In yet a further embodiment, the present invention provides a memory that includes a plurality of features formed in a first dielectric material, the features each having sidewalls; a first conductive material formed on the sidewalls of the features; and a layer of a second dielectric material deposited on the conductive material. The second dielectric material is oxidized by exposure to O₂, ultraviolet light, and heat.

[0009] Numerous additional embodiments are described below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Features of the present invention can be more clearly understood from the following detailed description considered in conjunction with the following drawings, in which the same reference numerals denote the same elements throughout.

[0011] FIG. 1 is a perspective drawing of an example arrangement of a memory cell according to some embodiments of the present invention.

[0012] FIG. 2 is a plan drawing of an example arrangement of a memory cell layout according to some embodiments of the present invention.

[0013] FIG. 3 is a flowchart depicting a first example method according to some embodiments of the present invention.

[0014] FIG. 4 is a flowchart depicting a second example method according to some embodiments of the present invention.

[0015] FIG. 5 is a flowchart depicting a third example method according to some embodiments of the present invention.

DETAILED DESCRIPTION

5 [0016] The present invention provides systems, methods, and apparatus to increase the capacitance of memory storage capacitors such as those used in DRAMs. Maximizing the capacitance is desirable to increase the data retention time and to increase the signal margin for sense amplifier
10 operation. In other words, the more capacitance a memory cell has, the longer data can be stored in the cell without having to refresh the cell (therefore the memory has lower power requirements) and the larger the amplitude of the signal generated from reading the memory cell, so that the value
15 stored in the cell can be read more accurately and reliably. Further, as DRAM designs are reduced in size, for example below 70 nm feature sizes, maintaining a threshold capacitance value becomes important to the operation of the memory cells. In other words, with higher memory densities, DRAM cell
20 dimensions become increasingly smaller, and the scaled down geometries do not have sufficient material to provide capacitances sufficient to function with existing memory systems. For example, 30fF/cell represents a threshold capacitance below which existing memory systems do not
25 function properly.

[0017] The inventors of the present invention have determined that materials such as Tantalum Oxide (Ta_2O_5) and Aluminum Oxide (Al_2O_3) maybe used as the dielectric material to generate higher capacitances per unit area than conventional

materials. Other high dielectric constant (high-K) materials such as, for example, Zinc Oxide (ZnO), Hafnium Oxide (HfO₂), and Zirconium Oxide (ZrO₂) may also be used. In addition, because merely using these materials in place of conventional material may result in higher leakage current, the inventors of the present invention have determined systems, methods, and apparatus to uniformly oxidize memory cell sidewall materials such as Ta, Al, Zn, Hf, or Zr without oxidizing supporting materials (e.g., other memory cell materials such as TiN, TaN, WN₂, etc.). In other words, memory cells that are formed in a feature (e.g., a cylindrical opening or hole) with sidewalls in a dielectric and include a conductive sidewall layer that is coated with a film of TaO or Al₂O₃ for example (as the capacitor dielectric), can be uniformly oxidized to minimize leakage current according to the methods and apparatus of the present invention. The present invention allows the retention of oxygen in the Ta₂O₅ or Al₂O₃ (or other material) without oxidizing the conductive sidewall layer (e.g., without oxidizing the TiN).

[0018] The present invention includes several embodiments. The embodiments described herein are intended merely to provide illustrative examples and are not intended to be an exhaustive listing of every possible variation of the invention. In a first embodiment, memory cell capacitance may be increased by oxidizing sidewall high dielectric constant materials such as Ta₂O₅, Al₂O₃, ZnO, HfO₂, or ZrO₂ films using ultraviolet (UV) light and ozone (O₃). After a sidewall conductor in a memory feature is coated with a dielectric film, ozone is flowed into the feature while UV light is

applied. The UV light breaks the ozone into oxygen radicals ($O\cdot$) that act as oxidants to oxidize the dielectric film.

[0019] In a second embodiment, the UV light is pulsed on and off after the ozone is flowed into the memory feature.

5 While the UV light is off, the ozone diffuses into the dielectric structure (e.g., the Ta_2O_5 , Al_2O_3 , ZnO , HfO_2 , or ZrO_2). Once the UV light is turned on, the UV light breaks the ozone both within the dielectric structure and being flowed into the memory feature. As with the first embodiment, the UV
10 light breaks the ozone into oxygen radicals ($O\cdot$) that act as oxidants to oxidize the dielectric structure. By turning off the UV light, the rate of oxidation may be carefully controlled so that the supporting materials are not oxidized with the dielectric structure. This pulsed mode of oxidizing
15 also allows the dielectric structure to be more uniformly oxidized. In various embodiments, the UV power, the wafer temperature, chamber pressure, ozone concentration, and UV on/off times may be varied to optimize the oxidation in terms of uniformity, thickness, and avoiding oxidation of supporting
20 materials. In some embodiments, by maintaining the wafer at temperatures below 300 degrees C, the ozone will have sufficient time to diffuse into the dielectric structure before breaking down into oxygen radicals and begin oxidation.

[0020] In a third embodiment of the present invention, UV
25 assisted thermal oxidation using oxygen (O_2) maybe used to oxidize the dielectric film of the capacitor. In other words, the application of both heat and UV light breaks the oxygen (O_2) into oxygen radicals ($O\cdot$) that act as oxidants to oxidize the dielectric structure.

[0021] Turning to FIGs. 1 and 2, an example of a memory cell structure 100 according to embodiments of the present invention is depicted. FIG. 1 depicts a perspective view and FIG. 2 provides a cross-sectional plan view of an example memory cell structure. Within a relatively thick horizontal dielectric layer 102, a feature 104 is formed. The feature 104 may be a cylindrical hole, via, or any convenient, practicable shape. The sidewalls of the feature 104 may be coated with a first conductive layer 106 which serves as one of the charge plates of the memory cell capacitor. The conductive layer 106 is coated with a dielectric film 108 or structure which serves as the capacitor dielectric. Finally, a second conductor 110 may be deposited to fill part or all of the remaining space within the feature 104 and to serve as the other charge plate of the capacitor.

[0022] The feature 104 of the structure 100 may be formed in any number of different insulating materials including silicon dioxide (SiO_2) or any other practicable material. The feature 104 may, for example, have an aspect ratio (e.g., height to width) of approximately 40:1. In some embodiments, the aspect ratio may be in the range of approximately 40:1 to approximately 60:1. Other aspect ratios outside this range may also be used. In some embodiments, the feature 104 may be approximately 20000 angstroms to approximately 50000 angstroms deep. Other depths outside this range may also be used. In some embodiments, the feature 104 may be approximately 300 angstroms to approximately 1000 angstroms in diameter. Other diameters outside this range may also be used.

[0023] As indicated above, the dielectric layer 102 may be formed from any practicable material such as for example, silicon dioxide, silicon nitride, silicon oxynitride or any other suitable insulating material. Any practicable method
5 may be employed to form dielectric layer 102 such as, for example, physical vapor deposition or any other suitable method. In some embodiments, dielectric layer 102 may be in the range of approximately 10 angstroms to approximately 100 angstroms thick. In other embodiments, other thicknesses may
10 be used for dielectric layer 102.

[0024] The first conductive layer 106 lining the sidewalls of the feature 104 may be TiN, TaN, WN₂, or any practicable conductive material. The conductive layer 106 may be deposited by any practicable method such as, for example,
15 physical vapor deposition, or any other suitable method. In some embodiments, conductive layer 106 may be in the range of approximately 100 angstroms to approximately 1000 angstroms thick. In other embodiments, other thicknesses may be used for conductive layer 106.

[0025] The dielectric film 108 on the first conductive layer 106 may be Ta₂O₅, Al₂O₃, ZnO, HfO₂, or ZrO₂ or any practicable high K dielectric material. The dielectric film 108 is formed according to methods of the present invention described in more detail below. In some embodiments, an
20 initial material such as Ta, Al, Zn, Hf, or Zr may be deposited by any practicable method such as, for example, physical vapor deposition or any other suitable method. As will be described below, the initial material may then be oxidized to form a high K dielectric film 108 of Ta₂O₅, Al₂O₃,
25

ZnO, HfO₂, or ZrO₂, respectively. In some embodiments, the high K dielectric film 108 may be in the range of approximately 5 angstroms to approximately 50 angstroms thick. In other embodiments, other thicknesses may be used for dielectric film 108.

[0026] The second conductor 110 may be formed as a layer on the dielectric film 108 or simply as a cylinder, which fills the remaining area within the feature 104. In either case, the second conductor 110 may be TiN, TaN, WN₂, or any practicable conductive material. The second conductor 110 may be deposited by any practicable method such as, for example, physical vapor deposition or any other suitable method. In some embodiments, the second conductor 110 may be in the range of approximately 10 angstroms to approximately 200 angstroms thick. In other embodiments, other thicknesses may be used for the second conductor 110.

[0027] Turning now to FIGs. 3 to 5, exemplary methods of the present invention are described. Note that the example methods are represented using flowcharts with discrete steps. However, one of ordinary skill would understand that the steps shown may include any number of sub-steps and/or may be combined to form fewer steps. Further, not all of the steps shown are required for every embodiment of the invention. In particular, steps shown surrounded by a dashed line may be optional in some embodiments. Further, the flowcharts are intended to illustrate novel features of the present invention. One of ordinary skill in the art would readily appreciate that many other processing steps not shown in FIGs. 3 to 5 and/or not specifically discussed in the specification

may be required to be performed in the manufacture of a memory cell array. For example, the flowcharts do not depict the steps of forming the dielectric layer 102 on a substrate, forming the features 104 in the dielectric layer 102, or
5 forming the second conductor 110 on the high K dielectric film 108. Each of the flowcharts begin with at least one feature 104 formed in a dielectric layer 102 on a substrate. The sidewalls of the feature 104 are lined with a conductive layer 106 which is coated with a dielectric film 108.

10 **[0028]** FIG. 3 depicts a first example method 300 according to some embodiments of the present invention. In step 302, a prepared substrate (including a dielectric layer 102 with a plurality of features 104, each feature including sidewalls that are lined with a conductive layer 106 coated with an
15 initial film) is loaded into a processing chamber. In some embodiments, the substrate may already be in the processing chamber from prior processing. In some embodiments, the plurality of features may be an array of openings adapted to hold memory cell components. Any number of features 104 may
20 be provided.

[0029] In step 304, the substrate is heated to a process temperature. In some embodiments, the process temperature may be in the range of approximately 200 degrees Celsius to approximately 350 degrees Celsius. Other temperatures outside
25 this range may also be used.

[0030] In step 306, oxidizing species are flowed into the chamber and into the features. The oxidizing species may include O_3 , O_2 , combinations of O_3 and O_2 , and other oxidizing species. In some embodiments, additional gases may be

combined with the oxidizing species. For example, nitrogen (N₂), argon (Ar), and/or other inert gases maybe used. In some embodiments, the flow rate of the oxidizing species may be in the range of approximately 5 standard cubic centimeters per minute (sccm) to approximately 20 sccm. Other flow rates may be used. In some embodiments, the pressure of the oxidizing species may be in the range of approximately 6 Torr to approximately 100 Torr. Other pressures may be used. In some embodiments, the concentration of the oxidizing species may be in the range of approximately 10 weight% to approximately 50 weight%. Other concentrations may be used.

[0031] Optionally, in step 308, the oxidizing species are given time to diffuse into the film 108 on the conductive layer 106. In some embodiments, the time period allowed for diffusion may be approximately 300 seconds to approximately 1800 seconds. Other time periods outside this range may also be used.

[0032] In step 310, an energy source, such as a ultra-violet (UV) light, is used to oxidize the film. In some embodiments, a microwave UV source with a broadband UV bulb may be used. For example, the CoolWave® 2 610 System model that is commercially available from Nordson Corporation of Westlake, Ohio may be used as a UV source. In some embodiments, any of the various practicable UV source technologies, bulbs, and resulting output types (e.g., broadband UV, single wavelength, spectral profile (e.g., UVA, UVB, UVC, IR, etc.)) may be used. In some embodiments, the output power of the UV source may be varied from approximately 60% to approximately 100%. Other output power percentages

outside this range may also be used. In some embodiments, the UV light may have an irradiance of approximately 100 W/m^2 to approximately 2000 W/m^2 . Other irradiance values outside this range may also be used. In some embodiments, the exposure
5 time period for oxidizing the film may be approximately 300 seconds to approximately 900 seconds. Other exposure time periods outside this range may also be used. In some embodiments, the UV light may be pulsed at a rate of approximately 0.033 hertz to approximately 0.2 hertz. Other
10 pulse rate values outside this range may also be used.

[0033] Optionally, in step 312, thermal oxidation may be performed. In some embodiments, the thermal oxidation may include heating the substrate to a temperature of approximately 200 degrees to approximately 450 degrees. Other
15 temperatures outside this range may also be used. In some embodiments, the time period allowed for thermal oxidation may be approximately 60 seconds to approximately 1800 seconds. Other time periods for thermal oxidation outside this range may also be used.

[0034] According to the present invention, using the method described above, memory cell capacitance may be increased by oxidizing sidewall high dielectric constant materials such as Ta_2O_5 , Al_2O_3 , ZnO , HfO_2 , or ZrO_2 films using UV light and oxidizing species (e.g., O_3 , O_2 , combinations of O_3 and O_2
25 etc.) After a sidewall conductor in a memory feature is coated with a dielectric film, oxidizing species are flowed into the feature 104 and UV light is applied. The UV light breaks the oxidizing species into oxygen radicals ($\text{O}\cdot$) that act as oxidants to oxidize the high K dielectric film.

[0035] FIG. 4 depicts a second example method 400 according to some embodiments of the present invention. In a second embodiment, the UV light is pulsed on and off after the ozone is flowed into the memory feature. While the UV light is off, the oxidizing species diffuses into the dielectric structure/film (e.g., the Ta₂O₅, Al₂O₃, ZnO, HfO₂, or ZrO₂). Once the UV light is turned on, the UV light breaks the oxidizing species both within the dielectric structure/film and being flowed into the memory feature 104. As with the first embodiment, the UV light breaks the oxidizing species into oxygen radicals (O•) that act as oxidants to oxidize the dielectric structure. By turning off the UV light, the rate of oxidation may be carefully controlled so that the supporting materials (e.g., the conductive layer 106) are not oxidized with the dielectric structure/film. This pulsed mode of oxidizing also allows the dielectric structure/film to be more uniformly oxidized. In various embodiments, the UV power, the wafer temperature, chamber pressure, oxidizing species concentration, and UV on/off times may be varied to optimize the oxidation in terms of uniformity, thickness, and avoiding oxidation of supporting materials. In some embodiments, by maintaining the substrate at temperatures below 300 degrees C, the oxidizing species will have sufficient time to diffuse into the dielectric structure/film before breaking down into oxygen radicals and beginning oxidation.

[0036] The following table provides a specific example of process variable values.

Step #	1		2		3		4		5		6	
Name	Stab 90-90		Diffusion		Lamp On 90-90		UV Treatment		Move to Lift		Pump	
ChLocation	Any		Any		Any		Any		Any		Any	
Mode	Time		Time		Time		Time		Endpoint		Time	
MaxTime	15		5		5		5		5		5	
LiftPos	Process		Process		Process		Process		Process		Lift	
HtrSpace1	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	1.6	1.6	1.6	1.6
Heater Temp	300		300		300		300		300		300	
PressMode	Servo		Servo		Servo		Servo		Servo		AbsCtrl	
Press	20		20		20		20		20			
TV position											90	
UV Lamp1 On Time			5	5	5	5	5	5				
UV Lamp Setpoint1	25	25	25	25	100	100	100	100	25	25	25	25
UV Lamp Rotator Home Rotator									No			
O ₃ (sccm)	10K	FToC	10K	FToC	10K	FToD	10K	FToD	10K	FToD	10K	FToD

FToC: Flow to Chamber, FToD: Flow to Divert

In the above table, example process values for six example steps (numbered 1 to 6 in each column heading) are listed. In Step 1, pressure and temperature is stabilized over 15 seconds, pressure is set at 20 Torr, temperature is set at 300 degrees Celsius (C), spacing is set at 400 mils, O₃ flow rate is set to 10000 sccm. In Step 2, O₃ is diffused into the sidewall structure for 5 seconds. In Step 3, the UV lamp is activated for 5 seconds. In Step 4, a UV cure is performed for 5 seconds. Next, the example process returns to Step 2 and steps 2 through 4 are repeated for a number of cycles (e.g., 200 cycles). In Step 5, the substrate is moved to the

lift over a 5 second period. In Step 6, the chamber is pumped down over a 5 second period.

[0037] With respect to FIG. 4, in step 402, a prepared substrate (including a dielectric layer 102 with a plurality of features 104, each feature including sidewalls that are lined with a conductive layer 106 coated with an initial film) is loaded into a processing chamber. In some embodiments, the substrate may already be in the processing chamber from prior processing. In some embodiments, the plurality of features may be an array of openings adapted to hold memory cell components. Any number of features 104 may be provided.

[0038] In step 404, the substrate is heated to a process temperature. In some embodiments, the process temperature may be in the range of approximately 200 degrees Celsius (C) to approximately 350 degrees C. Other temperatures outside this range may also be used.

[0039] In step 406, oxidizing species are flowed into the chamber and into the features. The oxidizing species may include O_3 , O_2 , combinations of O_3 and O_2 , and other oxidizing species. In some embodiments, additional gases may be combined with the oxidizing species. For example, nitrogen (N_2), argon (Ar), and/or other inert gases may be used. In some embodiments, the flow rate of the oxidizing species may be in the range of approximately 5 standard cubic centimeters per minute (sccm) to approximately 30 sccm. Other flow rates may be used. In some embodiments, the pressure of the oxidizing species may be in the range of approximately 6 Torr to approximately 100 Torr. Other pressures may be used. In some embodiments, the concentration of the oxidizing species may be

in the range of approximately 10 weight% to approximately 50 weight%. Other concentrations may be used.

[0040] In step 408, the oxidizing species are given time to diffuse into the film 108 on the conductive layer 106. In
5 some embodiments, the time period allowed for diffusion may be approximately 5 seconds to approximately 300 seconds. Other time periods outside this range may also be used. In some embodiments, the diffusion time period may be varied depending upon the number of oxidation cycles that have been performed,
10 the amount of oxidation that has occurred, and/or other factors.

[0041] In step 410, an energy source, such as a ultra-violet (UV) light, is used to oxidize the film. In some embodiments, a microwave UV source with a broadband UV bulb
15 may be used. For example, the CoolWave® 2 610 System model mentioned above with respect to the first example method embodiment may be used as a UV source. In some embodiments, any of the various practicable UV source technologies, bulbs, and resulting output types (e.g., broadband UV, single
20 wavelength, spectral profile (e.g., UVA, UVB, UVC, IR, etc.)) may be used. In some embodiments, the output power of the UV source may be varied from approximately 60% to approximately 100%. Other output power percentages outside this range may also be used. In some embodiments, the UV light may have an
25 irradiance of approximately 100 W/m² to approximately 2000 W/m². Other irradiance values outside this range may also be used. In some embodiments, the exposure time period for oxidizing the film may be approximately 300 seconds to approximately 900 seconds. Other exposure time periods

outside this range may also be used. In some embodiments, the exposure time period may be varied depending upon the number of oxidation cycles that have been performed, the amount of oxidation that has occurred, and/or other factors. In some
5 embodiments, the UV light may be pulsed at a rate of approximately 0.033 hertz to approximately 0.2 hertz. Other pulse rate values outside this range may also be used.

[0042] In step 412, the UV source is turned off to slow or suspend the oxidation. In step 414, the amount of oxidation
10 is evaluated. A determination of whether oxidation is complete may be made. For example, in some embodiments, X-ray Photoelectron Spectroscopy (XPS) may be used to determine whether complete oxidation has been achieved. Other methods may also be used. In some embodiments, a simple cycle counter
15 may be used to track the oxidation process. In some embodiments, the oxidation cycle may be repeated approximately 100 to approximately 200 times. If oxidation is not complete, flow reverts back to step 408 and the diffusion/oxidation cycle is repeated. If oxidation is complete, flow proceeds to
20 step 416.

[0043] Optionally, in step 416, thermal oxidation may be performed. In some embodiments, the thermal oxidation may include heating the substrate to a temperature of
approximately 200 degrees to approximately 450 degrees. Other
25 temperatures outside this range may also be used. In some embodiments, the time period allowed for thermal oxidation may be approximately 60 seconds to approximately 1800 seconds. Other time periods for thermal oxidation outside this range may also be used.

[0044] FIG. 5 depicts a third example method 500 according to some embodiments of the present invention. In the third embodiment of the present invention, UV assisted thermal oxidation using oxygen (O_2) maybe used to oxidize the dielectric film of the capacitor. In other words, the application of both heat and UV light breaks the oxygen (O_2) into oxygen radicals (O) that act as oxidants to oxidize the dielectric structure.

[0045] With respect to FIG. 5, in step 502, a prepared substrate (including a dielectric layer 102 with a plurality of features 104, each feature including sidewalls that are lined with a conductive layer 106 coated with an initial film) is loaded into a processing chamber. In some embodiments, the substrate may already be in the processing chamber from prior processing. In some embodiments, the plurality of features may be an array of openings adapted to hold memory cell components. Any number of features 104 may be provided.

[0046] In step 504, oxidizing species are flowed into the chamber and into the features 104. The oxidizing species may include O_3 , O_2 , combinations of O_3 and O_2 , and other oxidizing species. In some embodiments, additional gases may be combined with the oxidizing species. For example, nitrogen (N_2), argon (Ar), and/or other inert gases maybe used. In some embodiments, the flow rate of the oxidizing species may be in the range of approximately 5 standard cubic centimeters per minute (sccm) to approximately 30 sccm. Other flow rates may be used. In some embodiments, the pressure of the oxidizing species may be in the range of approximately 6 Torr to approximately 100 Torr. Other pressures may be used. In some

embodiments, the concentration of the oxidizing species may be in the range of approximately 10 weight% to approximately 50 weight%. Other concentrations may be used.

[0047] In step 506, the substrate is heated to a process temperature. In some embodiments, the process temperature may be in the range of approximately 200 degrees C to approximately 500 degrees C. Other temperatures outside this range may also be used. The substrate may be heated for approximately 600 seconds to approximately 1800 seconds. Other heating time periods outside this range may also be used.

[0048] Optionally, in step 508, the oxidizing species are given time to diffuse into the film 108 on the conductive layer 106. In some embodiments, the time period allowed for diffusion may be approximately 300 seconds to approximately 1800 seconds. Other time periods for diffusion outside this range may also be used.

[0049] In step 510, an energy source, such as a ultra-violet (UV) light, is used to oxidize the film. In some embodiments, a microwave UV source with a broadband UV bulb may be used. For example, the CoolWave® 2 610 System model noted above may be used as a UV source. In some embodiments, any of the various practicable UV source technologies, bulbs, and resulting output types (e.g., broadband UV, single wavelength, spectral profile (e.g., UVA, UVB, UVC, IR, etc.)) may be used. In some embodiments, the output power of the UV source may be varied from approximately 60% to approximately 100%. Other output power percentages outside this range may also be used. In some embodiments, the UV light may have an

irradiance of approximately 100 W/m^2 to approximately 2000 W/m^2 . Other irradiance values outside this range may also be used. In some embodiments, the exposure time period for oxidizing the film may be approximately 300 seconds to
5 approximately 900 seconds. Other exposure time periods outside this range may also be used. In some embodiments, the UV light may be pulsed at a rate of approximately 0.033 hertz to approximately 0.5 hertz. Other pulse rate values outside this range may also be used.

10 **[0050]** Optionally, in step 512, thermal oxidation may be performed. In some embodiments, the thermal oxidation may include heating the substrate to a temperature of approximately 200 degrees to approximately 450 degrees. Other temperatures outside this range may also be used. In some
15 embodiments, the time period allowed for thermal oxidation may be approximately 60 seconds to approximately 1800 seconds. Other time periods for thermal oxidation outside this range may also be used.

[0051] Persons of ordinary skill in the art will understand
20 that alternative memory cells in accordance with this invention may be fabricated using other similar techniques.

[0052] The foregoing description discloses only exemplary embodiments of the invention. Modifications of the above disclosed apparatus and methods which fall within the scope of
25 the invention will be readily apparent to those of ordinary skill in the art.

[0053] Accordingly, although the present invention has been disclosed in connection with some specific exemplary embodiments thereof, it should be understood that other embodiments may fall within the spirit and scope of the
5 invention, as defined by the following claims.

What is claimed is:

1. A method of manufacturing a memory cell comprising:
forming a feature having sidewalls in a first dielectric
5 material;
forming a first conductive material on the sidewalls of
the feature;
depositing a layer of a second dielectric material on the
conductive material; and
10 exposing the second dielectric material to oxidizing
species and ultraviolet light to oxidize the second dielectric
material.
2. The method of claim 1 further comprising forming a second
15 conductive material on the oxidized second dielectric
material.
3. The method of claim 1 wherein the first dielectric
material includes at least one of silicon dioxide, silicon
20 nitride, and silicon oxynitride.
4. The method of claim 1 wherein the first conductive
material includes at least one of TiN, TaN, and WN₂.
- 25 5. The method of claim 1 wherein the second dielectric
material includes at least one of Ta₂O₅, Al₂O₃, ZnO, HfO₂, and
ZrO₂.

6. The method of claim 1 wherein exposing the second dielectric material to oxidizing species and ultraviolet light includes diffusing ozone into the second dielectric material and then pulsing the diffused ozone with the ultraviolet light
5 to break the ozone into oxygen radicals.

7. The method of claim 1 wherein the materials are kept at a temperature of less than 300 degrees C.

10 8. A method of manufacturing a memory cell comprising:
forming a feature having sidewalls in a first dielectric material;
forming a first conductive material on the sidewalls of the feature;
15 depositing a layer of a second dielectric material on the conductive material; and
exposing the second dielectric material to O₂, ultraviolet light, and heat to oxidize the second dielectric material.

20 9. A memory cell comprising:
a feature formed in a first dielectric material, the feature including sidewalls;
a first conductive material formed on the sidewalls of the feature; and
25 a layer of a second dielectric material deposited on the conductive material,
wherein the second dielectric material is oxidized by exposure to oxidizing species and ultraviolet light.

10. The memory cell of claim 9 further comprising a second conductive material formed on the oxidized second dielectric material.

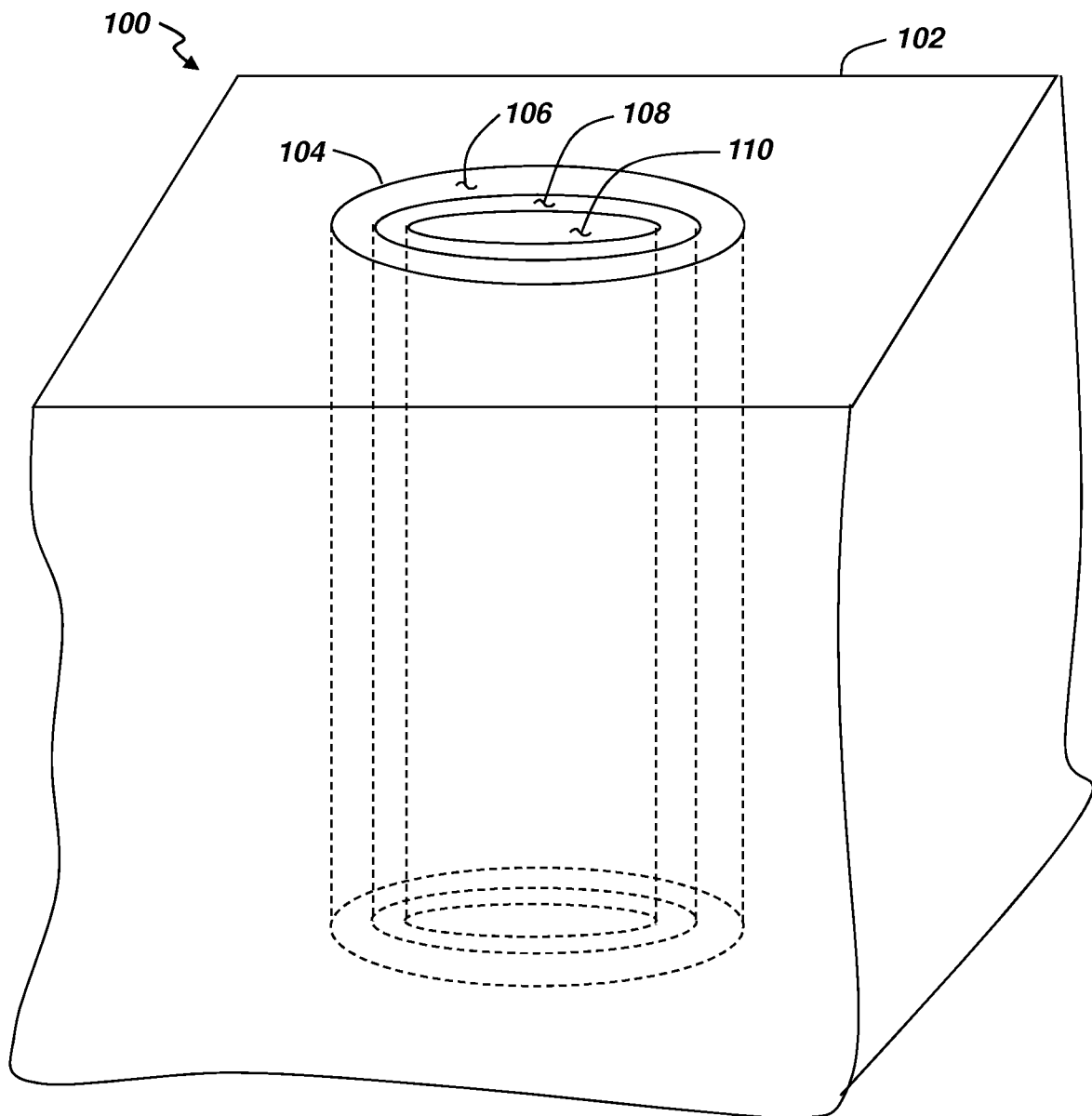
5 11. The memory cell of claim 9 wherein the first dielectric material includes at least one of silicon dioxide, silicon nitride, and silicon oxynitride.

12. The memory cell of claim 9 wherein the first conductive
10 material includes at least one of TiN, TaN, and WN_2 .

13. The memory cell of claim 9 wherein the second dielectric material includes at least one of Ta_2O_5 , Al_2O_3 , ZnO, HfO_2 , and ZrO_2 .

15 14. The memory cell of claim 9 wherein the second dielectric material is oxidized by diffusing ozone into the second dielectric material and then pulsing the diffused ozone with the ultraviolet light to break the ozone into oxygen radicals.

20 15. The memory cell of claim 9 wherein the materials are kept at a temperature of less than 300 degrees C.

**FIG. 1**

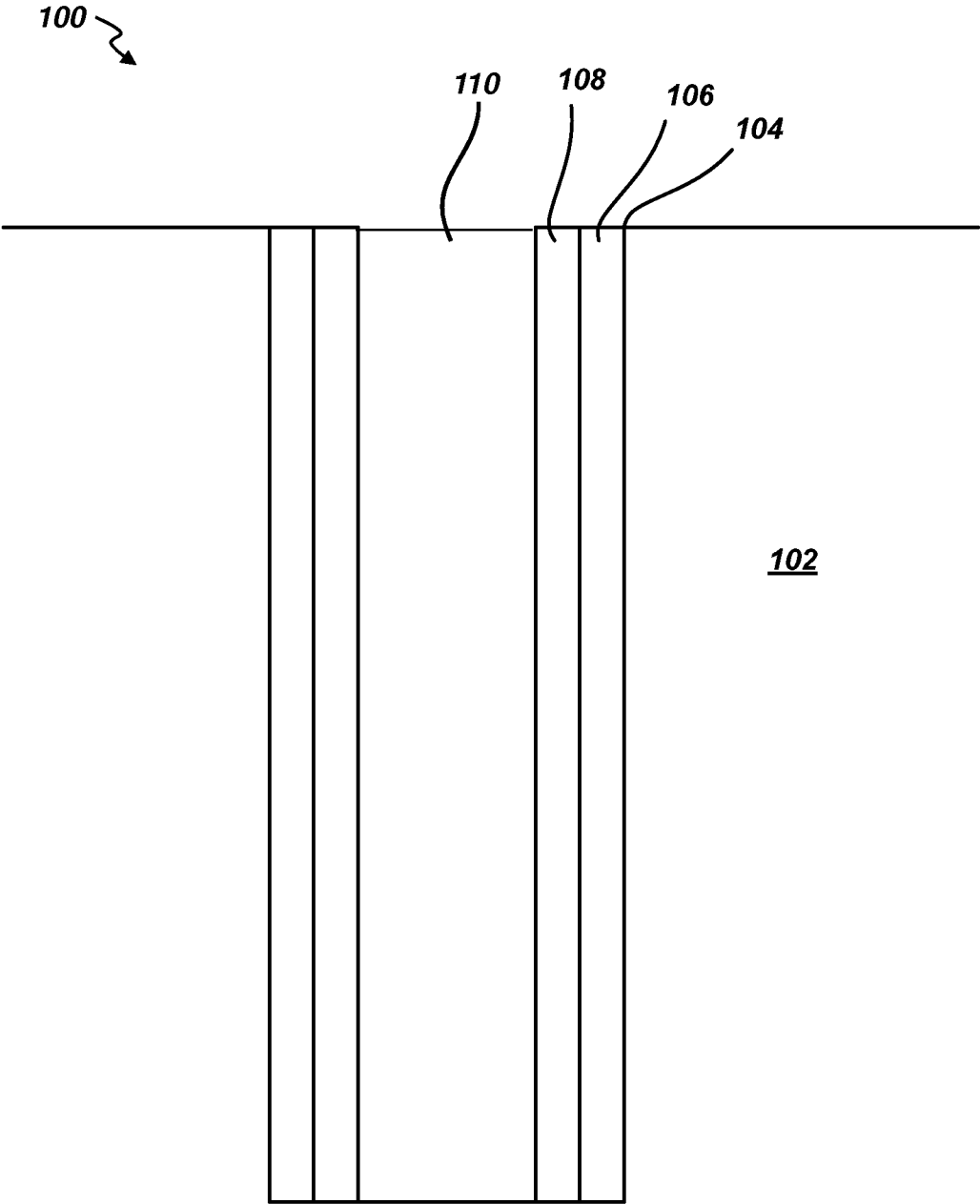
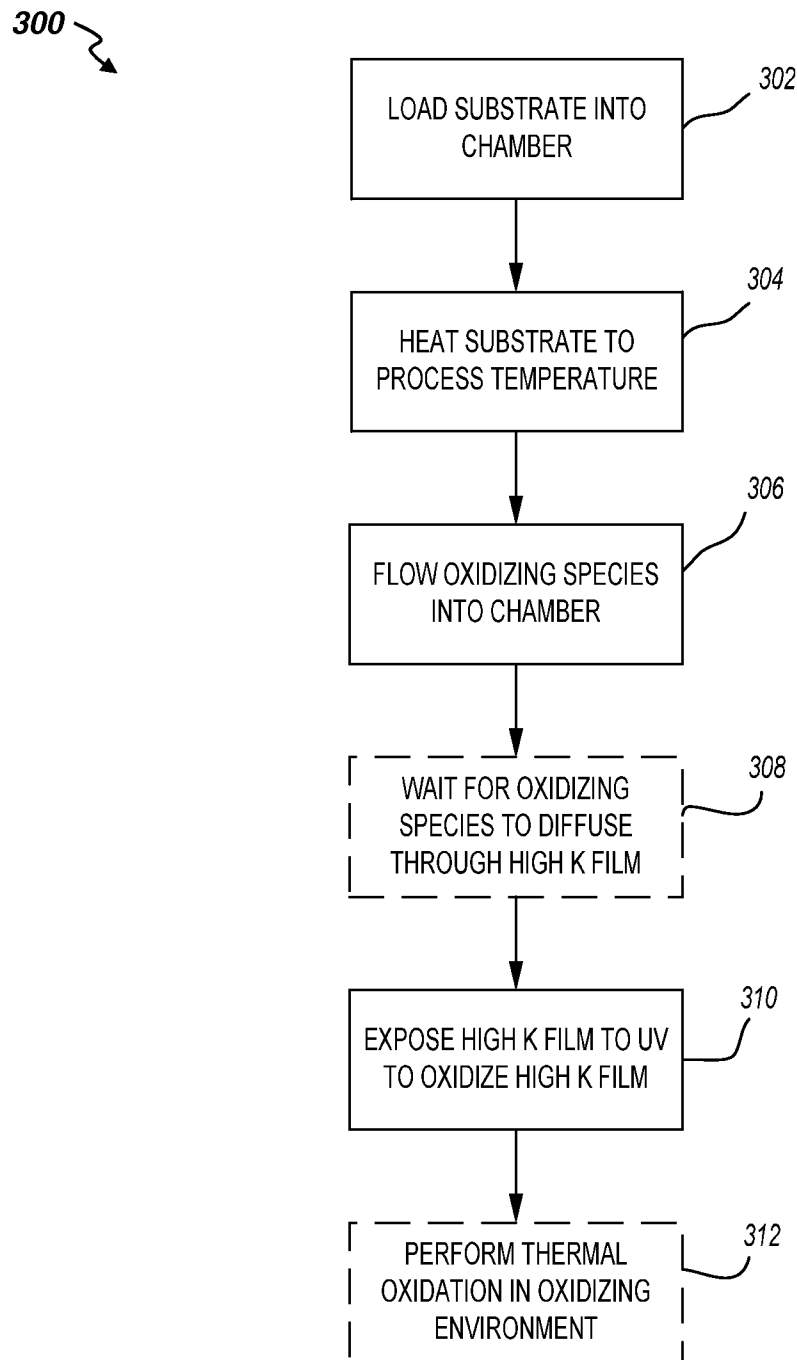
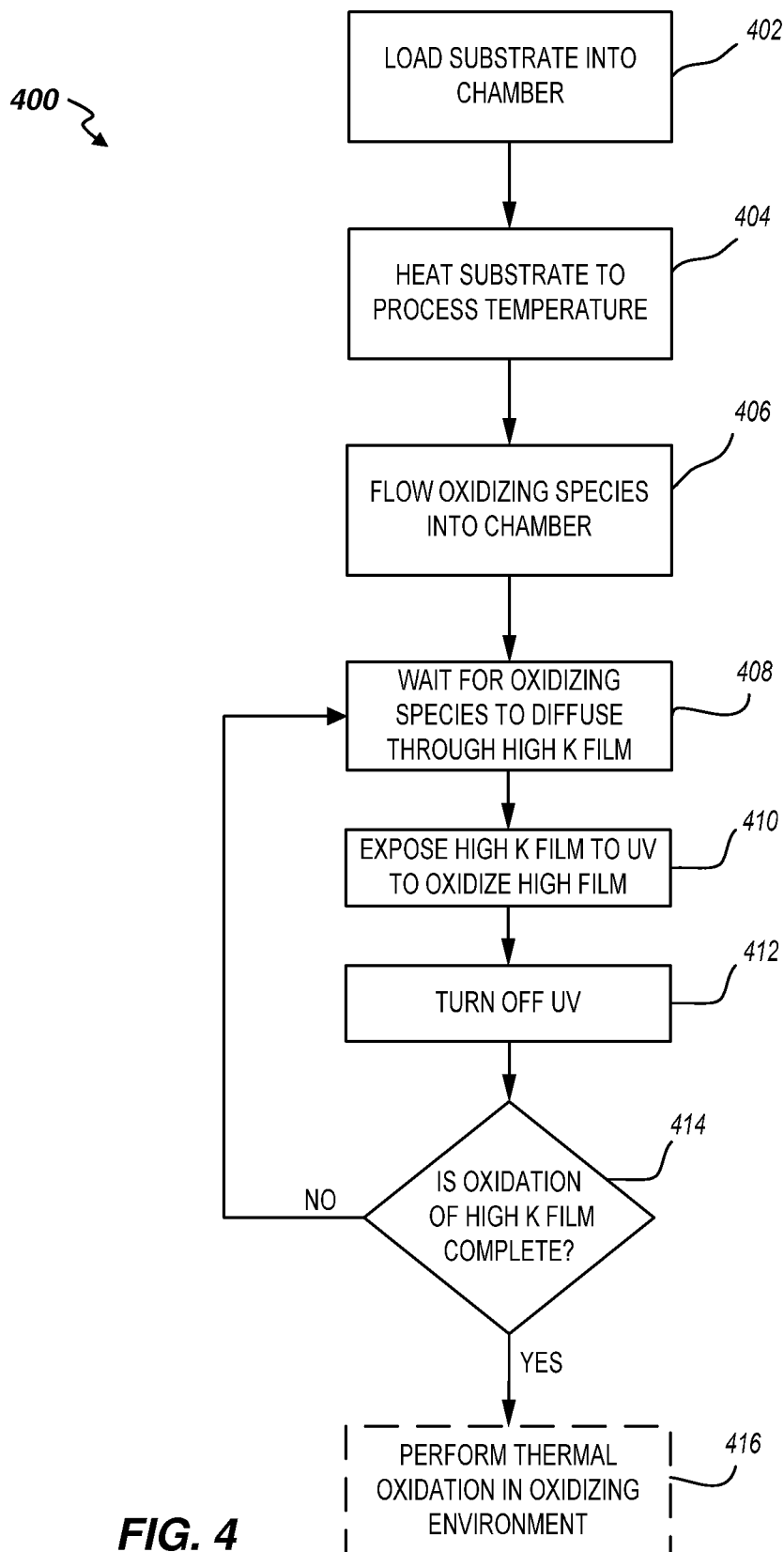
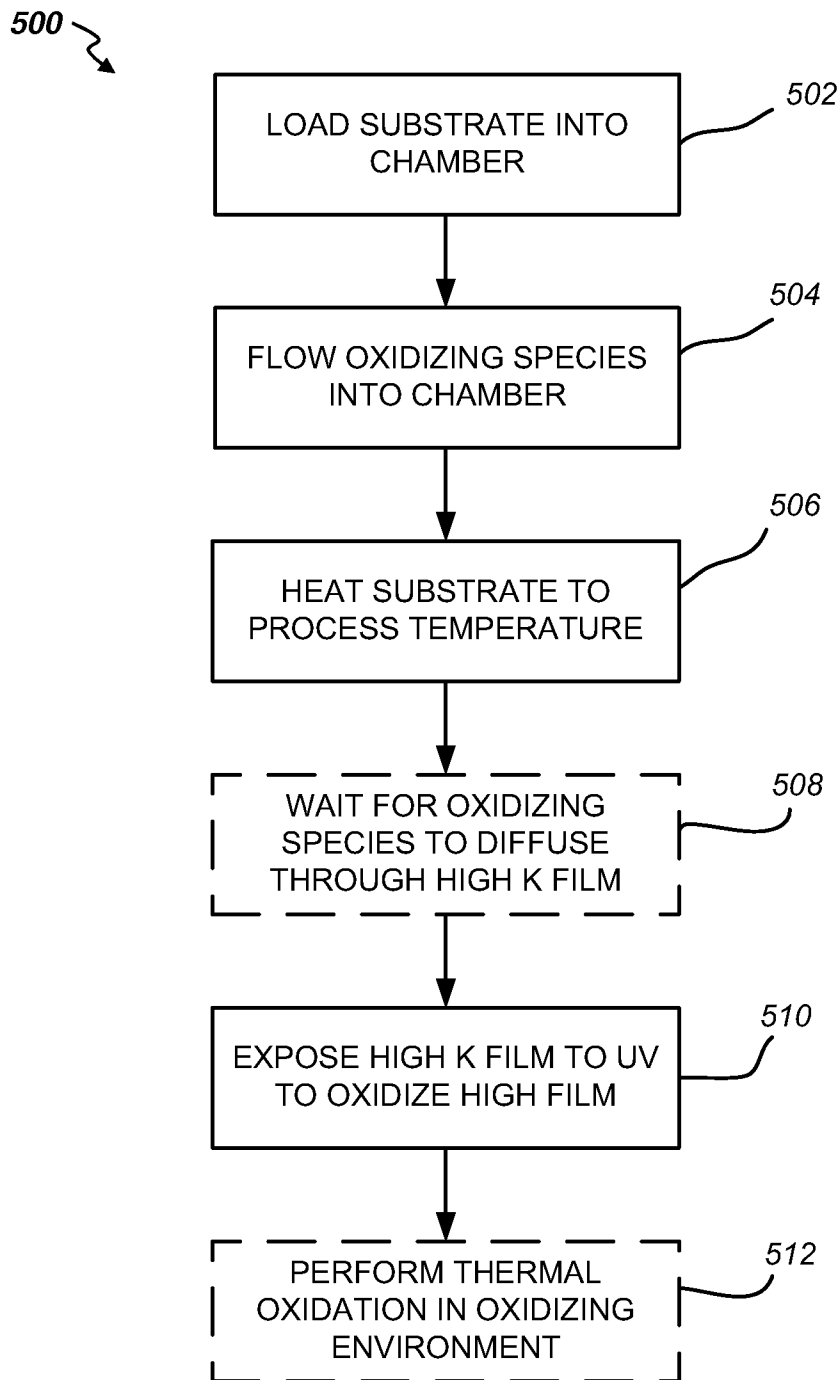


FIG. 2

**FIG. 3**

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**FIG. 4**

**FIG. 5**