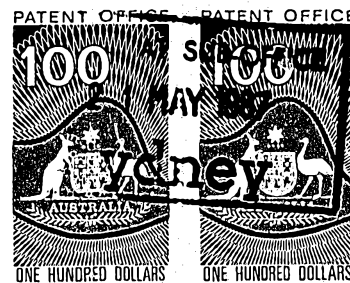




59766
APPLICATION ACCEPTED AND AMENDMENTS
14.3.87
COMMONWEALTH OF AUSTRALIA
Patents Act 1952



APPLICATION FOR A STANDARD PATENT

We, COMMONWEALTH OF AUSTRALIA, care of the Department of Science and Technology, Benjamin Offices, Belconnen Town Centre Australian Capital Territory, Australia, hereby apply for the grant of a standard patent for an invention entitled:

"COCHLEAR IMPLANT SYSTEM WITH PSYCHOPHYSICAL TESTING OR PROGRAMMING WITH MAPPED PATIENT RESPONSES PROVIDED TO ENCODER"

which is described in the accompanying complete specification.

This application is made by the virtue of Section 51

Number of original application: 26,683/84
filed 10.04.84

Person by whom application was made: COMMONWEALTH OF AUSTRALIA

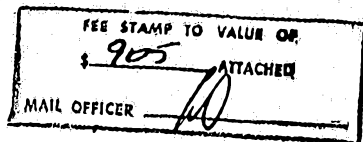
Our address for service is:

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21 MAY 1987
Sydney

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Dated this 19th day of May, 1987



COMMONWEALTH OF AUSTRALIA
by their Patent Attorneys
~~HALFORD & MAXWELL:~~

To: Commissioner of Patents
File: C 84 188



COMMONWEALTH OF AUSTRALIA

Patents Act 1952

DECLARATION IN SUPPORT OF AN APPLICATION
FOR A PATENT OR PATENT OF ADDITION

(1) Here
insert (in
full) Name
of Company

In support of the Application made by ⁽¹⁾ COMMONWEALTH OF AUSTRALIA

(2) Here
insert Title
of Invention.

for a patent for an invention entitled: ⁽²⁾ COCHLEAR IMPLANT
SYSTEM WITH PSYCHOPHYSICAL TESTING OR PROGRAMMING WITH
.....
.....MAPPED PATIENT RESPONSES PROVIDED TO ENCODER.....
.....

(3) Here
insert full
Name and
Address of
Company
Official
authorised
to make
declaration.

I, ⁽³⁾ BEVERLEY ANNE CLARKE, - ASSISTANT SECRETARY, DEPARTMENT
OF INDUSTRY, TECHNOLOGY AND COMMERCE.....
of 51 ALLARA STREET, CANBERRA CITY, ACT 2601.....

do solemnly and sincerely declare as follows:

1. I am authorized by ⁽¹⁾ COMMONWEALTH OF AUSTRALIA.....

(4) Here
insert (in
full) Name
and Address
of Actual
Inventor or
Inventors.

.....the applicant
for the patent.....to make this declaration on its behalf.

2. ⁽⁴⁾ PETER A. CROSBY, CHRISTOPHER N. DALY,

JAMES F. PATRICK, DAVID K. MONEY, PETER M. SELIGMAN.....
JANUSZ A. KUZMA.....

addresses on back hereof.....

is/are the actual inventor(s) of the invention, and the facts upon which ⁽¹⁾.....

COMMONWEALTH OF AUSTRALIA.....

is entitled to make the application are as follows:—

The said ⁽¹⁾ COMMONWEALTH OF AUSTRALIA.....

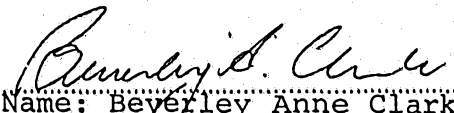
is the assignee of the said ⁽⁵⁾ PETER A. CROSBY, CHRISTOPHER N. DALY.....

JAMES F. PATRICK, DAVID K. MONEY, PETER M. SELIGMAN.....

DECLARED at CANBERRA & JANUSZ A. KUZMA

this TWENTY-FIFTH.....day of JANUARY.....1989.

(6) Signature.

⁽⁶⁾ 
Name: Beverley Anne Clarke
Position: Asst. Secretary

To:

THE COMMISSIONER OF PATENTS.

(12) PATENT ABRIDGMENT **(11) Document No. AU-B-73251/87**
(19) AUSTRALIAN PATENT OFFICE **(10) Acceptance No. 597661**

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COCHLEAR IMPLANT SYSTEM WITH PSYCHOPHYSICAL TESTING OR
PROGRAMMING WITH MAPPED PATIENT RESPONSES PROVIDED TO ENCODER
- International Patent Classification(s)
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483806 11.04.83 US UNITED STATES OF AMERICA
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- (62) Related to Division(s) : 26683/84
- (71) Applicant(s)
COMMONWEALTH OF AUSTRALIA
- (72) Inventor(s)
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JAMES F. PATRICK; PETER M. SELIGMAN
- (74) Attorney or Agent
PETER MAXWELL & ASSOC. PARRAMATTA
- (56) Prior Art Documents
WO 02767/80
EP 54418
US 3751605

(57) Claim

1. A cochlear implant system having a speech processor located external to a patient's body, said speech processor including a configurable sound-to-stimulation encoding means, a body-implantable receiver-stimulator for receiving transmitted electrical signals from said encoding means and an electrode array implantable in the cochlea of a patient for conducting electrical signals from said receiver-stimulator means to said cochlea characterized by:-

- i) means for performing psychophysical testing on the auditory nervous system of the patient while said receiver-stimulator is receiving said

electrical signals,

- ii) means, using the results of said testing, for preparing data in a map representing a patient stimulation strategy,
- iii) means for converting audio signal information to electrical signals in said sound-to-stimulation encoding means for that patient, and,
- iv) means for erasably programming and storing said mapped data in said encoding means, such that stimulation parameters for speech signals are optimized utilizing said stored data to enhance the ability of the patient to recognize speech signals.

13. A multichannel cochlear prosthesis system comprising:

- i) a patient implantable tissue stimulating multichannel electrode array,
- ii) a patient implantable multichannel stimulator connected to said array,
- iii) a patient externally worn sound-to-electrical signal stimulation encoding means said encoding means including memory means programmable after implantation of said electrode array and said stimulator in a patient,
- iv) means for programming said memory means based on the patient's auditory perceptions in response to various electrical stimulating pulse signals,
- v) means for transmitting electrical stimulation

signals representing speech parameters from said encoding means to said stimulator and to said array for stimulating tissue in accord with said programmed perceptions, and,

- vi) means for controlling said stimulator by said encoding means, such control including varieties of at least one or more of pulse rate, pulse amplitude, pulse duration, interval between phases of a biphasic current pulse, and selection of which two of any electrodes stimulus current is to be applied.



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Form 10

PATENTS ACT 1952

COMPLETE SPECIFICATION

(ORIGINAL)

FOR OFFICE USE

Short Title:

Int. Cl:

This document contains the amendments made under Section 49 and is correct for printing.

Application Number:

73251/87

Lodged:

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• Complete Specification—Lodged:

Accepted:

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Lapsed:

Published:

Priority: 11th April, 1983

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Related Art:

• • •

TO BE COMPLETED BY APPLICANT

Name of Applicant: THE COMMONWEALTH OF AUSTRALIA



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Complete Specification for the invention entitled:

"COCHLEAR IMPLANT SYSTEM WITH PSYCHOPHYSICAL TESTING OR PROGRAMMING WITH MAPPED PATIENT RESPONSES PROVIDED TO ENCODER"

The following statement is a full description of this invention, including the best method of performing it known to

This invention relates to a cochlear implant system for an auditory prosthesis and more particularly to such a system having psychophysical testing or programming with mapped patient responses being provided to the encoder of the system.

In many people who are profoundly deaf, the reason for deafness is absence of, or destruction of the hair cells in the cochlea which transduce acoustic signals into nerve impulses. These people are thus unable to derive any benefit from conventional hearing systems, no matter how loud the acoustic stimulus is made, because there is no way nerve impulses can be generated from sound in the normal manner.

The cochlear implant system seeks to bypass these hair cells in the cochlea by presenting electrical stimulation to the auditory nerve fibers directly, leading to the perception of sound in the brain. There have been many ways described in the past for achieving this object, including implantation of electrodes in the cochlea connected to the outside world via a cable and connector attached to the patient's skull; to sophisticated multi-channel devices communicating with an external computer via radio frequency power and data links.

In order to best understand the invention, it is necessary to be aware of some of the physiology and anatomy of human hearing, and have a knowledge of the characteristics of the speech signal. In addition, since the hearing sensations elicited by electrical stimulation are different from those produced by acoustic stimulation in a normal hearing person, it is necessary to discuss the psychophysics of electrical stimulation of the auditory system.

The Structure of the Cochlea

In a normal hearing person, sound impinges on the eardrum as illustrated in Fig. 1 and is transmitted via a system of bones called the ossicles which act as levers to provide amplification and acoustic impedance matching, to a piston, or membrane, called the oval window.

1 The cochlear chamber is about 35mm long when unrolled
2 and is divided along almost its whole length by a partition.
3 This partition is called the basilar membrane. The lower
4 chamber is called the scala tympani. An opening at the
5 remote end communicates between the upper and lower halves.
6 The cochlea is filled with a fluid with a viscosity of
7 about twice that of water. The scala tympani is provided
8 with another piston or membrane called the round window
9 which serves to take up the displacement of the fluid when
10 the oval window is moved.

11 When the oval window is acoustically driven via the
12 ossicles, the basilar membrane is displaced by the movement
13 of fluid in the cochlea. By the nature of its mechanical
14 properties, the basilar membrane vibrates maximally at the
15 remote end or apex for low frequencies and near the base
16 or oval window for high frequencies. The displacement of
17 the basilar membrane stimulates a collection of cells
18 called the hair cells situated in a special structure on
19 the basilar membrane. Movements of these hairs produce
20 electrical discharges in fibers of the VIIIth nerve or
21 auditory nerve. Thus the nerve fibers from hair cells
22 closest to the round window (the basal end of the cochlea)
23 convey information about high frequency sound, and fibers
24 more apical convey information about low frequency sound.
25 This is referred to as the tonotopic organization of nerve
26 fibers in the cochlea.

27 Hearing loss may be due to many causes, and is gener-
28 ally of two types. Conductive hearing loss is where the
29 normal mechanical pathways for sound to reach the hair
30 cells in the cochlea are impeded, for example by damage to
31 the ossicles. Conduction hearing loss may often be helped
32 by use of hearing aids, which amplify sound so that acoustic
33 information does reach the cochlea. Some types of conduc-
34 tive hearing loss are also amenable to alleviation by
35 surgical procedures.

36 Sensorineural hearing loss results from damage to the
37 hair cells or nerve fibers in the cochlea. For this type
38

1 of patient, conventional hearing aids will offer no improve-
2 ment, because the mechanisms for transducing sound energy
3 into nerve impulses have been damaged. It is by directly
4 stimulating the auditory nerve that this loss of function
5 can be partially restored.

6 In the system described herein, and in some other
7 cochlear implant systems in the prior art, the stimulating
8 electrode or electrodes is surgically placed in the scala
9 tympani, in close proximity to the basilar membrane as
10 shown in cross-section in Fig. 1B, and currents passed
11 between the electrodes result in neural stimulation in
12 groups of nerve fibers.

13 The human speech production system consists of a
14 number of resonant cavities, the oral and nasal cavities,
15 which may be excited by air passing through the glottis or
16 vocal chords, causing them to vibrate. The rate of vibra-
17 tion is heard as the pitch of the speaker's voice and
18 varies between about 100 and 400 Hz. The pitch of female
19 speakers is generally higher than that of male speakers.

20 It is the pitch of the human voice which gives a
21 sentence intonation, enabling the listener, for instance,
22 to be able to distinguish between a statement and a question,
23 segregate the sentences in continuous discourse and detect
24 which parts are particularly stressed. This together with
25 the amplitude of the signal provides the so-called prosodic
26 information.

27 Speech is produced by the speaker exciting the vocal
28 cords, and manipulating the acoustic cavities by movement
29 of the tongue, lips and jaw to produce different sounds.
30 Some sounds are produced with the vocal cords excited, and
31 these are called voiced sounds. Other sounds are produced
32 by other means, such as the passage of air between teeth
33 and tongue, to produce unvoiced sounds. Thus the sound
34 'z' is a voiced sound, whereas 's' is an unvoiced sound;
35 'b' is a voiced sound, and 'p' is an unvoiced sound, etc.

36 The speech signal can be analyzed in several ways.
37 One useful analysis technique is spectral analysis, whereby
38

1 the speech signal is analyzed in the frequency domain, and
2 a spectrum is considered of amplitude (and phase) versus
3 frequency. When the cavities to the speech production
4 system are excited, a number of spectral peaks are produced,
5 and the frequencies and relative amplitudes of these
6 spectral peaks also vary with time.

7 The number of spectral peaks ranges between about
8 three and five and these peaks are called FORMANTS. These
9 formants are numbered from the lowest frequency formant,
10 conventionally called F₁, to the highest frequency formants,
11 and the voice pitch is conventionally referred to as F₀.
12 Characteristic sounds of different vowels are produced by
13 the speaker changing the shape of the oral and nasal
14 cavities, which has the effect of changing the frequencies
15 and relative intensities of these formants.

16 In particular, it has been found that the second
17 formant (F₂) is important for conveying vowel information.
18 For example, the vowel sounds 'oo' and 'ee' may be produced
19 with identical voicing of the vocal cords, but will sound
20 different due to different second formant characteristics.

21 There is of course a variety of different sounds in
22 speech and their method of production is complex. For the
23 purpose of understanding the implant system however, it
24 is sufficient to remember that there are two main types of
25 sounds--voiced and unvoiced; and that the time course of
26 the frequencies and amplitudes of the formants carries
27 most of the intelligibility of the speech signal.

28 29 Psychophysics

30 The term Psychophysics is used here to refer to the
31 study of the perception elicited in patients by electrical
32 stimulation of the auditory nerve. For stimulation at
33 rates between 100 and 400 pulses per second, a noise is
34 perceived which changes pitch with stimulation rate. This
35 is such a distinct sensation that it is possible to convey
36 a melody to a patient by its variation.

37
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1 By stimulating the electrode at a rate proportional
2 to voice pitch (F_0), it is possible to convey prosodic
3 information to the patient. This idea is used by some
4 cochlear implant systems as the sole method of information
5 transmission, and may be performed with a single electrode.

6 It is more important to convey formant information to
7 the patient as this contains most of the intelligibility
8 of the speech signal. It has been discovered by psycho-
9 physical testing that just as an auditory signal which
10 stimulates the remote end of the cochlea produces a low
11 frequency sensation and a signal which stimulates the near
12 end produces a high frequency sensation, a similar phenom-
13 enon will be observed with electrical stimulation. The
14 perceptions elicited by electrical stimulation at different
15 positions inside the cochlea have been reported by the
16 subjects as producing percepts which vary in "sharpness"
17 or "dullness", rather than pitch as such. However, the
18 difference in frequency perceptions between electrodes is
19 such that formant, or spectral information can be coded by
20 selection of electrode, or site of stimulation in the
21 cochlea.

22 It has been found by psychophysical testing that the
23 perceived loudness of sounds elicited by electrical stimu-
24 lation of the auditory nerve has a larger dynamic range
25 than the dynamic range of the stimulation itself. For
26 example, a 2 to 20dB dynamic range of electrical stimula-
27 tion may produce perceptions from threshold or barely
28 perceivable, to threshold of pain. In normal hearing
29 people the dynamic range of sound perception is in the
30 order of 100dB.

31 It has also been discovered through psychophysical
32 testing that the pitch of sound perceptions due to elec-
33 trical stimulation is also dependent upon frequency of
34 stimulation, but the perceived pitch is not the same as
35 the stimulation frequency. In particular, the highest
36 pitch able to be perceived through the mechanism of changing
37 stimulation rate alone is in the order of 1 kHz, and
38

1 stimulation at rates above this maximum level will not
2 produce any increase in frequency or pitch of the
3 perceived sound. In addition, for electrical stimulation
4 within the cochlea, the perceived pitch depends upon
5 electrode position. In multiple electrode systems, the
6 perceptions due to stimulation at one electrode are not
7 independent of the perceptions due to simultaneous stimulation
8 of nearby electrodes. Also, the perceptual qualities of
9 pitch, 'sharpness', and loudness are not independently
10 variable with stimulation rate, electrode position, and
11 stimulation amplitude.

12 Some systems of cochlear implants in the prior art
13 are arranged to stimulate a number of electrodes simul-
14 taneously in proportion to the energy in specific frequency
15 bands, but this is done without reference to the perceptions
16 due to stimulus current in nearby stimulating electrodes.
17 The result is that there is interaction between the
18 channels and the loudness is affected by this.

19
20 Prior Art

21 A number of attempts have been made to provide useful
22 hearing through electrical stimulation of auditory nerve
23 fibers, using electrodes placed inside or adjacent to some
24 part of the cochlear structure. Systems using a single
25 pair of electrodes have been proposed by House (Ann. Otol.
26 Rhinol. Laryngol. 85, Supp. 27, 1976), Michelson (U.S.
27 patent 3,751,605) and Bartz (U.S. patent 3,752,939).

28 In each of these systems an external speech
29 processing unit converts the acoustic input into a signal
30 suitable for transmission through the skin to an implanted
31 receiver/ stimulator unit. These devices apply a
32 continuously varying stimulus to the pair of electrodes,
33 stimulating at least part of the population of auditory
34 nerve fibers, and thus producing a hearing sensation.

35 The stimulus signal generated from a given acoustic
36 input is different for each of these systems, and while
37 some degree of effectiveness has been demonstrated for
38 each, performance has varied widely across systems and

also for each system between patients. Because the design of these systems has evolved empirically, and has not been based on detailed psychophysical observations, it has not been possible to determine the cause of this variability. Consequently, it has not been possible to reduce it.

An alternative approach has been to utilize the tonotopic organization of the cochlea to stimulate groups of nerve fibers depending on the frequency spectrum of the acoustic signal. Systems using this technique have been proposed by Ricard (U.S. Patent 4,207,441), Hochmair (Med & Biol Eng. & Comput., 1981, 19, 141-148), Doyle (U.S. Patent 3,449,753), and Kissiah (U.S. Patent 4,063,048).

The system described by Kissiah uses a set of analog filters to separate the acoustic signal into a number of frequency components, each having a predetermined frequency range within the audio spectrum. These analog signals are converted into digital pulse signals having a pulse rate equal to the frequency of the analog signal they represent, and the digital signals are used to stimulate the portion of the auditory nerve normally carrying the information in the same frequency range. Stimulation is accomplished by placing an array of spaced electrodes inside the cochlea.

This system utilizes electrical stimulation at rates up to the limit of normal acoustic frequency range, say 10 kHz, and independent operation of each electrode. Since the maximum rate of firing of any nerve fiber is limited by physiological mechanisms to one or two kHz, and there is little perceptual difference for electrical pulse rates above 800 kHz it may be inappropriate to stimulate at the rates suggested. No consideration has been given to the interaction between the stimulus currents generated by different electrodes which in our experience may cause considerable, uncontrolled loudness variations, depending on the relative timing of stimulus presentations. Also, this system incorporates a percutaneous connector which has with it the associated risk of infection.

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1 The system proposed by Doyle limits the stimulation
2 rate for any group of fibers to a rate which would allow
3 any fiber to respond to sequential stimuli. It utilizes a
4 plurality of transmission channels, with each-channel
5 sending a simple composite power/data signal to a bipolar
6 pair of electrodes. Voltage source stimulation is used in
7 a time multiplexed fashion similar to that subsequently
8 used by Ricard and described below, and similar uncontrolled
9 loudness variations will occur with the suggested independent
10 stimulation of neighbouring pairs of electrodes. Further,
11 the requirement for a number of transmission links equal
12 to the number of electrode pairs prohibits the use of this
13 type of system for more than a few electrodes.

14 The system proposed by Ricard again utilizes a filter
15 bank to analyze the acoustic signal and a single radio
16 frequency link to transfer both power and data to the
17 implanted receiver/stimulator, which presents a time-
18 multiplexed output to sets of electrodes implanted in the
19 cochlea. Monophasic voltage stimuli are used, with one
20 electrode at a time being connected to a voltage source
21 while the rest are connected to a common ground line. An
22 attempt is made to isolate stimulus currents from one
23 another by placing small pieces of silastic inside the
24 scala, between electrodes. Since monophasic voltage
25 stimuli are used, and the electrodes are returned to the
26 common reference level after presentation of each stimulus,
27 the capacitive nature of the electrode/ electrolyte inter-
28 face will cause some current to flow for a few hundred
29 microseconds after the driving voltage has been returned
30 to zero. This will reduce the net transfer of charge (and
31 thus electrode corrosion) but this charge recovery phase
32 is now temporally overlapped with the following stimulus
33 or stimuli. Any spatial overlap of these stimuli would
34 then cause uncontrolled loudness variations.

35 The system described by Forster et al. (U.S. Patent
36 4,267,410) utilizes biphasic current stimuli of predeter-
37 mined duration, providing good temporal control of both
38

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1 stimulating and recovery phases. However, the use of
2 fixed pulse duration prohibits the variation of this
3 parameter which may be required by physiological variations
4 between patients. Further, the data transmission system
5 described in this system severely limits the number of
6 pulse rates available for constant rate stimulation.

7 A common feature of all implanted receiver/stimulator
8 units has been that the energy needed to power the implanted
9 electronics (if any) and deliver the stimulus signal has
10 been derived from an external power source, either directly
11 from the data signal or from a separate power signal.

12 The simplest and thus more reliable systems are those
13 utilizing a single link, such as those described by Ricard
14 and Hochmair. The Hochmair multichannel system uses FM
15 data coding to transfer energy continuously, even during
16 long intervals between stimuli. The energy efficiency of
17 this approach is inherently less than that of approaches
18 which transfer energy only when stimulation is imminent or
19 actually in progress such as the Ricard system, and the
20 system described herein.

21 In the Ricard system a start pulse providing enough
22 energy to power the electronics is sent at the start of
23 every stimulation sequence. Each electrode is stimulated
24 only once during each sequence, so for a series of stimuli
25 to any single electrode the number of start bursts is
26 equal to the number of stimuli. An improvement to this
27 technique is to eliminate the need for the start pulse by
28 minimizing the energy consumption of the electronics
29 between stimuli (when no energy being received), allowing
30 the electronics to still be in an active or powered state
31 when the second and subsequent stimulus data sequences are
32 received. This concept is utilized in the invention
33 described herein.

34 It is necessary to be able to configure the cochlear
35 implant system to take account of each individual patient's
36 psychophysical responses to stimulation. The system by
37 Merzenich uses an interconnection pad between the implanted
38

stimulator unit and the electrode array which enables him to select the electrode configuration to suit the patient's responses. This is done in a second surgical procedure after implantation. Other systems may use several implanted electrodes, and after testing, a choice is made of which electrode or electrodes are to be stimulated as a single channel.

According to the invention there is provided a cochlear implant system having a speech processor located external to a patient's body, said speech processor including a configureable sound-to-stimulation encoding means, a body-implantable receiver-stimulator for receiving transmitted electrical signals from said encoding means and an electrode array implantable in the cochlea of a patient for conducting electrical signals from said receiver-stimulator means to said cochlea characterized by:-

- (i) means for performing psychophysical testing on the auditory nervous system of the patient while said receiver-stimulator is receiving said electrical signals,
- (ii) means, using the results of said testing, for preparing data in a map representing a patient stimulation strategy,
- (iii) means for converting audio signal information to electrical signals in said sound-to-stimulation encoding means for that patient, and,
- (iv) means for erasably programming and storing said



mapped data in said encoding means, such that stimulation parameters for speech signals are optimized utilizing said stored data to enhance the ability of the patient to recognize speech signals.

5

In order that the invention may be more readily understood and put into practical effect reference will now be made to the accompanying drawings in which:-

Fig. 1A and 1B are interior views of the anatomy of the human ear and a cross-section of the cochlea, respectively,

10

Fig. 2 is a block diagram of an overall cochlear implant system,

Fig. 3 is a pictorial view of the components of the implant system, including the implantable parts, and the parts worn by the patient,

Fig. 4 is the biphasic current waveform utilized in this invention,

Fig. 5 is a block diagram of the body (ear) implantable receiver/stimulator,

Fig. 6 is the electrode switching circuit for bipolar stimulus current generation,

Fig. 7 is a block diagram of the distributed ground stimulus current generation,



Fig. 8 illustrates the power/data signal format
from the speech processor,

Fig. 9 is a block diagram of the implanted receiver/
stimulator digital circuit,

5 Fig. 10 is a block diagram of the implanted receiver/
stimulator analog circuit,

Fig. 11 is the burst detector and clock extraction
circuit,

Fig. 12 is the reference current generator,

Fig. 13 is a programmable current generator,

Fig. 14 shows the programmable current generator
timing waveforms,

Fig. 15 shows the output circuit (a) and output
timing waveforms (b) of the output mirror,

15 Fig. 16 is the output switching circuit of the
receiver/stimulator,

Fig. 17 is a block diagram of the speech processor,

Fig. 18 is a block diagram of the speech processor
front end,

20 Fig. 19 is a block diagram of the speech processor
encoder,

Fig. 20 is an address map for the programmable read
only memory,

25 Fig. 21 is a circuit diagram of the speech processor
output stage,

Fig. 22 is a block diagram of the speech processor interface unit,

Fig. 23a is a circuit diagram of the current trim network and Fig. 23b illustrates the nominal transfer function as a function of the external trim connections, and,

Fig. 24 illustrates the state and output timing of the output switching circuit.

The Cochlear Implant System

The cochlear implant system shown in Fig. 2 comprises several components. An Electrode Array 1 is implanted into the cochlea. In the system described, the electrode comprises a number of rings or bands of platinum moulded with a flexible silastic carrier. There are 32 bands of platinum in total, and the distal 22 bands are active electrodes, and have connecting wires welded to them. The proximal 10 electrode bands are used for stiffening, and to act as an aid to surgical insertion. In a typical array, the electrode rings are about 0.05mm in thickness with a width of 0.3mm, and have outside diameters ranging from 0.6mm at the proximal end to about 0.4mm diameter at the distal end. The diameter of the rings changes smoothly so that the array is tapered over the distal 10mm or so. The rings are spaced on 0.75mm centers, over the distal 25mm of the electrode array, and all of the exposed outside area of the rings is used as an active

electrode area. Silastic material may be MDX4-4210, manufactured by Dow Corning. The 22 electrode wires pass in a cable 2 from the electrode to the Receiver - Stimulator Unit (RSU) 3 via a connector 4.

5 The system described is not limited to the use of this design of electrode array, and a number of alternative electrode designs as have been described in the prior art could be used, provided the wires from the active electrode sites could be attached to the connector. Reference may be made to our co-pending Australian Patent Application No. 10 13,595/83 for details of the connector.

15 The RSU receives information and power from an external source through a tuned receiving coil 5 attached to the RSU and just beneath the skin. The RSU also provides electrical stimulating pulses to the electrode. The electrical connection between the electrode and the RSU is via a connector to allow the RSU to be replaced without requiring 20 explantation of the electrode.

25 The power, and data on which electrode to stimulate, and with what intensity, is transmitted across the skin using an inductive link 6 operating at radio frequencies, from an external Wearable Speech Processor (WSP) 7. In normal operation, the WSP picks up acoustic stimuli from a microphone 8 conveniently worn, and extracts from the signal, information which is used to determine stimulation electrode,

rate and amplitude.

Because each patient's response to electrical stimulation is different, it is necessary to configure each patient's WSP to his or her own requirements. Thus the WSP has an Eraseable Programmable Read Only Memory (EPROM) which is programmed to suit each patient.

The patient's response to electrical stimulation is tested some short time after implantation of the RSU, using the patient's WSP, and the results of these tests are used to set up the WSP for the patient's own particular requirements. This is done by connecting the WSP, via a connector and cables 9 to an Interface Unit (IU) 10. The IU is itself connected via a cable and connector 11 to a general purpose computer referred to as a Diagnostic and Programming Unit (DPU) 12.

A pictorial representation of the system used by the patient is shown in Fig. 3. The electrode array 20 is flexible and fits the shape of the cochlea as it is inserted along the basilar membrane separating the scala tympani from the remainder of the cochlea. The electrode array is connected via a silastic-covered cable 21 to the RSU 22. As pointed out in our Australian Patent Application No. 13,595/83, this cable is specially designed to provide some stress relief to prevent wire fracture. The receiving coil for information and power is a single turn of multi-strand platinum wire 23 which is transformer coupled to the implanted electronics in the RSU.

1 An externally worn coil 24 is simply held against the
2 head over the site of RSU implant by (for example)
3 adhesive tape or a fixture, and is connected to the Speech
4 Processor 29 by a coaxial cable 26. A conventional
5 hearing aid microphone 27 is worn on the same ear as the
6 transmitting coil, and a microphone lead 28 is contained
7 in the same cable as the coil coaxial lead. Alternative
8 microphone configurations are possible, including a
9 microphone 33 mounted in the WSP case, or worn on a tie
10 clasp or attached to the clothing, or attached to the
11 fixture holding the transmitting coil.

12 The cable is attached to the WSP by a demountable
13 connector 32. The WSP is powered by conventionally avail-
14 able batteries (eg: 3 AA size cells shown as 30). A
15 facility exists for plugging in external signal sources
16 31, such as a television, radio, or high quality
17 microphone to be handed around in a social situation.

18 Each component of the cochlear implant system will be
19 discussed in more detail in the following sections:

20
21 The Speech Processing Strategy

22 The main aim of this invention is to provide improved
23 speech communication to those people suffering from
24 profound hearing loss, and thus the emphasis in design has
25 been to optimize stimulation parameters for speech
26 signals. However, it is also important to be able to
27 convey environmental sounds, for example telephones,
28 doors, warning sirens, doorbells, etc., which form part of
29 a persons life. We have found that the approaches which
30 we have taken, although emphasizing speech communication,
31 also enable good awareness of environmental sounds, and we
32 feel that there is no loss of effectiveness in perception
33 of environmental sounds by this approach.

34 It is believed by those skilled in the art that it is
35 the second formant which carries most of the
36 intelligibility of the speech signal. This fact can be
37 demonstrated by high passing filtering a passage of speech
38 at 1 kHz. The result is as intelligible as the original

1 signal. Thus whilst the 1st formant contains much of the
2 naturalness of the signal, it contributes little to intelli-
3 gibility.

4 It may also be observed that the 3rd and higher
5 formants do not carry as much information as the 2nd.
6 Thus in view of the limitations of knowledge on the inter-
7 action between electrodes when a number of electrodes are
8 stimulated simultaneously, at the present time the most
9 effective method of stimulation has been found to be to
10 code the second formant on an appropriate electrode or
11 site in the cochlea to provide the most important formant
12 information. The amplitude of stimulation is derived from
13 the amplitude of the second formant.

14 The system described also provides prosodic
15 information in the form of pulse rate. However, whereas
16 other systems stimulate at the voice pitch rate, this
17 system compresses the stimulation rate to the range 100 to
18 250 Hz, the range in which the greatest pitch discrimination
19 from stimulation pulse rate is achieved.

20 An additional factor is that only the top 10 to 20 dB
21 of current acoustic stimulus level is used to determine
22 stimulus amplitude. That is, instead of compressing the
23 entire acoustic loudness range into the small range of
24 electrical stimulation available, only the top part is
25 used. In fact, the amplitude of the signal is internally
26 represented by a 5 bit binary code, which provides only 25
27 dB of dynamic range.

28 In summary, the speech processing strategy is:

- 29 1. The dominant spectral peak in the range of about
30 300 Hz to about 4 kHz is used to encode electrode
31 position.
- 32 2. The amplitude of the dominant spectral peak used
33 to encode electrode position is used to determine
34 stimulation amplitude.
- 35 3. Voice Pitch (F_0) is compressed and used to
36 determine stimulation rate.

37 For unvoiced sounds, and environmental sounds, the
38 system will still generate stimuli, but the stimulation

1 rate and electrode position will be determined by the
2 exact nature of the acoustic signal. For example, for
3 sibilant consonants ('s'), the stimulation rate will be
4 fairly fast, but not constant, and the electrode stimulated
5 will be one which elicits a high frequency percept.

6 A second alternative speech processing strategy has
7 also been found to be useful in some patients, and we have
8 discovered that it is advantageous to be able to offer a
9 choice of strategies to patients. The second strategy is
10 similar to the one mentioned above in that electrode
11 position is encoded from second formant frequency. However,
12 the stimulation rate is at the F1 or first formant frequency,
13 and the stimulation amplitude is determined from the value
14 of the peak of the acoustic signal at the time of the F1
15 peak. This has the advantage that the stimulation rate is
16 faster, and elicits more natural sounding speech perceptions
17 in some patients. In addition, since the F1 signal is
18 amplitude modulated and temporally patterned at the Fo
19 rate, the patients also perceive the Fo or voice pitch
20 which is useful for conveying prosodic information. The
21 two alternative strategies and the method for generating
22 them are later further discussed.

23 Another speech processing strategy we have considered
24 is to stimulate the patient at the rate of F1 extracted
25 from an incoming speech signal, but to pattern the stimu-
26 lation such that the stimuli are gated at the Fo rate.

27 The cochlear implant system described herein is not
28 limited to any one particular speech processing strategy.
29 Indeed, it is one of the strengths of the invention that
30 the implanted receiver unit is 'transparent' to the speech
31 processing or sound encoding strategy adopted, and that
32 future developments in this field will be able to be
33 adapted without changes to the implant necessitating
34 further surgery to the patient.

35

36 The Electrical Stimulation Pulse

37 The pulse which is used to electrically stimulate the

38

1 cochlea is BIPHASIC, as shown in Fig. 4. That is, it
2 comprises a period of negative current stimulation, followed
3 by an equal period of positive current stimulation of
4 equal amplitude, the two periods (known as phases phi 1
5 and phi 2), separated by a short period of no stimulation.
6 Phi 1 and phi 2 may be in the range of 50 to 400 micro-
7 seconds (typically 200 microseconds), and the intervening
8 interval is typically about 50 microseconds. The amplitude
9 of phi 1 and phi 2, their durations, and the duration of
10 the intervening interval are determined by the information
11 decoded from the signal transmitted by the speech processor.
12 The actual values of these parameters will be set up on an
13 electrode by electrode basis, for each patient, as a
14 result of psychophysical testing of the patient, as will
15 be described. The reversal in polarity of phi 1 and phi 2
16 is important since it ensures that there is no net DC
17 component in the stimulus. This is important because long
18 term DC excitation might cause electrode corrosion, and
19 possible subsequent damage to the cochlea itself.

20 The questions of electrode electrochemistry and
21 charge balance are thought to be more important in cochlear
22 implants than in, say, cardiac pacemakers which are well
23 known in the art. This is because a cochlear stimulator
24 will be stimulating nerve fibers, whereas a cardiac pacemaker
25 is designed to stimulate cardiac muscle. It is thought
26 that nerve tissues may be more susceptible to damage due
27 to electrical stimulation, and thus the cochlear implant
28 system described herein has been designed with more strin-
29 gent safety factors than cardiac pacemakers.

30 The system is carefully designed so that the same
31 stimulus source is used for both stimulation phases. The
32 biphasic pulse is produced simply by reversal of the
33 connections to the electrodes. Thus, extremely good
34 charge symmetry is obtained resulting in a high level of
35 safety provided the duration of phi 1 and phi 2 are equal.
36 In other systems in the prior art, capacitors are used in
37 series with the electrodes to overcome the problem of
38

1 charge asymmetry. The need for capacitors in a cochlear
2 implant puts constraints on the minimum volume possible,
3 since one capacitor would be required for each electrode.
4 Thus, for a 22 channel stimulator, 22 capacitors would be
5 required, of typically 0.5 microfarad, 25 volt rating chip
6 ceramic capacitor.

7 The stimulation circuitry is configured as a constant
8 current source. This has the advantage compared to a
9 constant voltage source that if the electrode impedance
10 changes (as has often been observed) the delivered current
11 to the electrode will remain unaltered over a large range
12 of electrode impedances. The current may be varied from a
13 few microamps to 2 mA, allowing a very large range of
14 loudness percepts to be produced and large variations
15 between patients to be accommodated.

16 In addition, the system has the unique feature that
17 the stimulus currents as delivered to the cochlea are
18 known, as the system of generating the constant current
19 stimulus is very well characterized, and has been designed
20 to be substantially independent of many parameters (such
21 as transmitting coil position) over a wide range.

22 The stimulus generation circuitry in the RSU has been
23 designed to operate in one of two modes. The first mode
24 is referred to as 'multipolar' or 'common ground' stimula-
25 tion. In this mode, one electrode is selected to be the
26 'active' electrode, and all other electrodes operate as a
27 common current source. In phase 2, the connections are
28 reversed so that the 'active' electrode acts as the current
29 source and the common electrodes act as a current sink.
30 The choice of stimulus order is not determined by any
31 limitations or restrictions in the circuit design, and
32 either way may be chosen when implementing the circuit design.

33 The second mode is 'bipolar' stimulation. In this
34 mode, stimulation is between two selected electrodes, let
35 us say A and B. In phase 1, current is sourced by A, and
36 sunk by B. In phase 2, current is sourced by B, and sunk
37 by A, and no other electrodes play any part in stimulation.

38

1 The RSU is configured so that any pair of electrodes may
2 be selected for bipolar stimulation. Thus, there is great
3 flexibility in choice of stimulation strategy.

4 It should be understood that only these two particular
5 stimulation modes have been chosen. Other stimulation
6 modes are not excluded by the system described herein. For
7 example, a multipolar or distributed ground system could
8 be used where not all other electrodes act as a distributed
9 ground, and any electrode could be selected at any time to
10 be a current source, current sink, or inactive during
11 either stimulation phase with suitable modification of the
12 receiver-stimulator.

13 14 Testing and WSP Programming

15 Once the receiver/stimulator and electrode have been
16 surgically implanted, the patient is allowed to recover
17 for a short time, usually two weeks or so. After recovery,
18 a number of psychophysical tests are carried out to deter-
19 mine the sensitivity and sharpness of perceptions elicited
20 by stimulating the electrodes. This is done by an audi-
21 ologist using the Diagnostic and Programming Unit ("DPU"),
22 Interface Unit, and the patient's own speech processor.

23 The testing may be done entirely under control of the
24 audiologist, who can set a stimulus level, present the
25 stimulus, and question the patient on his perceptions.
26 Another technique we have found to be useful is to allow
27 the patient to determine his own threshold stimulus level
28 by adjusting a knob, slider or other patient operated
29 control which can set the stimulus level. Thus, the
30 patient can be instructed to set the stimulus level to
31 threshold, or comfortable, at any level as required. This
32 method allows much faster patient testing.

33 When the necessary psychophysical information has
34 been gathered, the audiologist uses the DPU to run a
35 program to compile a "MAP" which contains the information
36 needed for the speech processor to operate in its normal
37
38

1 mode. This map contains data on which electrode to stimu-
2 late, and at what amplitude, for various combinations of
3 F2 frequency and F2 amplitude, for the first speech processing
4 strategy mentioned.

5 Before committing the information to the speech
6 processor's memory however, the audiologist is able to
7 talk to the patient using the patient's own speech processor
8 via a temporary MAP stored in the DPU. It is possible to
9 make changes to the MAP until it is decided that the
10 information it contains will give the patient the best
11 possible performance. When this has been done, the DPU is
12 used to write the MAP into the speech processor's EPROM
13 (eraseable, programmable, read-only-memory). The speech
14 processor may then be unplugged from the DPU and operated
15 independently from it.

16 We have also developed a device which enables function-
17 ing of the external speech processor to be monitored.
18 This is essentially the electronics from an implantable
19 receiver stimulator to which simple circuits have been
20 added to reconvert the stimulus current outputs to an
21 audio signal. In practice, the monitoring is done by
22 placing the transmitter coil from the patient's WSP over
23 the testing or monitoring device and listening on a pair
24 of headphones. This is useful, as it quickly and easily
25 verifies proper functioning of all components of the
26 system external to the body, and we have found it to be an
27 aid in finding suspected problems with the apparatus.

28 The Cochlear Implant in Use

29 In use, the patient locates the coil unit and micro-
30 phone behind the ear in a position directly over the
31 implanted package. A distance of no greater than 10 mm
32 between the exterior and interior coils has been found to
33 be satisfactory. The speech processor may be placed in
34 TEST mode to deliver a constant stimulus to aid coil
35 positioning. Once the coil has been correctly positioned,
36 the speech processor may be placed in RUN and used in its
37 normal mode.
38

1 In RUN mode, if there is a period where the sound
2 level is relatively constant, the WSP (Wearable Speech
3 Processor) interprets this as background noise and disables
4 the generation of stimulus pulses. This has the effect of
5 reducing unnecessary and annoying stimulation due to
6 background noise. In some situations, however, the patient
7 may not find the background disturbing and may want to
8 hear all of the signal. In these cases the SQUELCH OVERRIDE
9 position may be used.

10 The WSP may be worn in a shirt pocket, holster or
11 some other fitment to the clothing. The microphone is
12 located on or near the ear and is of a highly directional
13 type to allow the patient to focus his attention towards a
14 particular speaker. Alternatively, a socket is provided
15 into which a hand held microphone, radio or TV input may
16 be plugged.

17
18 Receiver Stimulator (IMPLANT); General Description

19 A diagrammatic representation of the Receiver/
20 Stimulator, or cochlear implant, is shown in Fig. 5.
21 Power and data is from a single externally worn coil 40
22 approximately 30 mm in diameter, and wound from about 8 to
23 15 turns of insulated copper wire. This coil is driven
24 from the externally worn WSP, and the information to be
25 transmitted is encoded by the WSP from the incoming speech
26 signal.

27 The power is received by a single turn platinum coil
28 consisting of multiple strands of fine platinum wire wound
29 together, and about 28 mm in diameter 41. Multistrand
30 wire is used to improve the mechanical properties of the
31 coil, and to reduce losses due to 'skin effect', which is
32 significant in platinum at these frequencies. Both coils
33 are "air" cored, that is, they do not make use of magnetic
34 materials to function. This has an advantage over systems
35 which do, in terms of bulk and weight savings.

36 While the transmitter coil has on the order of eight
37 to fifteen turns to obtain the required inductance, the
38

receiver coil, located inside the body has only one turn. This has the advantages that the single turn can be made very robust, insulation problems are greatly reduced and any electrical leakage to the surrounding tissues will be kept to a minimum due to the very low voltage present on the coil. The low voltage also has the effect that possible electrochemical effects on the coil itself will be kept to a minimum.

Electrical connection to this platinum receiving coil is made via two hermetic and insulated ceramic feed-throughs 42 into a titanium case 43. The design and method of manufacture of the implant package and feed-throughs has been described in our co-pending Australian Patent Application No. 13,595/83.

The energy received by this coil is stepped up to a usable voltage level by a small transformer specially wound on a ferrite bead 44. The capacitor 45 in the secondary circuit of the transformer serves to tune the entire receiving circuit including the platinum coil and transformer. The transformer has a second function in that it isolates the receiver/stimulator circuit from the external coil. If this was not done, then the external coil could act as an extracochlear electrode, should there be an electrical current path to the surround tissue. Use of the transformer to electrically isolate the external coil allows the coil to be in direct contact with such tissue. The implantable package is encased in silicone rubber for protection, but electrical isolation and insulation does not depend upon the silicone rubber.

The voltage induced in the transformer secondary is rectified by a silicon diode 46, and filtered by a power supply filter capacitor 48. The performance of the power coupling system has been found to give adequate power transfer over a range of about 10 mm when the transmitter and receiver coils are coaxial and a degree of lateral misalignment is possible at distances less than this.

1 Some measure of overvoltage protection is provided by the
2 zener diode 47.

3 The coil/transformer is also connected through conductor
4 49 directly to the Receiver/Stimulator integrated circuit
5 50 for data recovery.

6 Because of the nature of the inductive coupling, it
7 is possible that pulses at the start of stimulus bursts
8 may be missed (i.i., not detected), and the inductive
9 system may store sufficient energy to produce a few extra
10 cycles of oscillation on the receiver side even when the
11 transmitter has ceased sending energy. These effects mean
12 that the number of detected pulses at the receiver may
13 differ from the number of transmitted pulses by one or two
14 pulses, and the information encoding strategy must take
15 this into account.

16 An electrode array with platinum rings 52 (of which
17 twenty-one are shown in Fig.5) is implanted surgically
18 into the scala tympani (Fig. 1B) in contact with the
19 basilar membrane of the cochlea. The rings are embedded
20 in a tapered carrier shaped to fit loosely in the decreasing
21 cross-section of the scala tympani, and is inserted, for
22 example, through an opening made in the round window
23 membrane. The distance that the electrode will be able to
24 be inserted will be different for each patient, and depends
25 upon each patient's physiology, anatomy and actiology of
26 deafness. Typically, the electrode array can be inserted
27 a distance of 17 to 22mm. The electrode array is connected
28 via a cable 53 to a connector 54 described in the previous
29 Kuzma application. Connector 54 makes connection to the
30 integrated circuit outputs 55 to provide stimulus currents
31 of controlled amplitude and duration to the selected
32 electrode.

33 In the embodiment described here, a separate rectifier
34 diode and zener diode are used to provide power and protection
35 for the implant. Alternatively, the rectifier diode and
36 overvoltage protection may be incorporated in the
37 receiver/stimulator IC itself. This has the obvious
38 advantage of requiring fewer separate components inside

1 the implant, with attendant possible reductions in size,
2 and improvements in reliability.

3
4 Stimulus Current Generation

5 The method of generating the biphasic current pulse
6 is illustrated diagrammatically in Fig. 6. In this diagram,
7 Vdd is the most positive voltage in the RSU, and Vss is
8 the most negative, or ground. Typically, Vdd is 11 Volts,
9 with respect to Vss which is taken as zero volts.

10 The stimulus generation circuitry comprises a con-
11 trollable current sink 60, where the current is determined
12 by the data transmitted to the implant. Each of 22 elec-
13 trodes (e.g., electrode number 3 shown as 61) may be
14 connected either to the Vdd supply potential by switches
15 labelled 'a' (e.g., 1a, 2a, 3a, etc.) or the controlled
16 current sink by switches labelled 'b' (e.g., 1b, 2b, 3b,
17 etc.). These switches are realized by enhancement mode
18 MOS transistors, and are described in more detail in a
19 later section. In A, no electrodes are connected to any
20 active circuitry, and thus electrode potentials are
21 'floating'. This is the condition when the implant is
22 unpowered.

23 In B, electrode number 2 (designated the Reference
24 electrode) is connected to the positive supply by switch
25 2a being closed, and electrode number 3 (designated the
26 Active electrode) is connected to the current sink by
27 switch 3b being closed. Thus, current flows out of elec-
28 trode 2, through the cochlear structures, and into elec-
29 trode 3. The voltage across the electrodes is dependent
30 upon the electrode impedances, but the amount of charge
31 delivered is precisely known. This is phase 1, or ϕ_1 .

32 In C, the connections are changed so that now elec-
33 trode 2 is connected to the current sink, and electrode 3
34 is connected to the positive supply, so that the direction
35 of current flow is exactly reversed. Since the current
36 sink is the same for both phases, the current is identical
37 in magnitude, but opposite in sign. Thus, if the time of
38

1 current flow is the same for both phases, then the amount
2 of charge delivered in phase 1 is equal to that in phases
3 2, and the net DC charge delivered is zero.

4 In the bipolar configuration, two electrodes only are
5 connected to the current sink and all other electrodes are
6 left open circuited. For simple bipolar operation adjacent
7 electrodes are selected as Active and Reference, although
8 any pair of electrodes may be selected as Active and
9 Reference. Thus, bipolar electrodes may be separated by
10 any desired distance, up to the length of the array. This
11 capability provides the advantage of selecting an alterna-
12 tive electrode if the adjacent electrode is unsuitable, or
13 the possibility of utilizing different stimulation stra-
14 tegies which may become identified in the future. In
15 addition, it is possible to select the Active electrode
16 numerically preceding, or following the Reference electrode
17 to allow the capability to control the order of current
18 flow in the electrodes.

19 The other mode of stimulation uses the 'common
20 ground' or 'multipolar' electrode configuration, and is
21 illustrated in Fig. 7. In this mode, one electrode is
22 stimulated against all the other electrodes which are
23 connected together. That is, in phase 1* (Fig. 7A), elec-
24 trode 2 is connected to the current sink, and all other
25 electrodes connected to the positive supply. Thus current
26 is sunk by electrode 2, and sourced by all other electrodes.
27 The current distribution between the common ground elec-
28 trodes is dependent upon a number of factors, including
29 (predominantly) electrode impedance.

30 In phase 2, the connections are changed, as shown in
31 Fig. 7B, so that the Active electrode is now connected to
32 Vdd, and all other electrodes are connected to the current
33 sink. Thus, the current in the Active electrode (electrode
34 2 in this case) is the controlled biphasic current pulse.
35 The other electrodes will have current waveforms which are
36 also biphasic, but of lower amplitude, since the return
37 current is shared between all other electrodes. A wider
38

1 spread of current in the cochlea is thus produced by this
2 configuration.

3 Between stimuli, and while the implant is powered,
4 all electrodes are connected to Vdd by closing the 'a'
5 switches and opening the 'b' switches in Fig. 6. Thus,
6 since all electrodes are shorted together, any residual
7 electrode polarization will be dissipated. Charge imbalance
8 could occur, for example, if ϕ_1 were not equal to ϕ_2 ,
9 such as might occur if a different number of data
10 pulses were received by the RSU for the ϕ_1 and ϕ_2
11 times due to coil coupling variations. If this were the
12 case, if the electrodes were not connected together between
13 stimuli, then the electrodes could end up polarized after
14 stimulation and, over a period of years, corrosion of
15 electrodes could occur. Corrosion of electrodes can
16 adversely affect the performance of the electrode, and may
17 result in toxic corrosion products remaining in the cochlea.
18 Polarization of all electrodes relative to the body is not
19 theoretically possible because the system is closed. It
20 can be seen that the maintenance of charge balance between
21 electrodes is also done without the need for output capaci-
22 tors, as mentioned previously.

23 The advantage of having a number of possible modes of
24 stimulation is that the most natural sounding percepts or
25 those having the highest intelligibility may be selected
26 once the patient has been implanted, rather than having to
27 make this decision beforehand.

28

29 Data Transmission Format

30 The power/data link comprises two magnetically linked
31 inductors, having a coefficient of coupling which depends
32 on the placement of the external primary coil relative to
33 the implanted secondary. Data is transmitted by controlling
34 the number of cycles of excitation to the transmitter
35 coil, which is heavily damped between bursts of pulses.
36 At the receiver, the data signal energy is used for stimu-
37 lation and also to provide power for the stimulator
38 electronics.

1 Digital data is encoded in the number of cycles in a
2 burst, while analog functions are directly controlled by
3 the duration of the burst. At the receiver, both the
4 number of pulses detected and the received burst length
5 depend on the coupling between coils. Tests using the
6 coil configuration described below have shown a difference
7 between transmitted and received pulse counts of one and
8 occasionally two pulses, depending on coil position.
9 Thus, a method of coding digital data is used which is
10 tolerant to error counts of at least three pulses.

11 At the transmitter, the number N which is to be
12 transmitted, is encoded as the burst length $8N + 4$ pulses,
13 while the receiver divides the received pulse count by
14 eight in its decoding process. This process is summarized
15 in the following table for the first few integers:

16	<u>Integer</u>	<u>Encoded Length</u>	<u>Decoder range (no error)</u>
17	0	4	1- 7
18	1	12	8-15
19	2	20	16-23
20	3	28	24-31
21	4	36	32-39

22 Fig. 8 shows the format of the data transmission to
23 the implant. Each time a stimulus is required, a data
24 frame comprising six bursts of pulses at a pulse rate of
25 2.5 MHz is transmitted. This frequency of transmission
26 was selected to allow presentation of stimuli in excess of
27 1 kHz, but it is understood that alternative embodiments
28 using different frequencies would be within the spirit of
29 this invention. The data coding described above provides
30 a robust, self-clocking data format without requiring
31 elaborate error checking. This is in contrast to other
32 systems in which the data is digitally encoded, where the
33 addition or loss of one or two pulses can produce a gross
34 error.

35 The choice of transmission frequency depends upon a
36 number of factors. Firstly, in order to inductively
37 couple power through body tissues for any reasonable
38

1 distance, low frequencies (preferably less than a few tens
2 of MHz) are desirable. At frequencies in excess of 10 MHz
3 or so, it is not possible to efficiently transfer the
4 power required. Low frequencies are typically used in
5 pacemaker prior art for coupling information (and sometimes
6 power) into a pacemaker encased in a metal package, and a
7 frequency of 16 KHz may be used. At frequencies greater
8 than about 50 KHz it is not possible to couple power into
9 a metal container with acceptable efficiency, and receiver
10 coils must be exterior to the container, as is used in this
11 embodiment. Alternative packaging technologies which did
12 not use metal would allow transfer of power to a receiver
13 coil inside the package at higher frequencies. For the
14 coding system described above, and for any other coding
15 system which could be use to transfer the equivalent
16 amount of information at the same rates, the minimum
17 frequency which could be used is determined by the infor-
18 mation transfer rate of the channel, at the times it is in
19 use (i.e., in order to deliver a stimulus pulse with
20 minimum delay). Finally, the technology which has been
21 chosen for other reasons is CMOS, and contemporary CMOS
22 technology has reliable operating frequencies of only a
23 few MHz. Of course, it would be possible to use a
24 modulation-demodulation scheme (such as FSK, FM or phase
25 encoding) at a higher frequency to transmit the information,
26 but this would merely add complexity for no advantage.

27 Sequential pulse bursts must be separated by at least
28 a sufficient interval to allow the 'end of burst' to be
29 detected: an interburst interval of 20 clock periods is
30 used, and the system is designed to be tolerant of interburst
31 intervals in excess of this time. This feature offers an
32 advantage in that a constant time interval may be allocated
33 for each stimulus frame, and thus there will be no jitter
34 between stimulus pulses on different electrodes. Otherwise,
35 encoded frames would be of different lengths, and thus the
36 stimulus time relative to the start of the frame would
37 vary with encoded data.

38

1 The stimulator circuit has six possible states (S0 to
2 S5), and the detection of the end of each burst is used to
3 change the circuit state to the next sequential state.
4 These states are also shown on Fig. 8. A uniquely defined
5 burst (the SYNC burst, for which $N=0$) is used to reset the
6 system.

8 Sync Burst

9 The SYNC burst is sent at the start of the frame to
10 reset the system state to state S0. The received burst
11 length must be less than 8 pulses, and a transmitted burst
12 length of 4 pulses is preferred.

14 Electrode Selection

15 The Active electrode is selected by the number decoded
16 from the second burst. For example, electrode 5 is selected
17 as the Active electrode if the number 5 is decoded from
18 the second burst.

20 Mode Select

21 There are two basic stimulation modes possible as
22 described, Bipolar and Multipolar. With bipolar stimula-
23 tion, however, the reference electrode may be selected
24 from any of the remaining, i.e., not active, electrodes.
25 The number decoded from the third, or mode select, burst
26 is used to define the reference electrode as detailed
27 herein. This number is described as the Stimulation Mode.
28 For multipolar stimulation where an Active electrode is
29 stimulated against all other electrodes connected together,
30 Mode = 1.

31 For bipolar stimulation the Reference electrode
32 number is equal to the Active electrode number + (Mode
33 -1). For example, if the Active electrode is 6 and Mode =
34 4, then the Reference electrode is $6+4-1 = 9$. With this
35 arrangement, it would appear that the Active electrode
36 number must always be lower than the Reference electrode.
37 If, however, the selected Reference electrode number

38

1 exceeds 22 then the actual Reference electrode will be
2 that selected minus 22, for example:

3 Active electrode = 10

4 Mode = 15

5 Reference electrode use = $(10+15 = 25) - 22 = 3$

6 Current Amplitude Control

7 The amplitude of the output current is determined by
8 the duration of the amplitude burst. This burst has a
9 minimum length of 16 pulses, which produces the maximum
10 stimulus current of about 1 mA, and the amplitude is
11 reduced in steps of about 3% for every 400 nS increase in
12 burst duration. This is the increase in burst duration
13 caused by adding a single cycle of that period in the
14 burst. The relationship between perceptual loudness and
15 stimulus amplitude is also logarithmic, allowing best use
16 of the current steps available.

17 This approach of reducing amplitude with increasing
18 burst length was preferred over the alternative of increas-
19 ing amplitude with duration since it defines the maximum
20 stimulus which can be delivered. Further, because sensa-
21 tions of equal loudness may be elicited by stimuli of
22 approximately equal charge, this approach allows use of
23 maximum stimulus rates to be investigated using high
24 amplitude short duration stimuli.

25 Although the current amplitude is not coded numerically
26 to eliminate the effects of coupling variations (like the
27 electrode selection pulse burst), it can be seen that an
28 error of one or two received pulses will result in only a
29 small error in the stimulation current.

30
31 Pulse Duration Control

32 The durations of the two phases of the stimulation
33 pulse, phase 1 and phase 2 as shown in Fig. 4, are deter-
34 mined directly by the duration of the two stimulation
35 bursts. Since each burst is an integral number of trans-
36 mission cycles (each of duration 400nS for a 2.5 MHz
37 transmission frequency), then the pulse duration can be
38

1 adjusted in steps of 400ns. With the existing speech
 2 processor encoder, the maximum length of a stimulation
 3 burst is 1022 pulses, or 408.8 microseconds. However,
 4 there is nothing in the receiver circuitry itself to
 5 prevent use of longer bursts, if this is required. In
 6 normal use the durations of the two stimulus phases are
 7 equal, but they are set independently and may be different
 8 if so desired.

10 Functional Description

11 The receiver/stimulator embodiment described below
 12 uses standard and conventional metal gate CMOS technology,
 13 with the circuits being realized using a gate array some-
 14 times known as an uncommitted logic array available from
 15 AMI, TI, IMI, LSI Logic and Motorola. Logic arrays in
 16 general are available from a number of suppliers such as
 17 those listed. The particular logic array used is available
 18 from AWA Microelectronics and none of the suppliers listed.
 19 Many design features may also be realized using alternative
 20 technologies and techniques, for example, silicon gate
 21 technology and standard cell design philosophy, and such
 22 alternative embodiments are understood to be within the
 23 spirit of this invention.

24 The gate array used in this embodiment comprises some
 25 2000 n and p channel enhancement mode devices of similar
 26 dimensions in a central array, and additional devices
 27 located around the perimeter of the circuit.

28 For a single N channel array device having a threshold
 29 of V_{thn} , the drain current at sufficient drain source
 30 voltage (V_{ds}) is given (in the strong inversion region) by
 31 the expression:

$$32 \quad I_{ds} = K_n * ((V_{gs} - V_{thn})^2)$$

33 While for two devices connected in series, with a
 34 common gate connection,

$$35 \quad I_{ds} = (K_n/2) * ((V_{gs} - V_{thn})^2),$$

36 and for two parallel devices

$$37 \quad I_{ds} = (2 * K_n) * ((V_{gs} - V_{thn})^2).$$

38 The convention used in this description is to define

1 a single array device as a "1X" device, two devices in
2 series as a "1/2X" device, two devices in parallel as a
3 "2X" device, and so on, since this is how their drain
4 currents are related for equal Vgs. This convention
5 applies to connections of any number of devices.

6 Typically, $K_p = 10 \text{ uA}/(V^2)$ and $K_n = 20 \text{ uA}/(V^2)$ for
7 array devices.

8 The peripheral devices include buffer transistors for
9 which $K_{pb} = K_{bn} = 500 \text{ uA}/(V^2)$. Single, series or parallel
10 connections of these devices are indicated by B, 1/2B and
11 2B. The perimeter also includes "long" devices of low
12 transconductance, typically $K_{pl} = K_{nl} = 0.15 \text{ uA}/(V^2)$. In
13 addition are two zener diodes located on the periphery.

14 15 Functional Description of Digital Circuits

16 The stimulator integrated circuit contains both
17 digital and analog circuit functions.

18 A block diagram of the digital circuitry is shown in
19 Fig. 9. Received signal energy from the tuned transformer
20 400, 401 is rectified by the diode 402 and used to power
21 the circuit. A filter capacitor 403 maintains the supply
22 voltage between data frames. The Burst Detector and Burst
23 Clock Extraction circuit 404 is used to detect when a
24 signal is present, and to recover a clock signal from the
25 data signal 405, taken directly from the tuned circuit.
26 The envelope detector output BURST 407 is asserted during
27 signal bursts, while a threshold detector generates the
28 CLOCK signal 406 from the unrectified signal input.

29 The CLOCK signal is fed to the Prescaler and Sync
30 Detector circuit 408 which has three functions. First, it
31 carries out the divide by eight operation required to
32 decode digital data and generate CLOCK8 409. Second, it
33 asserts SYNC 412 for signal bursts of less than eight
34 pulses, and third, it asserts BURST16 during the time for
35 which a burst exceeds 16 clock cycles in length. BURST16
36 output 410 is used to control various analog functions as
37 described below.

38 At the heart of the circuit is the State Counter 422.

1 It has six outputs S0 - S5 (423-427,420) which control the
2 overall operation of the circuit. Only one output can be
3 asserted at any time, and thus the system State is defined
4 at any time as the output asserted at that time-

5 In normal operation, the State Counter is left in
6 State S5 between data frames, and the SYNC burst 412
7 generates a RESET 419 signal which sets the system State
8 to S0. The State Counter is incremented through to S5
9 during the remainder of the frame by DATA signal 418,
10 which is asserted at the end of every data (that is, not
11 SYNC) signal burst.

12 DATA and RESET are generated by the Error Detector
13 circuit 415 which also detects if a DATA burst is received
14 when in state S5, or if a SYNC burst occurs in a state
15 other than S5. These are error conditions, and stimulation
16 is inhibited through assertion of the INHIBIT signal 421.
17 INHIBIT is also asserted under two other conditions related
18 to the level of the supply voltage. These conditions are
19 detected by analog sections of the circuit and signalled
20 by assertion of VLOW 416 and VLOGIC 417. VLOW is asserted
21 if the supply voltage at the start of the first stimulus
22 phase is less than the voltage required for sufficient
23 voltage compliance for the output current source, while
24 VLOGIC is asserted if the supply voltage falls so low that
25 there may be possible loss of data. INHIBIT is reset by a
26 subsequent SYNC burst, received when in state S5.

27 The Electrode Counter 428 is reset by the signal S5
28 420 and incremented during State S0 as described below.
29 At the end of S0 its value is latched in the Active elec-
30 trode latch 31, having 22 outputs A1-A22, shown as 430.
31 During S1 the counter 428 may be further incremented and
32 its output is used directly to select the Reference elect-
33 rode outputs R1-R22, shown as 429.

34 The Mode gate 413 applies the CLOCK8 signal 409
35 directly to the Electrode Counter during state S0, while
36 during state S1 the initial CLOCK8 pulse is gated out.
37 The signal BIPOLAR 414 is asserted if the Mode burst
38 generates two or more CLOCK8 clock pulses. When Mode = 1,

1 in the multipolar mode, a single CLOCK8 pulse will be
2 generated during the MODE burst, the Active electrode will
3 always be the same as the Reference electrode and BIPOLAR
4 will not be asserted, while for bipolar operation the
5 Active and Reference electrodes will be different. The
6 counter used in the Electrode Counter circuit is cyclic,
7 that is the next count after 22 is 1, thus enabling the
8 Reference electrode number to be selected as lower than
9 the Active electrode.

10 Combinational logic is used to derive the signal STIM
11 411, which is asserted during both state S3 and state S4,
12 provided that BURST16 is asserted. The Active and Reference
13 electrode select signals AN and RN are asserted only if
14 STIM is asserted and INHIBIT 421 is not asserted.

15
16 Functional Description of Analog Circuits

17 A block diagram of the analog circuit functions is
18 shown in Fig. 10.

19 The Supply Voltage Monitor 250 asserts the digital
20 signals VLOW 416 and VLOGIC 417 under the conditions
21 described above, while VHIGH 251 is asserted if the supply
22 voltage exceeds a preset limit. VHIGH is used to control
23 the Shunt Regulator circuit 252, and typically limits the
24 maximum supply voltage to 2.0 volt above the VLOW value.

25 The Reference Current Generator 253 produces the
26 current I_r 261 which will vary from device to device as a
27 result of manufacturing process variations. The Current
28 Trim Network 254 is then used to set I_{ref} to within 10
29 percent of its nominal value of 1 uA. Trimming is carried
30 out by connecting the inputs A, B and C (255, 256, 257) to
31 Vss or Vdd as required.

32 The amplitude of the output current I_o 260 of the
33 Programmable Current Source 259 is set by the duration of
34 the amplitude burst, as expressed by the approximate
35 relationship

36 $I_o = I_{max} * \exp(-k*t)$ mA, where typically $I_{max} = 2.0\text{mA}$
37 $k = 0.1$
38 for t = amp burst length (in usec)

1 The output stage of this current source 259 has an
2 output impedance exceeding 1 Megohm. The current source
3 is connected to the selected electrode through the selected
4 Output Switching Networks (261 for example) during S3 and
5 S4, as described below.

6 During intervals between data frames, when the circuit
7 is in state S5, all analog circuits except the Reference
8 Current Generator and Supply Voltage Monitor are shut
9 down. The digital circuitry draws only leakage current,
10 and the total circuit current drain is less than 5 microamp.

11 The power supply capacitor is chosen to be as large
12 as possible to maintain the supply voltage above the VLOW
13 level for as long as possible in the absence of incoming
14 data signals, while being sufficiently small in value to
15 enable VDD to be raised above VLOW in as few stimulus
16 frames as possible when starting from VDD = 0. Too large
17 a capacitor will result in missing stimuli at the start of
18 a stimulus sequence (e.g., a sequence driven from a speech
19 utterance), while too small a capacitor will result in
20 lost stimuli because the receiver/stimulator is unable to
21 maintain Vdd above Vlogic between adjacent frames of the
22 same stimulus sequence. In the operation of the power
23 supply, the charge on the power supply capacitor does
24 decay between stimuli, whether caused by a speech input or
25 other signal source. It is for this reason that it is
26 important to minimize the power consumption of the circuit
27 between stimuli.

28 We have found that the best value for the power
29 supply filter capacitor with our circuit realization is
30 0.5 microfarad, which allows an interstimulus interval of
31 at least 200 mS (for VHIGH - VLOW = 2 volt) before the
32 next stimulus may be inhibited due to VDD falling below
33 VLOW. In practice, it has been observed that with normal
34 speech derived inputs this interval is rarely exceeded.
35 With this value of CS, up to 5-10 stimulus frames may be
36 required for precharging at maximum coil separation:
37 again, this brief delay is not perceived by implanted
38 subjects.

Detailed Circuit Description

Much of the design of the receiver/stimulator circuit uses conventional techniques as well known in the art. However, the stimulator contains a number of novel features, which are described here in detail.

Burst Detector and Clock Extraction Circuit

The Burst Detector and Clock Extraction circuit is shown in Fig. 11. The unrectified input signal 281 is applied, through the standard input protection network 282, to the inverter formed by devices 283 and 284. The characteristics of these devices are chosen so that the inverter threshold is set to 70-80% of VDD, increasing tolerance to ringing in the receiver circuits at the end of bursts. Inverter 285 restores signal polarity, and the buffer 286 distributes the signal CLOCK 293, which is asserted when the input signal is above threshold. The inverter 287 turns on the P channel device 288 when CLOCK is asserted, forcing the node DET 290 high. The constant current sink 291 is used to discharge the nodal capacitance of DET to Vss in the absence of the signal CLOCK. The magnitude of this discharge current is selected to pull DET below the following Schmitt trigger 292 threshold if CLOCK is not asserted for more than 3-5 microseconds. The Schmitt trigger provides noise-free operation, even for this relatively slow transition of the DET node.

Reference Current Generator

The function of the Reference Current Generator is to provide a stable reference current without the need for any external components. It is also required that the current consumption is low, as this circuit is not disabled during state S5, when the circuit is unpowered.

The basic circuit is shown in Fig. 12. A current mirror is formed by devices 301 and 304, which share the same Vgs. Since the K value for device 301 is four times that of device 304,

$$I_1 = 4 * I_2$$

1 Devices 300 and 303 are both "long P" devices, and
 2 have similar K values, K_{lp} , and threshold voltages V_{thlp} .
 3 The device 302 is an N channel peripheral device having
 4 its drain and P well connected to V_{dd} , its gate to V_{ss} ,
 5 and its source to device 303. So connected, it behaves as
 6 the bipolar npn device depicted in Fig. 12. The voltage
 7 drop across device 302 will be one V_{be} .

8 Suppose device 303 has the gate to source voltage
 9 V_{gs303} which exceeds the device threshold voltage by V_d ,
 10 then

$$\begin{aligned} 11 \quad & V_{gs303} = V_{thlp} + V_d \\ 12 \quad \text{then} \quad & I_2 = K_{lp} * ((V_{gs303} - V_{thlp})^2) \\ 13 \quad & = K_{lp} * (V_d^2) \end{aligned}$$

14 For device (300),

$$\begin{aligned} 15 \quad & V_{gs300} = V_{gs303} + V_{be} \\ 16 \quad & = V_{thlp} + V_d + V_{be} \end{aligned}$$

$$17 \quad \text{Thus} \quad I_1 = K_{lp} * ((V_d + V_{be})^2)$$

18 Since $I_1 = 4 * I_2$, then either $V_d = V_{be}$, or $I_1 = I_2 =$
 19 0.

20 That is, the circuit has two stable operating points,
 21 either zero current or

$$\begin{aligned} 22 \quad & I_1 = 4 * K_{lp1} * V_{be}^2 \\ 23 \quad & I_2 = K_{lp} * V_{be}^2 \end{aligned}$$

24 With the incorporation of appropriate startup circuitry
 25 the zero current operating point can be avoided, and then

$$26 \quad I_r = I_1 = 4 * K_{lp1} * V_{be}^2$$

27 The voltage drop V_{be} is well defined by the manufac-
 28 turing process, as are all K value ratios. The dominant
 29 cause of variability in I_r is thus the spread in absolute
 30 value of K_{lp} to be expected during manufacture. Typically,
 31 this will vary across devices by up to 2:1 and it is this
 32 variability which required the use of the Current Trim
 33 Network.

34 Those skilled in the art will recognize that sensi-
 35 tivity of this circuit to power supply variations may
 36 readily be improved by using cascode configurations for
 37 devices 300 and 304.

38

1 The value of I_r may be varied by either changing the
2 relative K values for devices 301, 304, 305 or by changing
3 the excess drive to device 300 from the value of one V_{be}
4 shown here.

5 The current trim network 254 is shown in full in
6 Figure 23a. It comprises a series of variable ratio
7 current mirrors, where the ratios and thus the overall
8 current transfer function of the network may be adjusted
9 using external connections to V_{ss} or V_{dd} . The table in
10 Figure 23b illustrates the nominal transfer function as a
11 function of the external trim connections. With this
12 circuit no external components are required to trim the
13 reference current source.

14 The operation of the circuit is illustrated by con-
15 sidering the effect of closing contacts B. With B open,
16 $I_1 = 2 * I_{in}$, while with B closed $I_1 = 3 * I_{in}$. With B
17 open, the transfer ratio is nominally 1.0, while it is 1.5
18 with B closed. Closing contacts A serves to increase the
19 current transfer ratio by a factor of 1.25, while closing
20 contacts C changes it by a factor of 0.444.

21

22 Programmable Current Source

23 The Programmable Current Source circuit is described
24 in two parts: the Programmable Current Generator, and its
25 associated Output Mirror. The circuit of the Programmable
26 Current Generator is shown in Fig. 13 with circuit timing
27 in Fig. 14, while the circuit and timing of the Output
28 Mirror is shown in Fig. 15.

29 The principles of operation of the Programmable
30 Current Generator are easily understood by considering a
31 large enhancement mode transistor which has its gate
32 voltage adjusted such that it is operating in the subthres-
33 hold region, where the I_{ds} to V_{gs} relationship is dominantly
34 exponential. The I_{ds} of this device is appropriately
35 multiplied through the use of current mirrors to become
36 the output current. A capacitor, called the SHC capacitor,
37 is connected between gate and source, and charged to the
38

1 Vgs voltage. A current sink is now connected to discharge
2 this capacitor. If the capacitor is discharged at a
3 constant rate, then Vgs will decrease linearly and the
4 output current will decrease exponentially with-time. The
5 final output current will be defined by the time for which
6 the SHC capacitor is discharged.

7 In Fig. 13, the large device described above is 334,
8 and the capacitor SHC is connected between the node SHC
9 and Vdd. Node SHC is discharged through the current
10 mirror formed by devices 335, 336 and 337, provided that
11 S2 and BURST16 are asserted, when TD is asserted and
12 device 335 is turned off. The rate of discharge is nomi-
13 nally 24uA, being $I_{ref} = 1 \text{ uA}$ multiplied by two in the
14 current mirror 320, 342 and again by twelve in the mirror
15 336, 337. The SHC capacitor is discharged only during
16 state S2, BURST16 asserted.

17 The SHC capacitor is charged during states S0, S1 and
18 the duration of S2 for which BURST is not asserted.
19 During this time the combinational logic 339, 340, 341 and
20 346 asserts the signals TREF 343 and TREFN ((344), active
21 low), turning on devices 332, 329 and 331. The current
22 mirror 342, 321 generates the current I_{ref} of approximately
23 5uA, and the feedback circuit comprising the current
24 source 332 and the controlled current sink 330 charges the
25 SHC capacitor such that I_{ds} of 334 is equal to I_{ref} .
26 Device 333 is used to cascode device 334. The stability
27 of the feedback loop is assured by the addition of resis-
28 tor 348 to provide phase compensation.

29 During states S3 and S4, after partial discharge of
30 the SHC capacitor has occurred, device 322 is turned off
31 and devices 326 and 324 are turned on. I_{ds} from device
32 334 is multiplied by a factor of about 50 by the mirror
33 323, 327 and again by another factor of two by a cascoded
34 arrangement of large P channel devices 328. The current
35 I_{pr} , having a maximum value of 0.5 mA is further multiplied
36 by a factor of four by the Output Mirror.

37
38

1 During S5, $I_{ref} = 0$ and device 324 is turned off,
2 reducing current consumption of this area of circuitry to
3 the leakage value. The P channel devices 338 and 341
4 limit the drift of the SHC node during this time.

5 The output mirror (Fig.15) is enabled during S3 and
6 S4 provided BURST16 is asserted. Under these conditions
7 device 314 is turned off and the transmission gate 313 is
8 turned on. A transmission gate is a p channel device
9 connected in parallel with an n channel device--gate to
10 gate, source to source, drain to drain. The current
11 mirror formed by devices 310 and 311 (Fig. 15) defines the
12 magnitude of the output current I_o as four times the
13 magnitude of the input current I_{pr} , while device 312 is
14 used to cascode device 310. The output impedance of this
15 current mirror is very high, even for large output currents,
16 being in excess of 1 Megohm for an output current of 2 mA.

17 When the output stage is not enabled, the output node
18 is clamped to Vdd by device 315. The initial conditions
19 for this node are thus the same at the start of each
20 output phase, improving the charge balance for equal
21 amplitude, equal duration output pulses.

22 Device 314 keeps device 312 turned off when the
23 circuit is not enabled and the transmission gate 313 is
24 open.

25 Output Switching Circuit

26 The receiver/stimulator contains 22 Output Switching
27 circuits, one for each electrode output. The schematic
28 for one such circuit is shown in Fig. 16: it connects the
29 output to Vdd if the signal S5 is asserted, and to Vdd or
30 the Programmable Current Source, if selected by the control
31 inputs An 368, Rn 369 and BIPOLAR 370. The signal S3 is
32 used to control the multiplexer 362, directing the An
33 input to the NOR gate 366 during state S3 and device 363
34 during state S4, and making the opposite connection for
35 the output from NOR gate 361.
36
37
38

1 During state S5, signal S5 is asserted, and the
2 output of NOR gate 366 is forced low, turning on device
3 363 and connecting the output to Vdd. At this time all
4 outputs are connected together.

5 If this output is selected as the Active electrode,
6 then An is asserted during states S3 and S4. When S3 is
7 asserted during state S3 device 364 is on, connecting the
8 output to the current sink, while when S4 is asserted
9 during S4, An is connected to the input of NOR gate 366,
10 forcing its output low and connecting the output to Vdd.

11 If the output is selected as the Reference electrode
12 (Bipolar mode) then the electrode is connected to VDD when
13 S3 is asserted and to the current sink when S4 is asserted.

14 For multipolar operation BIPOLAR is not asserted, and
15 either An and Rn are both asserted (for the Active elec-
16 trode) or neither are asserted (for all other electrodes).
17 If An is asserted, circuit operation is as for the Active
18 electrode (Bipolar mode) described above, with the AND
19 gate 361 being disabled. Otherwise, the output of AND
20 gate 361 is high, and the output node will be connected as
21 described for the Reference electrode (Bipolar mode).

22 In Figure 16 the signals An, Rn and BIPOLAR are
23 asserted only during S3 and S4. The signal S4 is thus not
24 required as an explicit input to the Output Circuit. The
25 state map for the output Output Switching Circuit, together
26 with explanatory notes is shown below.

27	An	Rn	BIPOLAR	S3	S5	OUTPUT	(see note 2)
28	(see Note 1)					CONNECTIONS	
29	0	0	0	0	1	Vdd and Io	
30	1	0	1	0	0	Vdd	BIPOLAR
31	1	0	1	1	0	Io	BIPOLAR
32	0	1	1	0	0	Io	BIPOLAR
33	0	1	1	1	0	Vdd	BIPOLAR
34	0	0	0	0	0	Io	MULTIPOLAR
35	0	0	0	1	0	Vdd	MULTIPOLAR
36	1	0	0	0	0	Vdd	MULTIPOLAR
37	1	0	0	1	0	Io	MULTIPOLAR

38

- 1 Note 1 An and Rn are asserted only during S3 and S4,
2 provided the BURST16 is asserted.
- 3 Note 2 When BIPOLAR is not asserted and An is not asserted,
4 then for S3 not asserted the multiplexer will set
5 the gate of device 364 to high. Device 364 will be
6 on only when S4 and BURST16 are asserted, when the
7 Output Current mirror is enabled and the voltage on
8 the Io line is more than a threshold below Vdd (see
Figure 15). Otherwise, the Io line is held at Vdd
and device 364 is off.

9 All state signal (S0 - S5) are generated by the State
10 Counter (422 Figure 9), at the times indicated in
11 Figure 8, and as indicated in Figure 24. This Figure
12 also shows the timing of the output control signals
An, Rn and BIPOLAR.

13 Wearable Speech Processor (WSP)

14 The function of the Wearable Speech Processor is to
15 accept an incoming acoustic signal from a microphone, and
16 after suitable processing, send the appropriate stimulation
17 frames to the implanted Receiver Stimulator Unit in the
18 patient. The WSP must be small, light, and low power, as
19 it is intended that the WSP be worn on the body, e. g., in
20 a shirt pocket, and be battery powered. Power consumption
21 must be minimized to achieve longest possible time between
22 change of battery, or recharging. The WSP must also be
23 able to be configured for each patient's unique character-
24 istics of psychophysics.

25 A block diagram of the speech processor is shown in
26 Fig. 17. A microphone 80 receives the acoustic input.
27 This microphone may be a conventional hearing aid micro-
28 phone, for example worn over the ear on a hook, or may be
29 a higher quality studio type microphone, or the microphone
30 may be replaced with another signal source such as the
31 audio output from a television or radio. This flexibility
32 of choice of input has advantages for the implant patient.

33 The main aim of the WSP design is to provide the user
34 with speech communication, and the stimulation strategy
35 and description of terms reflects this. However, it is
36 also important to provide the user with awareness of
37 environmental sounds, and the stimulation strategy makes
38

1 this possible also, although it is optimized for speech
2 communications. In addition, it is possible to select the
3 most appropriate strategy for each patient from a set of
4 possibilities.

5 The audio signal is amplified and processed by the
6 WSP front end 81. From this, three signals are produced:

7 START used to start the generation of a stimulus
8 pulse frame by the encoder

9 ELSEL a voltage used to determine which electrode
10 is to be selected for stimulation

11 STAMP a voltage used to determine the amplitude
12 of stimulation on the selected electrode.

13 The START signal is used to initiate a single stimulus
14 frame of pulse bursts by the Speech Processor Encoder 82
15 each time it occurs. The ELSEL and STAMP signals are used
16 to determine stimulus parameters of electrode and stimulus
17 level, according to which of the speech processing strate-
18 gies previously described has been selected. An alterna-
19 tive speech processing strategy based on F1 is also possible
20 using the invention described here.

21 An 8 bit Analog to Digital Convertor 83 ("ADC")
22 converts the ELSEL and STAMP signals into numbers for use
23 by the encoder. A two input analog multiplexer and sample
24 and hold circuit 92 is under control of the encoder (for
25 signal selection) and the ADC chip (for S/H control) so
26 that the correct signal is presented to the ADC at the
27 correct time. The encoder operates by way of a program
28 stored in a UV erasable PROM 84, which also stores the map
29 between F2 and electrode, and A2 and amplitude of stimula-
30 tion, for each electrode. The stimulation amplitude is
31 related to STAMP differently for each electrode, according
32 to stimulation thresholds for that electrode.

33 These three signals are derived from five basic
34 signals produced inside the WSP front end. It is possible
35 to configure each patient's speech processor to select
36 which of two or three alternative stimulation strategies
37 is to be used, and thus which set of three signals from
38

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1 the following six is to be used. The five basic signals
2 are:

- 3 Fo the voicing or fundamental frequency
- 4 Fo' the frequency translated Fo signal
- 5 F2 a voltage proportional to F2 frequency
- 6 A2 a voltage proportional to amplitude of the F2
- 7 signal
- 8 F1 a pulse train at the frequency of the dominant
- 9 spectral peak (F1)
- 10 A the overall acoustic signal amplitude.

11 Data from the front end are encoded by the encoder
12 chip into the format shown in Figure 8, and described
13 herein, and to the output stage 85, which is connected via
14 a coaxial cable 86 to the transmitting coil 87. The
15 transmitting coil is tuned to the correct frequency with a
16 single capacitor 88 located at the coil.

17 A connector 89 in the WSP allows connection to the
18 Interface Unit, or IU, which is used during the testing of
19 the patient, and allows the parameters to be programmed
20 into the patient's map in the WSP.

21 The WSP is powered from +5V and -5V supplies generated
22 by a DC-DC Convertor 90 operating from batteries 91.
23 Battery voltage may be in the range 3 to 7 volts, allowing
24 a wide choice in number and style of batteries, including
25 readily available primary cells, or rechargeable cells.

26 The speech processor is constructed in a small case
27 designed for easy carrying in a pocket, on a belt, or in a
28 pouch under the clothing. The cable from the microphone
29 and the coil on the ear attaches to the WSP by a connector
30 for ease of use.

31 Wearable Speech Processor Front End

32 Overview

33 To understand the speech processor front end it is
34 first necessary to be aware of the nature of the speech
35 signal. Speech may be divided into two categories:

1 voiced and unvoiced. Voiced speech is produced by a
2 vibration of the glottis which provides an excitation
3 source for a resonant system consisting of the oral and
4 nasal cavities. A number of resonances (formants) are
5 produced but of these the three lowest contain most of the
6 information.

7 Unvoiced speech does not use the glottis as an exci-
8 tation source but rather a noise produced by the passage
9 of air such as between the tongue and teeth (as in 's'
10 and 'th' and 'f'), or by explosive generation of sound
11 pulses (such as in 'p' and 't'), or by the passage of air
12 in the throat such as 'h').

13 The WSP is designed to use one of two stimulation
14 strategies, employing sets of three parameter estimates of
15 the acoustic input, as follows:

16 STRATEGY 1:

- 17 (a) The frequency of the second formant (resonant
18 frequency) (F2) is encoded into electrode position/
19 selection.
20 (b) The frequency of glottal excitation, if the sound
21 is voiced (voice pitch or Fo) is encoded into
22 stimulation rate.
23 (c) The amplitude of the second formant (A2) is encoded
24 into stimulation amplitude.

25 It has been found that these three parameters contain
26 a large proportion of the intelligibility of speech and
27 particularly information which is not available by lipread-
28 ing.

29 However, as pointed out in the section on Psychophysics
30 in the introductory parts above, the perceived pitch with
31 varying stimulus frequency is different to the stimulation
32 frequency. Thus, it is necessary to translate and offset
33 the speech Fo signal via a transformation which will allow
34 the stimulation frequency (Fo') to produce a percept
35 close to the actual Fo frequency.

36
37
38

1 STRATEGY 2:

2 (a) The frequency of the second formant (F2) is
3 encoded into electrode position/selection.

4 (b) The frequency of the first formant (F1) is
5 encoded into stimulation rate.

6 (c) The amplitude of the overall signal (A) is
7 encoded into stimulation amplitude.

8 This alternative speech processing strategy has the
9 advantage of providing a faster stimulation rate which we
10 believe may result in more naturally sounding speech for
11 some patients. In particular, since the stimulation rate
12 is F1, and the amplitude of stimulation is encoded from
13 overall amplitude of the acoustic input, for speech signals,
14 the Fo modulation of the speech signal is also perceived
15 by the patient as a modulation of stimulus amplitude.
16 However, this faster stimulation strategy may result in
17 greater power consumption, with accompanying reduction in
18 battery life.

19 We have found that the best choice of speech processing
20 strategy depends upon the patient, with some patients
21 'liking' one strategy more than another, even though
22 performance at speech communication tests may be similar
23 in both cases. It is thus an advantage to be able to
24 choose the optimal speech processing strategy for each
25 patient individually, and this feature is not available in
26 the prior art.

27 Fig. 18 is a block diagram of the WSP front end, with
28 circuit element blocks identified. In general, each block
29 is made in this embodiment with conventional circuit
30 techniques, and anyone skilled in the art could create a
31 circuit to reproduce the functions described. The choice
32 of stimulation strategy is made in the speech processor by
33 selection of circuit jumpers or switches 120 and 121.

34
35 Preamplifier and Squelch

36 The microphone or other signal source 100 is amplified
37 by a high gain low power microphone preamplifier 101,
38

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1 incorporating automatic gain control, or AGC. The AGC
2 allows the front end to operate without limiting, and
3 operates in the conventional manner, with an AGC attack
4 time of about 1 milliseconds, and an AGC decay time constant
5 of about 220 milliseconds. However, the voltage controlling
6 this gain is monitored and during periods of high gain
7 (i.e., low signal) is stored by a minimum detector 114 and
8 used as a reference level.

9 The preamplifier has a maximum gain of 80dB, with a
10 full gain bandwidth of 4.4 kHz. Pre-emphasis and de-
11 emphasis is possible to compensate for different microphones,
12 as conventional directional miniature hearing aid micro-
13 phones will require pre-emphasis of 6dB/octave above about
14 1kHz.

15 Circuitry is included to generate a SQUELCH signal
16 which is used to de-activate the encoder during periods of
17 no signal. When the incoming signal increases a preset
18 amount above the level held in the minimum detector (deter-
19 mined by the attenuator 115), a comparator 116 generates
20 a logic level signal to enable the speech processor encoder.
21 Otherwise it is assumed that background noise only is
22 present and the encoder and output stage is disabled. The
23 squelch circuit has a time out of about 200 milliseconds,
24 such that the encoder is de-activated 0.2 seconds after
25 the end of the last loud signal.

26 Thus, for speech, the SQUELCH signal will enable the
27 encoder during speech, and will allow up to 0.2 seconds
28 delay between words before disabling the encoder. For
29 nonspeech signals, such as environmental sounds like
30 warnings, telephones, doors, etc., which are impulsive,
31 the SQUELCH circuit will also enable the encoder to produce
32 stimuli.

33 The squelch circuitry provides the advantage that
34 battery life is conserved, as the encoder and output stage
35 are active only when sufficient signal is present. This
36 also has the advantage that the patient is not subjected
37 to annoying or incomprehensible stimulation when used in
38

1 environments with a high level of continuous background
2 noise. However, in some circumstances, it is desirable to
3 be aware of all background noise, and the patient has the
4 ability to disable the operation of the squelch circuitry
5 by a switch on the front panel of the WSP to continuously
6 enable the encoder and output stage.

7

8 Second Formant (F2) extraction

9 The frequency of the second formant varies according
10 to the utterance and the speaker, between about 800Hz and
11 3300 Hz. To extract this formant, a high pass filter 102
12 is used. Because each successive formant is of lower
13 amplitude than its predecessor, F1 values from some speakers
14 could dominate the output of the filter if it were turned
15 to a lower frequency. The filter is optimized to produce
16 a predominance of F2 for a range of speakers. This filter
17 uses an infinite gain multiple feedback circuit because of
18 the requirement for gain in the passband. Typically the
19 gain is 4.5, $Q = 1.3$ and $f_0 = 1.87$ kHz.

20 The output of the highpass filter is passed through a
21 zero crossing detector 103 which has hysteresis so as to
22 remove extraneous crossings produced by noise or the
23 intrusion of F3 frequencies. In order to accommodate
24 variations in peak signal amplitude, the hysteresis amount
25 is derived from the output of a peak detector 109 which
26 sets the level appropriately. The magnitude of the hysteresis
27 is about 20%.

28 The output of the zero crossing detector is input to
29 a Frequency to Voltage Converter 104 consisting of a
30 monostable followed by a lowpass filter. Because the
31 voltage produced by this circuit is subject to jitter a
32 further hysteresis circuit 105 operates on the voltage
33 representing the F2 frequency, with a hysteresis of about
34 14%. The final output of the F2 estimation circuitry is a
35 voltage proportional to frequency at 1kHz per volt.

36

37

38

1 Second Formant Amplitude (A2)

2 The amplitude of the F2 signal after the high pass
3 filter is obtained via the peak detector 109. The output
4 of a 2 pole linear phase lowpass filter with a corner
5 frequency of 35 Hz provides a smoothed estimate of the
6 formant amplitude A2.
7

8 Voice Pitch (Fo) Extraction

9 The periodic excitation of the resonant system of the
10 vocal tract during a voiced utterance results in an ampli-
11 tude modulated signal envelope. The excitation rate or
12 voice pitch is derived from this envelope by full wave
13 rectification using conventional full wave rectifier
14 circuit built around an operational amplifier 106. The
15 rectified signal has the DC level removed by AC coupling
16 in a capacitor 107 which introduces a zero at about 70 Hz,
17 and is then low pass filtered. This filter 108 is a 3
18 pole 200 Hz low pass filter in the Sallen and Keys configu-
19 ration. Full wave rectification is used to double the
20 "carrier" or resonance frequency thus easing the problem
21 of separating the first formant frequency from the voice
22 pitch.

23 The resulting signal is converted to a voltage propor-
24 tional to frequency with an identical circuit arrangement
25 to the F2 path (except for the appropriate time constants)
26 consisting of a zero crossing detector 110 with hysteresis
27 level set by a peak detector 117. A frequency to voltage
28 convertor 112 produces a voltage proportional to Fo fre-
29 quency, at 130 Hz per volt.

30 A voltage controlled oscillator 113 driven by this
31 voltage then produces another frequency Fo' which is
32 proportional to but not necessarily equal to Fo. The VCO
33 has adjustable input voltage range, and also an adjustable
34 offset to give a range of control over the linear conversion
35 from Fo to Fo'. This Fo' frequency is used as the stimula-
36 tion rate of a patient electrode, selected by F2 and
37 stimulated at a level related to A2.
38

1 First Formant (F1) and Amplitude Extraction Circuits

2 A peak detector 118 following the microphone preamp-
3 lifier follows peaks in the signal, which will be dominated
4 by peaks at the F1 rate. The value of the peak is held in
5 a Peak Hold circuit 119 and is used to determine stimulation
6 amplitude. This circuit is realized with an operational
7 amplifier charging a capacitor through a diode, with the
8 capacitor voltage returned to the summing junction of the
9 operational amplifier. Thus the capacitor voltage follows
10 the peaks in the signal, and the operational amplifier
11 output will have excursions between the negative supply
12 rail, and the present peak value. The output of the
13 operational amplifier is coupled with a capacitor and a
14 resistor to the START input of the encoder, to start the
15 encoder at the F1 rate, if this is selected. A START pulse
16 will be produced everytime the input signal amplitude
17 falls below the currently held peak value, and thus the
18 encoder will stimulate at the F1 rate, at an amplitude
19 determined by the value of the last peak in the signal
20

21 Other Circuits

22 The two voltages, ELSEL and STAMP are made available
23 to the ADC via a two input analog multiplexer and sample
24 and hold circuit under control of the ADC and encoder, as
25 shown in Fig. 17.

26 Additional control circuitry (not shown) allows the
27 patient to operate a TEST function by way of the front
28 panel switch on the WSP. The purpose of the TEST function
29 is to generate comfortable level stimulus at a constant
30 rate on the lowest frequency percept electrode. This
31 electrode is usually the most apical electrode. This
32 gives the patient a known and constant percept so that he
33 may easily and simply adjust the coil position. The TEST
34 function merely causes the input to the VCO 113 to be a
35 constant, low level, and the output of the A2 path to be
36 the maximum value. In addition, the TEST function is
37 configured to impose a dummy load on the power supply, and
38

1 light a LED if sufficient battery power remains. This is
2 a useful feature to warn the patient of battery failure.

3 4 Speech Processor Encoder

5 6 Overview

7 The speech processor encoder chip is used to generate
8 pulse burst sequences which are subsequently transmitted
9 via the output stage to the implantable receiver/stimulator
10 in the patient. The pulse burst sequence is under the
11 control of a program stored in an electronic memory device,
12 such as an EPROM (e.g. 27C16), and the number of pulses in
13 the variable parts of the pulse burst sequence is determined
14 by the output of an ADC, and the program in memory.

15 The speech processor encoder chip is essentially a
16 flexible, programmable pulse generator. The encoder chip
17 is able to produce sequences of constant frequency pulses
18 with the number of pulses and time between pulse bursts
19 determined either by the internal program or in response
20 to an externally applied analog signal (through an external
21 ADC). The frequency of output pulses is determined by the
22 frequency of the clock, and the system is designed to be
23 able to work from DC to a frequency determined by the
24 practical limits (about 10 MHz) of the CMOS technology in
25 which the invention is embodied.

26 In this invention, the encoder chip is used to generate
27 the frame of pulse bursts required for powering and con-
28 trolling the implantable receiver stimulator. The format
29 of these pulse burst frames is illustrated in Fig. 8.
30 However, the encoder chip has been designed to be flexible,
31 and will be useful in a number of applications where it is
32 necessary to produce bursts of pulses. In particular, it
33 is expected that the encoder chip will be useful in appli-
34 cations where a different data encoding format is used,
35 e.g., for use with future generations of receiver stimu-
36 lation designs.

37

38

1 Architecture

2 Fig. 19 is a block diagram of the encoder, showing
3 all functional blocks. In some ways, the architecture of
4 the encoder is similar to a conventional microprocessor in
5 that there is an Address Bus, a Data Bus, Instruction
6 Decode logic etc. However, in distinction from conventional
7 microprocessors, there is no Arithmetic Logic Unit (ALU),
8 as the encoder is not required to perform any arithmetic.

9 The encoder also has similarities to a conventional
10 state machine. The encoder, however, is not designed to
11 allow program branches or jumps dependent upon data gener-
12 ated in previous states, and the program running the
13 encoder has each instruction executed exactly once from
14 start to halt.

15 The function of the encoder is to generate a number
16 of pulses in a burst, dependent upon data presented to it
17 on the data bus, and the contents of the instruction
18 currently fetched from memory. The memory address bus has
19 its contents originating from either the program counter
20 (for instruction fetches, for example), internal registers
21 (Electrode Latch, F2 Latch, and A2 Latch), or the data
22 output from the ADC - or combinations of these.

23 Circuitry exists in the encoder so that operation is
24 enabled or disabled from external control lines shown
25 symbolically as 130. Provided the encoder chip is ENABLED,
26 each START pulse (shown symbolically as 131) initiates a
27 sequence of pulse bursts called a frame, as defined before.
28 START pulses occurring during a frame are ignored. This
29 is important for a cochlear implant encoder since it is
30 essential for the power/data signal format described above
31 for all frames to be properly finished.

32 Each burst of pulses is numbered sequentially from 0.
33 The number of bursts in each frame is constant and fixed
34 by the program in EPROM. The number of pulses in each
35 burst may be fixed, or determined from the EPROM mapping
36 between ADC value (an address) and the pulse count at that
37 address. A fixed delay between bursts (8 clock times) is
38

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1 required to decode the next instruction, and load the
2 pulse count for the next burst.

3 There is a start delay between the START pulse and
4 the first burst. This time is the same as the INTER-BURST
5 DELAY, with +2, -0 clock cycles jitter because the START
6 pulses are asynchronous with the internal clock. A frame
7 is only initiated by a START pulse if the chip is enabled.
8 Changes to the enabling inputs to the encoder during a
9 frame will have no effect and all frames will be finished.
10 This is an important safety feature in the cochlear implant
11 system, as it would be potentially dangerous or uncomfortable
12 to the patient if the frame of pulses was not of the
13 format required, because it could lead to generation of
14 incorrect stimulus pulses from the receiver-stimulator in
15 the patient.

16 The encoder is considered to exist in one of four
17 states as follows:

- | | | |
|----|----------|---|
| 18 | 1. HALT | awaiting a START pulse to initiate operation; |
| 19 | 2. FETCH | an instruction is fetched from the memory |
| 20 | | location determined by the program counter |
| 21 | | and loaded into the INSTRUCTION LATCH 134; |
| 22 | 3. DATA | the instruction so fetched is decoded and |
| 23 | | data from the PROM is loaded into the DATA |
| 24 | | LATCH 139. The register used to supply the |
| 25 | | address of this data is determined by bits |
| 26 | | set in the instruction latch, and as decoded |
| 26 | | by the Instruction Decoder 133; and |
| 27 | 4. COUNT | the 9 stage synchronous binary counter |
| 28 | | (Burst Counter 142 is enabled and counts |
| 29 | | up. When the COUNTER value equals the |
| 30 | | number in the DATA LATCH, the 9 Bit Binary |
| 31 | | Comparator 140 asserts the A=B signal 145 |
| 31 | | and the next cycle is initiated in the |
| 31 | | Internal Timing and State Generator 132. |

32 The operation of the encoder is that a START pulse
33 initiates the first instruction fetch from memory at an
34 address determined by the PROGRAM COUNTER 135. The
35 instruction so fetched is loaded into the INSTRUCTION
36 LATCH 134.

37
38

1 The next state is the DATA state, where data from the
2 memory is loaded into the DATA LATCH 139, and may also be
3 loaded into other latches as needed, including the ELECTRODE
4 LATCH 136, the F2 LATCH 137, or the A2 LATCH 138. The
5 memory address from which the data is obtained is determined
6 by the instruction, and various control signals (shown
7 symbolically as 148) are decoded from the instruction in
8 the INSTRUCTION DECODER 133.

9 The next state is the COUNT state, where the 9 BIT
10 BINARY COUNTER 142 counts up from its starting value to
11 the value of the number in the DATA LATCH 139 and a ninth
12 bit obtained from the current instruction. During counting,
13 the internal clock signal may be made available to the
14 OUTPUT pin, and is sent to the output stage, under control
15 of the BURST COUNTER CONTROL LOGIC 143. A 9 BIT BINARY
16 COMPARATOR 140 determines when the two numbers are equal,
17 and causes the counting to stop and the next state of
18 FETCH to be entered.

19 Thus the Encoder Chip continues through the states
20 of FETCH, DATA and COUNT until the HALT instruction is
21 fetched from memory, at which time further operation
22 stops, and the encoder now exists in the HALT state.

23 The input signals to the encoder are:

24 START A signal generated externally by the WSP front
25 end (i.e., Fo') at a rate determined by the
26 incoming speech signal.
27 ENABLE Enabling signal or signals (depending upon the
28 embodiment) which allow the encoder to generate
29 pulse frames in response to a START pulse.

30 In addition to these control signals, the Address Bus
31 146 is bidirectional, with the encoder putting out memory
32 addresses, and the ADC data sometimes being applied to the
33 address bus as well for mapping between F2, A2 and number
34 of pulses. Five bits of the 8 ADC data bits are connected
35 directly to the address bus (A7 to A3), and the other
36 three bits are input to special pins which are internally
37 connected to the address bus at the correct time (AD2-AD0).
38

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1 The data bus 147 is input to the encoder only, and
2 comes from the memory. Note that in the wearable speech
3 processor, the memory is a UV Erasable PROM, but it is not
4 a requirement that this type of memory be used exclusively.
5 In fact, a random access memory is used within the Inter-
6 face Unit of the Diagnostic and Programming Unit to emulate
7 the PROM. Other memory technologies, such as EE-PROM
8 could also be used.

9 The outputs for the encoder are:

10 OUTPUT: Bursts of output pulses sent to the RF output
11 stage of the wearable speech processor.
12 DAMP: A signal asserted when pulses are not being
13 output to allow damping of the RF output stage.
14 DOUT: An output line set/reset under program control
15 (as described below). This line is included for
16 expansion in the future, and may be particularly
17 useful for example for adjustment of transmitted
18 power level to conserve power, or expansion into
19 more memory address space under program control.

20 In addition to these input and output signals, numerous
21 control signals bus are used to interface the encoder to
22 the ADC and memory. Of particular importance is the
23 signal CE 149 which is used as the Chip Enable for the
24 Memory, and also as the Convert Start for the ADC. A
25 separate Chip Enable from the encoder instead of enabling
26 the memory the whole time allows the use of semiconductor
27 memories whose power consumption is less when not enabled.

28 The instruction fetched from the memory is an 8 bit
29 word with the bit allocation as defined below.

29		7	6	5	4	3	2	1	0
30	BIT:	MSB							LSB
31	LABEL:	EXT	BC1	BC0	RS2	RS1	RS0	A10D	MUX

32 where the functions of these bits is:

33 MUX Multiplexer. This bit is directly output to a
34 pin and is used to select one of two analog
35 inputs to the analog to digital converter under
36 program control. For interfacing convenience,
37 the complement of this bit is also output to a
38 pin.

- 1 A10D This bit is gated to the most significant bit of
- 2 the address bus during the data cycle and allows
- 3 data to be accessed from either half of the 2048
- 4 byte address space. The mapping strategy is
- 5 discussed in further detail below.
- 6
- 7 RS0 REGISTER SELECT. These bits determine which
- 8 RS1 register is to be gated on to the address bus
- 9 RS2 during the DATA cycle. A detailed explanation
- 10 is presented below.
- 11 BCO Burst Counter Control. These bits are used to
- 12 BCl decode the mode of operation of the burst counter
- 13 as described further below.
- 14
- 15 EXT (Extend) This bit is used to add an extra bit
- 16 input to the magnitude comparator to allow for
- 17 9 bit counting to extend the burst counter
- 18 timing interval by an extra 256 pulses of burst
- 19 counter clock.
- 20
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Address Selection

The data stored in the DATA LATCH is read from the memory during the DATA state. The location of this data in memory is determined by the contents of the address bus at the time. The Register Select bits in the control word are used to determine the source of the memory address in the DATA cycle. The bit assignment, and the use of each of the possibilities is described below. The register select bits may also be thought of as defining the instruction to be executed by the encoder from the set of 8 possible instructions.

In order to understand the following descriptions, it is helpful to examine Fig. 20 which graphically describes how the 1024 bytes of each half of the PROM address space is partitioned. The reader should note that this partitioning has been designed for maximum utilization of the available address space and this may explain some of the seemingly unusual bit allocations. In the register select bits, RS2, RS1, and RS0 is shown after the instruction name.

1 FIX-Fixed Data (000)

2

3 The program counter (which was incremented at the end
4 of FETCH) is gated onto the address bus. Thus, the DATA
5 stored in the next byte in memory after the instruction is
6 loaded into the DATA latch. The program counter is then
7 incremented. This mode is used for generation of fixed
8 duration delays or data bursts, as the number of pulses to
9 be sent in the burst is stored in the ROM.

10

11 FXDT-Fixed Data and Toggle DOUT (001)

12

13 This instruction is identical to the FIX instruction
14 except that the DOUT output line is changed in state.

15 NOTE: The DOUT line is always reset to 0 at
16 the start of a frame.

17

18 FXAT-Fixed Data and Toggle A10 Select Flip-Flop 101.

19

20 This instruction is the same as the FIX instruction
21 except that a flip-flop called the A10 select flip-flop is
22 toggled. This flip-flop is in the instruction decoder,
23 and is used to select either the A10D signal or AD2 (the
24 ADC input bit) for the mapping the inputs either to two
25 halves of memory or extending the amplitude precision by
26 one bit. See also notes on Fig. 20 for further explanation.

27 NOTE: The A10 select flip-flop is always reset
28 to 0 at the start of a frame.

29

30 F2ADC-ADC INPUT (F2 value) 111.

31

32 The 8 bits output from the ADC is gated onto bits 2
33 to 9 of the address bus (MSB is A9) and bits 0 and 1 of
34 the address bus are forced to logic 1. The data in this
35 area of PROM is the map between F2 and electrode number.
36 The ADC is so arranged with its reference voltage that it
37 can never reach a value of 11000000 (=224) or greater to
38

1 guarantee that the ADC value does not intrude into the
2 program address space.

3 Alternatively, it may be decided that the program in
4 PROM will occupy address space in one-half of the PROM
5 (e.g., $A_{10}=1$), and the F2 to electrode map will occupy the
6 other half ($A_{10} = 0$). This means that it is then unneces-
7 sary to restrict the F2 to electrode mapping address
8 space, and the full 8 bit range may be used.

9 At the same time the ADC is read, the 8 bit F2 value
10 is also stored in the F2 LATCH 137 of 8 bits, from which
11 it may be read again later.

12 Additionally, bits D7 to D2 of the DATA so generated
13 from the PROM (i.e., the electrode number) are stored in
14 the ELECTRODE LATCH 136, offset, and in bit reversed
15 order.

16 The arrangement shown in Fig. 20 is for the electrode
17 number to be encoded into bits 6 to 2 of the output from
18 the PROM, with $D_1 = 1$, and $D_0 = 0$. This will encode the
19 electrode number n , as $4*n + 2$. However, it is possible
20 to also encode the electrode number as $8*n + 4$, by shifting
21 the electrode number left 1 bit, and setting $D_2 = 1$, and
22 $D_0 = D_1 = 0$. As described in the system description
23 above, the electrode number is encoded in the pulse burst
24 to the implant by $8*n + 4$. The encoder chip design allows
25 flexibility in encoding electrode number to take advantage
26 of future designs which may utilize a different electrode
27 encoding scheme, which would have advantages in terms of
28 the maximum rate of stimulation.

29
30 F2L-Latch Input (011)

31
32 The data stored in the F2 LATCH previously generated
33 by an F2ADC instruction (111) (Fig.18) is again gated onto
34 the address bus. When used in conjunction with instruction
35 bit $A_{10}D$, this allows a choice of two DATA values for any
36 F2ADC value.

37
38

1 This is important because it allows the use of dif-
2 ferent stimulation strategies in the future, for example
3 utilizing more than one electrode for each F2 value, such
4 that electrodes are stimulated in pairs. Alternatively,
5 it may be desirable to have different stimulus pulse
6 lengths for each electrode, and this could be stored in
7 the second half of the memory address space, and accessed
8 with this instruction.

9

10 ADCE-ADC Input and Electrode (110).

11

12 The most significant 5 bits of the ADC are gated onto
13 bits A5-A9 of the address bus. The least significant 5
14 bits contain the contents of the electrode latch (Fig. 19)
15 in bit reversed order. The electrode number must be
16 constrained in the PROM to be no bigger than 1011 (23) to
17 prevent intrusion of this part of the address space into
18 the other address space. In the present design, this,
19 therefore, limits the number of electrodes to 23.

20

21 However, as mentioned above, the electrode latch is
22 of 6 bits in length, and the choice of which five of the
23 six bits are placed onto the address bus depends on the
24 choice of coding of electrode number as $4*n + 2$ or $8*n +$
25 4. An external control input to the encoder chip allows
26 the user to choose which encoding strategy is to be used
27 and thus which 5 of the 6 bits are to be placed onto the
28 address bus at this time.

29

30 It is possible to use one extra bit of precision in
31 the ADC by gating it onto A10 line if the FXAT instruction
32 has been executed an odd number of times (e.g.:1) since
33 the frame start. Otherwise, A10 will contain the contents
34 of A10D to allow generation of pulse sequences from either
35 half of memory.

36

37 At the same time as the ADCE instruction is executed,
38 the 6 most significant bits (A10 to A5) are stored in the
39 internal A2 LATCH 138 for later re-use. The A2 latch data
40 bit from A10 thus contains either AD2 (from ADC) or A10D
41 from the current instruction.

1 A2L-A2 Latch and Electrode (010)

2

3 This is identical to ADCE (described above) except
4 that the data previously stored in the A2 latch-by an ADCE
5 instruction is used instead of the ADC input. The data is
6 not re-latched into the A2 latch but retained.

7

8 HALT-Halt (100)

9

10 This is a special instruction which is used to signify
11 the end of a sequence and the initiation of the HALT
12 state. The whole encoder chip exists in the HALT state
13 between stimulation sequences.

14 The HALT instruction also generates a control signal
15 to read the ADC (RD). This guarantees the ADC will be
16 ready to convert the data available on the first instruction
17 to be executed in the frame so that ADC data, when first
18 read in the frame will be the value at the start of the
19 frame.

20

21 Burst Counter Control Bits

22 The burst counter control bits determine whether
23 clock pulses are transmitted during the burst count and
24 whether the burst counter is reset at the end of a burst.

25 BC0 is used to enable or disable the clock pulses to
26 the output pin for the duration of the burst.

27 BC1 is used to enable reset of the burst counter upon
28 detection of the equality of the burst counter and the
29 data in the data latch.

30 If BC0 and BC1 are both zero, then the clock input to
31 the burst counter is divided by two to allow a doubling of
32 the time the clock is enabled to the output and the sig-
33 nals RG (reset gate) on ON are forced high. The choice of
34 the source of the clock to the burst counter from either
35 the divide by two circuitry 141 (Fig. 19) or directly from
36 the clock generator 144 is done by an electronic switch
37 whose state is set by control lines from the instruction
38 decoder 133.

1 The burst counter and control logic 143 section is
2 used to generate pulses according to the number loaded
3 into the DATA LATCH 139 in the DATA cycle. The BURST
4 COUNTER 142 commences counting at the end of the DATA
5 cycle and counts until the value in a bit binary counter
6 142 equals the number in the DATA LATCH 139 at which stage
7 counting ceases and a new fetch cycle is initiated.

8 The BURST COUNTER 142 is a 9 stage synchronous binary
9 up counter. The control of the BURST COUNTER 142 is by
10 the bits EXT, and BCO and BC 1 in the current instruction.
11 The EXT bit effectively extends the 8 bit data to 9 bits
12 by adding an extra (most significant) bit. The state of
13 BCO determines whether or not the clock is enabled to the
14 OUTPUT pin for the duration of the burst (i.e., an ON
15 BURST or an OFF burst), BC1 determines whether or not the
16 BURST COUNTER is reset at the end of the current burst.

17 It is thus possible to generate a variable number of
18 pulses within a constant time interval. This feature is
19 important because by using it, it is possible to guarantee
20 that all stimulus frames are of constant time duration.
21 This is important to eliminate timing jitter between
22 stimulus pulses to the patient, as will be required for
23 some psychophysical research, and may be essential in some
24 speech processing strategies. For example, if a constant
25 time interval of 256 clock pulses was required, the follow-
26 ing sequence of events would occur.

- 27
- 28 1. At END of last instruction, BURST COUNTER is reset
29 (BC1 = 1 for that instruction).
- 30 2. The data for the number of pulses required (N) is
31 loaded into the DATA LATCH via the mapping in PROM,
32 and the output is enabled and the BURST COUNTER is
not reset at the end of the BURST (BC0 = 1, BC1 = 0).
- 33 3. The next instruction loads fixed data of 248 (248
34 pulses counted + 8 pulses for FETCH and DATA time =
35 256) with output not enabled and burst counter reset
36 at end (BC1 = 1, BC0 = 0). Thus the counter counts
37 from the last data value to the total pulses value
38 without output and the time interval from start of
pulse generation to end of OFF burst is constant.

1 This facility eliminates the need for any arithmetic
2 to be done inside the encoder chip.

3 A further condition where $BC0 = 0 = BC1$ (which would
4 normally be meaningless) is used for generating very long
5 bursts of pulses. In this condition, the input clock to
6 the burst counter is pre-divided by two so that the time
7 the counter is counting is exactly twice that when the
8 normal clock is used. Thus the number of output pulses
9 can be doubled for the same number in the data latch.
10 This condition is detected by the Instruction Decoder
11 circuit which asserts the appropriate internal control
12 signals.

13 The equality of the 9 bit up counter and 8 bit data
14 latch plus EXT bit from the current instruction is detected
15 by a combinational logic network arranged as a 9 bit
16 binary comparator 140. The equality signal ($A=B$) is fed
17 back to the internal timing and state generator 132 which
18 asserts signals to inhibit further counting of the up
19 counter.

20 If the ON signal is asserted (decoded from the current
21 instruction) the clock signal is gated to the OUTPUT pin
22 and the DAMP signal is asserted).

23
24 Internal Timing and State Generator.

25 The function of the internal timing and state generator
26 132 is to

- 27 - generate power on reset of encoder chip;
28 - generate the clock from the on chip crystal
29 oscillator 144;
30 - generate the initialization sequence which
31 starts the program in EPROM when a START pulse
32 is received if the chip is enabled.

33 The power on reset is detected from a pin PORN 151
34 which will go high sometime after power is applied. This
35 signal may be easily generated from a resistor and capacitor
36 network. The function of the power on reset is to ensure
37 that the encoder chip powers up to a known state. In
38

1 addition, in this embodiment, circuitry is included in the
2 speech processor front end to prevent the encoder from
3 operating if the power supply voltage is inadequate, as
4 may occur towards the end of battery life. This is an
5 important safety feature in the system to prevent spurious
6 pulse frames being transmitted to the implant due to
7 faulty operation of the logic circuits because of low
8 supply voltage.

9 A crystal oscillator is formed conventionally from a
10 chain of an odd number of inverters. This is then gated
11 into a divide by two circuit and the resulting clock is
12 buffered heavily and distributed to the rest of the chip.
13 The divider is only enabled while the encoder chip is
14 running to conserve power. This is important because, in
15 CMOS technology, practically all power consumption of the
16 chip is derived from capacitive charging and discharging
17 of nodal capacitance, whereas the DC power consumption is
18 effectively zero. The divide by two circuit guarantees
19 exactly equal mark/space ratio of the internal clock, and
20 thus the external output signal, which is important for
21 best efficiency of the output stage.

22 The initializing sequencer is set up so that all
23 enable inputs must be asserted to allow the START pulse to
24 initiate operation of the encoder. After the program in
25 memory has been started, further changes to START or the
26 Enable inputs will have no effect until the current frame
27 is complete (i.e., HALT instruction executed).

28

29 Instruction Latch and Instruction Decoder

30 The INSTRUCTION LATCH 134 is an 8 bit gated D latch
31 which is loaded with the current instruction in the FETCH
32 cycle. The contents of RS0-RS2 in the instruction latch
33 are then decoded by combinational logic 133 and are used
34 to determine the source of the address bus bits for obtain-
35 ing the burst count as described above. The memory contains
36 data on pulse burst length mapped from the ELSEL data and
37 the STAMP data from the Speech Processor Front End. The
38

1 INSTRUCTION DECODE LOGIC decodes the RS0-RS2 bits in the
2 current instruction and sets signals to enable the appro-
3 priate latched data or ADC data to the ADDRESS BUS in the
4 DATA cycle.

5 The timing during the DATA cycle is such that the
6 ADDRESS bus is set up by the various latch enable or ADC
7 read signals prior to the time when the memory data is
8 read into the DATA LATCH (and other latches as the case
9 may be). Thus the memory has about 2.5 clock cycles for
10 the data to be stable (about 1 μ S), which should be adequate
11 for even slow memories.

12 A network of gates is used to decode the current
13 instruction and assert the appropriate internal control
14 signals for gating signals on to the Address Bus. Also,
15 signals are generated for gating the contents of the Data
16 Bus into the electrode latch, the F2 latch or the amplitude
17 latch at the S2 time, depending on the instruction.
18 Various internal control signals 148 are distributed to
19 parts of the encoder circuit.

20 21 Address Bus Arbitration Logic and Program Counter

22 The memory contains both the program and the data for
23 the mapping between F2 and electrode number and electrode
24 number combined with amplitude data to number of pulses
25 (which will eventually control stimulus strength or dura-
26 tion). Thus provision is made so that the address bus
27 input to the memory may come from the following sources.

- 28 1. Program Counter 2. ADC (8 bits) 3. F2
- 29 latch (latched ADC data) 4. Electrode latch
- 30 plus most significant 5 bits
- 31 of ADC 5. Amplitude latch plus electrode
- 32 latch.

33 The address space is mapped as shown in Fig. 20 and
34 there are also gates to guarantee 1 states when using
35 program counter, ADC input or F2 latch as input on some
36 address bits.

37
38

1 The F2 LATCH 137 (Fig. 19), the A2 LATCH 138 and the
2 ELECTRODE LATCH 136 are all simple gated D-flip-flops,
3 which are loaded in the DATA cycle if the appropriate
4 condition codes are set up in the INSTRUCTION LATCH 134.
5 These latch outputs are gated to the ADDRESS BUS for the
6 whole of the DATA cycle by transmission gates if selected
7 by the instruction decode logic.

8 The PROGRAM COUNTER 135 is a 6 stage synchronous
9 binary down counter which is decremented once each FETCH
10 cycle, and once in the DATA cycle if fixed data is called
11 for. The PROGRAM COUNTER is reset by an internal signal
12 generated from a START pulse in the Internal Timing and
13 State Generator, or by PORN. The most significant bit of
14 the PROGRAM COUNTER is enabled to A10 during the FETCH
15 cycle. In the DATA cycle, and A10D bit from the INSTRUCTION
16 LATCH may be gated to A10 to enable either half memory
17 mapping (except in FIX type instructions).

18 The reason that the PROGRAM COUNTER is a down counter
19 is to reduce the possibility of ADC data intruding into
20 the program space in memory and generating erroneous pulse
21 bursts. Thus, the program always starts at address 7FF
22 (HEX) (the highest address) and goes down to address 783
23 (HEX), then continues from address 3FF (HEX) and down to
24 383 (HEX) for a total program space of 64 bytes. This
25 program space is adequate for even complicated pulse
26 bursts, such as might be used for multiple electrode
27 stimulation.

28 In fact, in this embodiment described here, it is
29 possible to determine the most significant bit of the
30 starting address of the program (i.e., A10) by strapping
31 an externally available pin to either logic high or low.
32 This has the advantage that it is possible to configure
33 the EPROM with two different programs in it, which may be
34 chosen by the user. For example, two different programs
35 may be established for noisy environments, and quiet envi-
36 ronments, or for music or speech, etc. Thus the starting
37 address may be set to be either 7FF (Hex) or 3FF (Hex).

38

1 Since the whole 8 bits of ADC input are not always
2 used, the least significant 3 bits are gated onto the
3 address bus by tri-state buffers enabled by signals gener-
4 ated by the instruction decode logic in response to instruc-
5 tions which require all bits (i.e., F2ADC). This is not
6 shown in the circuit diagram, as anyone skilled in the art
7 could duplicate this function.

8 The A10 bit may come from one of 3 sources:

- 9 1. The LSB of the AMPLITUDE LATCH
- 10 2. The MSB of the Program Counter
- 11 3. The A10D bit in the current instruction
- 12 4. The AD2 bit input of the analog to digital
13 converter.

14 Logic is provided to select between these inputs at
15 the appropriate time.

16 The electrode latch is a 6 bit latch and the six bits
17 of electrode number mapped from F2 input in response to
18 the F2ADC instruction are stored in the latch. Either the
19 upper 5 or lower 5 bits may be enabled to the address bus
20 for an ADCE or A2L instruction by means of an array of
21 multiplexors. This is to allow coding the electrode pulse
22 burst as either $4N+2$ OR $8n+4$ (according to receiver design)
23 without affecting EPROM addressing. The choice of which 5
24 bits are gated to the bus is made by strapping the externally
25 available ELOPT pin to VCC or GND. This logic circuitry
26 is not illustrated in Fig. 19 as it is only incidental to
27 the operation of the encoder.

28 The external address bus is driven by TRI-state bus
29 drivers. Address bits 5, 6, 7, 8 and 9 are put to TRI-state
30 level when the ADC is to be read as the ADC data is then
31 gated to the Address Bus. These output pins are also fed
32 back into the chip for storage in the internal latches as
33 needed.

34 Test Signal Selector (TEST)

35 Because of the limitation on number of pins, it is
36 not possible to have access to all internal signals directly.
37
38

1 However, all important internal signals are brought to
2 three 8 to 1 multiplexers in a Test Signal Selector 152.
3 The select signals for these multiplexers are brought
4 outside, and are labelled TPS0, TPS1 and TPS2. Thus 24
5 internal signals are available using only six pins. In
6 normal operation, TPS0, TPS1 and TPS2 are tied to logical 1,
7 and the signals available to outputs are signals which are
8 useful during normal operation of the encoder.

9 In addition, all address bus pins may be set to
10 TRI-state when the chip is in test mode (i.e., TPS0, TPS1,
11 and TPS2 not all tied to logic 1), and one of the enable
12 lines is asserted. This condition allows access to the
13 address bus externally (e.g., to program the EPROM while
14 in circuit).

15 This is an important feature for the ease of use of
16 the system as a whole, because it eliminates the need to
17 remove the EPROM from the circuit during psychophysical
18 testing of the patient. Apart from the advantages of ease
19 of use, it also means that it is possible to take advan-
20 tage of denser packaging technology (such as leadless chip
21 carriers) which are not amenable to nonpermanent fixation
22 to the printed circuit board in the WSP. In addition, it
23 allows the future possibility of more than one device
24 sharing the same address bus, for example if it was desired
25 to incorporate a microprocessor controlled speech processing
26 strategy, and it was desired to store the controlling
27 memory in the same PROM as the encoder program, and the
28 patient data map.

29

30 SAMPLE PROGRAM FOR SPEECH PROCESSOR ENCODER

31 An example program for sending stimulus frames to the
32 implant is shown below and will be used as the basis of
33 the following discussion. This program will generate a
34 train of pulse burts according to the stimulus pulse frame
35 definition shown in Figure 8. It should be understood
36 that other programs could be used to generate the same
37 stimulus frame, and may be used for different patients
38

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1 (e.g., to generate bipolar stimulation, or stimulus frames
2 with different stimulus pulse lengths--phi 1 and phi2).

4	STEP	ADDRESS (HEX)	EXT	BC1	BC0	RS2	RS1	RS0	A10	MUX	DATA_ MNEMONIC (HEX)
5											
6	1	7FF	0	1	1	0	0	0	0	1	61 FIX
7	2	7FB	0	0	0	0	0	1	0	0	04 CONST 4
8	3	7F7	0	0	1	1	1	1	0	0	3C F2ADC
9	4	7F3	0	1	0	0	0	0	0	0	40 FIX
10	5	7EF	1	1	1	1	1	0	0	0	F8 CONST 248
11	6	7EB	0	1	1	0	0	0	0	0	60 FIX
12	7	7E7	0	0	0	0	1	1	0	0	0C CONST 12
13	8	7E3	0	1	0	0	0	0	0	0	40 FIX
14	9	7DF	0	0	0	1	0	1	0	0	14 CONST 20
15	10	7D7	0	1	1	1	1	0	1	0	7A ADCE
16	11	7D3	0	1	0	0	0	0	0	0	40 FIX
17	12	7CF	0	0	0	1	0	1	0	0	14 CONST 20
18	13	7CB	0	1	1	0	0	0	0	0	60 FIX
19	14	7C7	1	1	1	1	1	1	1	1	FF CONST 255
20	15	7C3	0	1	0	0	0	0	0	0	40 FIX
21	16	7BF	0	0	0	1	0	1	0	0	14 CONST 20
22	17	7BB	0	1	1	0	0	0	0	0	60 FIX
23	18	7B7	1	1	1	1	1	1	1	1	FF CONST 255
24	19	7B3	0	0	0	1	0	0	0	1	11 HALT

19 This program consists of 11 steps. Each step will
20 consist of a FETCH, DATA, and COUNT cycle. The detailed
21 timing for the first step is given, and other steps will
22 have similar timing.

23 The program is initiated by the arrival of a START
24 pulse from the speech processor front end, assuming the
25 encoder is enabled. The START pulse causes the program
26 counter to be reset to 11111, the burst counter is reset
27 to 0, and starts the internal timing and state generator.
28 In the first FETCH cycle the address bus contains 7FF, the
29 address of the first instruction. The contents of this
30 address (61 HEX) are strobed into the instruction latch
31 during the first FETCH cycle. The program counter is
32 decremented at the end of the FETCH cycle.

33 In addition, the encoder and ADC is arranged so that
34 the ADC conversion is initiated when the first instruction
35 is fetched from memory. In this way, the ADC will be
36 converting the value presented to its input at the same
37 time as the encoder is executing the first instruction or
38

1 so. The ADC used is an Analog Devices AD 7574, and has
2 the desirable characteristic that further start convert
3 signals are ignored until the previous data is read.

4 In the data cycle, the instruction is decoded as a
5 fixed data instruction so the program counter is again
6 enabled to the address bus. The contents of the next byte
7 (at 7FB) in the program (04 HEX) are strobed into the data
8 latch during the DATA cycle and the program counter is
9 decremented again at the end of the DATA cycle. The burst
10 counter control bits have been set by the contents of the
11 instruction latch.

12 At the end of the DATA cycle, the COUNT cycle begins,
13 and the burst counter is enabled to count to 4 cycles.
14 After 4 cycles, the equality of the burst counter and the
15 data latch is detected, and a pulse is generated which
16 initiates the next FETCH cycle. These four pulses are
17 output to the OUTP pin and the burst counter is reset at
18 the end. These four cycles transmitted to the receiver/
19 stimulator are the Synch Burst referred to in Figure 8.

20 For step 2, the next instruction (3C HEX) is loaded
21 from address 7F7(HEX) and the program counter is decremented.
22 The data from the ADC is read. The ADC had a conversion
23 started during the first instruction read by the same line
24 which is used to chip enable the EPROM. The output of the
25 ADC (8 bits) is enabled to the address bus bits 2 to 9 as
26 shown in Figure 20, and a number is read from the EPROM at
27 the address so generated. This number will encode the
28 electrode selected as $8*n + 4$, and the number is output as
29 a number of pulses. The electrode number is also stored
30 in the ELECTRODE LATCH during the DATA cycle. The actual
31 electrode selected depends upon the way that the ELSEL
32 signal is mapped into electrode number for this particular
33 patient. A detailed discussion on the mapping algorithms
34 appears later in this disclosure.

35 The number mapped from the F2 ADC input is output as
36 a burst of pulses. At the end of this burst, the burst
37 counter is not reset but is left in the state at which EQ
38

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1 was detected. In step 3, the next instruction (40) is
2 gated into the INSTRUCTION LATCH at the next FETCH. The
3 constant data, 248 is gated into the DATA LATCH during the
4 DATA cycle. The burst counter is enabled to continue
5 counting from its end value to 248 at which time the
6 counter is reset and the next instruction is fetched.
7 Thus the active electrode burst and subsequent inter-burst
8 delay will take the time for 256 clock times, regardless
9 of the actual number transmitted to the receiver/stimulator.

10 Step 4 will result in the transmission of a 12 pulse
11 burst which, in this example, will code the stimulation
12 mode as 1, or multipolar. Other stimulation modes could
13 be used. Step 4 is followed by a constant period of no
14 output with the FIX instruction in Step 5 to provide the
15 inter-burst delay.

16 In Step 6, the instruction is ADCE, and the 5 bits in
17 the electrode latch are gated to Bits 4 to 0 of the address
18 bus in bit reversed order as shown in Figure 20, and the 5
19 most significant bits of the ADC output are gated to bits
20 9 to 5 of the address bus. The data at the location in
21 EPROM will then code the stimulus amplitude for the selected
22 electrode at the value of the input signal (STAMP) repre-
23 sented by the number read from the ADC. Step 7 generates
24 the interburst delay for the delay after the amplitude
25 burst generated in Step 6.

26 Steps 8, 9 and 10 generate the Phi 1 and Phi 2 times
27 which, in this example, are shown to be 255 clock pulses
28 long, although other Phi 1 and Phi 2 times could be chosen.

29 Finally, the last instruction in Step 11 is a HALT
30 instruction. This instruction causes the encoder to stop
31 sending data, and also reads the ADC to make sure that the
32 ADC is ready to begin a conversion on the first instruction
33 fetch of the next pulse frame. In addition, as shown in
34 this example, the HALT instruction changes the state of
35 the MUX bit so that the data presented to the ADC for the
36 start of the next frame will be ELSEL. Note that the MUX
37 bit is caused to change value with Step 1 of the program,
38

1 so that the next ADC conversion (for amplitude burst) will
2 cause the conversion of the STAMP signal. The MUX bit
3 operates a signal control line to select one of two analog
4 signals to the ADC convertor as shown in Figure-17.
5

6 OUTPUT STAGE

7 The output stage is a Class D RF output stage using
8 two enhancement mode power Field Effect Transistors (FETs),
9 and is illustrated in Fig. 21. The signal 'OUTPUT' from
10 the Encoder is level shifted from the logic levels of the
11 encoder by a capacitor 200 and resistor 201. An N channel
12 FET 204 selected to have a low ON resistance and a thresh-
13 old of less than the logic swing is turned on by this
14 level shifted signal. The drain of the FET is connected
15 to the coil 207 worn by the patient by a coaxial cable
16 205. A capacitor 206 is selected to tune the coil. The
17 value of the capacitor depends upon the length of the
18 coaxial cable, as the parallel capacitance of the coaxial
19 cable itself will contribute to the tuning capacitance.

20 The other end of the coil is connected to the most
21 positive supply. When the N channel FET turns on, current
22 is sunk through the coil. When this FET turns off, the
23 voltage across the coil rises sinusoidally to about 35
24 volts. The timing and tuning is arranged such that the
25 voltage across the coil is thus typical of a Class D
26 output stage, consisting of half sine wave shaped pulses,
27 of about 35 Volt amplitude.

28 A P channel enhancement mode FET 202 is in parallel
29 with the coil via a silicon diode 203. This FET is turned
30 on, and thus short circuits the coil, when the DAMP signal
31 from the Encoder is asserted. The purpose of this is to
32 damp out any residual oscillations in the tuned circuit
33 system at the end of each burst so that the correct number
34 of pulses will be received by the implanted receiver/
35 stimulator.

36 The design of the coil takes into account many factors,
37 such as:
38

- 1 1. The number of turns such that the turns ratio from
2 the external coil to the internal coil yields the
3 correct voltage at the receiver/stimulator.
- 4 2. The inductance to give the correct resonant frequency,
5 with high Q for high efficiency, not requiring too
6 large a tuning capacitor.
- 7 3. The diameter to give the best coupling efficiency to
8 the internally worn coil, and to allow some lateral
9 tolerance in position of coil.
- 10 4. The construction, so that the coil may be of simple,
11 flat construction, to allow the coil to be worn
12 inconspicuously under the patient's hair, over the
13 site of the implant.
14

15 Diagnostic and Programming Unit and Interface Unit

16 The Diagnostic and Programming Unit (DPU) and Interface
17 Unit (IU) are used together with a Wearable Speech Processor
18 during the testing of the patient's psychophysics, and to
19 set up the program and map in the WSP. The DPU is a
20 conventional, off-the-shelf microcomputer system, to which
21 software has been added. The IU is a specially designed
22 device to interface between the DPU and the WSP.

23 The DPU has available a communications interface
24 which enables communication between it and the IU. In the
25 embodiment described here, a 16 bit parallel communications
26 link is used, but other formats or configurations could be
27 used equally well, such as serial, or parallel with a
28 different width of the data path.

29 As described in the previous section, the WSP encoder
30 works by fetching instructions from the EPROM in the WSP,
31 and mapping the incoming formant data (F2 and A2) from the
32 speech processor front end into the appropriate selection
33 of electrode and amplitude to be sent to the implanted
34 receiver stimulator. The algorithms for mapping are
35 discussed in a subsequent section. During testing and
36 setup of the patient's WSP, the following functions must
37 be performed:
38

- 1 1. Presentation of known and controlled stimuli to the
2 patient, on nominated electrodes. The stimuli result
3 in a response from the patient which is recorded.
4 Several tests such as measurement of thresholds,
5 pitch ranking of electrodes, and loudness scaling of
6 stimulus intensity are performed.
- 7 2. Use of the psychophysical data obtained from the
8 tests above to generate a map between F2 and electrode
9 to be stimulated, and A2 and amplitude of stimulation
10 on each electrode.
- 11 3. Test the map so generated using the patient's own
12 speech processor using live audio input, such as
13 speech.
- 14 4. If suitable, install this program and data into the
15 PROM on the WSP. This involves erasing any data
16 which may have been previously in the PROM, and
17 programming the PROM with the new data which has been
18 generated on the basis of the patient's psychophysical
19 testing results.

20 A block diagram of the Interface Unit is shown in
21 Fig. 22. The IU is a microprocessor based device with
22 conventional structure. A processor 220 which is a Z80 in
23 this embodiment but which could be any of a number of
24 available processors, is the heart of the machine, and
25 drives a Data Bus, Address Bus, and a number of control
26 lines referred to as a Control Bus. System memory 221
27 comprises ROM and RAM, with necessary associated memory
28 decoding and interfacing circuitry.

29 A system event clock 222 is used for timing of events
30 such as presentation of stimuli, or time of erasure of the
31 PROM. A parallel communications interface 224 comprising
32 16 input and 16 output lines 225, with associated hand-
33 shaking lines, allows communication with the DPU. The
34 rest of the circuitry is used to control the WSP.

35 The principal of control of the WSP is that the PROM
36 in the WSP is disabled, and a SHADOW RAM 228 is made
37 available to the encoder instead. This RAM appears to the
38

1 WSP like the PROM, and is accessed through the Address,
2 Data and Control Buses on the WSP from the Encoder mentioned
3 in the previous section. However, this RAM may also be
4 accessed by the IU processor, so that the IU can set up
5 any programs or data in the shadow RAM, and thus control
6 the operation of the WSP.

7 Bus arbitration logic 231 is used to arbitrate between
8 the WSP or the IU processor for access to the shadow RAM.
9 It is possible to disable the address bus on the Encoder
10 by using the test signal selectors mentioned in the section
11 on the encoder. The WSP data bus is input only to the
12 Encoder. The bus arbitration logic thus disables the
13 encoder address bus, and disables the WSP PROM to make the
14 shadow RAM available to the IU processor, by enabling an
15 address bus switch 230 and a data bus switch 229. At the
16 same time, the Encoder itself is disabled to prevent
17 generation of any stimulus frames which might contain
18 spurious data and present unwanted stimuli to the patient.

19 The WSP uses the time varying data from the speech
20 processor front end to map and encode electrode number and
21 stimulus amplitude. When using the IU, it is necessary to
22 be able to present stimuli which are also time varying.
23 The way this is done is by use of an 8 bit latch 227 which
24 is loaded from the IU processor. In normal operation of
25 the encoder, when variable data is required, the ADC value
26 is input to the address bus, and the output data appears
27 on the data bus from the PROM. The mapping between the
28 variable ADC address, and the output data to be sent to
29 the implant, is fixed in the PROM.

30 Under control of the IU, the bus arbitration logic
31 determines when an ADC read is to occur by decoding the
32 WSP control lines. At this time, the WSP PROM, and the IU
33 shadow RAM are disabled, and the 8 bit data latch is
34 enabled to the data bus. Thus, the IU processor is able
35 to update the data latch on a byte by byte basis to present
36 variable data to the WSP encoder. In other words, the
37 normal process of mapping variable ADC data from an address
38

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1 to data is bypassed. The IU is arranged so that the data
2 in the data latch may be updated on a pulse burst by pulse
3 burst basis, so that it is possible to send bursts with
4 variable numbers of pulses to the implant, under control
5 of the IU via the DPU.

6 The communications protocol between the DPU and the
7 IU is designed in the form of transactions which include
8 hardware handshaking (embedded in the circuit design) and
9 software handshaking, to enhance the reliability of data
10 communications. This is important to make sure that
11 erroneous data received by the IU from the DPU as a result
12 of a hardware fault or 'glitch' in the system will not
13 cause improper stimuli to be delivered to the patient.

14 The normal stimulus protocol for patient testing is
15 to use stimulus sequences where the amplitude of stimulus
16 pulses delivered to the patient follows a trapezoidal
17 waveform. In other words, starting from minimum possible
18 stimulus, rising to the desired stimulus level in a known
19 time and staying at that level for the required time, and
20 then falling linearly to the minimum stimulus again. In
21 order to present this shape of stimulus envelope, the IU
22 processor must be able to update the data latch very
23 rapidly, at the same time as performing other tasks such
24 as communications with the host DPU computer. The software
25 inside the IU is structured to facilitate this, in that
26 all input and output of communications, and also variable
27 data to the encoder, is done via ring buffers in the
28 conventional manner, with output to the data latch awarded
29 the highest priority.

30 In addition, the IU is able to generate the rising,
31 falling and constant sections of the trapezoidal stimulus
32 amplitude envelope with internal software in response to
33 concise instructions from the DPU. This is an important
34 feature as it allows the best economical use of the IU
35 processor, without always tying up the DPU to calculate
36 stimuli on a burst by burst basis. However, it is possible
37 as well to present stimuli in any random fashion where all
38

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1 variable bursts may be set upon on a burst by burst basis
2 from the DPU. This has an advantage in that hitherto
3 unused or unthought of stimuli may be presented in the
4 future if it is found to be useful for psychophysical
5 testing or research.

6 Thus communication transactions between the DPU and
7 IU are defined which include loading and reading the
8 contents of the shadow RAM or WSP PROM; setting up stimuli
9 with controllable time between stimuli, and definable
10 contents of each burst in the frame; and various house-
11 keeping functions such as PROM erasure, reset, and queue
12 management.

13 The process of patient testing is to present stimuli
14 on specified electrodes at known stimulus levels, and
15 question the patient for a response. The stimulus presen-
16 tation is under control of the DPU, from instructions
17 typed in at the keyboard by the user (e. g., an audiologist).
18 The software in the DPU has been carefully written to make
19 it difficult to present stimuli to the patient which may
20 be uncomfortably loud, although the levels able to be
21 presented by the implant are insufficient to be physi-
22 ologically damaging.

23 The patient may be asked to nominate thresholds,
24 comfortable levels, and maximum comfortable levels on each
25 or a subset of electrodes. Another test the patient may
26 be asked to participate in is called pitch ranking, where
27 the patient is asked to rank order psychophysically equally
28 loud stimuli on different electrodes in order of pitch.
29 This pitch ranking process is facilitated by the DPU
30 software which generates random pairs of electrodes to be
31 stimulated, to which the patient is required to nominate
32 if the second is higher or lower in pitch than the first.
33 When all possible pairs have been tested, a confusion
34 matrix may be constructed, and the electrodes are then
35 pitch ranked.

36 An additional test is called Loudness Scaling, where
37 the patient is asked to assign loudness weights to different
38

1 stimuli levels on an electrode (or electrodes), so that
2 the relationship between stimulus current and psychophysical
3 loudness perceptions may be developed.

4 Once the patient testing is complete, the data from
5 the tests is used to generate a map or translation table
6 from VF2 to electrode number, and from A2 to amplitude.
7 This translation process is done by the software in the
8 DPU. One of the powerful features of the system is the
9 ability to use any mapping algorithm between acoustic
10 signal parameters and stimulation parameters merely by
11 altering the software in the DPU. Thus, as experience
12 with cochlear implants accrues, and more psychophysics
13 information is available, more stimulation strategies or
14 mapping algorithms may be adopted to advantage. The
15 mapping algorithms used in this embodiment are discussed
16 in detail in a subsequent section.

17 The map so generated must be programmed into the PROM
18 in the patient's WSP. Thus it is necessary to be able to
19 erase and reprogram the PROM in the patient's WSP. One
20 way of doing this would be to have the operator (e.g.,
21 audiologist) remove the PROM from the speech processor,
22 erase using conventional erasing devices, and program the
23 PROM using conventional programming equipment. However,
24 it would be an obvious advantage if this error prone
25 process could be avoided, and thus circuitry is included
26 in the IU to enable erasing and reprogramming of the EPROM
27 while still plugged into the WSP.

28 The ability to erase and reprogram the PROM without
29 removing it from the WSP has the following advantages:
30 1. less error prone process, as unskilled people are not
31 required to handle delicate electronic components;
32 2. more reliable construction possible, as the PROM may
33 be permanently soldered into the circuit. In addition,
34 it makes it possible to take advantage of newer
35 packaging technologies (such as leadless chip carriers)
36 which will allow a reduction in the size of the WSP;

37
38

- 1 3. more robust construction of the WSP, as the only
- 2 externally accessible parts required are battery
- 3 access and the connector for connection to the IU. A
- 4 small window for exposure to ultraviolet light for
- 5 PROM erasure may easily be incorporated in the WSP
- 6 case; and
- 7 4. less internal volume required in the WSP as a PROM
- 8 socket is not required.
- 9

10 MAPPING OF ACOUSTIC PARAMETERS TO STIMULATION PARAMETERS

11 One of the most powerful features of the system

12 described in this disclosure is the ability to configure

13 the system on a patient to patient basis. After implanta-

14 tion, the patient is tested with the DPU/IU system to

15 measure the patient's psychophysical characteristics.

16 These characteristics are used to generate a map between

17 acoustic signal parameters and stimulation parameters,

18 which is stored in an EPROM in the patient's own wearable

19 speech processor. In essence, the psychophysical variables

20 are separated from the acoustic variables, with the link

21 being through the map.

22 In generating the map, two major parameters are of

23 importance. These are the selection of electrode based on

24 F2 frequency, or the way in which the electrodes are

25 allocated portions of the frequency spectrum; and the way

26 in which acoustic stimulus level (or acoustic loudness) is

27 mapped into electrical stimulus level which results in

28 perceptual loudness.

29 As mentioned above, advantage is taken of the tonotopic

30 arrangement of electrodes spaced along the basilar membrane.

31 Thus it should be the case that electrodes further from

32 the round window (the apical electrodes) will elicit the

33 lowest frequency percepts, and electrodes closest to the

34 round window (the basal electrodes) will elicit the highest

35 frequency percepts and the perceived frequency should

36 increase in a monotonic function from low to high from

37 apical to basal. In an ideal system, equally spaced

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1 electrodes should be allocated logarithmically equal
2 portions of the acoustic spectrum of F2 range. Thus, for
3 an F2 range from about 800 Hz to about 3kHz, each of the
4 22 electrodes used in this embodiment would have about a
5 tenth of an octave allocated to it. The Output of the WSP
6 front end produces an F2 signal which is a voltage linearly
7 proportional to F2 frequency. In order to provide equal
8 logarithmic frequency separations of electrodes, it is
9 thus necessary to map the linear F2 signal logarithmically,
10 and 8 bits of precision in the ADC is needed to do this.

11 However, the situation is complicated in real life,
12 because it is sometimes necessary to allocate nonequal
13 frequency portions to electrodes. For example, it may be
14 found that a patient may not have all electrodes operating
15 correctly, for example due to an absence of functioning
16 nerve fibers in one part of the basilar membrane. Thus an
17 equal logarithmic partitioning of the frequency spectrum
18 would be inappropriate, and a different scheme would be
19 necessary. The system described herein has the powerful
20 feature that any arbitrary allocation of frequency bands
21 to electrode (provided that bands are not overlapping) in
22 the map, and the DPU allows this allocation to be made.
23 Since the assignment of frequency bands to electrodes is
24 done by merely placing the appropriate numbers into the
25 EPROM in the WSP, this may be done according to a number
26 of mapping algorithms.

27 The second facet of mapping is the scaling of acoustic
28 loudness to stimulation current. This is a particularly
29 complicated subject, particularly in this embodiment where
30 the subject of acoustic to psychophysical mapping is
31 obscured by the AGC and Squelch characteristics of the WSP
32 front end, and the nonlinear circuits used in the WSP
33 front end to generate the STAMP signal. The DPU/IU system
34 can be used to present stimuli of various current level to
35 the patient on selected electrodes to determine the threshold
36 level (i.e., the lowest level at which stimulation is
37 reliably perceived), and maximum comfortable loudness,
38

1 which is the maximum stimulus level which the patient can
2 tolerate for sustained periods. The problem then becomes
3 one of mapping the acoustic signal range as represented by
4 the STAMP signal into this stimulation range.

5 One way of generating this map is to present stimuli
6 to the patient at all possible levels between threshold
7 and maximum comfortable loudness, and ask the patient to
8 scale the perceived loudness, e.g., on an arbitrary scale
9 between 1 and 100. This loudness scaling data may then be
10 incorporated into the map so that acoustic loudness is
11 correctly represented to the patient as perceived loudness.
12 The software required in the DPU to perform this is quite
13 straightforward.

14 However, the time required to perform these tests is
15 great, as each electrode must have loudness scaling tests
16 performed individually. We have found from measurements
17 on a number of patients that it is adequate to model the
18 loudness growth function between stimulus level and perceived
19 loudness analytically, and use this to generate the map.
20 Thus the loudness mapping between acoustic loudness,
21 stimulus level, and perceived loudness can be generated
22 sufficiently accurately by measurement only of threshold
23 and comfortable levels.

24 Assume a function between perceived loudness, L , to
25 the stimulus charge delivered, c . For constant width
26 pulses (Φ_1 and Φ_2 equal, and constant), the charge
27 delivered is related to stimulus current, i , and a power
28 law is assumed, thus

29
$$L = k * i^x$$
 where k and x are constants, with x
30 found to be in the order of 10. Thus

31
$$\log(L) = \log(k) + x \log(i)$$
. The stimulus current
32 i , and the number encoded into the stimulus amplitude
33 burst length, C , are related by another power law. This
34 power law is determined by the stimulator integrated
35 circuit characteristics and choice of components, and is
36 approximately

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1 $i = a \cdot b^C$ and $a \cdot b^C = 2$ mA approximately, when
 2 the number transmitted is 0, and a is a constant and b is
 3 the ratio of successive current steps, (about 0.97).
 4 Actually, the exponent should be not C but C-16 since the
 5 programmable current generator circuit requires 16 pulses
 6 to start up, but this factor is ignored for the moment, as
 7 it represents a constant to be added to the number to be
 8 stored in the map. Thus,

9 $\log(i) = \log(a) + C \cdot \log(b)$ The amplitude of the
 10 second formant, A, is related to the loudness of the
 11 acoustic second formant signal, L', by a power law

12 $L' = d \cdot A^{0.6}$ where d is a constant and the
 13 exponent, 0.6 has been determined experimentally and
 14 published, as will be known by those skilled in the art.

15 The speech processor must relate the current level C,
 16 to the measured amplitude, A. Thus a relationship between
 17 the loudness of the input signal, L', and the perceived
 18 loudness, L, must be proposed. The simplest one is $L' = L$,
 19 and could be used. This implies that the patient is being
 20 presented with a stimulus level which is an analogue of
 21 the speech amplitude at the AGC output, not the original
 22 speech signal.

23 Combining the above equations yields

24 $\log(L) = \log(k) + x \cdot (\log(a) + C \cdot \log(b))$

25 $= f + g \cdot C$ where f and g are constants to
 26 be determined from the loudness scaling data on each
 27 particular patient. However, tests on a number of patients
 28 allow the constant f and g to be determined empirically,
 29 and are used with the threshold and maximum comfortable
 30 levels determined for each electrode to establish the
 31 mapping between acoustic level and stimulus amplitude.

32 The system as described herein has provision for only
 33 31 loudness levels to be mapped into the range of stimulus
 34 levels between threshold and maximum comfortable loudness
 35 level. Experiments have shown that this should be adequate.
 36 However, the system is not limited to varying stimulus
 37 level by varying stimulus current alone, as it is also

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1 possible to change the amount of delivered charge in the
2 stimulus by altering the durations of Phi 1 and Phi 2.
3 Different scaling algorithms, or different speech processing
4 strategies as may be discovered in the future could use
5 this mechanism of varying stimulus level to achieve finer
6 control. The design of the encoder chip allows any or all
7 of the bursts to be sent to the receiver/stimulator to be
8 variable, and thus different mapping or encoding strategies
9 may be easily developed.

10 An additional part of the Diagnostic and Programming
11 System not shown in the Figures is a means for acoustically
12 monitoring the information output of the speech processor
13 which is transmitted to the implantable receiver/stimulator.
14 The purpose of such a device is as a troubleshooting aid,
15 for when a patient reports a malfunction. The audiologist
16 is able to apply the patient's own speech processor and
17 coil to a simulator, and listen to an acoustic simulation
18 of the stimulator output. In addition, in our embodiment,
19 the simulator includes a display of which electrode is
20 being stimulated for each stimulation frame. This feature
21 allows a visual interpretation of the extent of use of
22 each electrode, and may assist the audiologist in best
23 configuring the pitch ranking of the map to make best use
24 of the available electrodes in the acoustic environment.

25 In its simplest embodiment, such a simulator comprises
26 a complete receiver/stimulator circuit as described in
27 this invention. However, instead of the outputs of the
28 receiver stimulator being connected to an electrode array,
29 each output is connected via a light emitting diode to a
30 dummy load such as a pair of headphones. Thus, when each
31 stimulation pulse comes along, the active electrode will
32 cause the LED associated with it to be illuminated for the
33 duration of Phi 1 or Phi 2 (depending on polarity), and a
34 sound pulse will be heard in the headphones, with the
35 intensity of the sound proportional to the stimulation
36 current.

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1 Other embodiments have also been built which use
2 conventional readily available integrated circuits to
3 decode the data stream as defined in Figure 8 to illuminate
4 an indicator showing selected electrode, and to generate
5 an auditory pulse whose amplitude is related to coded
6 stimulus current amplitude. It is also possible to incorporate
7 circuitry (such as a number of tuned filters) to generate
8 a pulse burst at a frequency proportional to electrode
9 selected to give an indication of frequency percept to be
10 expected from the patient.

11

12 SAFETY FEATURES

13 Several features of the system combine to prevent
14 painful or uncomfortable stimuli to the patient or incorrect
15 stimuli, e.g., wrong electrode:

- 16 1. In terms of gross safety, because the system is
17 powered externally through an inductive link, it is
18 physically impossible to transmit enough power to
19 electrocute the patient.
- 20 2. In terms of prevention of harmful stimuli, several
21 factors play a part:

22 The amplitude pulse burst is coded so that
23 more pulses equal lower amplitude. Thus there
24 is an absolute maximum current which can be
25 delivered, as set by the minimum width pulse
26 burst, and any communication link errors (which
27 usually result in extra pulses) will result in
28 lower current.

29 The comfortable levels for each electrode
30 for each patient are measured after implantation
31 using the WSP, DPU and IU. This maximum level
32 is then stored in the map in the WSP and thus it
33 is not possible to encode stimulus current
34 greater than the maximum comfortable level, no
35 matter what acoustic input is received.

36 Because the same current source is used for
37 Phi 1 and Phi 2, and the durations are (equal
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1 and) set by the program in the EPROM in the WSP,
2 excellent charge symmetry is maintained. This
3 is further improved by shorting all electrodes
4 together when not stimulating. Thus, over long
5 time scales, electrode corrosion will not be a
6 problem.

- 7 3. The prevention of delivery of incorrect stimuli is
8 achieved also with several means in addition to those
9 mentioned above:

10 The information bursts which must communicate
11 numbers (i.e., electrode select and mode select
12 bursts) are encoded to be tolerant of the wrong
13 number of pulses received.

14 The receiver stimulator has circuits to
15 detect the power supply voltage, and delivery of
16 stimulus is inhibited if insufficient voltage is
17 available to provide voltage compliance for the
18 current to be delivered.

19 The receiver/stimulator has circuits to
20 detect the correct sequence of pulse bursts. If
21 the correct sequence is not detected, then
22 stimulation is inhibited.

23 Thus, it can be seen that there is a combination of factors
24 which act to prevent harmful, incorrect, or unwanted
25 stimuli.

26 The above description of embodiments of this invention
27 is intended to be illustrative and not limiting. Other
28 embodiments of this invention will be obvious to those
29 skilled in the art in view of the above disclosure.

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THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:-

1. A cochlear implant system having a speech processor located external to a patient's body, said speech processor including a configureable sound-to-stimulation encoding means, a body-implantable receiver-stimulator for receiving transmitted electrical signals from said encoding means and an electrode array implantable in the cochlea of a patient for conducting electrical signals from said receiver-stimulator means to said cochlea characterized by:-

- i) means for performing psychophysical testing on the auditory nervous system of the patient while said receiver-stimulator is receiving said electrical signals,
- ii) means, using the results of said testing, for preparing data in a map representing a patient stimulation strategy,
- iii) means for converting audio signal information to electrical signals in said sound-to-stimulation encoding means for that patient, and,
- iv) means for erasably programming and storing said mapped data in said encoding means, such that stimulation parameters for speech signals are optimized utilizing said stored data to enhance the ability of the patient to recognize speech signals.

2. The cochlear implant system of claim 1 including patient operated controls in said testing means for



determining stimulation thresholds and comfort levels.

3. The cochlear implant system of claim 1 in which said sound to stimulation encoding means includes memory means for storing a configuration of said configureable sound to stimulation encoding means.

4. The cochlear implant system of claim 3 in which said memory means is an erasable programmable read-only-memory.

5. The cochlear implant system of claim 1 in which the means for performing psychophysical testing include means for stimulation, logging, display, and storage of the results of providing a plurality of electrical stimulation inputs to the auditory nervous system of a patient.

6. The cochlear implant system of claim 1 in which the means for performing psychophysical testing includes means for determining the mapping between acoustic parameters and stimulation parameters, and means for testing the mapping before incorporating the mapping into the patient's stimulation encoding means.

7. A multichannel cochlear prosthesis system for use with a patient comprising:

- i) a multichannel electrode array suitable for implantation in the ear of a person,
- ii) a multichannel stimulator connected to said electrode array, said stimulator being suitable for implantation in said person and being used to provide electrical signals to stimulate said electrode array,



- iii) means for encoding sound to an electrical stimulation signal, said means for encoding being suitable to be worn externally by said person,
- iv) means for transmitting encoded electrical signals representative of speech stimulation parameters from said means for encoding to said multichannel stimulator,
- v) means, external to the patient, for testing the patient's psychophysical responses to stimulation of the patient's auditory nerves by selected electrical signals applied to said electrode array by said multichannel stimulator through the means for encoding,
- vi) means for mapping the psychophysical responses in the form of data of the patient to stimulation of the patient's auditory nerves by said selected electrical signals applied to said electrode array by said multichannel stimulator through said means for encoding to optimize the ability of the patient to perceive certain sounds, and,
- vii) means for storing data from the results of said responses in said means for encoding to encode said data, said results being utilized to determine a relationship between auditory input and said electrical stimulation parameters to optimize the ability of the patient to perceive sounds.



8. The system of claim 7 in which said electrode array comprises series of spaced platinum rings fixed on a flexible strip carrier of tapering diameter.

9. The system of claim 7 including means in said stimulator for providing a leakage current to electrodes not selected for stimulation of less than 10 microamps.

10. The system of claim 7 in which said electrodes are stimulated with a biphasic constant current thereby to provide zero D.C. current to the electrodes and substantially prevent corrosion problems.

11. The system of claim 7 including selection means for selecting bipolar stimulation from any pair of said electrodes in said array.

12. The system of claim 11 in which said selection means is contained in said encoding means.

13. A multichannel cochlear prosthesis system comprising:

- i) a patient implantable tissue stimulating multichannel electrode array,
- ii) a patient implantable multichannel stimulator connected to said array,
- iii) a patient externally worn sound-to-electrical signal stimulation encoding means said encoding means including memory means programmable after implantation of said electrode array and said stimulator in a patient,
- iv) means for programming said memory means based on



the patient's auditory perceptions in response to various electrical stimulating pulse signals,

- v) means for transmitting electrical stimulation signals representing speech parameters from said encoding means to said stimulator and to said array for stimulating tissue in accord with said programmed perceptions, and,
- vi) means for controlling said stimulator by said encoding means, such control including varieties of at least one or more of pulse rate, pulse amplitude, pulse duration, interval between phases of a biphasic current pulse, and selection of which two of any electrodes stimulus current is to be applied.

14. The system of claim 13 wherein the selection of which two electrodes are to be used for stimulation is done in the external sound to stimulation encoding means.

15. The system of claim 13 wherein said memory means is a programmable read-only-memory.

16. The system of claim 13 wherein said memory means is an erasable programmable read-only-memory.

17. The system of claim 13 including means in the encoding means for preventing the delivery of uncomfortable stimuli to the patient.

18. The system of claim 17 wherein said means for preventing delivery of uncomfortable stimuli comprises a data map stored in said encoding means wherein the maximum



allowable electrical stimulus to the patient capable of being generated by the data in said data map is beneath the level which causes discomfort.

19. The system of claim 17 wherein said means for preventing delivery of uncomfortable stimuli comprises means for providing a common current source for biphasic current stimulation of equal duration and amplitude.

20. The system of claim 13 wherein said means for programming said memory means is separably attachable to said encoding means when it is desired during patient testing to configure or reconfigure the memory means based on the patient's perceptions.

21. The system of claim 13 wherein said means for programming the memory means includes means to select subsets of up to all of the electrodes in said array to be used for stimulation in response to a given auditory input signal.

22. The system of claim 13 including means to select the order of pitch ranking of the electrodes in the array and to configure the encoding means in response to the patient's selections of such rankings.

23. The system of claim 13 including means for simultaneous independent selection of particular electrodes for stimulation, the stimulation rate and stimulation amplitude for each stimulation.

24. The system of claim 20 wherein said means for programming the memory means further includes acoustic stimulation means for monitoring the stimulus signals delivered to the implanted stimulator.



25. The system of claim 13 further including means for displaying continuously a visual indication of the two electrodes selected by the transmitted data from the sound to stimulation encoding means for the purpose of monitoring.

26. The system of claim 13 further including means in the sound to stimulation encoding means for generating information leading to the application of a known and unvarying train of stimulus pulses from the implantable stimulator to selected electrodes to verify operation of the system.

27. The system of claim 13 in which said means to control the stimulator by said sound to stimulator encoding means includes means to transmit power and data and means to receive power and data, said means to receive power and data including a receiver coil means, said coil means being tunable.

28. The system of claim 27 in which said receiver coil means is coupled via a transformer to a power and data circuit in said stimulator.

29. The system of claim 13 including means in said encoding means for permitting selection of various stimulation strategies.

30. The system of claim 29 wherein in said encoding means encoding of sound is oriented to speech; said speech comprising frequency domain groupings termed formants and including a second speech formant; and wherein the frequency of the second speech formant is encoded into electrode selection, voicing frequency of said speech is encoded into



stimulation rate and the amplitude of the second speech formant is encoded into stimulation amplitude, and wherein each encodation is made in said encoding means.

31. The system of claim 29 wherein in said encoding means the encoding of sound is oriented to speech; said speech comprising frequency domain groupings termed formants and including a second speech formant; and wherein the frequency of the second speech formant is encoded into stimulation rate and the amplitude of the speech in total is encoded into stimulation amplitude and wherein each encodation is made in said encoding means.

32. The system of claim 22 or 23 wherein said means for programming said memory means is utilized to allow choice of an optimal speech processing strategy.

33. The system of claim 13 including means in said encoding means to generate a signal to deactivate the sound to stimulation encoding means during periods of relatively constant acoustic signal.

34. The system of claim 13 including means for configuring the program in said memory means for different patient psychophysical variables.

35. The system of claim 13 including means for preventing operation of said encoding means if an inadequate power supply voltage is present so as to prevent spurious pulses being transmitted to said stimulator.

36. The system of claim 13 including means for preventing of delivery of stimuli by the stimulator to the electrode array if a power supply voltage to said stimulator



is insufficient to give required voltage compliance to said electrode array.

37. The system of claim 13 including means for programming the memory means while the memory means is connected to said encoding means.

38. The system of claim 13 including pulse burst forming means in said encoding means and means to control said pulse burst forming means, said control means including said memory means indicative of the patient auditory perceptions in response to electric stimuli perceived.

39. The system of claim 38 in which said encoding means and said implantable stimulator comprise integrated circuits, the circuit of said encoding means being programmed to produce sequences of constant frequency pulses with the number of pulses and time between pulse bursts being determined by either of said control means.

40. The system of claim 38 wherein said pulse bursts are formatted in successive frames of data bursts, each frame comprising a reset start burst, an active electrode select burst, an electrode configuration mode burst, an amplitude burst, and two bursts for the two phases of stimulation pulses, and means to provide a time interval between each of said bursts within each said frame.

41. The system of claim 40 further including means to minimize energy consumption by said stimulator to allow said stimulator to be in an active state when subsequent stimulus data frames are transmitted, so as to eliminate the need for a start power pulse in every stimulation frame.



42. The system of claim 38 including a frame of data bursts including two phase simulation bursts of constant time duration.

43. The system of claim 38 further including means in said encoding means to determine amplitude of said electrode stimulus current and means in said encoding means to code said amplitude in a pulse burst such that increasing the duration of said pulse burst decreases amplitude of said electrode stimulus current.

44. The system of claim 13 wherein said stimulator comprises a digital circuit including an error detection circuit to generate signals to a state counter, means to reset said counter, said state counter being incremented through frame sequences of data bursts from said encoding means by a signal asserted at the end of every data burst other than reset.

45. The system of claim 16 further including means to erase and reprogram said memory while it is plugged into said encoding means.

46. The system of claim 13 wherein said means for programming said memory means is tailored to each patient's perceptions and said memory means is programmed to reflect said perceptions.

47. The system of claim 46 further including means in said sound to stimulation encoding means for selecting a subset of from two to all of said electrodes for stimulation.



48. The system of claim 13 further including means for providing a monotonic substantially exponentially decreasing relationship between a coded current amplitude of a stimulus to said electrodes and the actual current delivered to said electrodes.

49. The system of claim 48 including means for limiting the maximum current to be delivered to said electrodes.

50. The cochlear system of claim 13 further including means in said encoding means for disabling the generation of speech stimulation signals during a delay period of constant background noise.

Dated this 2nd day of March, 1990.

COMMONWEALTH OF AUSTRALIA

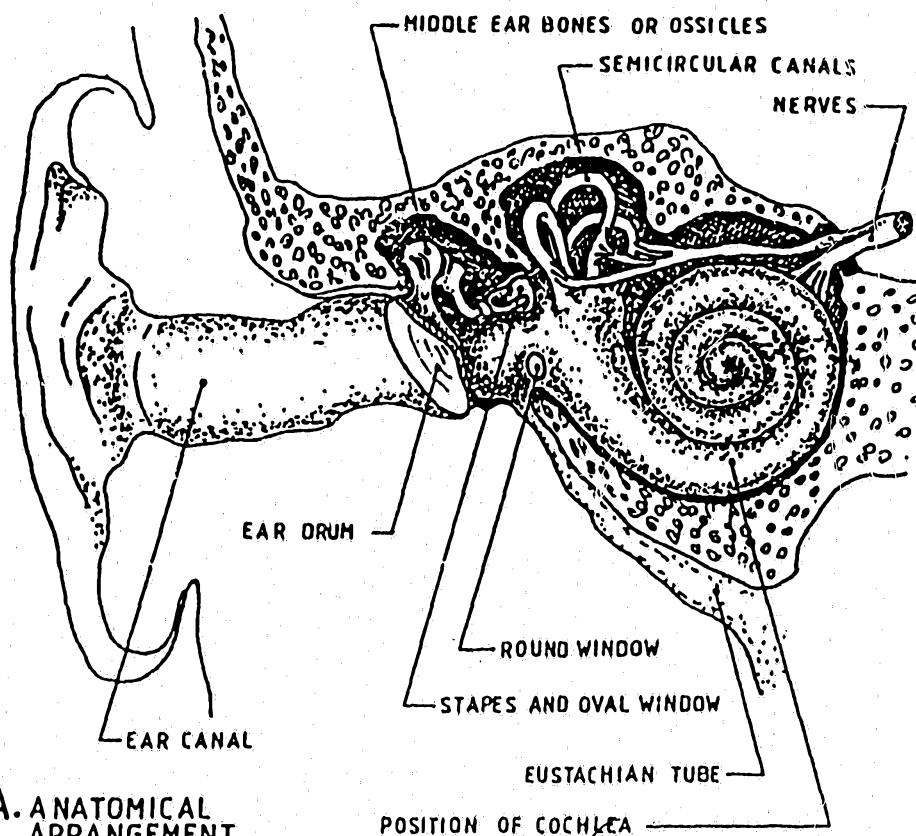
by their Patent Attorneys:

PETER MAXWELL & ASSOCIATES.

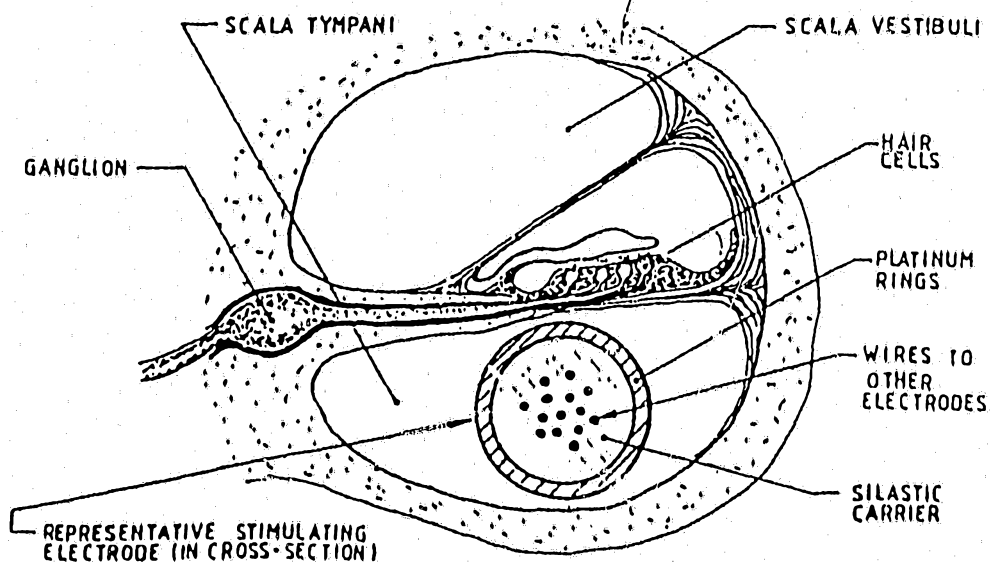
P.F. Maxwell



com/841188



A. ANATOMICAL
ARRANGEMENT



B. COCHLEA IN CROSS-SECTION

FIG.1 The Cochlea

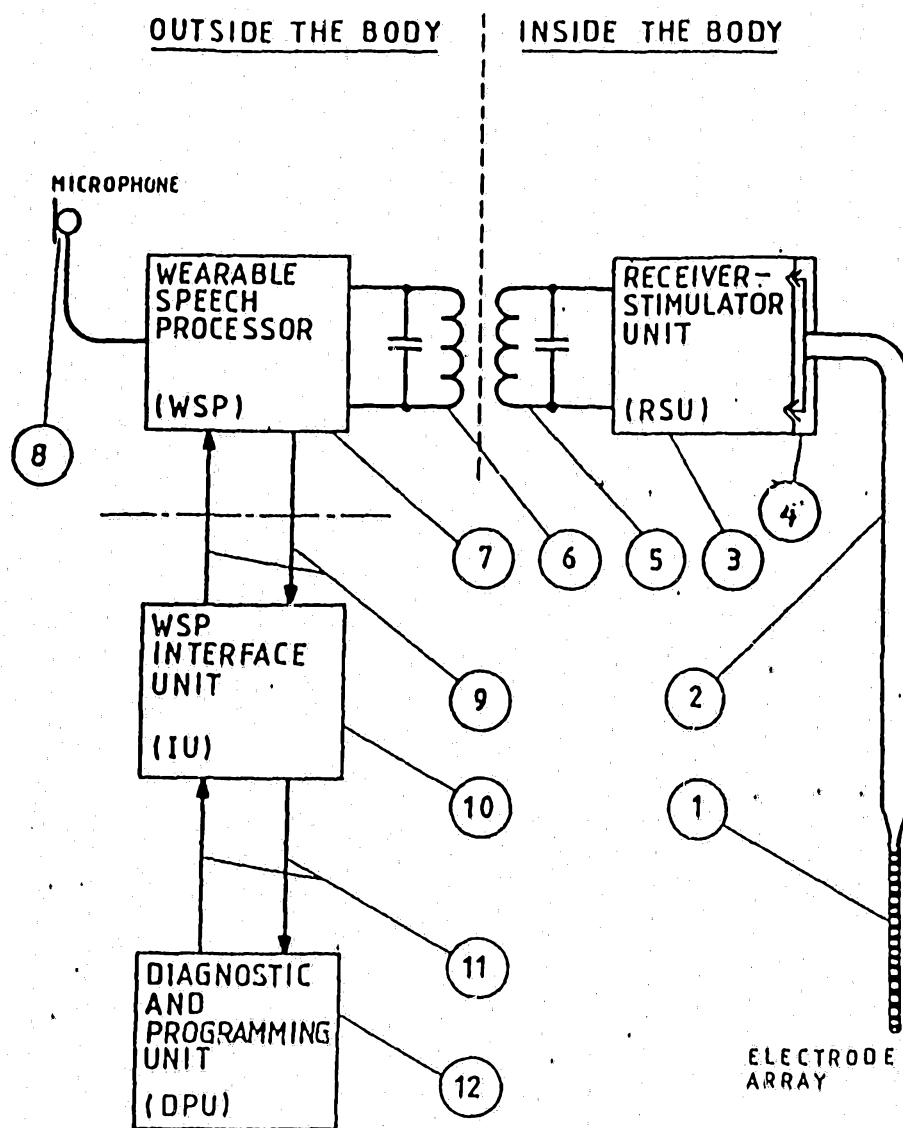
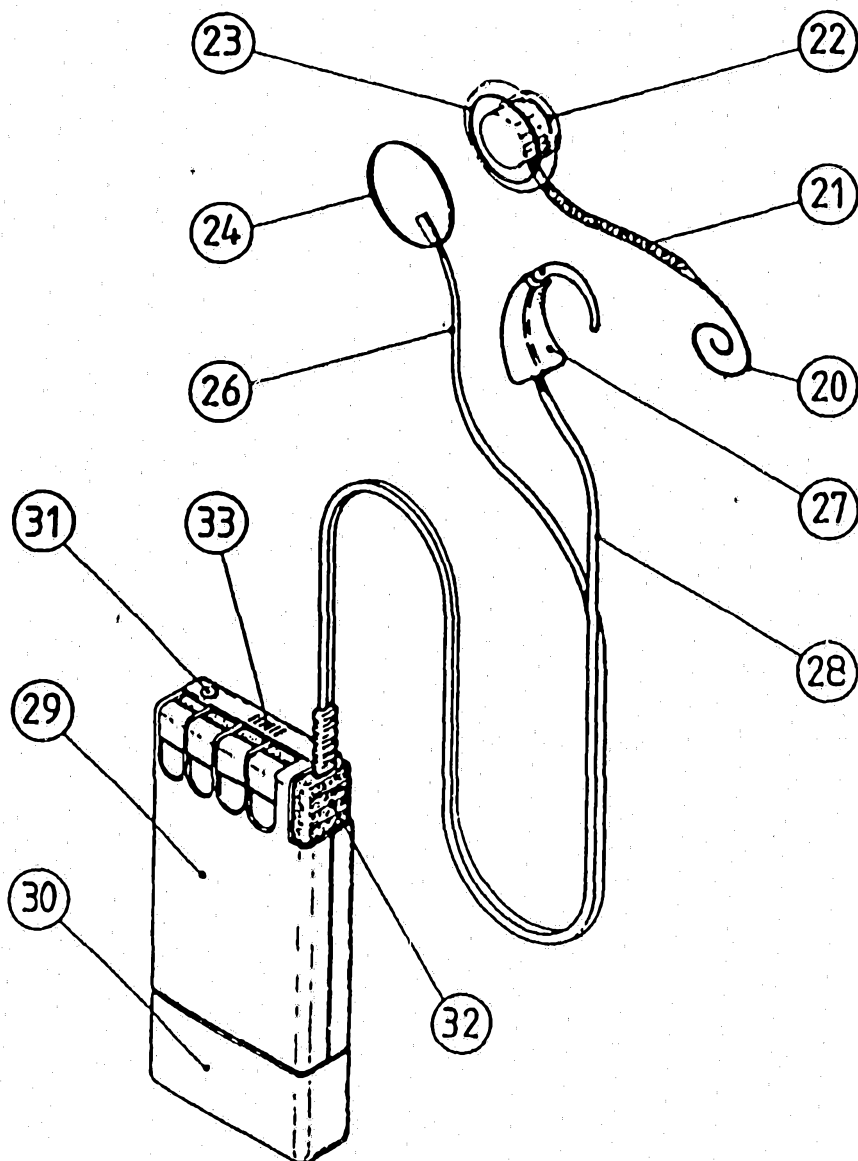
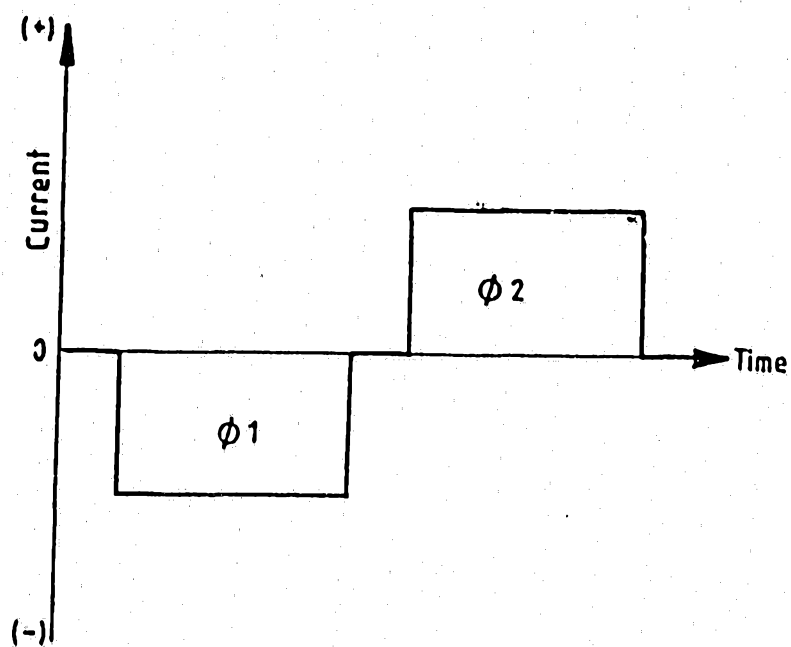


FIG.2 Cochlea Implant System Block Diagram

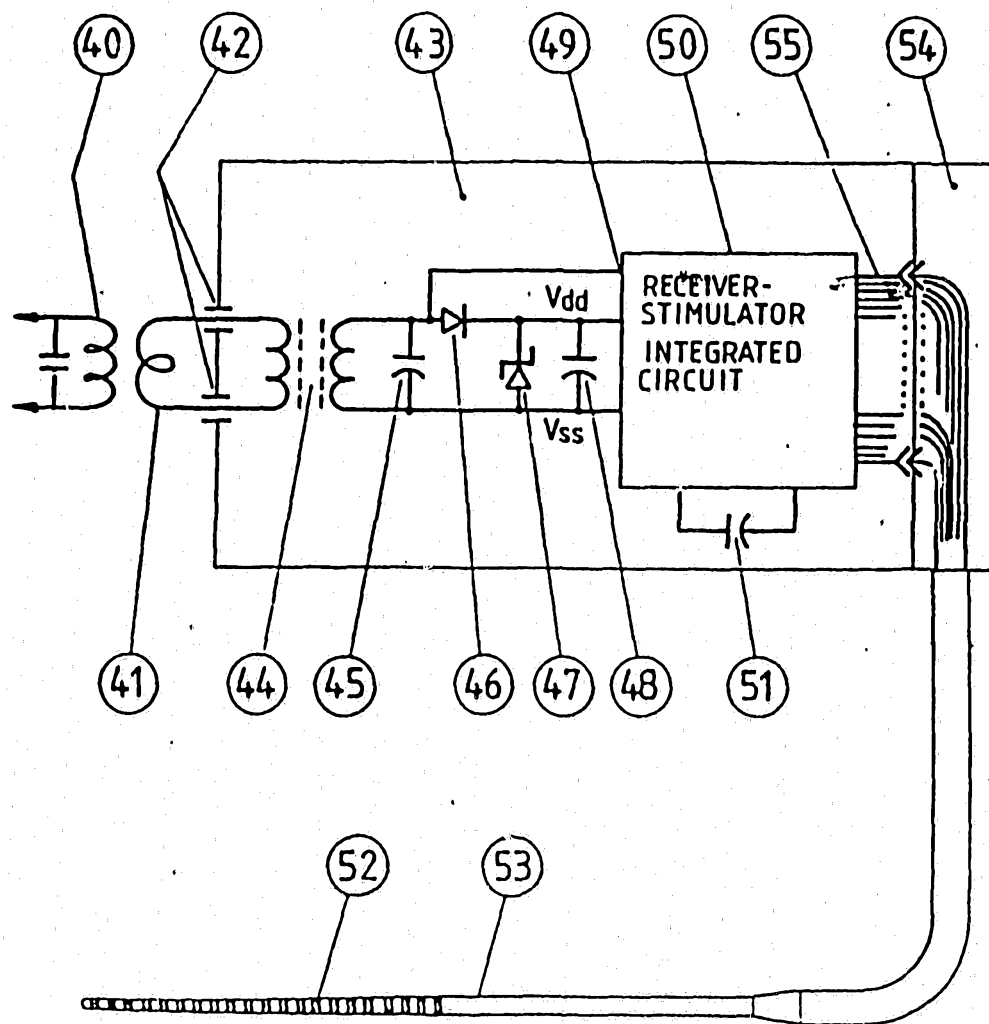
73251/87



Cochlear Implant System - Pictorial Representation
FIG. 3



Active Electrode Stimulus Current
FIG.4



Implantable Receiver/Stimulator
FIG. 5

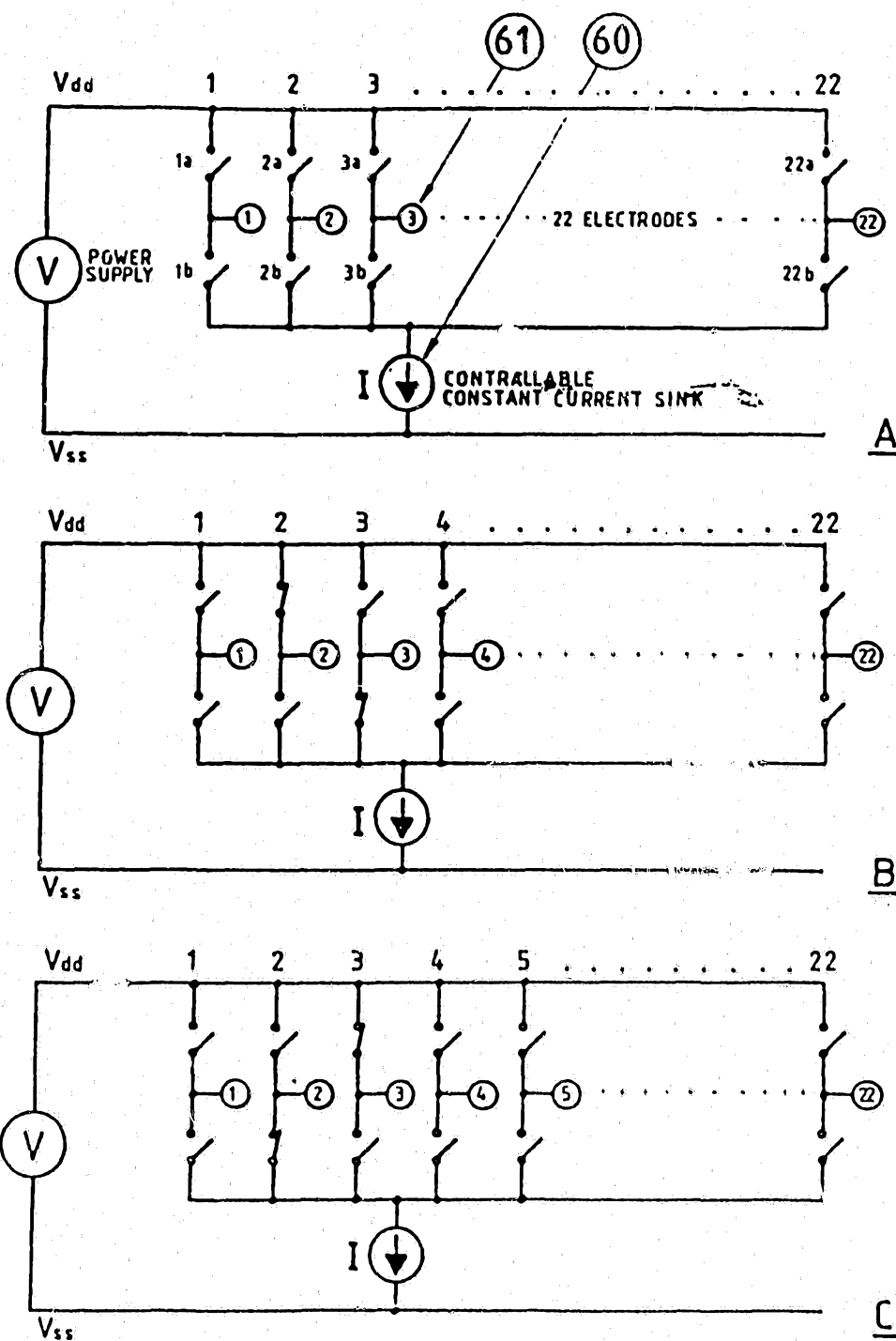


FIG.6: Stimulus Current Generation - Bipolar Mode

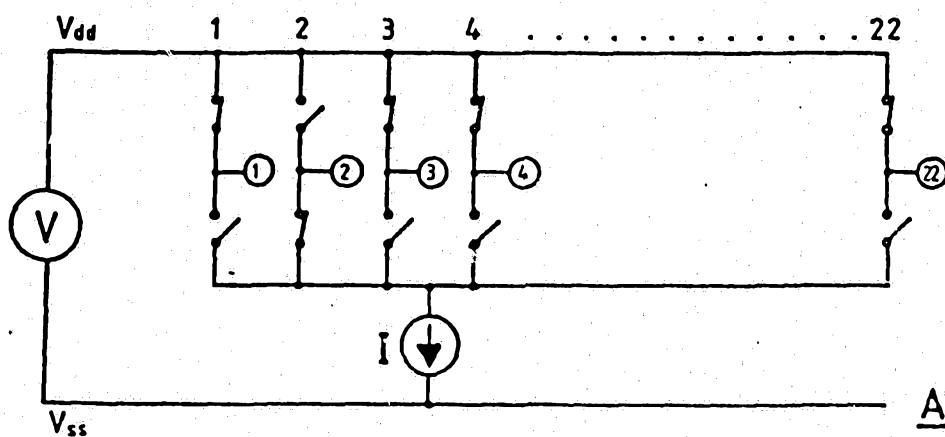
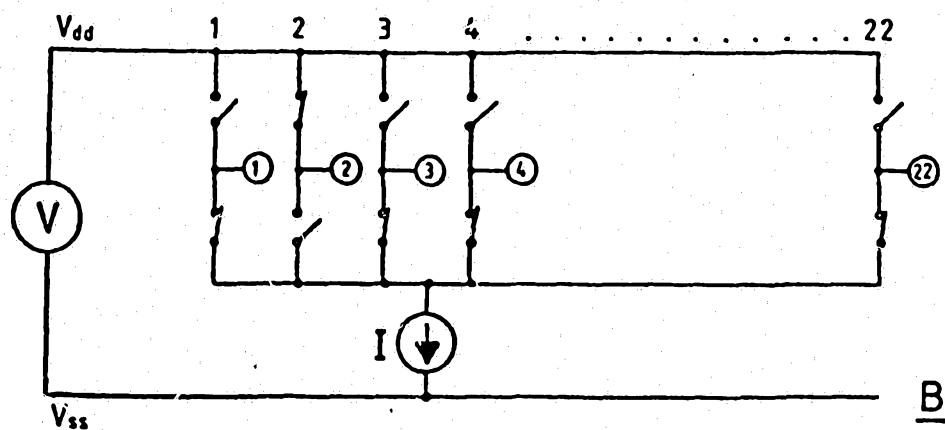


FIG.7 Distributed Ground Stimulus
Current Generation

21 507 7301

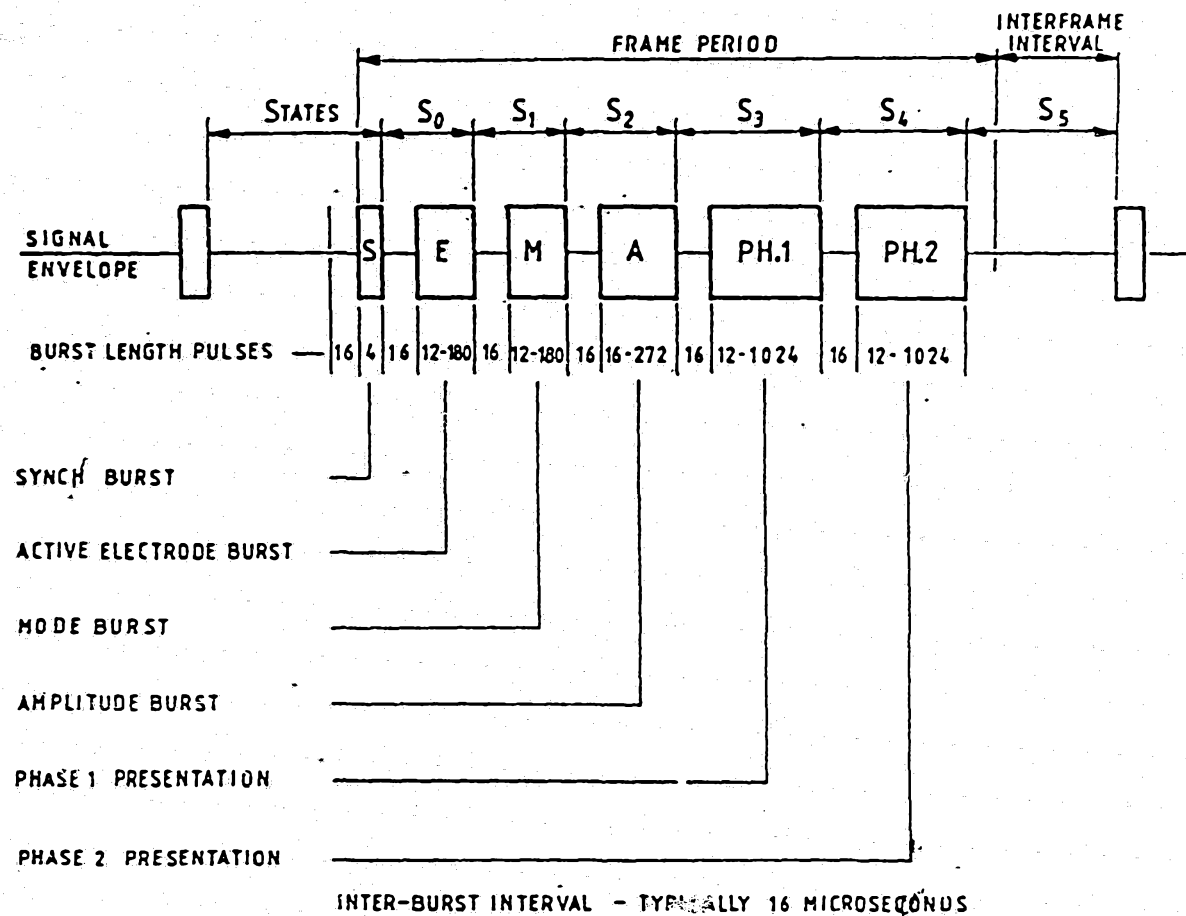
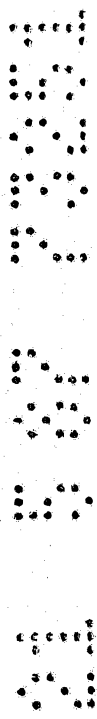


FIG. 8 POWER / DATA SIGNAL FORMAT



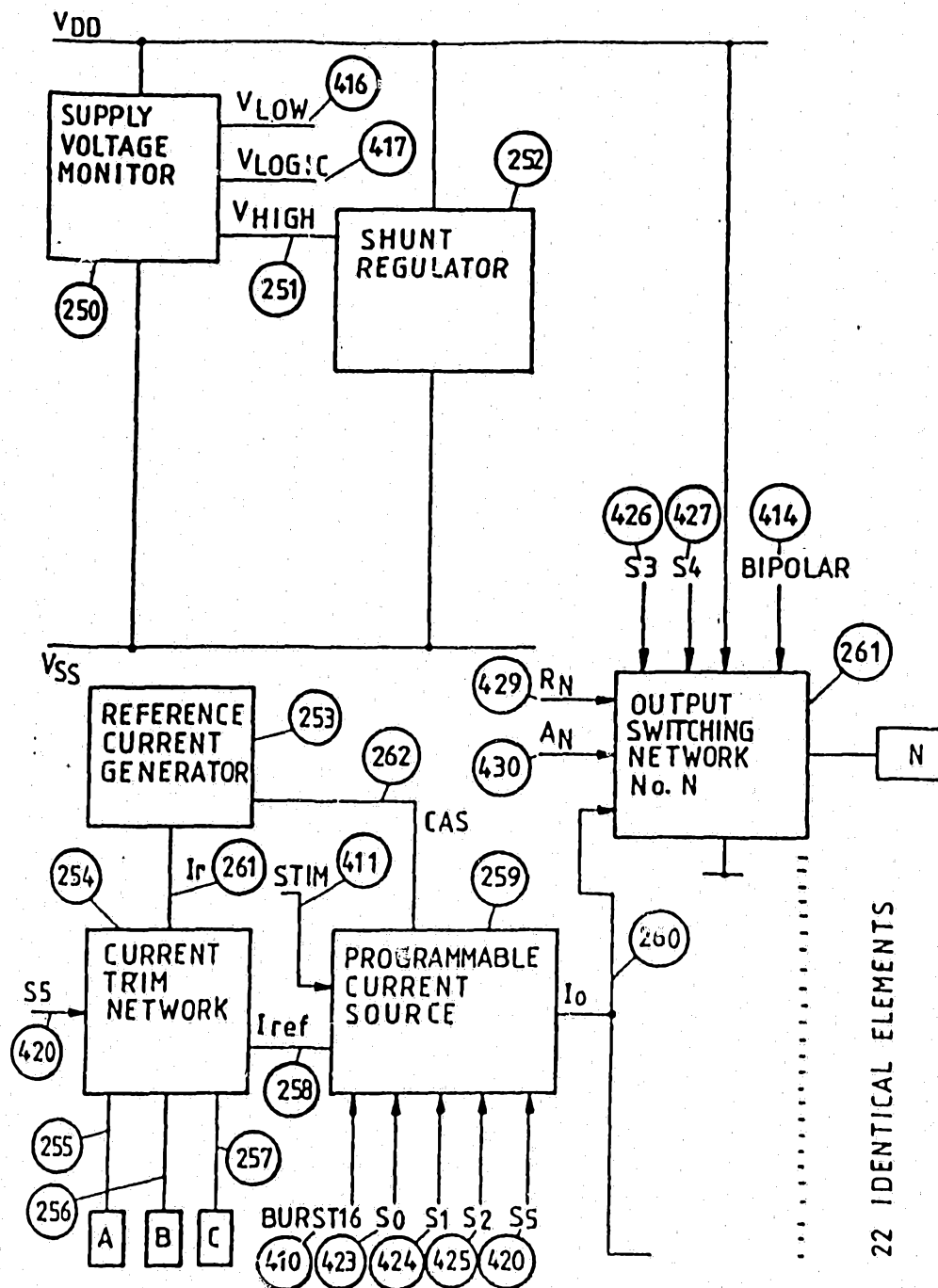


FIG.10: Receiver Stimulator Analog Circuit.
Block Diagram

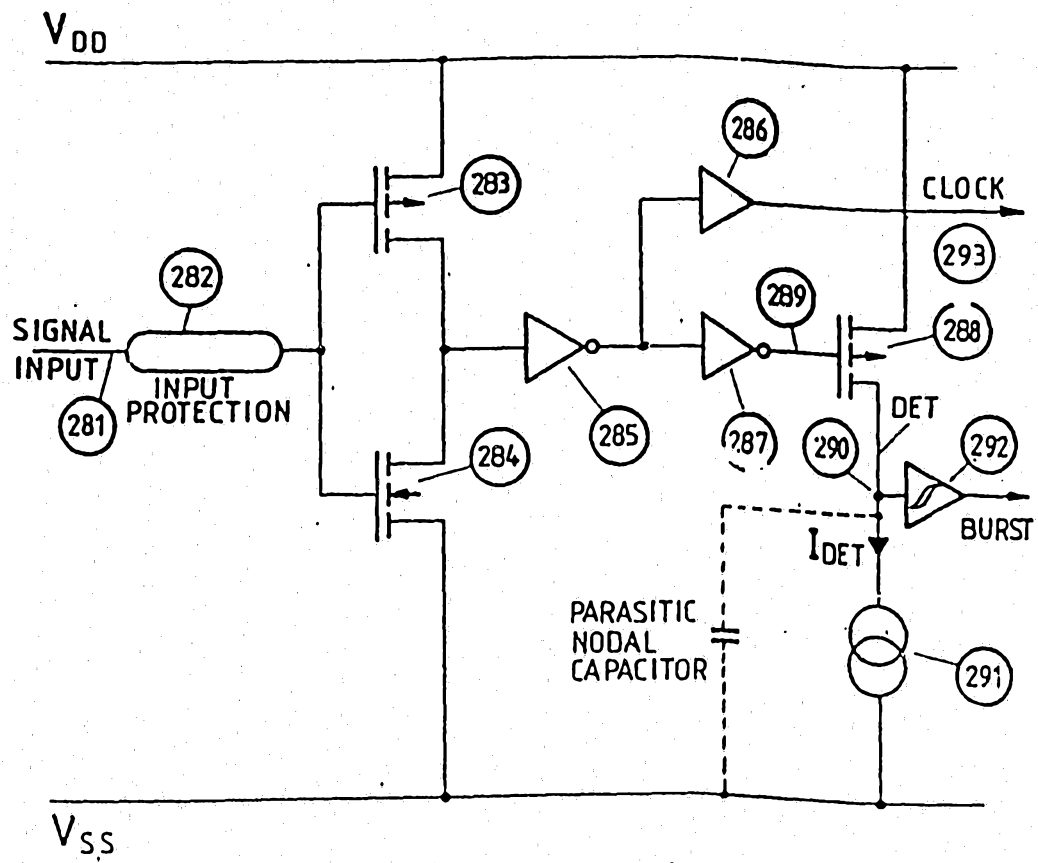


FIG.11: Burst Detector & Clock Extraction Circuit

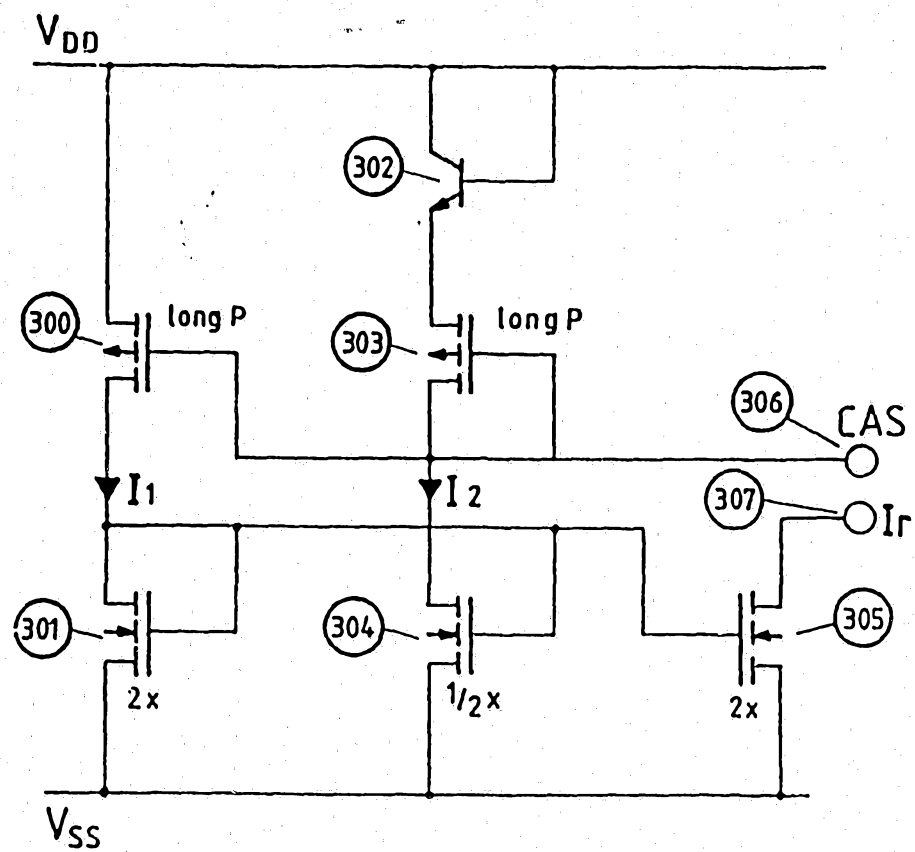


FIG.12: Reference Current Generator

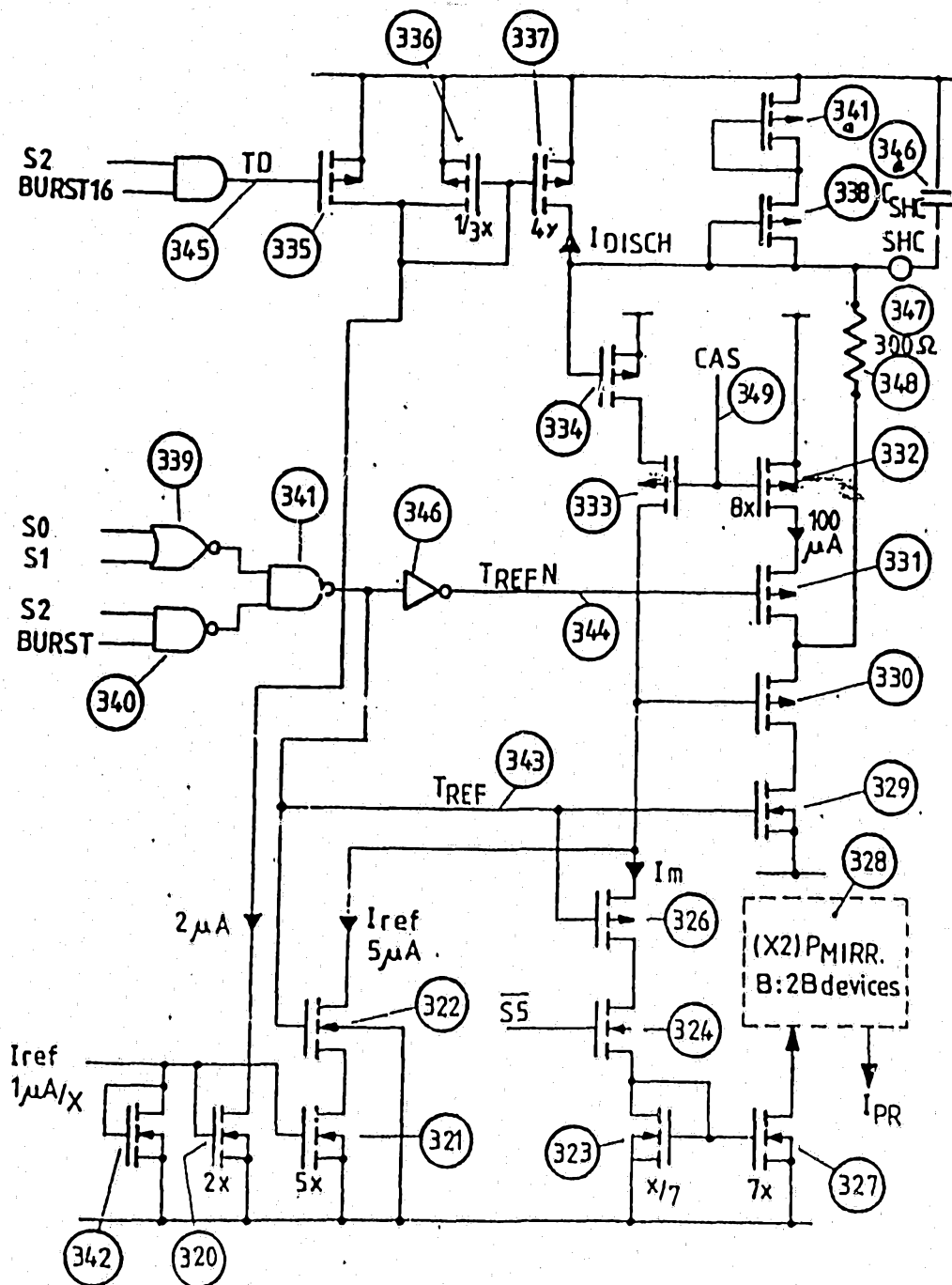


FIG.13: Programmable Current Generator

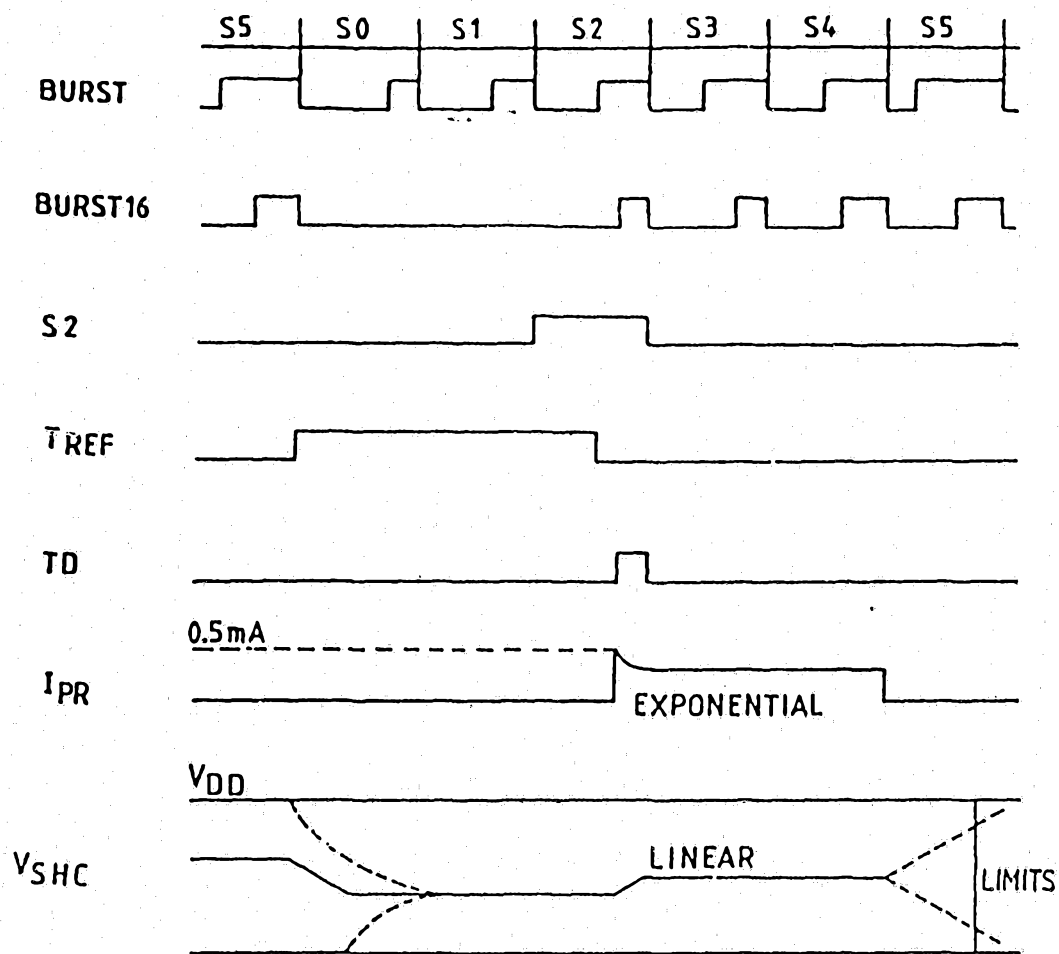
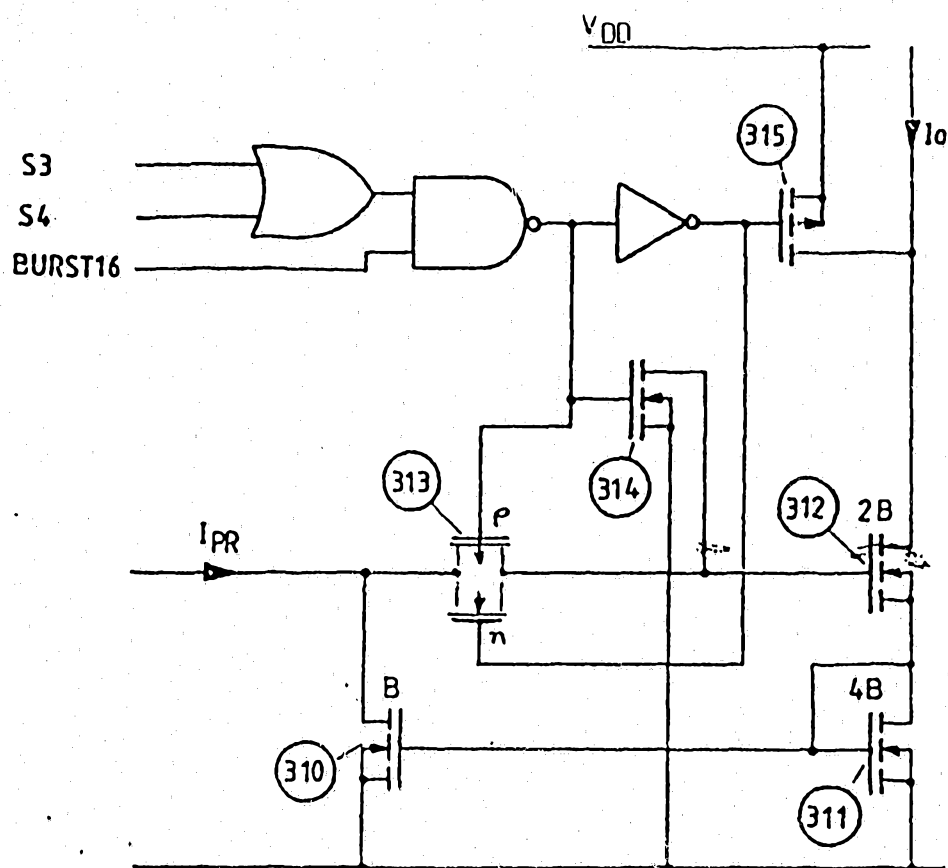
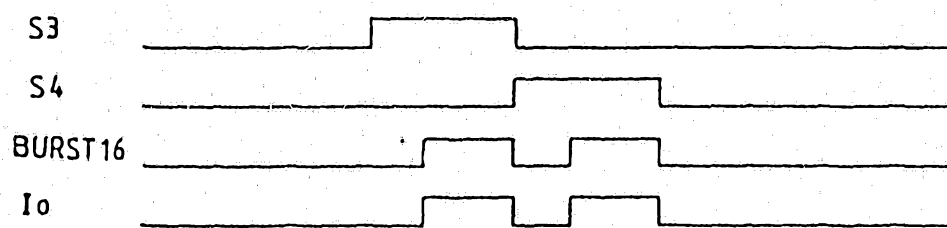


FIG.14: Programmable Current Generator Timing



(a) Current source - output circuit



(b) Output mirror timing

FIG.15 Output Mirror

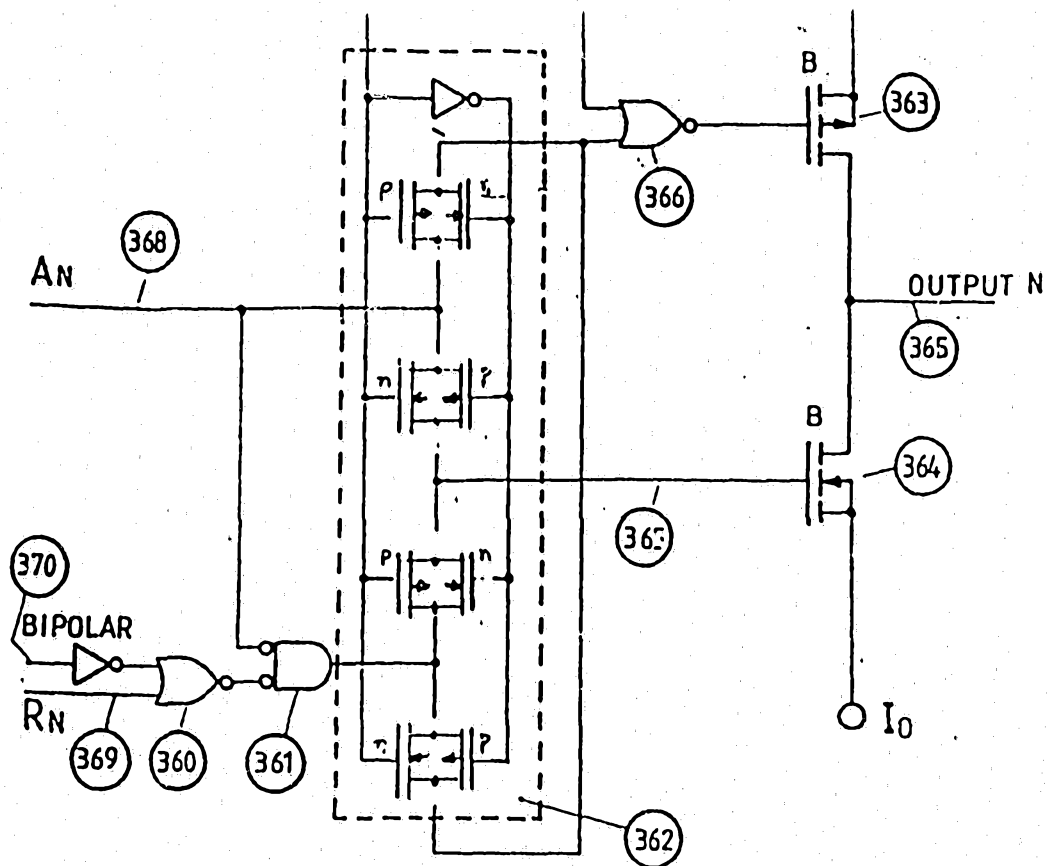


FIG.16: Output Switching Circuit,(output N)

21 5 0 7 7 3 2 5 1

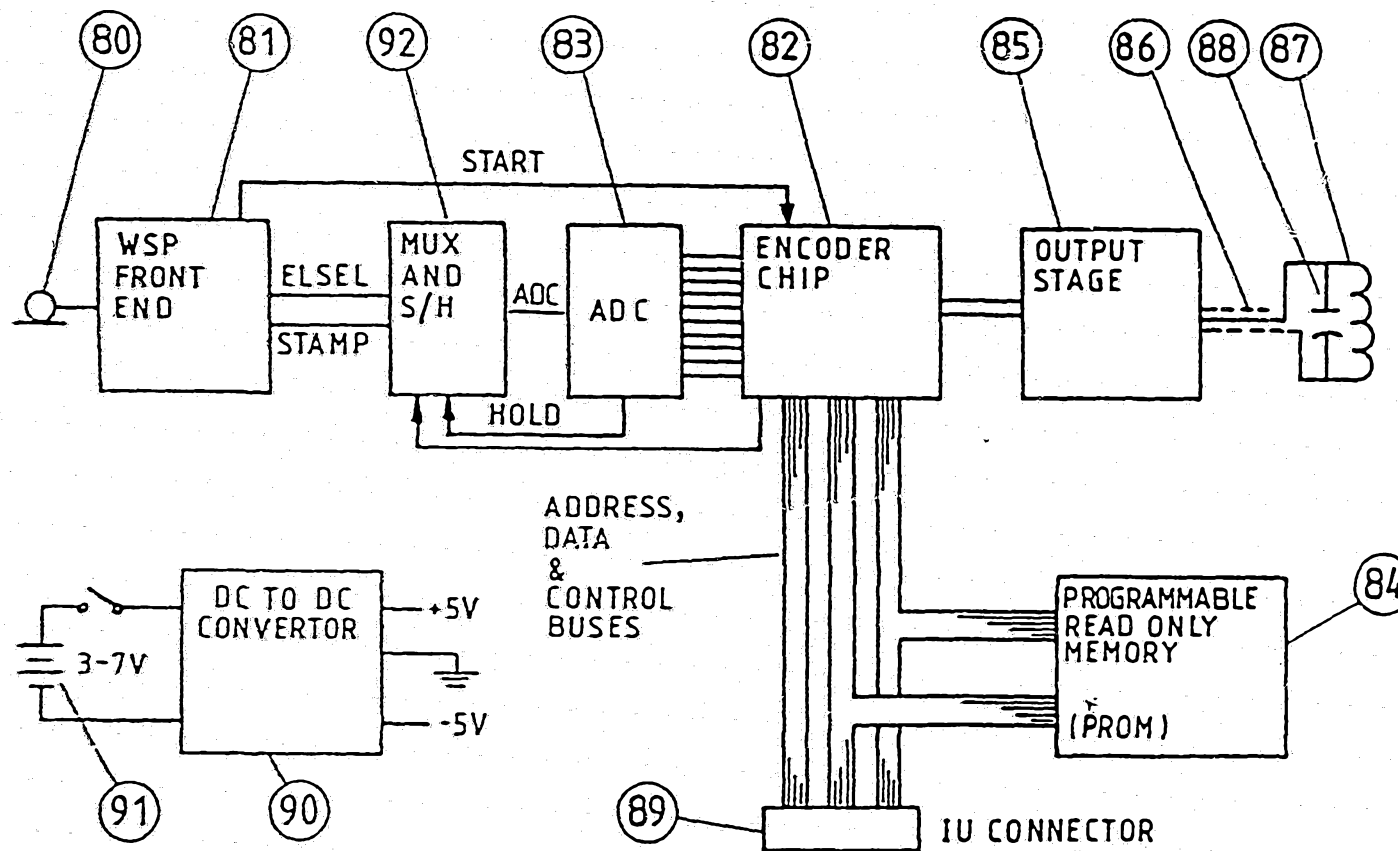


FIG.17 Wearable Speech Processor Block Diagram

FIG.18 WSP Front End Block Diagram

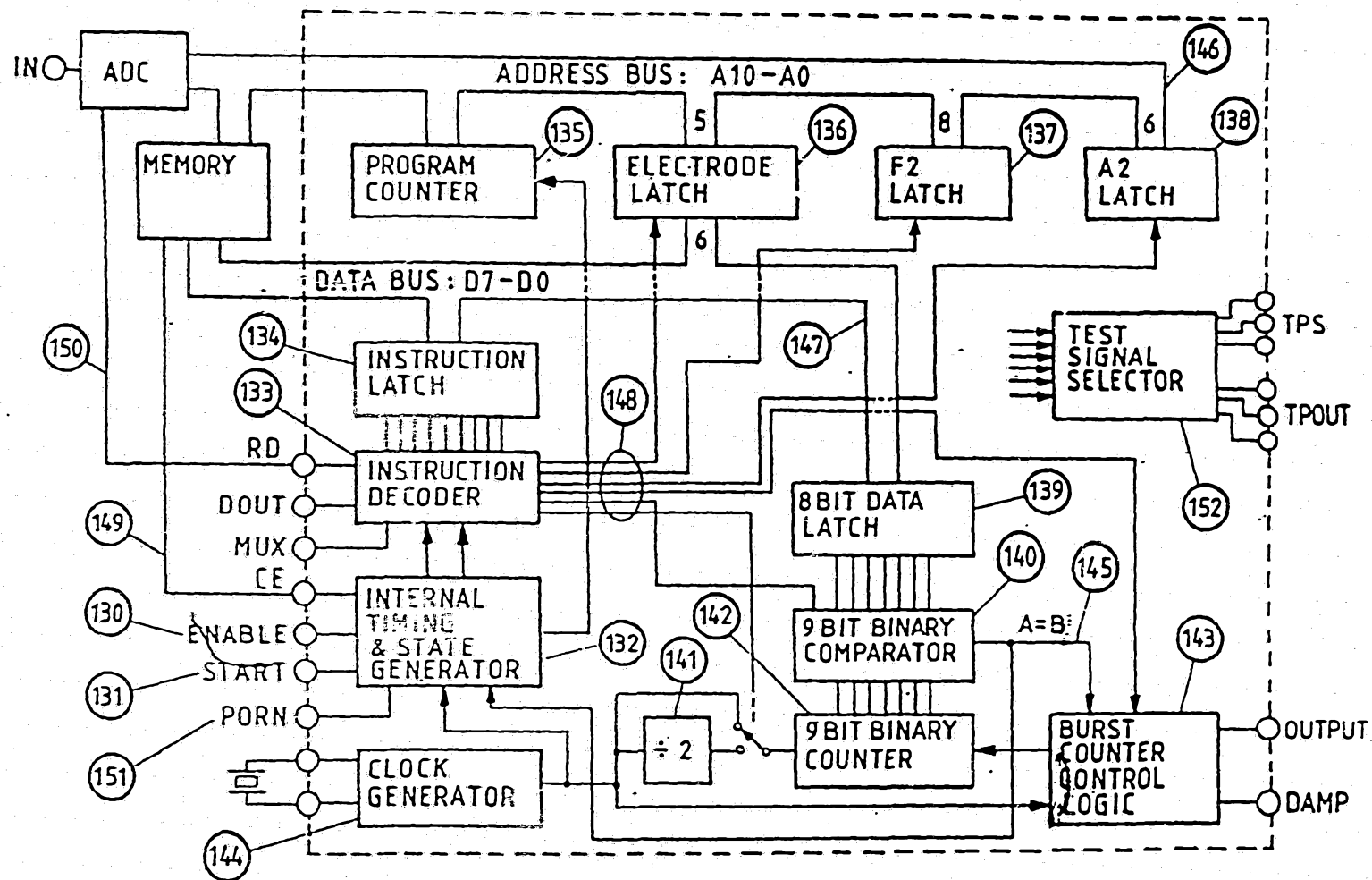


FIG.19 Speech Processor Encoder



PROM ADDRESS MAP

	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	DESCRIPTION	D7	D6	D5	D4	D3	D2	D1	D0
a)	1/0									1	1	F2 Input, electrode output	0						1	0
b)	1/0	1	1	1						1	1	instruction address space								
c)	1/0											amplitude + electrode input, stimulus length output								

NOTES ON BIT 10 UTILIZATION

- When address input is ADC value (8 bits), the A10 bit is used to select which half of the 2Kx8 PROM space the F2 to electrode mapping is to be found. A10 is thus set by A100 under program control.
- In the Instruction Address Space, A10 is the most significant bit of the Program Counter.
- In electrode and amplitude (ADC) input, the A10 bit may be used in two ways:
 - to determine which half of the address space the mapping is to be found (like in "a") under program control with A100.
 - as an extra (least significant) bit of ADC input to extend the precision of amplitude ADC data input from 5 to 6 bits.

The choice of i or ii is under program control.

FIG. 20

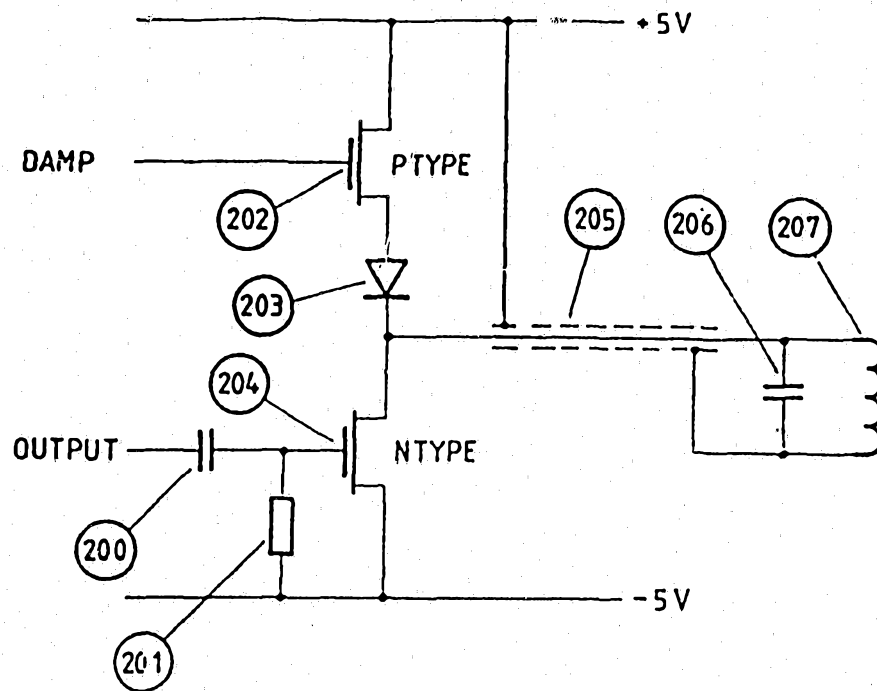


FIG.21 WSP Output Stage

21 5 07 7351

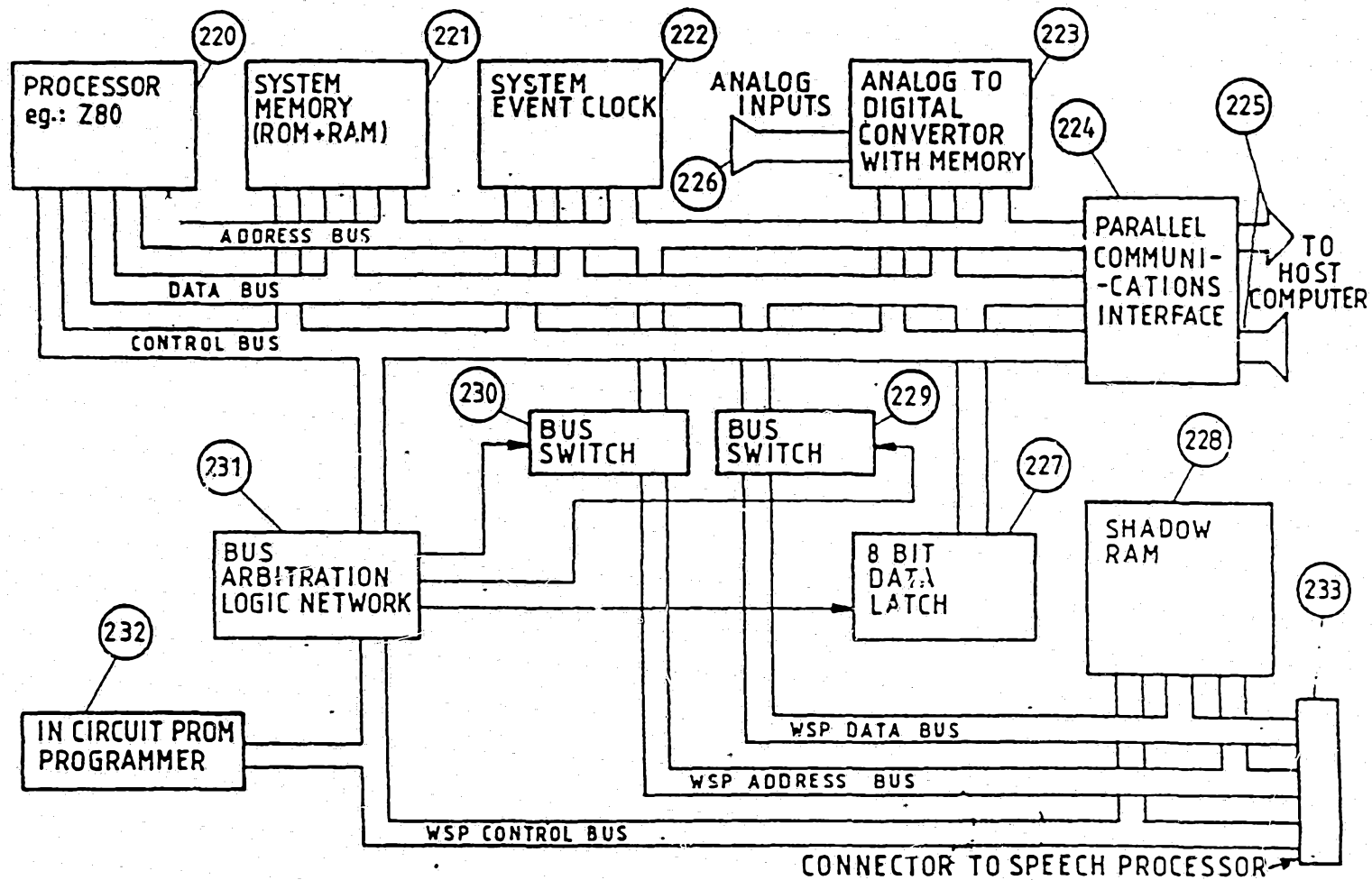
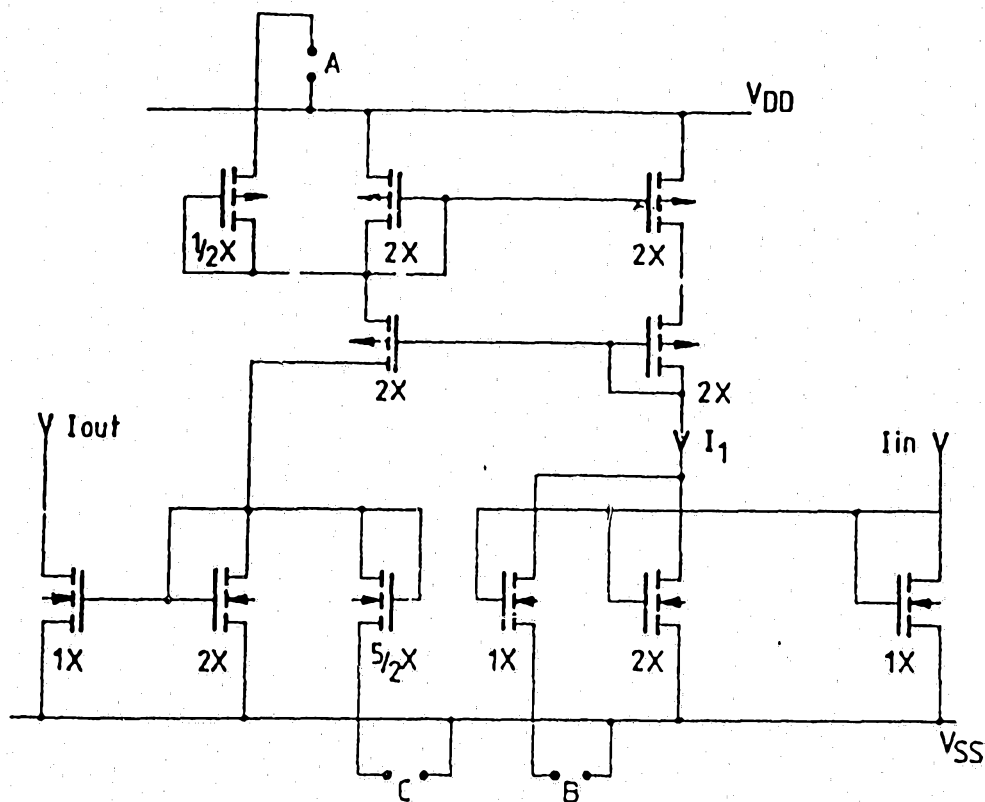


FIG. 22: Interface Unit



A	B	C	I_o/I_{in}
0	0	0	1
1	0	0	1.25
0	1	0	1.5
1	1	0	1.875
0	0	1	0.444
1	0	1	0.555
0	1	1	0.666
1	1	1	0.8325

FIG. 23b

Current Trim Network

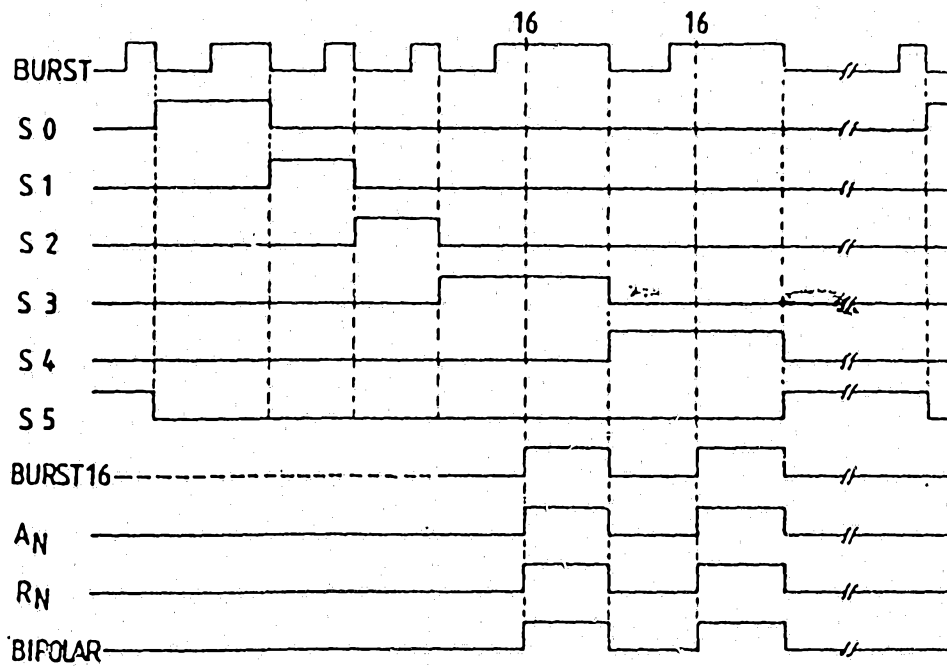


FIG.24
STATE and OUTPUT TIMING