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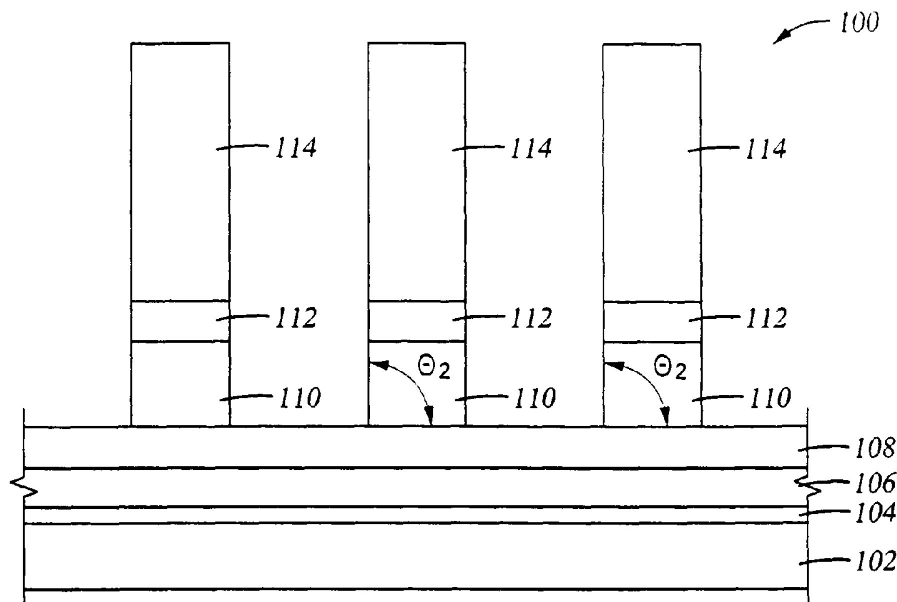
(54) Title: METHOD OF ETCHING A SILICON-CONTAINING DIELECTRIC MATERIAL



(57) Abstract: Disclosed herein is a method of pattern etching a layer of a silicon-containing dielectric material. The method employs a plasma source gas comprising CH_2F_2 to CF_4 is within the range of about 1 : 2 to about 3 : 1, and where O_2 comprises about 2 to about 20 volume % of the plasma source gas. Etching is performed at a process chamber pressure within the range of about 4 mTorr to about 10mTorr. The method provides a selectivity for etching a silicon-containing dielectric layer relative to photoresist of at least 2 : 1. The method also provides an etch profile sidewall angle ranging from about 84° to about 90° between the etched silicon-containing dielectric layer and an underlying horizontal layer in a semiconductor structure.

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1 [0001] METHOD OF ETCHING A SILICON-CONTAINING
2 DIELECTRIC MATERIAL

3 [0002] BACKGROUND OF THE INVENTION

4 [0003] 1. Field of the Invention

5 [0004] The present invention pertains to a method of etching a silicon-containing
6 dielectric material. In particular, the invention pertains to a method of pattern etching a
7 layer of a silicon-containing dielectric material for use as a hard mask for subsequent pattern
8 etching of underlying layers in a semiconductor structure.

9 [0005] 2. Brief Description of the Background Art

10 [0006] Silicon-containing dielectric materials (such as silicon nitride, silicon oxide, and
11 silicon oxynitride) are often used as hard masks for pattern etching of underlying layers in
12 a semiconductor structure. The silicon-containing dielectric layer itself is typically patterned
13 using an overlying, patterned photoresist. Selectivity for etching the silicon-containing
14 dielectric layer relative to an overlying, organic photoresist is important during the mask
15 patterning step. As used herein, the term "selectivity" or "etch selectivity" refers to a ratio
16 of the etch rate of a first material (*e.g.*, a silicon-containing dielectric material) to the etch
17 rate of a second material (*e.g.*, photoresist) using a given plasma source gas and processing
18 conditions.

19 [0007] Conventional plasma etch processes for pattern etching silicon-containing
20 dielectric materials utilize a source gas which is a combination of CF_4 and CH_2F_2. While
21 this etch chemistry typically provides good (at least 2 : 1) selectivity for etching the silicon-
22 containing dielectric layer relative to the overlying photoresist, the resulting etch profile of
23 the silicon-containing dielectric layer is typically tapered, as shown with reference to layer
24 110 in Figure 1B. Because the silicon-containing dielectric layer will be used as a hard
25 mask for subsequent pattern etching of underlying material layers, it is important that the

1 patterned etch profile of the silicon-containing dielectric layer exhibit a sidewall angle, with
2 respect to a horizontal base, which is as close to 90° as possible (typically about 88° to
3 about 92°). Any deviation from a substantially 90° etch profile will be reflected in the etch
4 profiles of the underlying layers.

5 [0008] **SUMMARY OF THE INVENTION**

6 [0009] We have discovered a method of pattern etching a layer of a silicon-containing
7 dielectric material which provides both good selectivity for etching the silicon-containing
8 dielectric layer relative to photoresist and excellent etch profile control. The silicon-
9 containing dielectric material is typically silicon nitride, but may alternatively be silicon
10 oxide or silicon oxynitride, for example and not by way of limitation. The method is
11 particularly useful for feature sizes in the range of about 0.13 μm to about 0.25 μm.

12 [0010] The source gas used for plasma etching the silicon-containing dielectric material
13 includes CF_4, CH_2F_2, and O_2. Carbon tetrafluoride (CF_4) provides an excellent source of
14 fluorine etchant species, while CH_2F_2 provides polymer generation and passivation of
15 exposed photoresist surfaces, extending the lifetime of the photoresist. However, as the
16 volumetric ratio of CH_2F_2 to CF_4 increases, the etch profile of the silicon-containing
17 dielectric layer becomes more tapered. For example, in a pattern of lines and spaces, the
18 width of a trench etched into the silicon-containing dielectric is wider at the top of the line
19 than at the interface with the underlying substrate. As a result, the line produced after
20 etching is wider at the interface with the underlying substrate than at the top of the line. The
21 sidewall angle of the etched line with respect to the horizontal base typically may be 80° or
22 less. The addition of a small amount of O_2 (typically, less than 20 % by volume of the
23 plasma source gas) assists in profile control. However, the presence of O_2 in the plasma
24 source gas reduces the selectivity for etching the silicon-containing dielectric material
25 relative to the photoresist, resulting in more rapid erosion of the photoresist.

1 [0011] Therefore, it is important to achieve a balance between etch profile of the etched
2 line and photoresist preservation. We have discovered that a volumetric ratio of CH_2F_2 to
3 CF_4 in the plasma source gas within the range of about 1 : 2 to about 3 : 1 provides a good
4 balance between etching and passivation, when used in combination with oxygen at a
5 plasma source gas concentration of 20 volume % or less. Often, the volumetric ratio of
6 CH_2F_2 to CF_4 ranges between about 1 : 2 and about 2 : 1. More typically, the volumetric
7 ratio of CH_2F_2 to CF_4 ranges between about 1 : 1 and about 2 : 1. We have found that a
8 plasma source gas comprising about 30 to about 70 volume % CH_2F_2, about 30 to about 70
9 volume % CF_4, and about 2 to about 20 volume % O_2 provides good (at least 2 : 1)
10 selectivity for etching the silicon-containing dielectric layer relative to an overlying
11 photoresist, as well as excellent etch profile control. More typically, the plasma source gas
12 composition comprises about 50 to about 70 volume % CH_2F_2, about 30 to about 50 volume
13 % CF_4, and about 5 to about 15 volume % O_2. Typically, the sidewall angle for a patterned
14 line ranges from about 84° to about 90°.
15 [0012] The plasma source gas composition may further include a nonreactive diluent gas
16 such as helium, argon, neon, xenon, or krypton, by way of example and not by way of
17 limitation. Often, the nonreactive diluent gas is helium. Helium is typically present in the
18 source gas at a concentration within the range of about 50 to about 70 volume %. Often, the
19 plasma source gas is selected to include about 10 to about 25 volume % CH_2F_2, about 10 to
20 about 25 volume % CF_4, about 2 to about 10 volume % O_2, and about 50 to about 70
21 volume % helium.
22 [0013] The etch method works particularly well when performed in a semiconductor
23 processing chamber having a decoupled plasma source. The process chamber pressure
24 during etching in such a processing chamber is typically within the range of about 4 mTorr
25 to about 10 mTorr.

1 [0014] We have found that the etch method described above works especially well in
2 combination with a photoresist which is sensitive to 248 nm radiation, of the kind commonly
3 used in the art. The method provides a selectivity for etching a silicon-containing dielectric
4 layer relative to the photoresist of about 2 : 1 or better. The method also provides a line etch
5 profile sidewall angle ranging from 84° to 90° between the etched silicon-containing
6 dielectric layer and an underlying horizontal layer in the semiconductor structure. In
7 addition, the method provides an etched sidewall roughness of about 5 nm or less.

8 [0015] **BRIEF DESCRIPTION OF THE DRAWINGS**

9 [0016] Figure 1A shows a typical starting structure 100 which was used in the example
10 embodiments described herein. Structure 100 includes the following layers, from top to
11 bottom: a patterned photoresist layer 114 which is sensitive to 248 nm imaging radiation;
12 a patterned bottom anti-reflective coating (BARC) layer 112; a silicon nitride layer 110; a
13 tungsten layer 108; a polysilicon layer 106; and a gate layer 104, all deposited overlying a
14 substrate 102.

15 [0017] Figure 1B shows a schematic cross-sectional front view of structure 100 after
16 pattern etching of silicon nitride layer 110, when a previously known, comparative method
17 is used to etch the silicon nitride layer 110.

18 [0018] Figure 1C shows a schematic front view of structure 100 after pattern etching of
19 silicon nitride layer 110 using an embodiment method of the invention.

20 [0019] Figure 2 shows a schematic cross-sectional front view of a silicon nitride layer
21 200, etched in a lines and spaces pattern, where the etched trench exhibits a tapered profile.

1 [0020] Figure 3 shows a schematic cross-sectional front view of silicon nitride layer 300
2 etched in a lines and spaces pattern using an embodiment method of the invention, where
3 the etched line exhibits a more vertical sidewall profile, where the angle between the line
4 sidewall and a horizontal surface at the base of the line sidewall ranges between about 84°
5 and about 90°.

6 [0021] Figure 4 is a schematic of a CENTURA® DPS II™ (Model of Apparatus) etch
7 chamber of the kind which was used to carry out the experimentation described herein.

8 [0022] **DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS**
9 [0023] Disclosed herein is a method of pattern etching a layer of a silicon-containing
10 dielectric material. Exemplary processing conditions for performing various embodiments
11 of the method of the invention are set forth below.
12 [0024] Although the method embodiments described below pertain to the use of a
13 silicon-containing dielectric material as a hard mask in the etching of a gate structure, the
14 etch chemistry and processing conditions described below can be used any time a silicon-
15 containing dielectric material is used as a masking layer, for example, in the etching of a
16 trench or contact via or other semiconductor feature.
17 [0025] As a preface to the detailed description, it should be noted that, as used in this
18 specification and the appended claims, the singular forms "a", "an", and "the" include plural
19 referents, unless the context clearly dictates otherwise.

20 [0026] I. AN APPARATUS FOR PRACTICING THE INVENTION
21 [0027] The embodiment etch methods described herein are typically performed in a
22 plasma etch chamber having a Decoupled Plasma Source (DPS) of the kind described by
23 Yan Ye et al. at the Proceedings of the Eleventh International Symposium of Plasma

1 Processing, May 7, 1996, and as published in the Electrochemical Society Proceedings,
2 Volume 96-12, pp. 222 - 233 (1996). In particular, the embodiment example etch processes
3 described herein were carried out in a CENTURA® DPS II™ plasma etch chamber
4 available from Applied Materials, Inc., of Santa Clara, California. This apparatus used to
5 carry out the etching described herein is discussed in detail below; however, it is
6 contemplated that other plasma etch chamber apparatus known in the industry may be used
7 to carry out the invention.
8 [0028] Figure 4 shows a schematic of a cross-sectional view of a CENTURA® DPS II™
9 plasma etch chamber 400 of the kind which was used to carry out the etching processes
10 described herein. During processing, a substrate 422 is introduced into the chamber 400
11 through a slit valve 434. The substrate 422 is held in place by means of a static charge
12 generated on the surface of an electrostatic chuck (ESC) cathode 424, by applying a DC
13 voltage to a conductive layer located under a dielectric film on the chuck surface (not
14 shown). Etch gases are introduced into the chamber 400 by means of a gas distribution
15 assembly 416. The etch chamber 400 uses an inductively coupled plasma RF source power
16 402, which is connected to an outer inductive coil 404 and an inner inductive coil 406 for
17 generating and sustaining a high density plasma 414 in plasma processing region 412.
18 Plasma source power 402 is split off into a first power distribution system 408, which
19 provides power to outer coil 404, and a second power distribution system 410, which
20 provides power to inner coil 406. The substrate 422 is biased by means of an RF source 428
21 and matching network 426. Power to the plasma source 402 and substrate biasing means
22 428 are controlled by separate controllers (not shown). Etch byproducts and excess
23 processing gases 413 are exhausted from the chamber through throttle valve 430, by means
24 of pump 432, which maintains the desired process chamber pressure. The temperature of
25 the semiconductor substrate 422 is controlled using the temperature of the electrostatic
26 chuck cathode 424 upon which the substrate 422 rests. Typically, a helium gas flow is used

1 to facilitate heat transfer between the substrate and the pedestal.
2 [0029] Although the etch process chamber used to process the substrates described in the
3 Examples presented herein is shown in schematic in Figure 4, one skilled in the art may use
4 any of the etch processors available in the industry, with some readily apparent adjustments.
5 For example, the method of the invention may alternatively be performed in an etch
6 processing apparatus wherein power to a plasma generation source and power to a substrate
7 biasing means are supplied by a single power supply, such as the Applied Materials' MXP
8 or MXP+ polysilicon etch chamber.

9 [0030] II. EXEMPLARY METHODS OF PATTERN ETCHING
10 A SILICON-CONTAINING DIELECTRIC LAYER

11 [0031] Figure 1A shows a typical starting structure 100 for performing the embodiment
12 etching methods described herein. Structure 100 includes the following layers, from top to
13 bottom: a patterned 193 nm photoresist layer 114; a patterned bottom anti-reflective coating
14 (BARC) layer 112; a silicon-containing dielectric layer 110; a tungsten layer 108; a
15 polysilicon layer 106; and a gate oxide layer 104, all overlying a single-crystal silicon
16 substrate 102. However, it is understood that, in practicing the invention, layers underlying
17 the silicon-containing dielectric layer 110 may be different.
18 [0032] The various layers in the embodiment example semiconductor structure 100 are
19 deposited using conventional deposition techniques known in the art, as follows.
20 [0033] Gate oxide layer 104 was a silicon oxide layer, which was formed by thermal
21 oxidation, according to techniques known in the art. Gate oxide layer 104 had a thickness
22 within the range of about 15 Å to 50 Å.
23 [0034] Polysilicon layer 106 was deposited by chemical vapor deposition (CVD),
24 according to techniques known in the art. Polysilicon layer 106 had a thickness within the
25 range of about 500 Å to about 2000 Å.

1 [0035] Tungsten layer 108 was deposited by CVD, according to techniques known in the
2 art. Tungsten layer 108 had a thickness within the range of about 300 Å to about 1000 Å.
3 [0036] In the Examples described below, silicon-containing dielectric layer 110 was
4 silicon nitride. However, silicon-containing dielectric layer 110 may alternatively comprise
5 silicon oxide or silicon oxynitride. Optionally, silicon-containing dielectric layer 110 may
6 be a dual layer, with an upper layer of silicon oxide and a lower layer of silicon nitride, for
7 example, and not by way of limitation.
8 [0037] Silicon nitride layer 110 is typically deposited by low pressure CVD (LPCVD)
9 or plasma-enhanced CVD (PECVD), according to techniques known in the art. Silicon
10 nitride layer 110 typically has a thickness within the range of about 1000 Å to about
11 2500 Å.
12 [0038] Antireflective coatings are used in combination with photoresists to reduce
13 standing waves and back-scattered light, so that the imaging within the photoresist can be
14 better controlled. When the ARC layer lies beneath the photoresist layer, it is commonly
15 referred to as a bottom antireflective coating (BARC). An organic BARC layer 112 is
16 typically deposited by spin-on techniques known in the art. BARC layer 112 typically has
17 a thickness within the range of about 500 Å to about 1500 Å.
18 [0039] Photoresist layer 114 is, in the present instance, a photoresist which is sensitive
19 to radiation within the range of about 200 nm to about 300 nm. Typically, the photoresist
20 is a chemically amplified version of an organic, polymeric-based composition which is
21 available from a number of manufacturers, including AZ Electronic Materials (Somerville,
22 NJ) and Shipley, Inc. (Marlboro, MA). A typical film thickness for such a photoresist
23 ranges from about 4000 Å to about 6000 Å. The thickness and patterning method for the
24 photoresist layer 114 will depend on the particular photoresist material used and the pattern
25 to be etched in the underlying substrate. In the present instance, for etching a pattern of lines
26 and spaces which are 0.2 μm wide lines and 0.2 μm wide spaces through a 2000 Å thick

1 layer of silicon nitride, the resist thickness is typically about 5000 Å. The maximum
2 thickness of the photoresist is limited by the aspect ratio of the photoresist being developed
3 and the particular characteristics of the photoresist used. To obtain advantageous results,
4 the aspect ratio of the developed photoresist is typically about 4 : 1 or less; more typically,
5 about 3 : 1 or less.

6 [0040] Patterned photoresist layer 114 is used as a mask to transfer the pattern to
7 underlying BARC layer 112. Pattern etching of lines and spaces through an organic BARC
8 layer 112 is typically performed using a plasma source gas including CF_4 and argon.
9 Typical process conditions for pattern etching of BARC layer 110 in a decoupled plasma
10 source etch chamber are as follows: 100 sccm of CF_4; 100 sccm of Ar; 4 mTorr to 20 mTorr
11 process chamber pressure; 300 W to 1000 W plasma source power; 30 W to 100 W substrate
12 bias power (about -60 V to -1000 V substrate bias voltage); and 40°C to 80°C substrate
13 temperature. Etching time will depend on the composition and thickness of the particular
14 BARC layer being etched. For an organic BARC layer having a thickness of 800 Å, the etch
15 time is typically within the range of about 20 seconds to about 30 seconds.

16 [0041] III. COMPARATIVE SILICON NITRIDE ETCH EXAMPLE

17 [0042] The following comparative example was performed using the starting structure
18 100 shown in Figure 1. Thicknesses of the various layers were as follows: a 5000 Å thick
19 patterned 248 nm photoresist layer 114; a 600 Å thick patterned BARC layer 112; a
20 2000 Å thick silicon nitride layer 110; a 500 Å thick tungsten layer 108; a 1500 Å thick
21 polysilicon layer 106; and a 15 Å thick silicon oxide gate layer, all deposited overlying a
22 single-crystal silicon substrate 102.

23 [0043] After patterning of BARC layer 112 in the manner described above, the silicon
24 nitride layer 110 was etched. Silicon nitride etching was performed in an Applied Materials'
25 DPS II plasma etch chamber (shown in Figure 4). Plasma etching of silicon nitride layer

1 110 was performed using the following plasma source gas composition and etch process
2 conditions: 30 sccm CF_4; 60 sccm CH_2F_2; 4 mTorr process chamber pressure; 800 W
3 plasma source power; 250 W substrate bias power; and a 60°C substrate temperature.
4 [0044] Figure 1B shows a schematic cross-sectional front view of the structure 100 after
5 pattern etching of silicon nitride layer 108, when etching was performed using the CF_4 /
6 CH_2F_2 / He etch chemistry and process conditions set forth above. Note the tapered profile
7 of etched silicon nitride layer 108, where the line sidewall angle θ1 was about 78°.
8 [0045] Figure 2 is a schematic drawing based on a photomicrograph taken of a silicon
9 nitride layer 200, etched in a lines and spaces pattern, where etching was performed using
10 the CF_4 / CH_2F_2 / He etch chemistry and process conditions set forth above. Figure 2 shows
11 a schematic cross-sectional front view of silicon nitride layer 200. The etched line exhibits
12 the tapered profile described above.
13 [0046] Because the silicon-containing dielectric layer will be used as a hard mask for
14 subsequent pattern etching of underlying material layers, it is important that the patterned
15 etch profile of the silicon-containing dielectric layer exhibit a sidewall angle, with respect
16 to a horizontal base, which is as close to 90° as possible. Any non-uniformity in the etch
17 profile of the mask opening will be reflected in the etch profiles of the underlying layers.
18 [0047] Therefore, we needed to a develop a method of pattern etching a layer of silicon-
19 containing dielectric material which provides a vertical (*i.e.*, as close to 90° as possible, and
20 typically ranging between about 88° and about 92°) etch profile.

21 [0048] IV. INVENTION EMBODIMENT EXAMPLES
22 [0049] We have found that the addition of a small amount of O_2 (typically, less than
23 20 % by volume of the plasma source gas) provides excellent profile control, without
24 significantly suppressing the etch rate of the silicon-containing dielectric material. A
25 volumetric ratio of CH_2F_2 to CF_4 in the plasma source gas within the range of about 1 : 2 to

1 about 2 : 1 was found to provide a good balance between etching and passivation, when used
2 in combination with oxygen at a plasma source gas concentration of 20 volume % or less.
3 [0050] The following examples were performed using the starting structure 100 shown
4 in Figure 1. Thicknesses of the various layers were as follows: a 5000 Å thick patterned
5 248 nm photoresist layer 114; a 600 Å thick patterned organic BARC layer 112; a 2000 Å
6 thick silicon nitride layer 110; a 500 Å thick tungsten layer 108; a 1500 Å thick polysilicon
7 layer 106; and a silicon oxide gate layer 104, all deposited overlying a single-crystal silicon
8 substrate 102.
9 [0051] After patterning of BARC layer 112 in the manner previously described, a silicon
10 nitride layer 110 was etched. Silicon nitride etching was performed in the same Applied
11 Materials' DPS II plasma etch chamber referred to with respect to the comparative example.
12 Silicon nitride etch process conditions which were used during each experiment are
13 presented in Table One, below.

1 [0052] Table One. Process Conditions Used During Etching of Silicon Nitride

Process Parameter	Run #1	Run #2	Run #3	Run #4	Run #5	Run #6
CH_2F_2 Flow Rate (sccm)	60	60	50	60	30	60
CF_4 Flow Rate (sccm)	30	30	30	30	15	30
O_2 Flow Rate (sccm)	15	5	5	5	5	--
He Flow Rate (sccm)	--	--	--	--	300	--
Process Chamber Pressure (mTorr)	4	4	4	4	4	4
Plasma Source Power (W)	800	800	800	1200	1200	800
Substrate Bias Power (W)	250	250	250	250	250	250
Substrate Temp. (°C)	60	60	60	60	60	60
Etch Time (sec)	75	70	72	57	65	60
Si_xN_y : PR Selectivity, no overetch*	2.2	5.6	2.7	4	--	6.7
Si_xN_y : PR Selectivity, w/50% overetch**	--	--	2	2.4	1.7	--
Etch Profile Angle (θ)	88	84	85	86	87	78

18 * Silicon nitride : photoresist etch selectivity, with no overetch step.
19 ** Silicon nitride : photoresist etch selectivity, with 50 % overetch. (Overetch process was
20 the same as the main etch.)

21 [0053] The Run # 6 data are presented as a comparison, to show the tapered etch profile
22 angle which is obtained when the plasma source gas does not include oxygen.
23 [0054] Figure 1C shows a schematic cross-sectional front view of the structure 100 after
24 pattern etching of silicon nitride layer 108 using a method of the invention which provided
25 a nearly vertical etch profile exhibiting etch profile angle θ_2. Figure 3 shows a schematic
26 cross-sectional front view of silicon nitride layer 300 etched in a lines and spaces pattern
27 using an embodiment method of the invention, where the etched line exhibits a vertical
28 sidewall profile, where the angle θ3 between the line sidewall and a horizontal surface at the

1 base of the sidewall ranges between about 84° and about 92°.

2 [0055] According to the present method embodiment, etching of a silicon-containing
3 dielectric material is typically performed using a plasma generated from a source gas which
4 includes CH_2F_2, CF_4, and O_2, where a volumetric ratio of CH_2F_2 to CF_4 is within the range
5 of about 1 : 2 to about 3 : 1, and where O_2 is comprises about 2 to about 20 volume % of the
6 plasma source gas. Often, the volumetric ratio of CH_2F_2 to CF_4 ranges between about 1 : 2
7 and about 2 : 1. More typically, the volumetric ratio of CH_2F_2 to CF_4 ranges between about
8 1 : 1 and about 2 : 1. We have found that a plasma source gas comprising about 30 to about
9 70 volume % CH_2F_2, about 30 to about 70 volume % CF_4, and about 2 to about 20 volume
10 % O_2 provides good (at least 2 : 1) selectivity for etching the silicon-containing dielectric
11 layer relative to an overlying photoresist, as well as excellent etch profile control. More
12 typically, the plasma source gas composition comprises about 50 to about 70 volume %
13 CH_2F_2, about 30 to about 50 volume % CF_4, and about 5 to about 15 volume % O_2.
14 Typically, the sidewall angle for a patterned line ranges from about 84° to about 92°.

15 [0056] The plasma source gas composition may further include a nonreactive diluent gas
16 such as helium, argon, neon, xenon, or krypton, by example and not by way of limitation.
17 Often, the nonreactive diluent gas is helium. Helium is typically present in the source gas
18 at a concentration within the range of about 50 to about 70 volume %. Often, the plasma
19 source gas is selected to include about 10 to about 25 volume % CH_2F_2, about 10 to about
20 25 volume % CF_4, about 2 to about 10 volume % O_2, and about 50 to about 70 volume %
21 helium.

22 [0057] The present etch method works particularly well when performed in a
23 semiconductor processing chamber having a decoupled plasma source. Typical process
24 conditions for etching of a silicon-containing dielectric material, according to the present
25 embodiment method, in a decoupled plasma chamber (such as a CENTURA® DPS II™),
26 are provided in Table Two, below:

1 [0058] Table Two. Typical Process Conditions for Etching
2 of a Silicon-Containing Dielectric Material

Process Parameter	Range of Process Conditions	Typical Process Conditions	Advantageous Process Conditions
CH_2F_2 Flow Rate (sccm)	10 - 100	10 - 100	30 - 60
CF_4 Flow Rate (sccm)	30 - 100	30 - 100	30 - 60
O_2 Flow Rate (sccm)	3 - 30	3 - 30	5 - 20
He Flow Rate (sccm)	0 - 200	0 - 200	0 - 200
Process Chamber Pressure (mTorr)	3 - 20	4 - 10	4 - 10
Plasma Source Power (W)	200 - 1800	300 - 1500	500 - 1000
Substrate Bias Power (W)	30 - 400	50 - 300	150 - 250
Substrate Temperature (°C)	20 - 80	20 - 80	40 - 60
Etch Time Period (sec)*	40 - 100	40 - 100	40 - 100

14 * For a 2000 Å thick silicon nitride layer.

15 [0059] The etch method described above works particularly well in combination with
16 a photoresist which is sensitive to 248 nm radiation, of the kind commonly used in the art.
17 Such photoresists are available from AZ Electronic Materials / Clariant (Somerville, NJ) and
18 Shipley, Inc. (Marlboro, MA), by way of example and not by way of limitation.

19 [0060] The method provides a selectivity for etching a silicon-containing dielectric layer
20 relative to such a photoresist of about 2 : 1 or better. The method also provides an etch
21 profile sidewall angle ranging from 84° to 92° between the etched silicon-containing
22 dielectric layer and an underlying horizontal layer in the semiconductor structure. In
23 addition, the method provides an etched sidewall roughness of about 5 nm or less.

1 [0061] Although the Examples above are described with reference to the use of a silicon-
2 containing dielectric material as a hard mask in the etching of a gate structure, the etch
3 chemistry and processing conditions described above can be used any time a silicon-
4 containing dielectric material is used as a masking layer, for example, in the etching of a
5 shallow trench or other semiconductor feature.
6 [0062] The above described exemplary embodiments are not intended to limit the scope
7 of the present invention, as one skilled in the art can, in view of the present disclosure
8 expand such embodiments to correspond with the subject matter of the invention claimed
9 below.

[0063]

CLAIMS

We claim:

1 1. A method of pattern etching a layer of a silicon-containing dielectric material on
2 a semiconductor substrate, wherein a patterned photoresist layer overlies said silicon-
3 containing dielectric layer, said method comprising exposing said silicon-containing
4 dielectric layer to a plasma generated from a source gas comprising CH_2F_2, CF_4, and O_2,
5 wherein a volumetric ratio of CH_2F_2 to CF_4 is within the range of about 1 : 2 to about 3 : 1,
6 and wherein O_2 comprises about 2 to about 20 volume % of the plasma source gas.

1 2. The method of Claim 1, wherein said silicon-containing dielectric material is
2 selected from the group consisting of silicon nitride, silicon oxide, silicon oxynitride, and
3 combinations thereof.

1 3. The method of Claim 1, wherein a volumetric ratio of CH_2F_2 to CF_4 is within the
2 range of about 1 : 2 to about 2 : 1.

1 4. The method of Claim 3, wherein a volumetric ratio of CH_2F_2 to CF_4 is within the
2 range of about 1 : 1 to about 2 : 1.

3 5. The method of Claim 1, wherein said source gas comprises about 30 to about 70
4 volume % CH_2F_2, about 30 to about 70 volume % CF_4, and about 2 to about 20 volume %
5 O_2.

1 6. The method of Claim 6, wherein said source gas comprises about 50 to about 70
2 volume % CH_2F_2, about 30 to about 50 volume % CF_4, and about 5 to about 15 volume %
3 O_2.

1 7. The method of Claim 1, wherein said source gas further includes helium.

1 8. The method of Claim 7, wherein said helium is present in said source gas at a
2 concentration within the range of about 50 to about 70 volume %.

1 9. The method of Claim 8, wherein said source gas comprises about 10 to about 25
2 volume % CH_2F_2, about 10 to about 25 volume % CF_4, about 2 to about 10 volume % O_2,
3 and about 50 to about 70 volume % helium.

1 10. The method of Claim 1, wherein said photoresist is sensitive to 248 nm radiation.

1 11. The method of Claim 1, wherein said silicon-containing dielectric layer is used
2 as a hard mask during pattern etching of an underlying semiconductor structure, and wherein
3 said semiconductor structure includes features having a feature size of about 0.13 μm or
4 larger.

1 12. The method of Claim 1, wherein said silicon-containing dielectric layer has a
2 thickness within the range of about 1000 Å to about 2500 Å.

1 13. The method of Claim 1, wherein etching is performed at a process chamber
2 pressure within the range of about 4 mTorr to about 10 mTorr.

1 14. The method of Claim 1, wherein said method is performed in a semiconductor
2 processing chamber having a decoupled plasma source.

1 15. The method of Claim 1, wherein said method provides a selectivity for etching
2 said silicon-containing dielectric layer relative to said photoresist of at least 2 : 1.

1 16. The method of Claim 1, wherein said method provides a sidewall etch profile
2 angle ranging from 84° to 92° between said etched silicon-containing dielectric layer and
3 an underlying horizontal layer.

1 17. A method of pattern etching a layer of silicon nitride on a semiconductor
2 substrate, wherein a patterned photoresist layer overlies said silicon nitride layer, said
3 method comprising exposing said silicon nitride layer to a plasma generated from a source
4 gas comprising CH_2F_2, CF_4, and O_2, wherein a volumetric ratio of CH_2F_2 to CF_4 is within
5 the range of about 1 : 2 to about 3 : 1, and wherein O_2 comprises about 2 to about 20 volume
6 % of the plasma source gas.

1 18. The method of Claim 1, wherein a volumetric ratio of CH_2F_2 to CF_4 is within the
2 range of about 1 : 2 to about 2 : 1.

1 19. The method of Claim 18, wherein a volumetric ratio of CH_2F_2 to CF_4 is within
2 the range of about 1 : 1 to about 2 : 1.

1 20. The method of Claim 1, wherein said source gas comprises about 30 to about 70
2 volume % CH_2F_2, about 30 to about 70 volume % CF_4, and about 2 to about 20 volume %
3 O_2.

1 21. The method of Claim 20, wherein said source gas comprises about 50 to about
2 70 volume % CH_2F_2, about 30 to about 50 volume % CF_4, and about 5 to about 15 volume
3 % O_2.

1 22. The method of Claim 1, wherein said source gas further includes helium.

1 23. The method of Claim 22, wherein said helium is present in said source gas at a
2 concentration within the range of about 50 to about 70 volume %.

1 24. The method of Claim 23, wherein said source gas comprises about 10 to about
2 25 volume % CH_2F_2, about 10 to about 25 volume % CF_4, about 2 to about 10 volume % O_2,
3 and about 50 to about 70 volume % helium.

1 25. The method of Claim 1, wherein said photoresist is sensitive to 248 nm radiation.

1 26. The method of Claim 1, wherein said silicon nitride layer is used as a hard mask
2 during pattern etching of an underlying semiconductor structure, and wherein said
3 semiconductor structure includes features having a feature size of about 0.13 μm or larger.

1 27. The method of Claim 1, wherein said silicon nitride layer has a thickness within
2 the range of about 1000 Å to about 2500 Å.

1 28. The method of Claim 1, wherein etching is performed at a process chamber
2 pressure within the range of about 4 mTorr to about 10 mTorr.

1 29. The method of Claim 1, wherein said method is performed in a semiconductor
2 processing chamber having a decoupled plasma source.

1 30. The method of Claim 1, wherein said method provides a selectivity for etching
2 said silicon nitride layer relative to said photoresist of at least 2 : 1.

1 31. The method of Claim 1, wherein said method provides a sidewall etch profile
2 angle ranging from 84° to 92° between said etched silicon nitride layer and an underlying
3 horizontal layer.

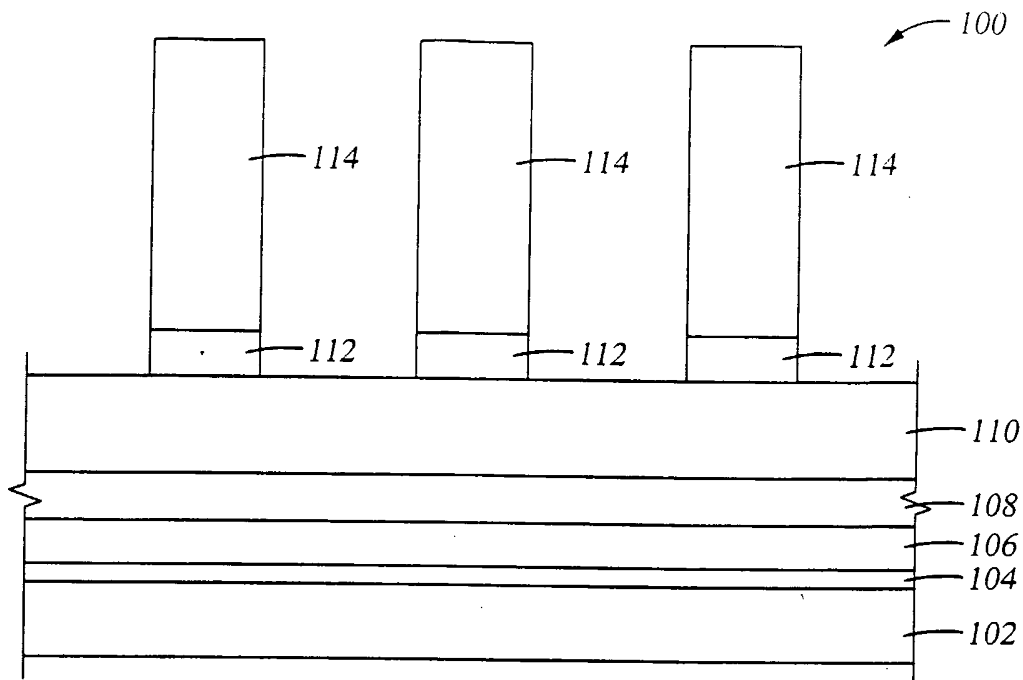


Fig. 1A
(PRIOR ART)

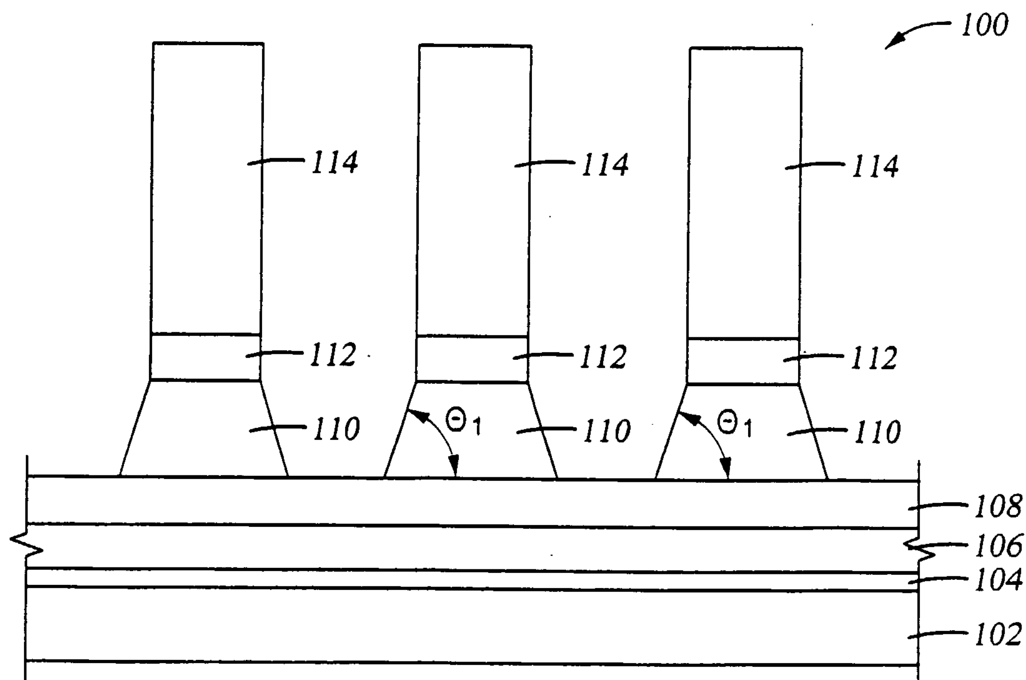


Fig. 1B
(PRIOR ART)

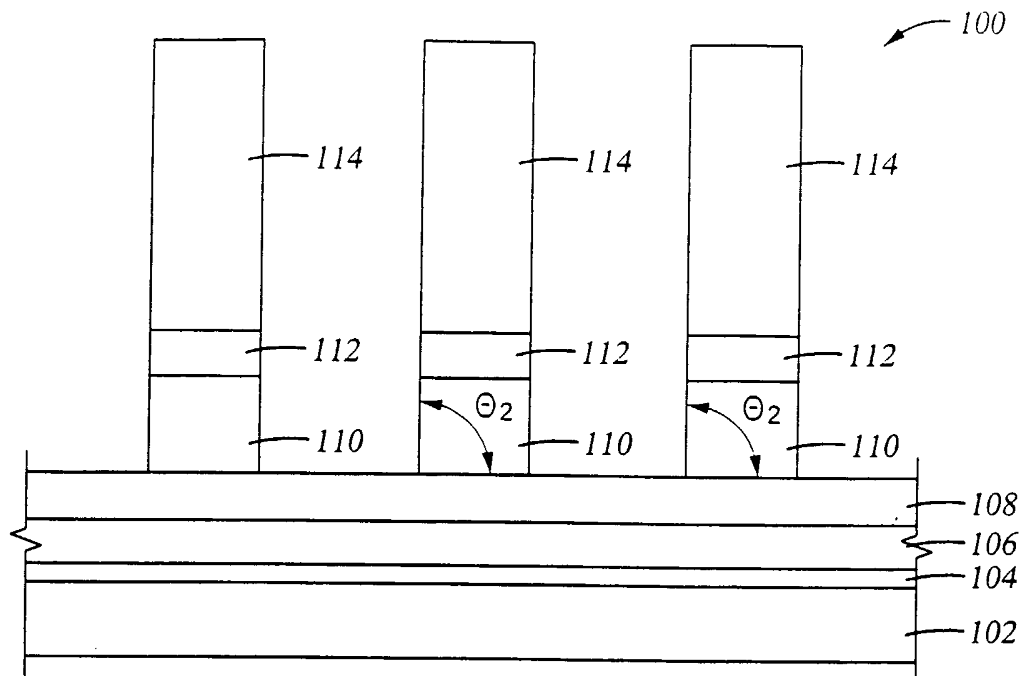


Fig. 1C

Fig. 2
(PRIOR ART)

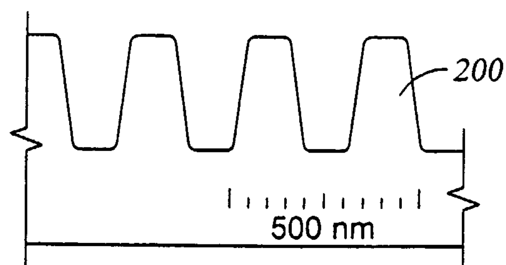
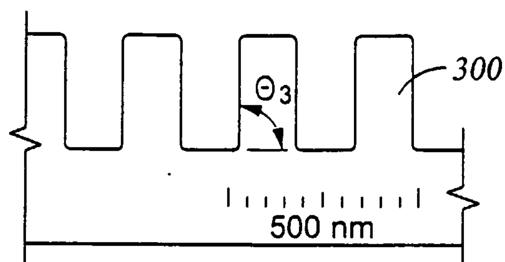


Fig. 3



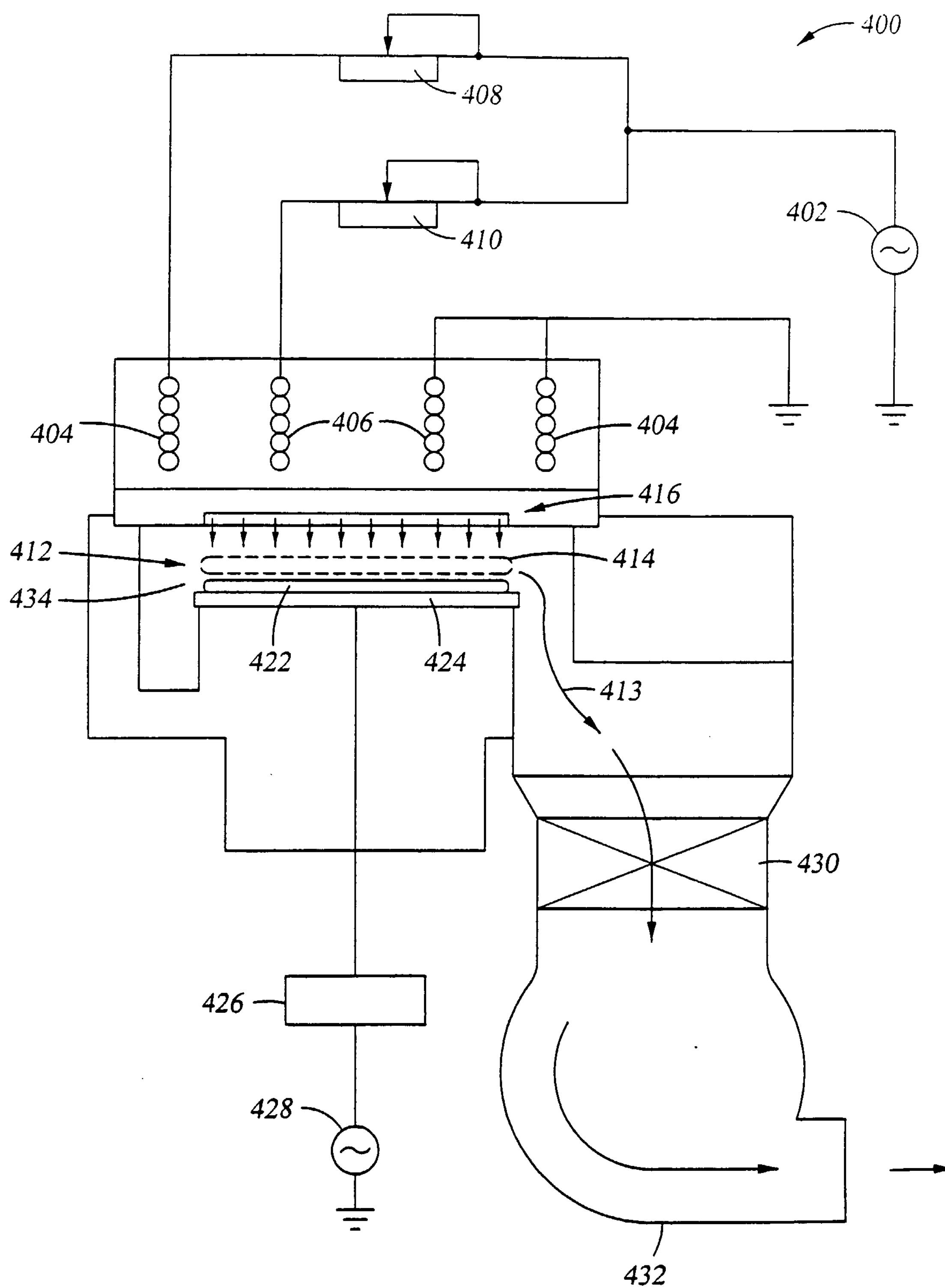


Fig. 4

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 03/33217

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/311 H01L21/3213

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ, INSPEC, CHEM ABS Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 362 109 B1 (KOMATSU TAKEHIKO ET AL) 26 March 2002 (2002-03-26) table 3	1-4, 10-19, 25-31
X	US 6 432 832 B1 (MELAKU YOSIAS ET AL) 13 August 2002 (2002-08-13) column 9, line 57 -column 10, line 16	1-9, 11-16
X	US 6 218 309 B1 (MILLER ALAN J ET AL) 17 April 2001 (2001-04-17) column 9	1-9, 11-16
X	US 6 309 962 B1 (CHAO LI-CHI ET AL) 30 October 2001 (2001-10-30) example 1	1-6, 11-14, 16-21, 26-29,31

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 March 2004	26/03/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Szarowski, A

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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International Application No
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