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(71) Applicant *(for all designated States except US)*: **CREE, INC.** [US/US]; 4600 Silicon Drive, Durham, NC 27703 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **EMERSON, David** [US/US]; 5519 New Rise Court, Chapel Hill, NC 27516 (US). **KELLER, Bernd** [DE/US]; 1335 San Antonio Creek Road, Santa Barbara, CA 93111 (US). **HUSSELL, Christopher** [US/US]; 101 Glenmore Road, Cary, NC 27519 (US). **SALTER, Amber** [US/US]; 900 Andrews Chapel Road, Durham, NC 27703 (US). **COLLINS, Brian** [US/US]; 6921 Springcreek Cove, #10, Raleigh, NC 27613 (US). **BERGMANN, Michael** [US/US]; 5700 Hideaway Drive, Chapel Hill, NC 27516 (US). **EDMOND, John** [US/US]; 1517 Colvard Farms Road, Durham, NC 27713 (US). **TARSA, Eric** [US/US]; 105 Dearborn Place, #41, Goleta, CA 93117 (US). **ANDREWS, Peter** [US/US]; 221 Continental Drive, Durham, NC 27712 (US).

(74) Agents: **PHILPOTT, Brian, J.** et al.; 2815 Townsgate Road, Suite 215, Westlake Village, CA 91361 (US).

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(54) Title: LED PACKAGE WITH INCREASED FEATURE SIZES

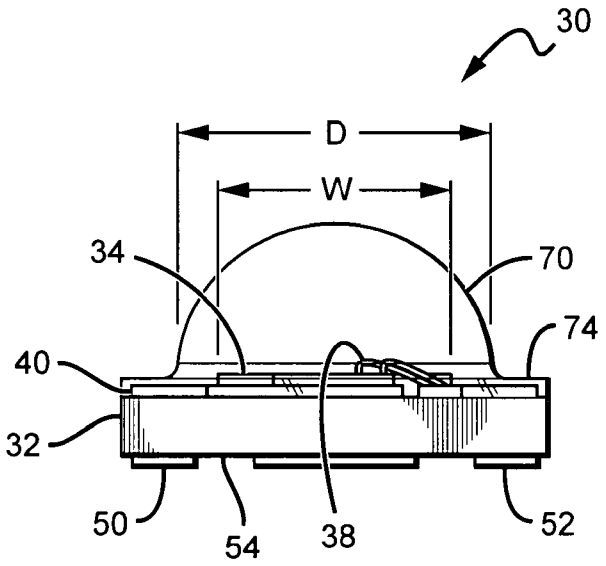

FIG. 4

(57) Abstract: A light emitting diode (LED) package (30) having increased feature sizes for improved luminous flux and efficacy. A LED chip (34) is disposed on a submount (32) with a lens (70) that covers the LED chip. In some cases, the ratio of the width of the light LED chip to the width of said lens in a given direction is 0.5 or greater. Increased feature sizes allow the package to • emit light more efficiently. Some packages, include submounts having dimensions greater than 3.5 mm per 3.5 mm used in conjunction with larger LED chips. Materials having high thermal conductivities are used to fabricate the submounts, such as APN, providing the package with better thermal management.

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LED PACKAGE WITH INCREASED FEATURE SIZES

[0001] This application is a continuation-in-part of prior U.S. Patent Application No. 11/982,275, filed 31 October 2007. This application claims the benefit of U.S. Provisional Application No. 61/173,550, filed 28 April 2009.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] This invention relates to light emitter packages, and in particular to light emitting diode (LED) packages having a molded lens.

Description of the Related Art

[0003] Light emitting diodes (LED or LEDs) are solid state devices that convert electric energy to light, and generally comprise one or more active layers of semiconductor material sandwiched between oppositely doped layers. When a bias is applied across the doped layers, holes and electrons are injected into the active layer where they recombine to generate light. Light is emitted from the active layer and from all surfaces of the LED.

[0004] In order to use an LED chip in a circuit or other like arrangements, it is known to enclose an LED chip in a package to provide environmental and/or mechanical protection, color selection, light focusing and the like.

An LED package can also include electrical leads, contacts or traces for electrically connecting the LED package to an external circuit. FIG. 1A shows a conventional LED package that generally comprises a single LED chip 12 mounted on a reflective cup 13 by means of a solder bond or conductive epoxy. One or more wire bonds 11 connect the ohmic contacts of the LED chip 12 to leads 15A and/or 15B, which may be attached to or integral with the reflective cup 13. The reflective cup 13 can be filled with an encapsulant material 16 which can contain a wavelength conversion material such as a phosphor. Light emitted by the LED at a first wavelength can be absorbed by the phosphor, which can responsively emit light at a second wavelength. The entire assembly is then encapsulated in a clear protective resin 14, which may be molded in the shape of a lens over the LED chip 12.

[0005] FIG. 1B shows another conventional LED package 20 that may be more suited for high power operations that can generate more heat. In the LED package 20, one or more LED chips 22 are mounted onto a carrier such as a printed circuit board (PCB) carrier, substrate or submount 23. A reflector 24 can be included on the submount 23 that surrounds the LED chip(s) 22 and reflects light emitted by the LED chips 22 away from the package 20. Different reflectors can be used such as metal reflectors, omni-directional reflectors (ODRs), and distributed Bragg reflectors (DBRs). The reflector 24 can also provide mechanical protection to the LED chips 22. One or more wirebond connections 11 are made between ohmic contacts on the LED chips 22 and electrical traces 25A, 25B on the submount 23. The mounted LED chips 22 are then covered with an encapsulant 26, which may provide

environmental and mechanical protection to the chips while also acting as a lens. The metal reflector 24 is typically attached to the carrier by means of a solder or epoxy bond.

[0006] While a package such as the package 20 illustrated in FIG. 1B may have certain advantages for high power operation, there may be a number of potential problems associated with using a separate metal piece as a metal reflector. For example, small metal parts may be difficult to manufacture repeatable with a high degree of precision at a reasonable expense. In addition, since the reflector is typically affixed to a carrier using an adhesive, several manufacturing steps may be required to carefully align and mount the reflector, which may add to the expense and complexity of the manufacturing process for such packages.

SUMMARY OF THE INVENTION

[0007] A light emitter package according to one embodiment of the present invention comprises the following elements. A submount is provided. A light emitter chip is mounted on the submount. A lens is disposed over the light emitter chip. The ratio of the width of the light emitter chip to the width of the lens in a given direction is 0.5 or greater.

[0008] A light emitting diode (LED) package according to an embodiment of the present invention comprises the following elements. A submount comprising top and bottom surfaces is provided. A plurality of top electrically and thermally conductive elements are disposed on the top surface of the submount. An LED chip is disposed on one of the top elements. The electrically conductive elements are arranged to spread heat from the LED chip across the

majority of the submount top surface. A bottom thermally conductive element is on the bottom surface and not in electrical contact with the top elements. The bottom thermally conductive element is arranged to conduct heat from the submount. A lens is disposed over the LED chip. The ratio of the width of the LED chip to the width of the lens in a given direction is 0.5 or greater.

[0009] A light emitter package according to an embodiment of the present invention comprises the following elements. A submount comprising aluminum nitride (AlN) is provided. A light emitter chip is disposed on the submount. The light emitter emitting light has an approximate average wavelength in the range of 430-460 nm. A lens is on the light emitter chip. The ratio of the width of the light emitter chip to the width of the lens in a given direction is 0.5 or greater.

[0010] A light emitter package according to an embodiment of the present invention comprises the following elements. A single light emitting diode (LED) chip is disposed on a submount having dimensions of 3.5 mm square or larger. A molded lens is disposed over the LED chip on the submount.

[0011] A light emitter package according to an embodiment of the present invention comprises the following elements. A light emitter chip is disposed on a submount comprising a material having a thermal conductivity of 30 W/m·K or higher. A molded lens is disposed over the emitter on the submount.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIG. 1A is a sectional view of a prior art LED package;

[0013] FIG. 1B is a sectional view of another prior art LED package;

[0014] FIG. 2 is a perspective view of one embodiment of an LED package according to the present invention without the lens;

[0015] FIG. 3 is a perspective view of the LED package shown in FIG. 2 from the opposite side;

[0016] FIG. 4 is a side view of LED package shown in FIG. 2 with a lens covering the LED chip;

[0017] FIG. 5 is a bottom perspective view of the LED package shown in FIG. 4;

[0018] FIG. 6 shows the conductive traces on the top surface of the submount for the LED package shown in FIG. 2;

[0019] FIG. 7 shows the conductive traces on the bottom surface of the submount for the LED package shown in FIG. 2;

[0020] FIG. 8 shows the top surface of the LED package as shown in FIG. 6, with a solder mask;

[0021] FIG. 9 shows the bottom surface of the LED package as shown in FIG. 7, with a solder mask;

[0022] FIG. 10 is a graph presenting data related to various lamps according to embodiments of the present invention;

[0023] FIG. 11 is a graph of the luminous intensity as a function of the CIE x-value of the output light for

several lamps according to embodiments of the present invention;

[0024] FIG. 12 is a graph of thermal resistance as a function of chip size; and

[0025] FIG. 13 a graph of relative luminous flux expressed as a percent versus wavelength in nanometers for several LED devices according to embodiments of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0026] The present invention is directed to compact, simple and efficient high power LED packages and methods for manufacturing same. Different embodiments can comprise one or more high power LEDs that typically operate at elevated power levels and temperatures. Packages according to the present invention can include features that allow for higher output power with still provided for thermal management by arranging features to help spread the heat from the LED. The heat can then dissipate into the ambient. The packages according to the present invention can also comprise a lens molded directly over the one or more LEDs to protect the LED while still allowing for efficient emission characteristics.

[0027] In conventional LED packages, light is most efficiently extracted through the molded lens for LEDs when the ratio of the width of the LED chip to the lens diameter is relatively low. LED chips with a smaller footprint (or width) compared to the diameter of the lens more closely emulate a point light source under the lens. This allows most LED light to reach lens surface within the critical angle for the light to escape from the lens,

so that most LED light escapes to contribute to useful emission for the LED package. For LED packages having a LED chip width to lens diameter ratio of 0.4 or less, most of the light from the LED chip escapes through the lens.

[0028] It is desirable to provide high power LED packages that emit elevated levels of light while at the same time maintaining the same size LED package footprint. One way to provide an LED package that emits elevated levels of light is by utilizing larger LED chips while maintaining the size of the LED package. This typically results in LED packages having a larger LED chip width to lens diameter ratio. As this ratio becomes higher, i.e. the width of the LED chip comes closer to the diameter of the lens, output power can decrease when this ratio exceeds a certain level. This is predominantly caused by an increased amount of the LED chip light reaching the surface of the lens at an angle that is outside the critical escape angle, such that the light experiences total internal reflection (TIR). TIR light can be absorbed into the components of the LED package following reflection so that it does not have the opportunity to escape from the LED package to contribute to useful light emission. In most conventional LED packages the LED chip width to lens diameter ratio does not exceed 0.4.

[0029] Some embodiments of the present invention provide for a high power LED package utilizing an increased LED chip width to lens diameter ratio. This allows the LED packages to provide increased output power while at the same time providing an LED package footprint of the same size as lower powered LED packages. Despite the increase in TIR at the surface of the lens that can result from the increased LED chip width to lens diameter ratio, the

LED packages according to the present invention are arranged with different features or characteristics that allow for an overall increase in emitted light. Some of the features include LED packages with LED chips having lower current density and/or a conversion coating utilizing having larger phosphor particle sizes.

[0030] The present invention provides low cost, relatively small size LED packages that provide an efficient but small light source. The packages according to the present invention are particularly adapted to surface mount technologies and provide features that allow for the good thermal dissipation, allowing the packages to operate at elevated power levels without overheating. The LED chips can also provide scattering features that scatter the LED chip light as it emits from the package to provide for increased uniformity. The LED chips can also provide electrostatic discharge (ESD) protection circuits to protect the LED chip from damage do to an ESD event.

[0031] The present invention is described herein with reference to certain embodiments, but it is understood that the invention can be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. In particular, the present invention is described below in regards to certain LED packages in certain configurations, but it is understood that the present invention can be used for many other LED packages having many different configurations. The components can have different shapes and sizes beyond those shown and different features can be included in the LED packages to provide increased output power. The LED packages can include more than one LED chip with one or all of the LED chips being coated with a down-converter

coating that can comprise a phosphor loaded binder. It is understood, however, that LED chips can be used that do not have a conversion material.

[0032] It is understood that when an element such as a layer, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. Furthermore, relative terms such as "inner", "outer", "upper", "above", "lower", "beneath", and "below", and similar terms, may be used herein to describe a relationship of one layer or another region. It is understood that these terms are intended to encompass different orientations of the device in addition to the orientation depicted in the figures.

[0033] Although the terms first, second, etc., may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer or section from another region, layer or section. Thus, a first element, component, region, layer or section discussed below could be termed a second element, component, region, layer or section without departing from the teachings of the present invention.

[0034] Embodiments of the invention are described herein with reference to cross-sectional view illustrations that are schematic illustrations of idealized embodiments of the invention. As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances are expected. Embodiments of the invention should not be construed as limited to the

particular shapes of the regions illustrated herein but are to include deviations in shapes that result, for example, from manufacturing. A region illustrated or described as square or rectangular will typically have rounded or curved features due to normal manufacturing tolerances. Thus, the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the precise shape of a region of a device and are not intended to limit the scope of the invention.

[0035] FIGs. 2 through 9 show different features of one embodiment of an LED package 30 according to the present invention generally comprising a substrate/submount ("submount") 32 that can hold one or more LEDs emitting the same or different colors. In the embodiment shown a single LED 34 is mounted on the submount 32. The LED 34 can have many different semiconductor layers arranged in different ways. LED structures and their fabrication and operation are generally known in the art and only briefly discussed herein. The layers of the LED 34 can be fabricated using known processes with a suitable process being fabrication using metal organic chemical vapor deposition (MOCVD). The layers of the LEDs 34 generally comprise an active layer/region sandwiched between first and second oppositely doped epitaxial layers all of which are formed successively on a growth substrate. LEDs can be formed on a wafer and then singulated for mounting in a package. It is understood that the growth substrate can remain as part of the final singulated LED or the growth substrate can be fully or partially removed. In embodiments where the growth substrate remains, it can be shaped or textured to enhance light extraction.

[0036] It is also understood that additional layers and elements can also be included in the LED 34, including

but not limited to buffer, nucleation, contact and current spreading layers as well as light extraction layers and elements. It is also understood that the oppositely doped layers can comprise multiple layers and sub-layers, as well as super lattice structures and interlayers. The active region can comprise single quantum well (SQW), multiple quantum well (MQW), double heterostructure or super lattice structures. The active region and doped layers may be fabricated from different material systems, with preferred material systems being Group-III nitride based material systems. Group-III nitrides refer to those semiconductor compounds formed between nitrogen and the elements in the Group III of the periodic table, usually aluminum (Al), gallium (Ga), and indium (In). The term also refers to ternary and quaternary compounds such as aluminum gallium nitride (AlGaN) and aluminum indium gallium nitride (AlInGaN). In a preferred embodiment, the doped layers are gallium nitride (GaN) and the active region is InGaN. In alternative embodiments the doped layers may be AlGaN, aluminum gallium arsenide (AlGaAs) or aluminum gallium indium arsenide phosphide (AlGaInAsP).

[0037] The growth substrate can be made of many materials such at sapphire, silicon carbide, aluminum nitride (AlN), GaN, with a suitable substrate being a 4H polytype of silicon carbide, although other silicon carbide polytypes can also be used including 3C, 6H and 15R polytypes. Silicon carbide has certain advantages, such as a closer crystal lattice match to Group III nitrides than sapphire and results in Group III nitride films of higher quality. Silicon carbide also has a very high thermal conductivity so that the total output power of Group-III nitride devices on silicon carbide are

typically not limited by the thermal dissipation of the substrate (as may be the case with some devices formed on sapphire). SiC substrates are available from Cree Research, Inc., of Durham, North Carolina and methods for producing them are set forth in the scientific literature as well as in a U.S. Patents, Nos. Re. 34,861; 4,946,547; and 5,200,022.

[0038] The LED 34 can also comprise a conductive current spreading structure 36 on its top surface, as well as one or more contacts 38 accessible at its top surface for wire bonding. The spreading structure 36 and contact can both be made of a conductive material such as Au, Cu, Ni, In, Al, Ag or combinations thereof, conducting oxides and transparent conducting oxides. The current spreading structure 36 generally comprises conductive fingers 37 arranged in a grid on the LED 34 with the fingers spaced to enhance current spreading from the contacts 38 into the LED's top surface. In operation, an electrical signal is applied to the contacts 38 through a wire bond as described below, and the electrical signal spreads through the fingers 37 of the current spreading structure 36 and the top surface into the LED 34. Current spreading structures are often used in LEDs where the top surface is p-type, but can also be used for n-type materials.

[0039] The LED can be coated with one or more phosphors with the phosphors absorbing at least some of the LED light and emitting a different wavelength of light such that the LED emits a combination of light from the LED and the phosphor. In a preferred embodiment the LED emits a white light combination of LED and phosphor light. The LED can be coated using many different methods and with many different conversion materials, with suitable methods and materials being described in U.S. Patent

Applications Serial Nos. 11/656,759 and 11/899,790, both entitled "Wafer Level Phosphor Coating Method and Devices Fabricated Utilizing Method", and both of which are incorporated herein by reference. Alternatively the LEDs can be coated using other methods such an electrophoretic deposition (EPD), with a suitable EPD method described in U.S. Patent Application No. 11/473,089 entitled "Close Loop Electrophoretic Deposition of Semiconductor Devices", which is also incorporated herein by reference. It is understood that LED packages according to the present invention can also have multiple LEDs of different colors, one or more of which may be white emitting.

[0040] The submount 32 can be formed of many different materials with a preferred material being electrically insulating. Suitable materials include, but are not limited to ceramic materials such as aluminum oxide, aluminum nitride or organic insulators like polyimide(PI) and polyphthalamide (PPA). In other embodiments the submount 32 can comprise a printed circuit board (PCB), sapphire or silicon or any other suitable material, such as T-Clad thermal clad insulated substrate material, available from The Bergquist Company of Chanhassen, Minn. For PCB embodiments different PCB types can be used such as standard FR-4 PCB, metal core PCB, or any other type of printed circuit board. LED packages according to the present invention can be fabricated using a method that utilizes a submount panel sized to accommodate a plurality of sumbmounts. Multiple LED packages can be formed on the panel, with the individual packages being singulated from the panel.

[0041] As noted, many materials can be used to fabricate the submount element. In various embodiments, it is

desirable to have a submount that is a good electrical insulator with low thermal resistance or high thermal conductivity (e.g., aluminum nitride). Some materials that may be used have a thermal conductivity of approximately 30 W/m·K or higher, such as zinc oxide (ZnO). Other acceptable materials have thermal conductivities of approximately 120 W/m·K or higher, such as aluminum nitride (AlN) which has a thermal conductivity that can range from 140-180 W/m·K. In terms of thermal resistance, some acceptable materials have a thermal resistance of 2 °C/W or lower. Other materials may also be used that have thermal characteristics outside the ranges discussed herein.

[0042] FIG. 12 shows thermal resistance in °C/W as a function of chip size in a package. The data represents four actual devices having ceramic submounts shown as diamonds and two actual devices having aluminum nitride submounts. The data for the ceramic submounts has been extrapolated out to estimate the thermal resistance for two larger chips. The data show that thermal resistance is reduced as chip size increases. Also the thermal resistance is lower for the chips with aluminum nitride submounts as compared to similarly sized chips with ceramic submounts. The data in FIG. 12 is included to support the general propositions discussed above. It is understood that the data should not limit the scope of any embodiments of the present invention.

[0043] A submount having these properties allows for a device package in which the LED can be operated with higher drive currents. Because the submount has a relatively low thermal resistance, the additional heat generated by the higher drive current is more easily dissipated into the ambient. A higher drive current can

produce a brighter output from the LED. Similarly, a device incorporating a low thermal resistance submount can be operated at a given drive current for a longer period of time when compared to a device having a submount with a higher thermal resistance. That is, the lifetime and reliability of the device can be increased. Additionally, devices having a low thermal resistance submount can operate in higher ambient (or background) temperatures, making them useful in applications designed for harsh environmental conditions.

[0044] In devices according to one embodiment, an output power of greater than 150 lumens/watt of white emission within a 7-step MacAdams ellipse along the black body curve has been achieved using an 3.5 mm square aluminum nitride (AlN) submount in combination with a 1.4 mm square LED chip. This device may be scalable to achieve similar results at larger submount/LED size combinations.

[0045] In some embodiments it may be advantageous to use LED chips emitting light having an average wavelength in the range of 430-460 nm. In some cases the ranges may be narrower, for example, 430-450 nm or 440-445 nm. LEDs emitting at shorter wavelengths, such as the ranges given, may exhibit better brightness and/or reliability when operated at higher ambient temperatures as compared to LEDs emitting light having a longer average wavelength and operating at the same temperature.

[0046] FIG. 13 shows a graph of relative luminous flux expressed as a percent versus wavelength in nanometers for several LED devices that might be used in LED packages according to embodiments of the invention. The relative luminous flux was calculated by dividing the luminous flux at a temperature of 80 °C (measured at a

solder point) by the luminous flux at room temperature and expressing the quotient as a percentage. Thus, in some embodiments LED chips emitting shorter wavelength light may be desirable to increase brightness and reliability.

[0047] As best shown in FIG. 4, an optical element or lens 70 is formed on the top surface 40 of the submount 32, over the LED 34, to provide both environmental and/or mechanical protection. The lens 70 can be in different locations on the top surface 40 with the lens located as shown with at approximately the center of the submount 32, with the LED 34 at approximately the center of the lens base. In some embodiments the lens can be formed in direct contact with the LED 34 and the submount's top surface 40. In other embodiments there may be an intervening material or layer between the LED 34 and top surface 40. Direct contact to the LED 34 provides certain advantages such as improved light extraction and ease of fabricating.

[0048] The lens 70 can be molded using different molding techniques such as those described in U.S. Patent Applications Serial Nos. 11/982,275 entitled "Light Emitting Diode Package and Method for Fabricating Same", which is incorporated herein by reference. The lens can be many different shapes depending on the desired shape of the light output. One suitable shape as shown is hemispheric, with some examples of alternative shapes being ellipsoid bullet, flat, hex-shaped and square. Many different materials can be used for the lens such as silicones, plastics, epoxies or glass, with a suitable material being compatible with molding processes. Silicone is suitable for molding and provides suitable optical transmission properties. It can also withstand

subsequent reflow processes and does not significantly degrade over time. It is understood that the lens 70 can also be textured to improve light extraction or can contain materials such as phosphors or scattering particles. In some embodiments, the lens 70 can comprise two portions: a flat portion 70a and a dome portion 70b. The flat portion 70a is disposed over the LED 34, with the dome portion 70b positioned on the flat portion 70a. These portions 70a, 70b can be made from the same material or they may be made of two different materials.

[0049] The LED package 30 can also comprise a protective layer 74 covering the submount's top surface 40 between the lens 70 and edge of the submount 32. The layer 74 provides additional protection to the elements on the top surface to reduce damage and contamination during subsequent processing steps and use. Protective layer 74 can be formed during formation of the lens 70 and can comprise the same material as the lens 70. It is understood, however, that the LED package 30 can also be provided without the protective layer 74.

[0050] The lens 70 should also be able to withstand certain sheer forces before being displaced from the submount 32. In one embodiment, the lens can withstand a 1 kilogram (kg) or more sheer force. In embodiments of the LED package using silicones that are harder after curing and have a higher durometer reading, such as Shore A 70 or higher, tend to better withstand sheer forces. Properties such as high adhesion and high tensile strength may also contribute to the ability of the lens to withstand sheer forces.

[0051] The lens arrangement of the LED package 30 is also easily adapted for use with secondary lens or optics that

can be included over the lens by the end user to facilitate beam shaping. These secondary lenses are generally known in the art, with many of them being commercially available.

[0052] The present invention can be used in LED packages having different sizes or footprints, with one important factor being the ratio between the LED chip width (W) and the diameter or width of the lens (D) in a given direction. In one embodiment of package 30 the footprint can be essentially the same dimension as the effective heat spreading area in the first and second attach pads 42, 44, and 46. As described above, different embodiments of the present invention are directed to providing LED packages having increased power output while maintaining the same LED package size or footprint. By maintaining the same package footprint, the lens would generally have the same size. As mentioned above, one way to increase output power is to increase the size (i.e. width W) of the LED chip in LED package. That is, for different embodiments according to the present invention the surface area of the LED covers an increased percentage of the surface area of the LED packages submount. In some embodiments according to the present invention the surface area of the LED chip covers more than 10% of the submounts surface area, while in other embodiments it covers more than 15% of the submounts surface area.

[0053] FIG. 4 shows the chip width W and lens diameter D. LED package embodiments according to the present invention can have different W to D ratios, with some embodiments having a ratio greater than 0.5. One embodiment of an LED package 30 according to the present invention can comprise a submount 32 that is approximately 3.45 mm square (i.e., 3.45 mm x 3.45 mm)

and a lens having a diameter of approximately 2.55 mm. In conventional LED packages this size of submount would hold a LED chip having a size in the range of 0.7 to 1.0 mm square. The LED package 30 is arranged to hold a larger LED chip that is approximately 1.4 mm square such that the W to D ratio is 0.55. In this embodiment, the LED chip's surface area covers more than 16% of the submount's surface area.

[0054] In other embodiments, a submount having dimensions of 5 mm square is desirable. Such a submount can accommodate larger LED chip sizes including 1.75 mm square, 2 mm square, and 3 mm square. One example of a submount/LED chip combination is a 5 mm square submount with a 1.75 mm square LED chip. In one particular embodiment a 2 mm square LED chip is used in combination with a 5 mm square aluminum nitride submount. In another particular embodiment a 3 mm chip is used with a 5 mm submount. For the 5 mm submount packages, a molded lens having a diameter of approximately 4.52 mm is disposed over the chip. The given sizes are exemplary. It is understood that larger or smaller lenses, submounts, and LED chips are possible and that many different combinations of lenses, submounts, and LED chips having various sizes are possible. Furthermore, although the submounts discussed herein refer to dimensions indicating a square shaped submount, it is understood that other submounts may have a circular or rectangular shape, for example.

[0055] Several LED devices according to embodiments of the present invention which include 2 mm square chips were built and tested. Devices exhibiting a luminous flux of 160 lm or higher at efficacies of 160 lm/W or higher were achieved with a drive current of 350 mA. Devices

exhibiting a luminous flux of 750 lm or higher at efficacies of 110 lm/W or higher were achieved with a drive current of 2 A. For example, a 2 mm square chip device was manufactured that was measured to output 168.5 lm at a drive current of 350 mA and a voltage of 2.86 V for 168 lm/W. Another 2 mm square chip was fabricated that was measured to output 791.6 lm at a drive current of 2001 mA and a voltage of 3.4 V for 116 lm/W. Chips with similar characteristics may be used in LED packages according to embodiments of the present invention.

[0056] As described above, increasing the ratio of W to D can result in an overall decrease in output power as a result of TIR of the LED chip light at the surface of the lens. LED packages according to the present invention can have additional features that overcome the decrease associated with TIR to provide an overall increase in output power compared to LED packages with a smaller W to D ratio. In one embodiment, the overall increase can be partially attributable to lower overall current density based on the increases LED chip area. Decreased current density can provide for increased LED chip emission efficiency. In the embodiment described above, the increase in LED chip size from a conventional 0.7mm or 1.0mm LED chip to the larger 1.4mm LED chip can result in reduced current density that provides an overall approximate output power increase of 6%.

[0057] FIG. 10 is a graph presenting data related to various lamps that were built and tested which embody aspects of the present invention. The color points of the output light from several lamps are plotted on a portion of the 1931 CIE Curve with an overlay indicating some of Cree's standard white light chromaticity regions (bins). For this particular set of lamps, the color points are

distributed over several standard Cree bins (i.e., WK, WB, WE, WC, WF and WG) in the white light region of the CIE Curve. The large data point found within the WG bin corresponds to a lamp which exhibited a luminous flux of approximately 148 lm as best shown in FIG. 11.

[0058] FIG. 11 shows a graph of the luminous intensity as a function of the CIE x-value of the output light for several lamps embodying aspects of the present invention which were produced and tested. The graph shows lamps ranging in luminous flux from approximately 127-149 lm. These particular lamps were driven with a current of 350 mA. It is understood that a higher drive current would yield a higher luminous flux. As noted above, the large data point represents a lamp which corresponds to a CIE x-value of approximately 0.32, having a luminous flux of approximately 148 lm. As shown in FIG.10, this particular lamp has a color point that falls within Cree's WG white light bin. All of the lamps in FIGs. 10 and 11 were produced to have a given submount size (footprint) of approximately 3.45 mm x 3.45 mm. From the data, it is possible to establish a minimum ratio of luminous flux to footprint size for a given x-value on the CIE Curve. For example, a lamp having output light with a CIE x-value of approximately 0.286 exhibited a ratio of luminous flux to footprint size of approximately:

$$127 \text{ lm} / (3.45 \text{ mm})^2 \approx 10.67 \text{ lm/mm}^2$$

In another example, a different lamp having a CIE x-value of approximately 0.32 exhibited a ratio of luminous flux to footprint size of approximately:

$$148 \text{ lm} / (3.45 \text{ mm})^2 \approx 12.43 \text{ lm/mm}^2$$

[0059] The luminous flux of the lamps can be increased by increasing the footprint size according to the exemplary minimum ratios. It is understood that these examples are only meant to establish minimum ratios of luminous power to footprint size for a given CIE x-value. Higher luminous fluxes and, hence, higher ratios are possible. Furthermore, although not shown in FIGs. 10 and 11, it is possible to establish ratios of luminous flux to footprint size for various y-values on the CIE Curve and various x-y paired values (color points) on the CIE curve.

[0060] In other embodiments, the overall increase in emission efficiency can be attributable to the use of larger sized phosphor particles for the conversion material. Many conventional LED chips utilize a conversion material with particle sizes of approximately 5 microns. Some embodiments according to the present invention utilize a conversion material having a D_{50} phosphor particle size of greater than 5 microns, with suitable conversion materials having a D_{50} phosphor particle size of greater than 10 microns; other embodiments may include particle sizes of approximately 20 microns or greater. In one embodiment according to the present invention, the conversion material comprises YAG having a D_{50} particle size of approximately 16 microns. In some embodiments the use of increased phosphor particle sizes can result in increased power output of 8% or more. These embodiments provide for a relatively small overall lens combined with a phosphor having a relatively large D_{50} particle size, independent of chip size. In some embodiments, the ratio of D_{50} particle size of at least 10 microns to lens diameter or width of 2.55mm (or 2550 microns) can be greater than approximately 0.4%. In

other embodiments, the ratio of D50 particle size of at least 16 microns to lens diameter or width of 2.55mm can be greater than 0.6%.

[0061] Although applicant does not want to be bound by any one theory, it is believed that this increase is due to the fact that larger particle sizes typically do not backscatter as much LED light as smaller sized phosphor particles. As a result, less light is absorbed by the LED chip or the other LED package components after it is backscattered. In some embodiments, however, this can result in reduced emission uniformity from the LED package with one possible reason being that less light is backscattered and as a result there is less opportunity to mix the LED light and downconverted light from conversion material. The relationship between emission efficiency and phosphor particle size may be related to the defect density on or within a phosphor particle. Phosphor defects tend to be more concentrated on the surfaces of a phosphor particle and therefore as particle sizes increase the defect density decreases. Stated differently, a conversion material with a larger average phosphor particle size may have a lower total number of defects. Some of the surface densities can include surface roughness, dislocations, cracks or impurities. Some of the internal phosphor particle defects can comprise bubbles, delaminations, or impurities. In some embodiments, an increase in emission efficiency may be attained by providing a conversion material that includes a phosphor with reduced surface defects for any average particle size, such as a D_{50} as low as 3 microns or as high as 25 microns. The use of larger is phosphor particles greater that 10 microns is described in U.S. Patent Application No. 12/024,400, entitled

"Semiconductor Light Emitting Devices With High Color Rendering", which is incorporated herein by reference.

[0062] The above are only two of the features or characteristics for LED packages according to the present invention that can lead to an overall increase in light emission.

[0063] In some applications the decreased emission uniformity mentioned above can be acceptable in certain applications such as in street lighting. In other embodiments the decreased emission uniformity can be compensated for at the systems level using different mechanisms such as diffusers or scattering elements. To provide improved uniformity at the LED package level, scattering materials can be provided in different locations in the LED package. In some embodiments, the scattering material can be in the conversion material, while in other embodiments it can be included in or on the lens. In still other embodiments it can comprise a layer of material on the top of the LED chip. Scattering particles can comprise many different materials, including:

silica gel;
zinc oxide (ZnO);
yttrium oxide (Y_2O_3);
titanium dioxide (TiO_2);
barium sulfate ($BaSO_4$);
alumina (Al_2O_3);
fused silica (SiO_2);
fumed silica (SiO_2);
aluminum nitride;
glass beads;
zirconium dioxide (ZrO_2);

silicon carbide (SiC);
tantalum oxide (TaO_5);
silicon nitride (Si_3N_4);
niobium oxide (Nb_2O_5);
boron nitride (BN); or
phosphor particles (e.g., YAG:Ce, BOSE)

Other materials not listed may also be used and various combinations of materials may be used to achieve a particular scattering effect. In one embodiment, the scattering particles can comprise a D_{50} particle size of larger than approximately 4 microns. A suitable embodiment comprises a D_{50} particle size in the range of 15 - 20 microns, with one embodiment D_{50} particle size of larger than approximately 4 microns having a D_{50} particle size approximately the same size as the conversion materials D_{50} particle size.

[0064] Similar to the larger sized phosphor particles, it is believed that the larger sized scattering particles result in reduced backscattering due to reduced particle defects. With less backscattering there can be less opportunity for light to be absorbed in the LED chip components. This reduced backscattering can also result in less opportunity for light to mix, thereby reducing the overall mixing efficiency of the scattering particle. Light from the LED chip, however, interacts with the phosphor particles in such a way that light is redirected the scattering particles with most of the light not being backscattered. The scattering particles can also be arranged so light from the LED chip interacts with the scattering particles a limited number of times to further reduce the possibility of backscattering. This can be accomplished by controlling the scattering particle layer thickness or concentration of scattering particles. This

redirecting of light while controlling the number of light interactions can result in light that is substantially forward scattered.

[0065] Different embodiments according to the present invention can have a conversion material with larger phosphor particles as described above, so that most of the light converted by the phosphor particles is not backscattered. That is, the light is forward converted to increase efficiency. To achieve the desired emission uniformity, a scattering material can be included that also has the characteristic of most of the light not being backscattered. That is, the light is forward scattered. The increased efficiency with the desired emission uniformity of these embodiments can be attributable to forward light conversion followed by forward scattering.

[0066] LED packages according to the present invention also comprise heat management features to allow operation at elevated temperatures. As best shown in FIG. 6 (but partially shown in other figures), the top surface 40 of the submount 32 comprises patterned conductive features that can include a die attach pad 42 with an integral first contact pad 44. A second contact pad 46 is also included on the submount's top surface 40 with the LED 34 mounted approximately at the center of the attach pad 42. These patterned conductive features provide conductive paths for electrical connection to the LED 34 using known contacting methods. The LED can be mounted to the attach pad 42 using known methods and material mounting such as using conventional solder materials that may or may not contain a flux material or dispensed polymeric materials that may be thermally and electrically conductive.

[0067] The attach pad 42 and first and second contact pads 44, 46 can comprise much different material such as metals or other conductive materials. In one embodiment the pads 42, 44, 46 comprise copper deposited using known techniques such as plating. In typical plating process a titanium adhesion layer and copper seed layer are sequentially sputtered onto a substrate. Then, approximately 75 microns of copper is plated onto the copper seed layer. The resulting copper layer being deposited can then be patterned using standard lithographic processes. In other embodiments the layer can be sputtered using a mask to form the desired pattern.

[0068] In some embodiments according to the present invention some of the conductive features can include only copper, with others of the features including additional materials. For example, the attach pad 42 can be plated or coated with additional metals or materials to the make the attach pad 42 more suitable for mounting an LED 34. For example, the attach pad 42 can be plated with adhesive or bonding materials, or reflective and barrier layers.

[0069] A gap 48 (best shown in FIGs. 6 and 8) is included between the second pad 46 and the attach pad 42 down to the surface of the submount 32 that, with the gap providing electrical isolation between the attach pad 42 and second pad 46. As further described below, an electrical signal is applied to the LED 34 through the second pad 46 and the first pad 44, with the electrical signal on the first pad 44 passing directly to the LED 34 through the attach pad 42 and the signal from the second pad passing into the LED 34 through wire bonds. The gap 48 provides electrical isolation between the second pad

46 and attach pad to prevent shorting of the signal applied to the LED 34.

[0070] In some embodiments and electrical signal can be applied to the package 30 by providing external electrical contact to the first and second bond pads 44, 46 such as by solder contacts or other conductive paths to a PCB. In the embodiment shown the LED package 30 is arranged for mounting using surface mount technology and having internal conductive paths. The LED 30 comprises first and second surface mount pads 50, 52 (best shown in FIGs. 5, 7 and 9) that can be formed on the submount's back surface 54, at least partially in alignment with the first and second contact pads 44, 46, respectfully. Electrically conductive vias 56 are formed through the submount 32 between the first mounting pad 50 and the first contact pad 44, such that when a signal is applied to the first mounting pad 50 is conducted to first contact pad 44. Similarly, conductive vias 56 are formed between the second mounting pad 52 and second contact pad to conduct an electrical signal between the two. The first and second mounting pads 50, 52 allow for surface mounting of the LED package 30 with the electrical signal to be applied to the LED 34 applied across the first and second mounting pads 50, 52. The vias 56 and contact pads 44,46 can made of many different materials deposited using different techniques, such as those used for the attach and contact pads 42, 44, 46.

[0071] It is understood that the mounting pads 50, 52 and vias 56 can be arranged in many different ways and can have many different shapes and sizes. It is also understood that instead of vias, one or more conductive traces can be provided on the surface of the submount

between the mounting pads and contact pads, such as along the side surface of the submount.

[0072] Referring now to FIGs. 2, 3, 8 and 9, a solder mask 58 made of conventional materials can be included on the submount's top surface 40, at least partially covering the attach pad 42 and the first and second contact pads 44, 46, and at least partially covering the gap 48. The solder mask 58 protects these features during subsequent processing steps and in particular mounting the LED 34 to the attach pad 42 and wire bonding. During these steps there can be a danger of solder or other materials depositing in undesired areas, which can result in damage to the areas or result in electrical shorting. The solder mask serves as an insulating and protective material that can reduce or prevent these dangers. The solder mask comprises opening for mounting the LED 34 to the attach pad 42 and for attaching wire bonds to the second contact pad 46. It also comprises side openings 60 to allow convenient electrical access to the contact pads 44, 46 for testing the package 30 during fabrication. The solder mask 58 also has alignment holes that provide for alignment during fabrication of the package 30 and also allow for alignment when mounted in place by the end user.

[0073] Referring now to FIG. 6, in some embodiments the conductive traces can be provided with a symbol or indicator 69 to illustrate which side of the LED package 30 should be coupled to the plus or minus of the signal to be applied to the package. This can ensure accurate mounting of the LED package 30 to a PCB or other fixture, whether by machine or hand. In the embodiment shown the symbol 69 comprises a plus (+) sign over the first contact pad 44, indicating that the package 30 should be

mounted with the positive of the signal coupled to the first surface mount pad 52. The minus of the signal would then be coupled to the second mount pad 54. It is understood that many different symbol types can be used and that a symbol can also be included over the second conductive pad 46. It is also understood that the symbols can be placed in other locations other than the solder mask 58.

[0074] The package 30 can also comprise elements to protect against damage from electrostatic discharge (ESD). In the embodiment the ESD element is on-chip, and different elements can be used such as various vertical silicon (Si) Zener diodes, different LEDs arranged in parallel and reverse biased to the LED 34, surface mount varistors and lateral Si diodes. In the embodiment shown a Zener diode 62 is utilized and is mounted to the attach pad 42 using known mounting techniques. The diode is relatively small so that it does not cover an excessive area on the surface of the submount 32. In the embodiment shown, the diode 62 is mounted adjacent to the LED chip 34 and in some embodiments it can be on a separate attach pad. The diode 62 should be mounted to the submount 32 as close as possible to the center of submount's center without interfering with other components of the LED package 30.

[0075] It is noted that the solder mask 58 includes an opening for the ESD diode 62 so that it can be mounted to the attach pad 42. Different mounting materials and methods can be used such as those used to mount the LED 34 to the attach pad 42. An ESD wire bond 64 is included between the second contact pad 46 at the solder mask opening and the ESD diode 62. Two LED wire bonds 65 are also included between the solder mask opening in the

second contact pad 46 and wire bond pads 38 on the LED 34. In other embodiments only one wire bond can be included between the LED 34 and second contact pad. This LED 34 and ESD diode 62 arrangement allows excessive voltage and or current passing through the LED package 30 from an ESD event to pass through the diode 62 instead of the LED 34, protecting the LED 34 from damage. The wire bonds 64 and 65 can be applied using known methods and can comprise known conductive materials, with a suitable material being gold (Au). It is understood that in other embodiments of an LED package according to the present invention can be provided without an ESD element/diode or with an ESD element/diode that is external to the LED package 30.

[0076] As mentioned above, heat typically does not spread efficiently into the submount 32, particularly those made of materials such as ceramic. When a LED is provided on an attach pad that extends generally only under the LED, heat does not spread through most of the submount, and is generally concentrated to the area just below the LED. This can cause overheating of the LED which can limit the operating power level for the LED package.

[0077] To improve heat dissipation in the LED package 30 the pads 42, 44, 46 provide extending thermally conductive paths to conduct heat away from the LED 34 such that it can spread to other areas of the submount beyond the areas just below the LED 34. The attach pad 42 covers more of the surface of the submount 32 than the LED 34, with the attach pad extending from the edges of the LED 34 toward the edges of the submount 32. In the embodiment shown, the attach pad 42 is generally circular and extending radially from LED 34 toward the edges of the submount 32. A portion of the attach pad 42

intersects with the first and second contact pads 44, 46, with the gap 48 separating part of the attach pad adjacent to the second contact pad 46. It is understood that the contact pad 42 can be many other shapes and in some embodiments can extend to the edge of the submount 32. The contact pads 44, 46 also cover the surface of the submount 32 between the vias 56 and the edges of the submount 32. By extending the pads 42, 44 and 46 this way, the heat spreading from the LED 34 is improved. This improves thermal dissipation of heat generated in the LED 34, which improves its operating life and allows for higher operating power. The pads 42, 44, and 46 can cover different percentages of the top surface 40 of the submount 32, with a typical coverage area being greater than 50%. In other embodiments the coverage area can be greater than 75%.

[0078] The LED package 30 further comprises a metalized area 66 (best shown in FIGs. 5 and 9) on the back surface 54 of the submount 32, between the first and second mounting pads 50, 52. The metalized area is preferably made of a heat conductive material and is preferably in at least partial vertical alignment with the LED 34. In one embodiment, the metalized area is not in electrical contact with the elements on top surface of the submount 32 or the first and second mounting pads on the back surface of the submount 32. Although heat from the LED is spread over the top surface of the submount by the attach pad 42 and the pads 44, 46 more heat will pass into the submount 32 directly below and around the LED 34. The metalized area can assist with this dissipation by allowing this heat to spread into the metalized area where it can dissipate more readily. It is also noted that the heat can conduct from the top surface of the

submount 32, through the vias 56, where the heat can spread into the first and second mounting pads 50, 52 where it can also dissipate. For the package 30 used in surface mounting, the thickness of the metalized area 66 and the first and second pads 50, 52 should be approximately the same such that all three make contact to a lateral surface such as a PCB. It is also understood that thermal vias can be included between the attach pad 42 and different features of the LED package 30 to dissipate heat from the LED chip 34. In one embodiment, thermal vias (not shown) can be included that pass through the submount between the attach pad 42 and the metalized area 66 such that heat will more efficiently spread from the LED chip 34 through the submount 32 and to the metalized area 66.

[0079] The LED package according to the present invention can also include additional features to aid in the manufacturing accuracy and reliability. As the ratio of W to D increases, the width of the LED chip 34 becomes closer to the diameter of the lens 70. As a result, it can become more important to properly align the LED chip 34 in the center of the submount 32 so that it is below the lens 70. To aid in this alignment, the attach pad 42 had LED alignment features that can take many different forms, shapes and sizes and in the embodiment shown comprise square cut-outs 74. When mounting the LED chip to that attach pad, the corners of the LED chip fit on the inside edge of the cut-outs for proper alignment.

[0080] The LED package can also include features such as solder dams in the area around the attach pad 42, with the solder dams also serving to help center the LED and to reduce movement of the LED from the mounting area during while the mounting solder is in liquid form. When

the liquid solder encounters any one of the dams, movement past is slowed or stopped. This helps reduce the movement of the LED until the solder hardens.

[0081] In other embodiments the shape of the lens over the LED chip can change to assist in light emitting efficiency. As one example, the radius of curvature for the lens can be varied, with one embodiment having an increased radius of curvature.

[0082] Although the present invention has been described in detail with reference to certain preferred configurations thereof, other versions are possible. Therefore, the spirit and scope of the invention should not be limited to the versions described above.

WE CLAIM:

1. A light emitter package, comprising:

a submount;

a light emitter chip mounted on said submount;

a lens over said light emitter chip, the ratio of the width of said light emitter chip to the width of said lens in a given direction being 0.5 or greater.

2. The light emitter package of claim 1, wherein the current density in said light emitter chip is lower compared to a light emitter chip with a smaller width.

3. The light emitter package of claim 1, further comprising a conversion material proximate to said light emitter chip, said conversion material comprising phosphor particles having a D_{50} particle size of greater than 10 microns.

4. The light emitter package of claim 3, further comprising scattering particles.

5. The light emitter package of claim 4, wherein said scattering particles are substantially the same size as said phosphor particles.

6. The light emitter package of claim 1, said light emitter package emitting higher light output power compared to a light emitter package having a smaller light emitter chip with similar features.

7. The light emitter package of claim 1, further comprising chip alignment features on said submount.

8. The light emitter package of claim 1, further comprising an electrostatic discharge (ESD) protection device.

9. The light emitter package of claim 1, said submount comprising aluminum nitride (AlN).

10. The light emitter package of claim 1, said light emitter chip emitting light having an average wavelength of approximately 430-460 nm.

11. The light emitter package of claim 1, said submount having dimensions of approximately 3.5 mm square to 5 mm square.

12. The light emitter package of claim 1, said light emitter chip having dimensions of approximately 0.7 mm square to 3 mm square.

13. The light emitter package of claim 1, said light emitter chip being approximately 1.4 mm square, said submount being approximately 3 mm square.

14. The light emitter package of claim 13, said package exhibiting an output power 150 lumens/watt or higher during operation.

15. The light emitter package of claim 1, said light emitter chip being approximately 1.75 mm square, said submount being approximately 5 mm square.

16. The light emitter package of claim 1, said light emitter chip being approximately 2 mm square, said submount being approximately 5 mm square.

17. The light emitter package of claim 16, said package exhibiting higher than 150 lumens/watt during operation.

18. The light emitter package of claim 1, said light emitter chip being approximately 3 mm square, said submount being approximately 5 mm square.

19. The light emitter package of claim 18, said package exhibiting higher than 150 lumens/watt during operation.

20. The light emitter package of claim 1, said light emitter chip comprising a light emitting diode (LED) chip.

21. The light emitter package of claim 1, wherein said light emitter chip covers more than 10% of the surface area of said submount.

22. The light emitter package of claim 1, wherein said light emitter chip covers more than 15% of the surface area of said submount.

23. A light emitting diode (LED) package, comprising:

a submount comprising a top and bottom surface;

a plurality of top electrically and thermally conductive elements on said top surface of said submount;

an LED chip on one of said top elements, said electrically conductive elements arranged to spread heat from said LED chip across the majority of said submount top surface;

a bottom thermally conductive element on said bottom surface not in electrical contact with said top elements and arranged to conduct heat from said submount; and

a lens over said LED chip;

wherein the ratio of the width of said LED chip to the width of said lens in a given direction is 0.5 or greater.

24. The LED package of claim 23, wherein said LED chip covers more than 10% of the surface area of said submount.

25. The LED package of claim 23, wherein said LED chip covers more than 15% of the surface area of said submount.

26. The LED package of claim 23, further comprising a conversion material proximate to said LED chip, said conversion material comprising phosphor particles having a D_{50} particle size of greater than 10 microns.

27. The LED package of claim 26, further comprising scattering particles.

28. The LED package of claim 27, wherein said scattering particles are substantially the same size as said phosphor particles.

29. The LED package of claim 23, said LED package emitting higher light output power compared to an LED package having a smaller LED chip with similar features.

30. The LED package of claim 23, further comprising chip alignment features on said submount.

31. The LED package of claim 23, further comprising an electrostatic discharge (ESD) protection device.

32. The LED package of claim 23, said submount comprising aluminum nitride (AlN).

33. The LED package of claim 23, said LED chip emitting light having an average wavelength of approximately 430-460 nm.

34. The LED package of claim 23, said submount having dimensions of approximately 3.5 mm square to 5 mm square.

35. The LED package of claim 23, said LED chip having dimensions of approximately 0.7 mm square to 3 mm square.

36. The LED package of claim 23, said LED chip being approximately 1.4 mm square, said submount being approximately 3 mm square.

37. The LED package of claim 36, said LED package exhibiting an output power of 150 lumens/watt or greater during operation.

38. The LED package of claim 23, said LED chip being approximately 1.75 mm square, said submount being approximately 5 mm square.

39. The LED package of claim 23, said LED chip being approximately 2 mm square, said submount being approximately 5 mm square.

40. The LED package of claim 39, said LED package exhibiting an output power of 150 lumens/watt or greater during operation.

41. The LED package of claim 23, wherein said top elements cover more that 50% of said submount top surface.

42. The LED package of claim 23, further comprising first and second mounting pads on said bottom surface and a plurality of conductive vias running though said submount.

43. The LED package of claim 23, further comprising a solder mask covering at least a portion of said top elements.

44. The LED package of claim 23, further comprising a protective layer between the edge of said lens and the edge of said top surface, said protective layer covering said submount top surface and said top elements.

45. A light emitter package, comprising:

a submount comprising aluminum nitride (AlN);

a light emitter chip on said submount, said light emitter emitting light having an approximate average wavelength in the range of 430-460 nm; and

a lens on said light emitter chip;

wherein the ratio of the width of said light emitter chip to the width of said lens in a given direction is 0.5 or greater.

46. A light emitter package, comprising:

a single light emitting diode (LED) chip;

a submount having dimensions of 3.5 mm square or larger;

a molded lens over said LED chip on said submount.

47. The light emitter package of claim 46, said submount having dimensions of approximately 5 mm square, said LED chip having dimensions of approximately 2 mm square, and said molded lens having a diameter of approximately 4.52 mm.

48. The light emitter package of claim 46, said submount comprising aluminum nitride.

49. The light emitter package of claim 46, said package outputting white light at an efficacy of 150 lm/W or more within a 7-step MacAdam ellipse along the black body curve when operated with a drive current of 350 mA.

50. The light emitter package of claim 46, said package outputting 160 lm or more at an efficacy of 160 lm/W or more when operated with a drive current.

51. The light emitter package of claim 50, said drive current being approximately 350 mA.

52. The light emitter package of claim 46, said submount having dimensions of 4 mm square or larger

53. The light emitter package of claim 52, said package outputting 750 lm or more at an efficacy of 110 lm/W or more when operated with a drive current.

54. The light emitter package of claim 53, said drive current being approximately 2 A.

55. A light emitter package, comprising:
a light emitter chip;

a submount comprising a material having a thermal conductivity of 30 W/m·K or higher; and

a molded lens over said emitter on said submount.

56. The light emitter package of claim 55, said submount having a thermal conductivity of 50 W/m·K or higher.

57. The light emitter package of claim 55, said submount having a thermal conductivity of 100 W/m·K or higher.

58. The light emitter package of claim 55, said submount having a thermal conductivity of 120 W/m·K or higher.

59. The light emitter package of claim 55, said submount comprising aluminum nitride.

60. The light emitter package of claim 55, further comprising a conversion material proximate to said light emitter chip, said conversion material comprising phosphor particles having a D_{50} particle size of greater than 10 microns.

61. The light emitter package of claim 55, further comprising chip alignment features on said submount.

62. The light emitter package of claim 55, further comprising an electrostatic discharge (ESD) protection device.

63. The light emitter package of claim 55, said light emitter chip emitting light having an average wavelength of approximately 430-460 nm.

64. The light emitter package of claim 55, said submount having dimensions of approximately 3.5 mm square to 5 mm square.

65. The light emitter package of claim 55, said light emitter chip having dimensions of approximately 0.7 mm square to 3 mm square.

66. The light emitter package of claim 55, said light emitter chip being approximately 1.75 mm square, said submount being approximately 5 mm square.

67. The light emitter package of claim 55, said light emitter chip being approximately 2 mm square, said submount being approximately 5 mm square.

68. The light emitter package of claim 67, said package exhibiting higher than 150 lumens/watt during operation.

69. The light emitter package of claim 55, said light emitter chip being approximately 3 mm square, said submount being approximately 5 mm square.

70. The light emitter package of claim 69, said package exhibiting higher than 150 lumens/watt during operation.

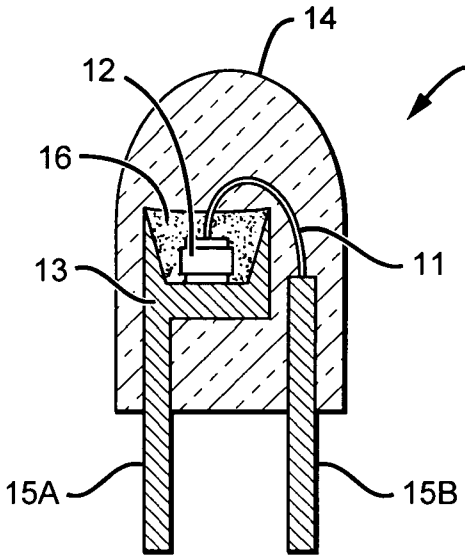
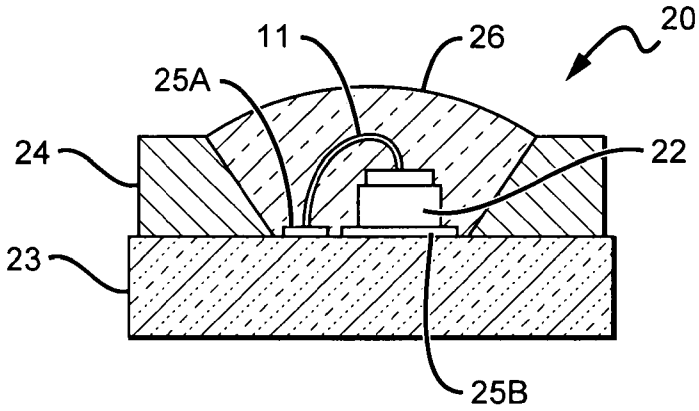


FIG. 1A
PRIOR ART

FIG. 1B
PRIOR ART



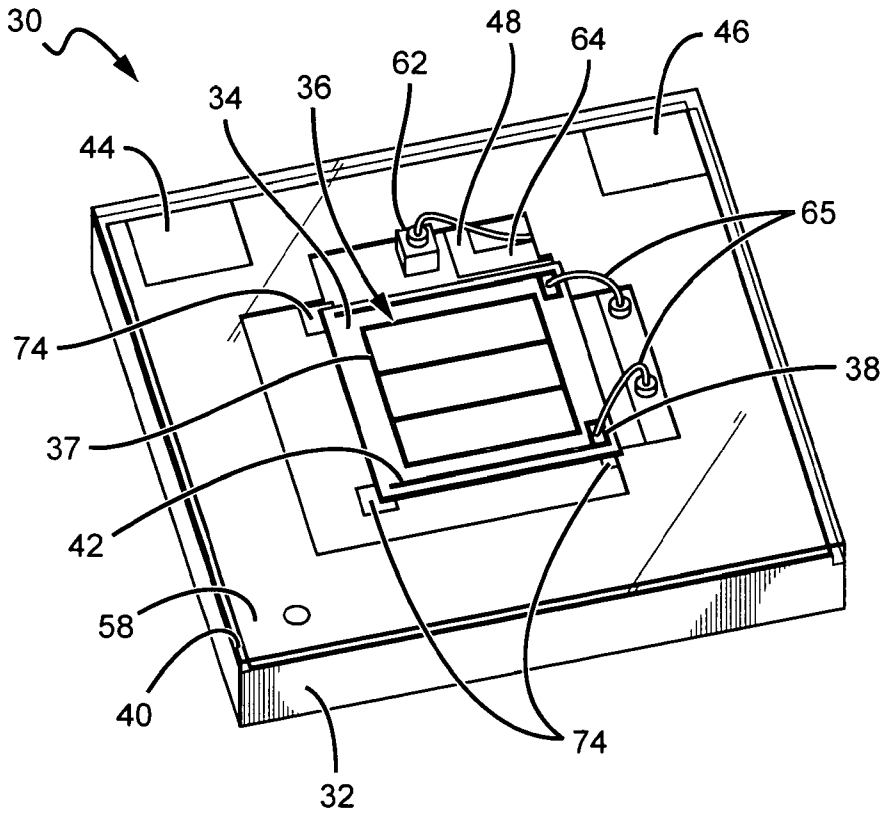
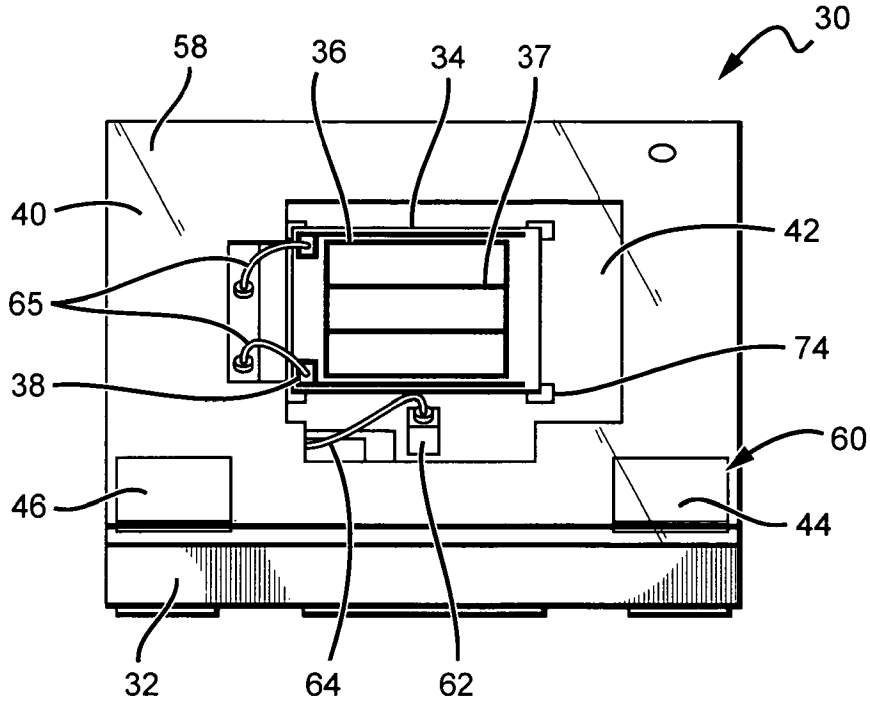


FIG. 2

FIG. 3



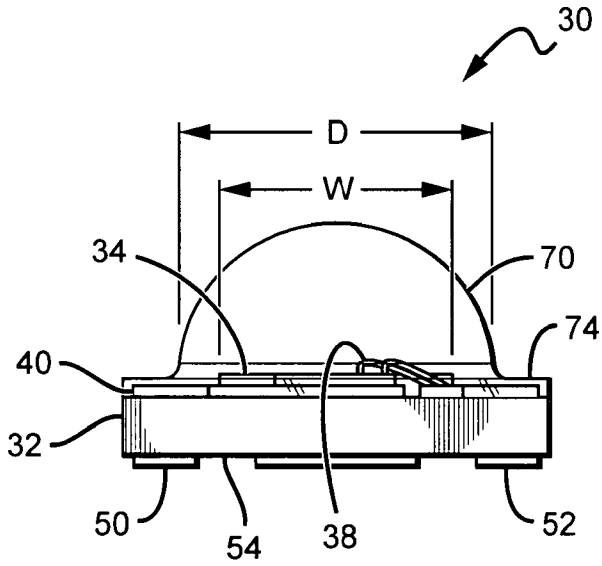


FIG. 4

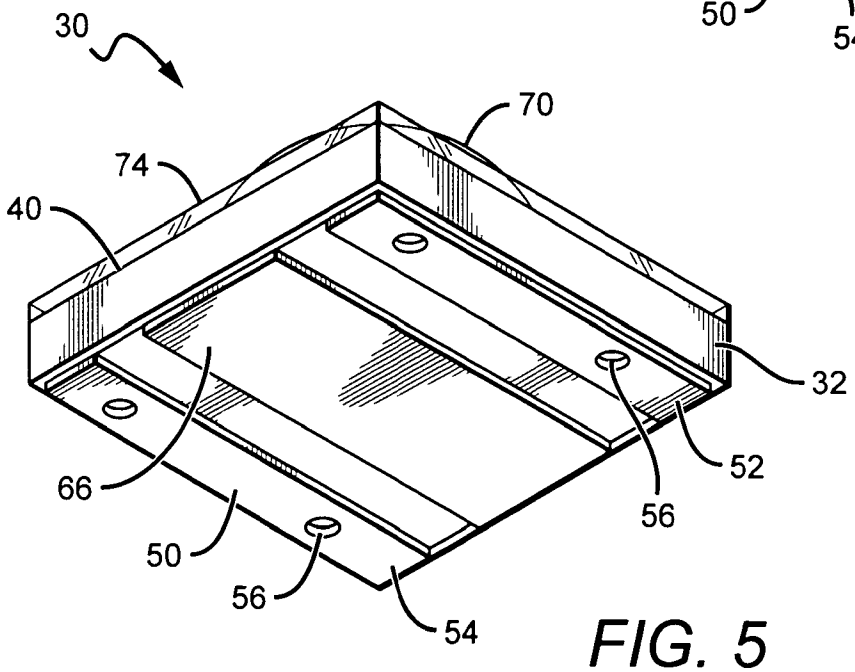


FIG. 5

FIG. 6

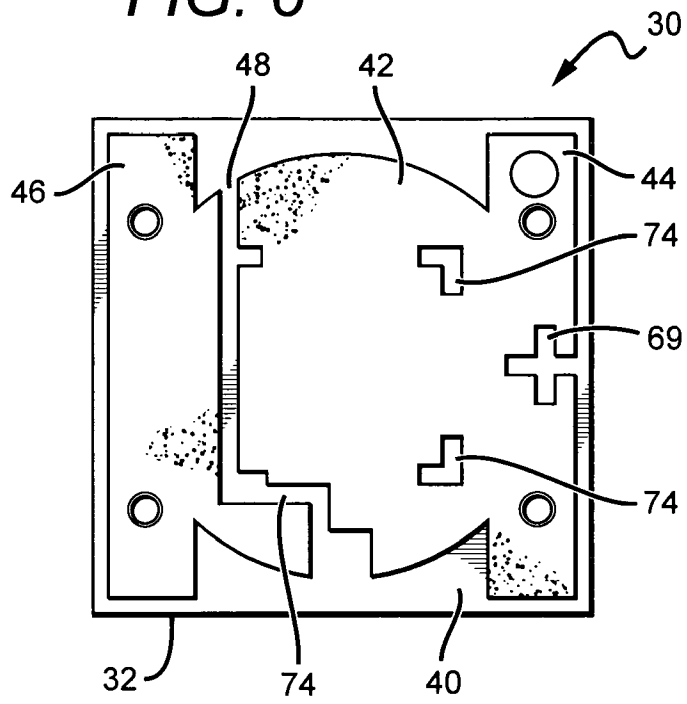
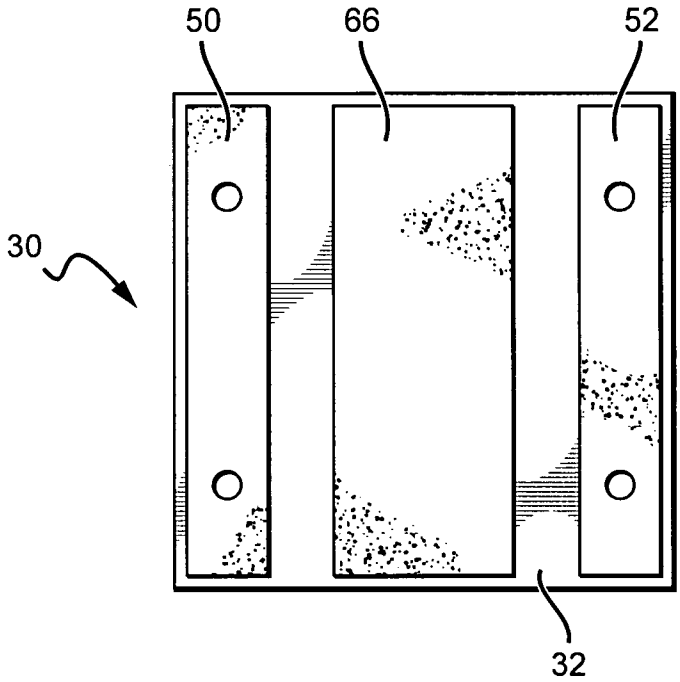


FIG. 7



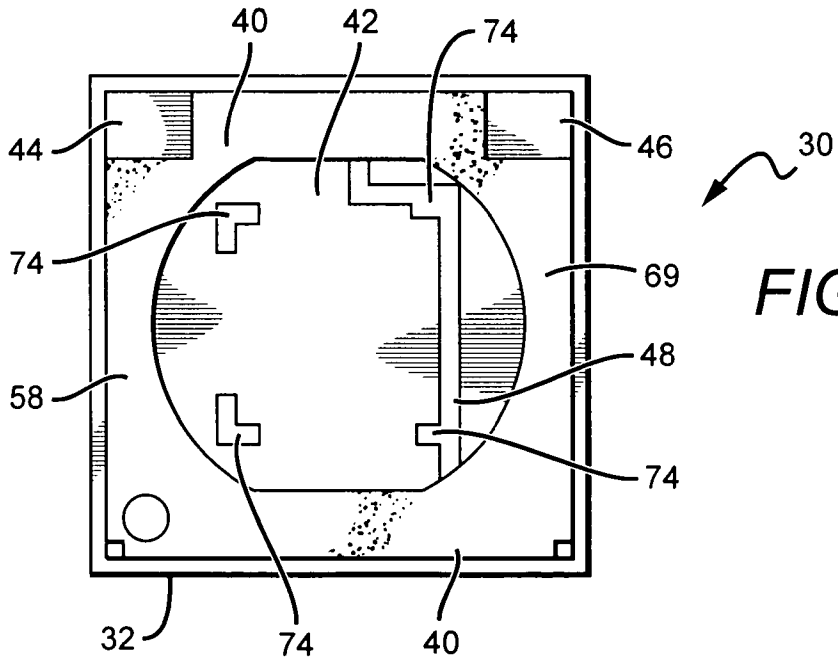


FIG. 8

FIG. 9

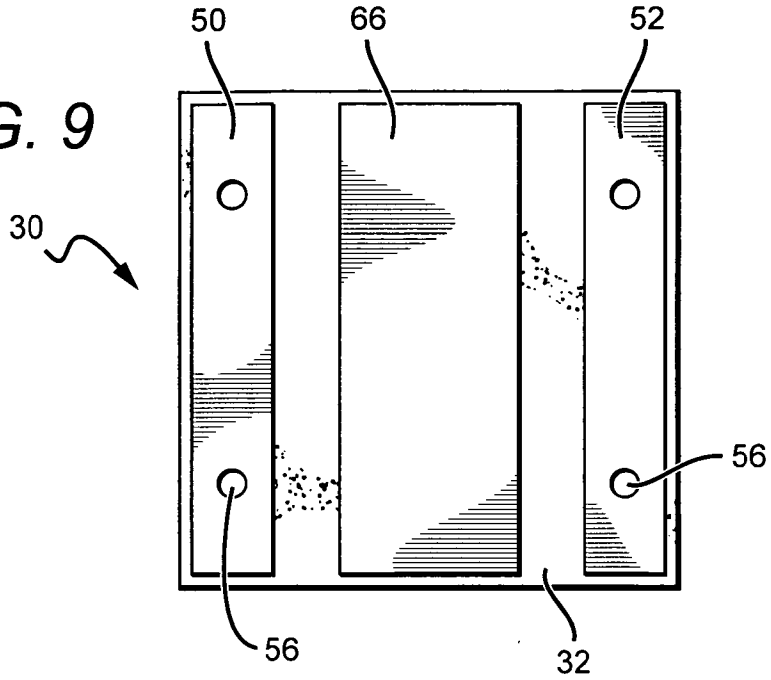


FIG. 12

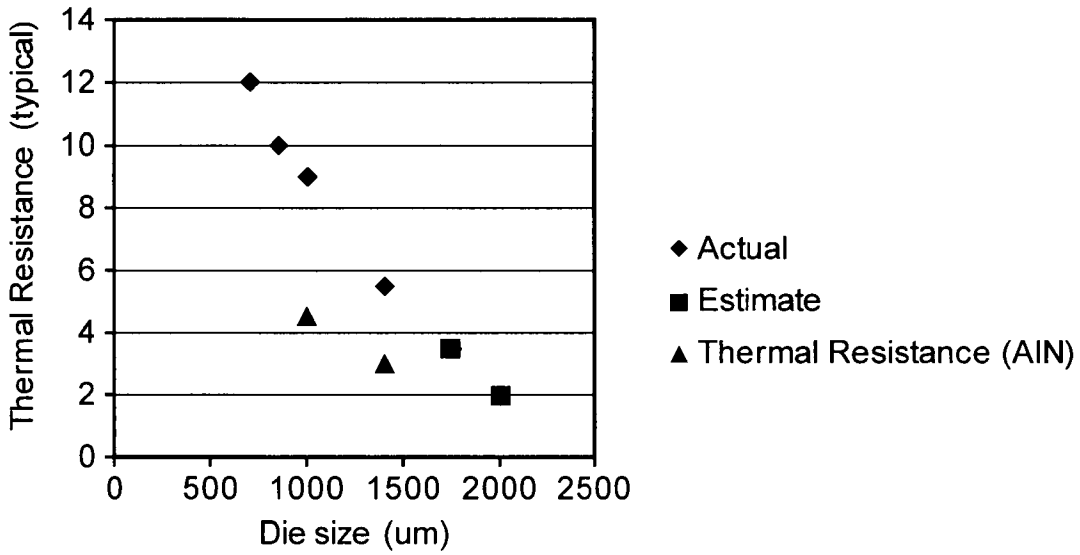
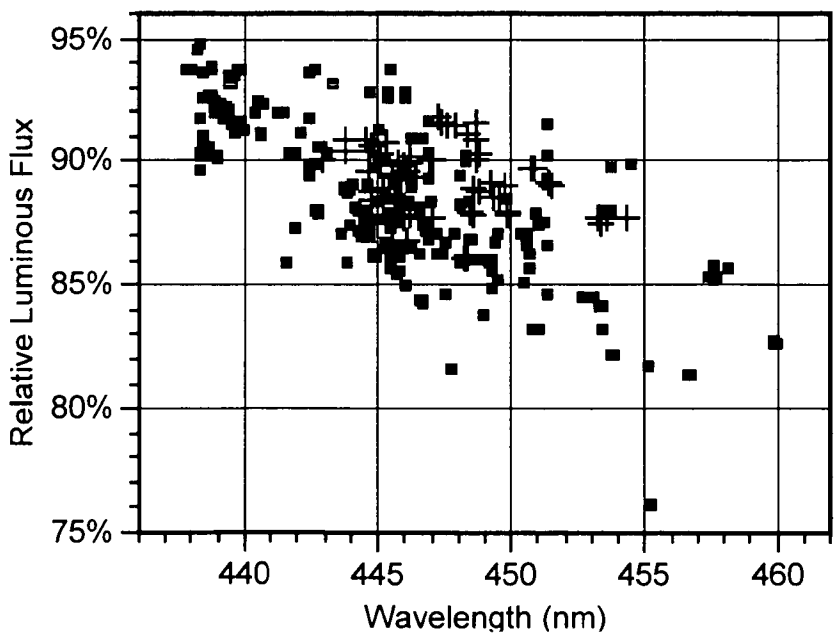


FIG. 13



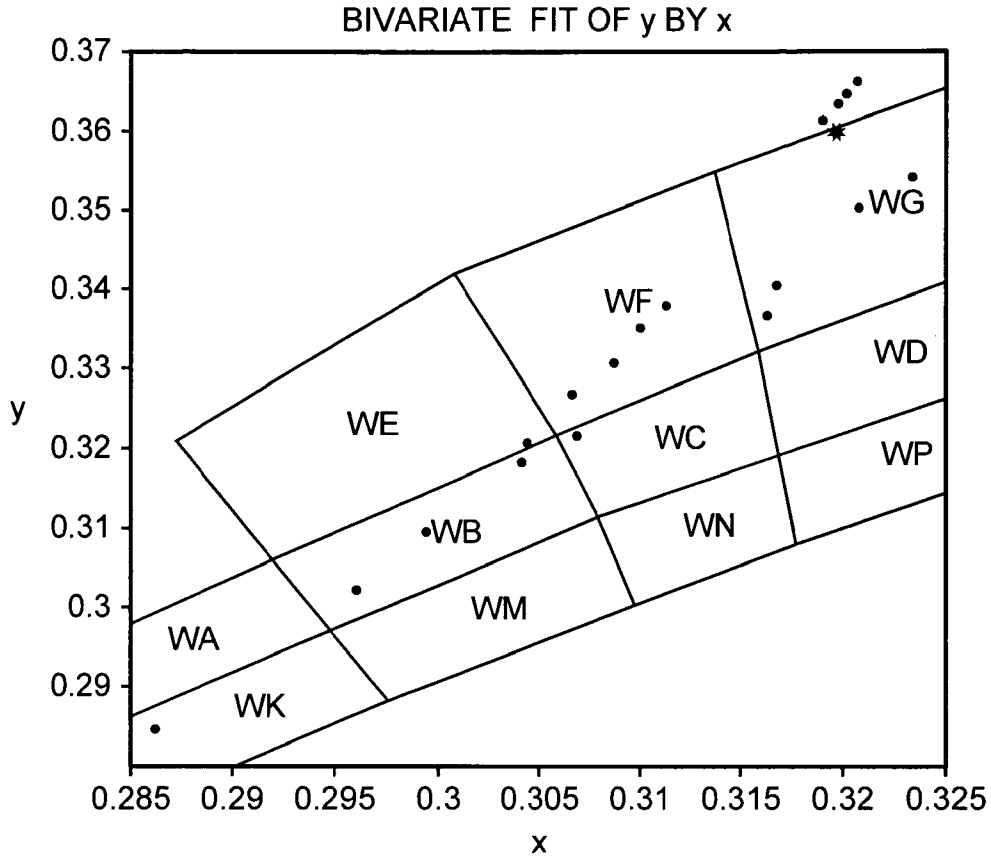
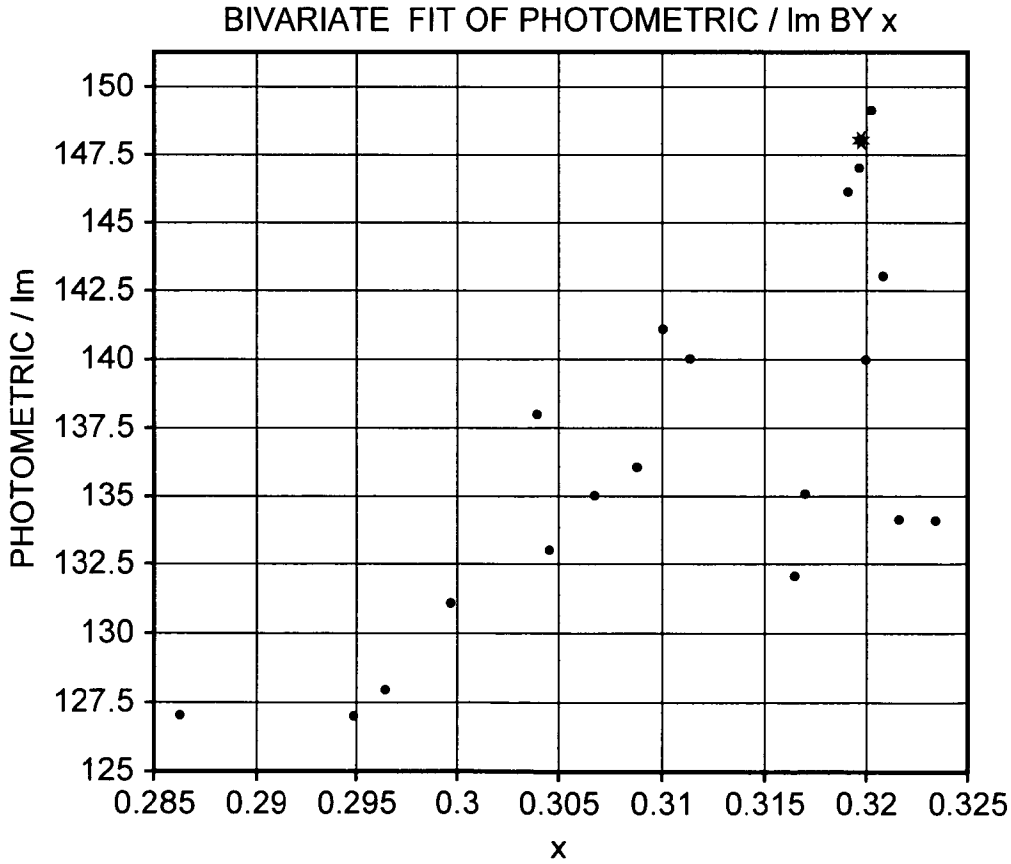

BIVARIATE FIT OF y BY x
0.37
0.36
0.35
0.34
0.33
0.32
0.31
0.3
0.29
y
WG
WF
WD
WE
WC
WP
WB
WN
WM
WA
WK
0.285 0.29 0.295 0.3 0.305 0.31 0.315 0.32 0.325
x

FIG. 10

FIG. 11


BIVARIATE FIT OF PHOTOMETRIC / lm BY x
PHOTOMETRIC / lm
150
147.5
145
142.5
140
137.5
135
132.5
130
127.5
125
0.285 0.29 0.295 0.3 0.305 0.31 0.315 0.32 0.325
x

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/001255

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L33/58 H01L33/64
ADD. H01L33/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009/050924 A1 (EDMOND JOHN ADAM [US]) 26 February 2009 (2009-02-26)	1-3,6,7, 9-22, 45-61, 63-70
A	paragraphs [0007], [0025] - [0037]; figures 2-8 paragraph [0039]; figures 11,12	23-44
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A	paragraphs [0023], [0030], [0070]; figures 1,4,28 paragraphs [0048] - [0053]; figures 16A,B; table 2	3

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
27 July 2010	13/08/2010

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Tinjod, Frank

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/001255

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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A	paragraphs [0008], [0012], [0055], [0058] - [0060], [0062]; figures 2A-H paragraphs [0066] - [0069]; figures 5A-5I paragraph [0071]; figure 7	23-29, 31-33, 42,48, 55-60, 62,63
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A	paragraphs [0039] - [0054]; figures 1A,B,2A-C,3	23
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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/001255

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International application No
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