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(54) **READ-WRITE METHOD AND MEMORY DEVICE**

LESE-SCHREIB-VERFAHREN UND SPEICHERVORRICHTUNG

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EP 4 006 710 B1

Description

CROSS REFERENCE

[0001] This application claims priority to Chinese Patent Application No. 202010249989.5, titled "METHOD FOR READING AND WRITING AND MEMORY DEVICE" and filed on April 1, 2020.

TECHNICAL FIELD

[0002] The present disclosure relates to the field of semiconductor memory technologies, and more particularly, to a method for reading and writing and a memory device.

BACKGROUND

[0003] Semiconductor memories are memory components for storing various data and information. With the increase in circuit complexity, various forms of memory devices are inevitably prone to produce defective or damaged memory cells during manufacturing or during use, resulting in reduced reliability and lifespan of the semiconductor memory devices.

[0004] Therefore, how to improve the reliability of the memory devices and prolong the lifespan of the memory devices has become an urgent problem to be solved at present.

[0005] US 2020/0004652 A1 discloses an apparatus including a plurality of stacked integrated circuit dies that include a memory cell die and a logic die. Memory addresses that produce a read error are been marked in an address table and mapped with addresses in a spare storage area of the memory cell die.

[0006] US 2019/0371391 A1 discloses a semiconductor memory device including a memory cell array, an error correction code (ECC) engine, a refresh control circuit, a scrubbing control circuit and a control logic circuit.

[0007] US 2014/0376320 A1 discloses a memory subsystem employing spare memory cells external to one or more memory devices. Memory addresses producing read errors above a threshold number of times are been marked in a mapping table and associated with cells in a spare cell array.

[0008] US 2010/0332895 A1 discloses remapping memory devices.

SUMMARY

[0009] The invention is set out in independent claims 1 and 10 of the appended set of claims. Further preferred embodiments are defined by their dependent claims.

[0010] Advantages of the present disclosure are as below. When a user performs a read operation on the memory device, a memory cell with data error may be replaced by the spare memory cell in real time. That is, every time when the read operation is performed, the memory cell with data error may be replaced by the spare memory cell, such that when the user performs the read operation or the write operation on the memory device, the read/write operation may be performed on the spare memory cell instead of the memory cell with data error, thereby avoiding data error or data loss. Therefore, the reliability of the memory device is greatly improved, and the lifespan of the memory device is prolonged.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011]

FIG 1 is a schematic flow diagram of a method for reading and writing according to a first embodiment of the present disclosure;

FIG 2 is a schematic flow diagram of a method for reading and writing according to a second embodiment of the present disclosure;

FIG 3 is a schematic flow diagram of a method for reading and writing according to a third embodiment of the present disclosure;

FIG 4 is a schematic structural diagram of a memory device according to a first embodiment of the present disclosure;

FIG 5 is a schematic structural diagram of a memory device according to a second embodiment of the present disclosure;

FIG 6 is a schematic structural diagram of a memory device according to a third embodiment of the present disclosure;

FIG 7 is a schematic structural diagram of a memory device according to a fourth embodiment of the present disclosure;

FIG 8 is a schematic structural diagram of a memory device according to a fifth embodiment of the present disclosure; and

FIG 9 is a schematic structural diagram of a memory device according to a fifth embodiment of the present disclosure.

DETAILED DESCRIPTION

[0012] Embodiments of a method for reading and writing and a memory device provided by the present disclosure are described below in detail with reference to the accompanying drawings.

[0013] A common method for improving reliability of a memory device includes: encoding data as an error correction code (ECC) before the data is written into the memory device, and simultaneously storing the data and the ECC into the memory device. When reading, both the data and the ECC are read simultaneously, and the ECC is decoded to restore data where an error likely occurs.

[0014] However, it is found that the ECC can only correct data when the data is read out, and in a memory there still exists a memory cell with data error. In a

subsequent data storage process, if at least one memory cell with data error reoccurs in a memory segment corresponding to the above memory cell with data error, in this memory segment there may exist at least two memory cells with data error. However, the ECC will be unable to correct the error, causing this memory segment to be unserviceable, or even causing the memory device to be unserviceable, thereby having a negative effect on the reliability and lifespan of the memory device.

[0015] By study, it is found that when a user uses the memory device, it may be avoided performing a read/-write operation on the memory cell with data error (i.e., an invalid memory cell) by differentiating the memory cell with data error in real time and replacing the memory cell with data error by a spare memory cell, which can greatly improve the reliability of the memory device and prolong the lifespan of the memory device. Therefore, the present disclosure provides a method for reading and writing, which can differentiate a memory cell with data error in real time, and replace the memory cell with data error by a spare memory cell.

[0016] Specifically, with reference to FIG 1, a schematic flow diagram of the method for reading and writing according to the first embodiment of the present disclosure is illustrated, and the method for reading and writing includes following steps.

[0017] In Step S10, a read command is applied to the memory device, wherein the read command points to address information. For example, the address information pointed to by the read command is denoted by A0.

[0018] In Step S11, data to be read out is read from a memory cell corresponding to the address information pointed to by the read command. For example, data to be read out is read from a memory cell corresponding to the address information A0.

[0019] In Step S12, it is determined whether an error occurs in the data to be read out.

[0020] If an error occurs in the data to be read out, this means that the memory cell is invalid. In this case, the address information pointed to by the read command is associated with the spare memory cell, and the data to be read out is stored into the spare memory cell. That is, an invalid memory cell is replace by the spare memory cell to improve the reliability of the memory device. Further, in another embodiment of the present disclosure, when the error occurs in the data to be read out, if the data to be read out is corrected, the corrected data instead of the data to be read out is stored into the spare memory cell.

[0021] Further, to associate the address information pointed to by the read command with the spare memory cell, in this embodiment, the method for reading and writing also includes Step S13. In Step S13, an identification code configured for identifying the spare memory cell is generated, the identification code is stored into the lookup table 10, and the address information pointed to by the read command is associated with the spare memory cell through the identification code. It is to be understood that different spare memory cells correspond to different identification codes to ensure that the spare memory cells associated with the address information pointed to by the read command are not repetitive, thereby avoiding data storage error.

[0022] In this embodiment, a lookup table 10 is provided, wherein the lookup table 10 is provided with an address information bar ADD and a numerical bar DATA.

[0023] All address information of the memory device is prestored in the address information bar ADD, such as A0, A1, A2, A3, A4, A5, A6...An. The amount of the address information may be set based on actual situations of the memory device.

[0024] The numerical bar DATA is configured for storing a numerical code corresponding to the address information. Each of the address information corresponds to one numerical code. The numerical code at least includes an identification code configured for identifying the spare memory cell or a meaningless code.

[0025] In this embodiment, the numerical code is composed of a first type code and a second type code.

[0026] The first type code is configured for marking whether the address information is valid. For example, the first type code is 0 or 1, wherein 0 represents a valid marked value indicating that the address information is valid, and 1 represents an invalid marked value indicating that the address information is invalid.

[0027] Specifically, if an error occurs in the data to be read out, this means that the memory cell is invalid. In this case, the address information pointed to by the read command is marked as invalid. For example, if an error occurs in the data to be read out read from the memory cell corresponding to the address information A0 pointed to by the read command, the first type code of the numerical code corresponding to the address information A0 pointed to by the read command is marked as the invalid marked value 1 in the lookup table 10. If the error occurs in the data to be read out read from the memory cell corresponding to the address information A4 pointed to by the read command, the first type code of the numerical code corresponding to the address information A4 pointed to by the read command is marked as the invalid marked value 1 in the lookup table 10.

[0028] The second type code is configured for recording the identification code or the meaningless code. The second type code may be a multi-bit code, which may be determined according to number of the spare memory cells. For example, the second type code is a three-bit code, which may be 000, 001, 010, 100, 101, 011, 110, 111, and so on.

[0029] When the first type code is the invalid marked value indicating that the address information is invalid (for example, when the first type code is 1), the second type code is the identification code, the address information pointed to by the read command is associated with the spare memory cell through the identification code, and data obtained by correcting the data to be read out is stored into the spare memory cell. For example, if the first type code of the numerical code corresponding to the

address information A0 is the invalid marked value 1, the second type code 001 of the numerical code corresponding to the address information A0 is an identification code that can identify a spare memory cell, the address information pointed to by the read command is associated with the spare memory cell through the identification code 001, and data obtained by correcting the data to be read out is stored into the spare memory cell identified by the identification code 001. If the first type code of the numerical code corresponding to the address information A4 is the invalid marked value 1, the second type code 010 of the numerical code corresponding to the address information A4 is an identification code that can identify a spare memory cell, the address information pointed to by the read command is associated with the spare memory cell through the identification code 010, and data obtained by correcting the data to be read out is stored into the spare memory cell identified by the identification code 010.

[0030] If no error occurs in the data to be read out, this means that the memory cell is valid. In this case, in the lookup table 10, the first type code of the numerical code corresponding to the address information pointed to by the read command is the valid marked value, and the second type code is a meaningless code. The meaningless code is configured for filling numerical digits, and is not configured for identifying any one spare memory cell.

[0031] Specifically, in this embodiment, if no error occurs in the data to be read out read from the memory cell corresponding to the address information A1 pointed to by the read command, the first type code of the numerical code corresponding to the address information A1 pointed to by the read command is marked as the valid marked value 0 in the lookup table 10, and the second type code is a meaningless code 000. If no error occurs in the data to be read out read from the memory cell corresponding to the address information A2 pointed to by the read command, the first type code of the numerical code corresponding to the address information A2 pointed to by the read command is marked as the valid marked value 0 in the lookup table 10, and the second type code is the meaningless code 000. In this embodiment, the meaningless code is denoted by a numerical value 000. In other examples of the present disclosure, the meaningless code may also be denoted by other numerical values.

[0032] In the present disclosure, there are following two processing modes for setting the first type code of the numerical code corresponding to the address information pointed to by the read command as the valid marked value.

[0033] The first processing modes for setting the first type code of the numerical code corresponding to the address information pointed to by the read command as the valid marked value is as below. The numerical codes corresponding to all the address information are initially set as a combination of the valid marked value and the meaningless code in the lookup table. If no error occurs in the data to be read out, the numerical code in the lookup table is not revised, i.e., initial settings of the numerical code are retained. For example, if no error occurs in the data to be read out read from the memory cell corresponding to the address information A1 pointed to by the read command, the initial settings of the numerical code corresponding to the address information A1 pointed to by the read command are retained in the lookup table 10. That is, the initial settings of the numerical code are not revised. In this embodiment, the first processing mode is adopted.

[0034] In the first processing mode, if an error occurs in the data to be read out read from the memory cell corresponding to the address information pointed to by the read command, the first type code of the numerical code corresponding to the address information pointed to by the read command is revised from the valid marked value to the invalid marked value in the lookup table 10, and the second type code of the numerical code is revised from the meaningless code to the identification code. For example, if an error occurs in the data to be read out read from the memory cell corresponding to the address information A0 pointed to by the read command, the first type code of the numerical code corresponding to the address information A0 pointed to by the read command is revised from the valid marked value to the invalid marked value in the lookup table 10, and the second type code of the numerical code is revised from the meaningless code to the identification code.

[0035] Further, in the first processing mode, when the memory device is powered on or shipped out of factory, the numerical codes corresponding to all the address information are initially set as a combination of the valid marked value and the meaningless code. It is to be understood that in the use of the memory device, after performing the read operation or the write operation on the memory device for many times, in the lookup table, the numerical code corresponding to the address information likely is a combination of the invalid marked value and the identification code, or likely is a combination of the valid marked value and the meaningless code. Therefore, when a read command is applied to the memory device, the lookup table obtained after a previous read/write operation is performed is an initial lookup table of the current read operation, and the numerical code corresponding to the address information of the memory cell after the previous read/write operation is recorded in the initial lookup table, wherein the numerical code is an initial numerical code of the current read operation, and the numerical code likely is a combination of the invalid marked value and the identification code, or likely is a combination of the valid marked value and the meaningless code. If an error occurs in the data to be read out, the numerical code corresponding to the address information pointed to by the read command is revised as a combination of the invalid marked value and the meaningless code in the lookup table 10.

[0036] Further, the method for reading and writing provided by the present disclosure also includes following Step. In Step S14, number of revising times of the second type code is recorded, and the corresponding identification code is generated according to the number of revising times. Specifically, if a data error occurs in the address information pointed to by the read command, the second type code needs to be revised as the identification code to associate the address information with a spare memory cell through the identification code. To avoid the spare memory cells associated with different address information to be repetitive, different identification codes may be generated according to the number of revising times of the second type code, i.e., different address information corresponds to different identification codes. In this way, different address information is associated with different spare memory cells. For example, when the number of revising times of the second type code is 0, the identification code is 001. When the number of revising times of the second type code is 1, the identification code is 010. When the number of revising times of the second type code is 2, the identification code is 100..., and so on. The corresponding identification code is generated according to the number of revising times.

[0037] The second processing modes for setting the first type code of the numerical code corresponding to the address information pointed to by the read command as the valid marked value is as below. If no error occurs in the data to be read out, the first type code of the numerical code corresponding to the address information pointed to by the read command is marked as the valid marked value in the lookup table 10, and a position of the second type code is filled with the meaningless code. For example, if no error occurs in the data to be read out read from the memory cell corresponding to the address information A1 pointed to by the read command, the first type code of the numerical code corresponding to the address information A1 pointed to by the read command is marked as the valid marked value 0 in the lookup table 10, and the position of the second type code is filled with the meaningless code.

[0038] In another example of the present disclosure, the numerical code may be only composed of the second type code. That is, the numerical code only includes the identification code configured for identifying the spare memory cell or the meaningless code. If an error occurs in the data to be read out, this means that the memory cell is invalid. In this case, the numerical code corresponding to the address information corresponding to the memory cell is the identification code. If no error occurs in the data to be read out, this means that the memory cell is valid. In this case, the numerical code corresponding to the address information corresponding to the memory cell is the meaningless code. Further, the present disclosure also provides a method for determining whether an error occurs in the data to be read out. Specifically, the step of reading data to be read out from a memory cell corresponding to the address information pointed to by the read command further includes: reading, from the memory cell corresponding to the address information pointed to by the read command, a first error correction code (ECC) corresponding to the data to be read out. For example, number of bits of data read from the memory cell corresponding to the address information pointed to by the read command is 64b+8b, wherein 64b represents the number of bits of the data to be read out, and 8b represents the number of bits of the first ECC. According to a corresponding algorithm, the first ECC is decoded to restore data where an error likely occurs. The algorithm belongs to the existing technologies, and thus is not to be described in detail. Therefore, it may be determined whether an error occurs in the data to be read out by decoding the first ECC.

[0039] The present disclosure enumerates a method for determining whether an error occurs in the data to be read out by decoding the first ECC. This method includes following steps. The data to be read out is re-encoded to form a new ECC, and an XOR comparison is made between the new ECC and the first ECC. If the new ECC is consistent with the first ECC in each bit, this means that no error occurs in the data to be read out, and the memory cell is valid. In this case, the lookup table 10 is not revised, and the first type code of the numerical code corresponding to the address information corresponding to the memory cell is the valid marked value. If the new ECC is inconsistent with the first ECC, this means that an error occurs in the data to be read out, and the memory cell is invalid. In this case, the first type code of the numerical code corresponding to the address information pointed to by the read command is revised the invalid marked value in the lookup table 10.

[0040] If no error occurs in the data to be read out, the data to be read out is used as output data of the memory device. If an error occurs in the data to be read out, the first ECC may be employed to correct the data to be read out, the corrected data is used as the output data of the memory device, and the corrected data is stored into the corresponding spare memory cell.

[0041] According to the method for reading and writing provided by the present disclosure, when a user performs a read/write operation on the memory device, a memory cell with data error is differentiated in real time and is replaced by the spare memory cell in real time. That is, every time when the read operation is performed, the memory cell with data error may be replaced by the spare memory cell, such that when the user performs the read/-write operation on the memory device subsequently, the read/write operation may be performed on the spare memory cell instead of the memory cell with data error. Therefore, the reliability of the memory device can be greatly improved, and the lifespan of the memory device can be prolonged.

[0042] The method for reading and writing provided by the present disclosure also provides a second embodiment. After applying a read command to the memory device, and before reading data to be read out from a

memory cell corresponding to the address information pointed to by the read command, the method also includes a step of determining whether the address information pointed to by the read command is valid. Specifically, with reference to FIG 2, a schematic flow diagram of the method for reading and writing according to the second embodiment of the present disclosure is illustrated.

[0043] In Step S20, a read command is applied to the memory device, wherein the read command points to address information.

[0044] In Step S21, it is determined whether the address information pointed to by the read command is valid.

[0045] Specifically, when applying a read command to the memory device, the mark is looked up from the lookup table 20 by taking the address information pointed to by the read command as an index. In the lookup table 20, if the first type code of the numerical code corresponding to the address information pointed to by the read command is the valid marked value, this means that the address information pointed to by the read command is valid. However, if the first type code of the numerical code corresponding to the address information pointed to by the read command is the invalid marked value, this means that the address information pointed to by the read command is invalid.

[0046] For example, if the address information pointed to by the read command is the address information A1, the mark is looked up from the lookup table 20 by taking the address information A1 pointed to by the read command as an index. In the lookup table 20, if the first type code of the numerical code corresponding to the address information A1 pointed to by the read command is the valid marked value 0, this means that the address information A1 pointed to by the read command is valid.

[0047] For another example, the address information pointed to by the read command is the address information A4. The mark is looked up from the lookup table 20 by taking the address information A4 pointed to by the read command as the index. In the lookup table 20, if the first type code of the numerical code corresponding to the address information A4 pointed to by the read command is the invalid marked value 1, this means that the address information A4 pointed to by the read command is invalid.

[0048] If the address information pointed to by the read command is valid, the read operation is performed on the memory cell corresponding to the address information pointed to by the read command, i.e., Step S22 is performed. For example, in the lookup table 20, if the first type code of the numerical code corresponding to the address information A1 pointed to by the read command is the valid marked value 0, this means that the address information A1 pointed to by the read command is valid. In this case, the read operation is performed on the memory cell corresponding to the address information A1 pointed to by the read command, i.e., Step S22 is performed. In Step S22, the address information pointed to by the read command is the address information A1.

[0049] Further, if the first type code of the numerical code corresponding to the address information pointed to by the read command is the valid marked value, the second type code of the numerical code is not identified.

[0050] However, if the address information pointed to by the read command is invalid, i.e., in the lookup table 20, if the first type code of the numerical code corresponding to the address information pointed to by the read command is the invalid marked value, this means that the memory cell corresponding to the address information pointed to by the read command is invalid. In this case, it is stopped performing the read operation on the memory cell corresponding to the address information pointed to by the write command, and Step S23 is performed. For example, in the lookup table 20, if the first type code of the numerical code corresponding to the address information A4 pointed to by the read command is the invalid marked value 1, it is stopped performing the read operation on the memory cell corresponding to the address information A4 pointed to by the write command, and Step S23 is performed.

[0051] Further, in another example of the present disclosure, the numerical code also may be only composed of the second type code. That is, the numerical code only includes the identification code configured for identifying the spare memory cell or the meaningless code. When applying a read command to the memory device, the numerical code is looked up from the lookup table 20 by taking the address information pointed to by the read command as an index. In the lookup table 20, if the numerical code corresponding to the address information pointed to by the read command is the meaningless code, this means that the memory cell corresponding to the address information pointed to by the read command is valid. In this case, the read operation is performed on the memory cell. If the numerical code corresponding to the address information pointed to by the read command is the identification code, this means that the memory cell corresponding to the address information pointed to by the read command is invalid. In this case, the read operation is performed on the spare memory cell corresponding to the identification code.

[0052] In Step S22, the data to be read out is read from the memory cell corresponding to the address information pointed to by the read command. For example, the data to be read out is read from the memory cell corresponding to the address information A1 pointed to by the read command. This step is the same as Step S11 in the first embodiment.

[0053] In Step S23, the read operation is performed on the spare memory cell identified by the second type code (i.e., the identification code) of the numerical code corresponding to the address information pointed to by the read command. For example, in the lookup table 20, if the first type code of the numerical code corresponding to the address information A4 pointed to by the read command is the invalid marked value 1, the read operation is

performed on the spare memory cell identified by the second type code 101 of the numerical code corresponding to the address information A4 pointed to by the read command. Step S25 is performed after Step S23 is performed.

[0054] In Step S24, it is determined whether an error occurs in the data to be read out. This step is the same as Step S12 in the first embodiment. If an error occurs in the data to be read out, in the lookup table 20, the first type code of the numerical code corresponding to the address information pointed to by the read command is marked as the invalid marked value, the second type code is revised as the identification code configured for identifying the spare memory cell, and the data to be read out is stored into the spare memory cell. If no error occurs in the data to be read out, in the lookup table 20, the first type code of the numerical code corresponding to the address information pointed to by the read command is revised the valid marked value, the second type code is filled with the meaningless code, or the lookup table is not revised when all the numerical codes in the lookup table 20 are initially set as a combination of the valid marked value and the meaningless code. In this embodiment, the mode of not revising the lookup table is adopted. Further, in another embodiment of the present disclosure, when the error occurs in the data to be read out, if the data to be read out is corrected, the corrected data instead of the data to be read out is stored into the spare memory cell. In Step S25, data is outputted. In this step, the outputted data may be the data stored in the spare memory cell, or may be corrected or uncorrected data to be read out in the memory cell.

[0055] It is to be noted that in another embodiment, after Step S23 is performed, it may be continued to determine whether an error occurs in data read out from a corresponding spare memory cell. The data is outputted if no error occurs in the data read out. If an error occurs in the data read out, a numerical value of the second type code corresponding to the address information pointed to by the read command is changed, the address information pointed to by the read command is associated with another spare memory cell, and the data to be read out or the corrected data to be read out may be stored into the new spare memory cell.

[0056] In the second embodiment, after a read command is applied to the memory device, it is determined whether the address information pointed to by the read command is valid, such that the read command may be selectively executed on the address information pointed to by the read command. Thus, the reliability of the memory device can be improved. In addition, after the data to be read out is read out, it may be selected whether to mark the address information of the memory cell according to a fact whether an error occurs in the data to be read out. The memory cell is replaced by the spare memory cell if an error occurs in the data to be read out. Furthermore, the corrected data is stored into the spare memory cell to provide a basis for a subsequent read/-write operation. In this way, the reliability and the lifespan of the memory device is greatly improved.

[0057] The method for reading and writing provided by the present disclosure also provides a third embodiment. In the third embodiment, a write operation is performed on the memory device. Specifically, with reference to FIG 3, a schematic flow diagram of the method for reading and writing according to the third embodiment of the present disclosure is illustrated.

[0058] In Step S30, a write command is applied to the memory device, wherein the write command points to address information. For example, a write command is applied to the memory device, wherein the write command points to address information A0.

[0059] In Step S31, it is determined whether the address information pointed to by the write command is valid.

[0060] In this embodiment, a mark corresponding to the address information is looked up from the lookup table by taking the address information pointed to by the write command as an index, to determine whether the address information pointed to by the write command is valid based on the mark.

[0061] For example, if the write command points to the address information A0, the first type code of the numerical code corresponding to the address information A0 is looked up from the lookup table 30 by taking the address information A0 pointed to by the write command as an index, to determine whether the address information A0 pointed to by the write command is valid based on the first type code. If the write command points to the address information A1, the first type code of the numerical code corresponding to the address information A1 is looked up from the lookup table 30 by taking the address information A1 pointed to by the write command as an index, to determine whether the address information A1 pointed to by the write command is valid based on the first type code.

[0062] A write operation is performed on a memory cell corresponding to the address information pointed to by the write command if the mark of the address information pointed to by the write command is valid. It is stopped performing the write operation on the memory cell corresponding to the address information pointed to by the write command if the first type code of the numerical code corresponding to the address information pointed to by the write command is the invalid marked value. In this case, the second type code of the numerical code is identified, and the write operation is performed on the spare memory cell identified by the second type code.

[0063] For example, in the lookup table 30, if the first type code of the numerical code corresponding to the address information A0 pointed to by the write command is the invalid marked value 1, it is stopped performing the write operation on the memory cell corresponding to the address information A0 pointed to by the write command, the second type code 001 of the numerical code is identified, and the write operation is performed on the

spare memory cell identified by the second type code 001. In the lookup table 30, if the first type code of the numerical code corresponding to the address information A1 pointed to by the write command is the valid marked value 0, the write operation is performed on the memory cell corresponding to the address information A1 pointed to by the write command.

[0064] Further, in another embodiment of the present disclosure, the numerical code also may be only composed of the second type code. That is, the numerical code only includes the identification code configured for identifying the spare memory cell or the meaningless code. When applying a write command to the memory device, the numerical code is looked up from the lookup table 30 by taking the address information pointed to by the write command as an index. In the lookup table 30, if the numerical code corresponding to the address information pointed to by the write command is the meaningless code, this means that the memory cell corresponding to the address information pointed to by the write command is valid. In this case, the write operation is performed on the memory cell. If the numerical code corresponding to the address information pointed to by the write command is the identification code, this means that the memory cell corresponding to the address information pointed to by the write command is invalid. In this case, the write operation is performed on the spare memory cell corresponding to the identification code.

[0065] Further, in this third embodiment, the method for reading and writing also includes: forming a second ECC corresponding to data to be written in the write operation, and writing the second ECC together with the data to be written into the memory cell corresponding to the address information pointed to by the write command. When reading data in the memory cell, both the data and the second ECC are read simultaneously, and the second ECC is decoded to restore data where an error likely occurs.

[0066] In this third embodiment, according to the method for reading and writing provided by the present disclosure, after a write command is applied to the memory device, it is determined whether the address information pointed to by the write command is valid. If the address information is determined as invalid, the write operation is performed on the spare memory cell corresponding to the address information instead of the invalid memory cell. In this way, the reliability of the memory device is improved, and the lifespan of the memory device is prolonged.

[0067] The present disclosure also provides a memory device that can implement the above method for reading and writing. The memory device includes, but is not limited to, a volatile memory such as a dynamic random access memory (DRAM) and a static random access memory (SRAM), and a non-volatile memory such as an NAND flash memory, an NOR flash memory, a ferroelectric random access memory (FeRAM), a resistance random access memory (RRAM), a magnetic random access memory (MRAM), and a phase change random access memory (PCRAM), etc.

[0068] With reference to FIG 4, a schematic structural diagram of a memory device according to a first embodiment of the present disclosure is illustrated. The memory device includes: a command receiving unit 40, a memory cell 41, an associating unit 42, an execution unit 43, and a spare memory cell 44.

[0069] The command receiving unit 40 is configured to receive a read command or a write command applied to the memory device, or address information pointed to by the read/write command.

[0070] The memory cell 41 corresponds to the address information pointed to by the read command or the write command, and is configured to store data. In the present disclosure, the memory cell 41 may be a memory unit well known to those skilled in the art, such as a basic memory cell, a memory segment, memory pages, and memory blocks, which are not limited by the present disclosure.

[0071] The associating unit 42 is configured to associate the address information with the spare memory cell 44. In this embodiment, the associating unit 42 is also configured to store mark information configured for recording whether the address information is valid or invalid. Specifically, in this embodiment, the associating unit 42 is a lookup table. Address information of the memory cell 41 and a numerical code corresponding to the address information are recorded in the lookup table. The numerical code is composed of a first type code and a second type code, wherein the first type code is configured for marking whether the address information is valid, and the second type code is configured for recording an identification code of the spare memory cell 44. If an error occurs in the data to be read out, in the lookup table, the first type code of the numerical code corresponding to the address information pointed to by the read command is revised as the invalid marked value, and the second type code is revised as the identification code configured for identifying the spare memory cell 44.

[0072] The execution unit 43 is configured to perform a read operation or a write operation on the memory cell 31. The execution unit is also connected to the associating unit 42, and the execution unit is configured to perform a read operation or a write operation on the memory cell 41 corresponding to the address information, or to stop performing the read operation or the write operation on the memory cell 41 corresponding to the address information according to mark information of the associating unit 42. Specifically, if the first type code of the numerical code corresponding to the address information pointed to by the read command or the write command is the valid marked value, the execution unit 43 performs the read operation or the write operation on the memory cell corresponding to the address information. However, if the first type code of the numerical code corresponding to the address information pointed to by the read command or the write command is the invalid marked value, the execution unit 43 stops performing the read operation or the write operation on the memory cell corresponding to

the address information, and performs the read operation or the write operation on the spare memory cell identified by the second type code according to the second type code of the numerical code.

[0073] The spare memory cell 44 corresponds to the address information pointed to by the read command or the write command through the second type code, and is configured to store data. In the present disclosure, the spare memory cell 44 may be a memory unit well known to those skilled in the art, such as a basic memory cell, a memory segment, memory pages, and memory blocks, which are not limited by the present disclosure.

[0074] It is to be noted that in other implementations, the associating unit 42 may be merely connected to the execution unit 43, and the command receiving unit 40 may be directly connected to the execution unit 43. The present disclosure does not limit this connection mode, and those of ordinary skill in the art may set to implement the above functions as required.

[0075] Further, the memory device of the present disclosure also provides a second embodiment. With reference to FIG 5, a schematic structural diagram of the memory device according to the second embodiment of the present disclosure is illustrated. The second embodiment differs from the first embodiment in that the memory device also includes an identification code generating unit 45. The identification code generating unit 45 is configured to generate an identification code configured for identifying the spare memory cell. The identification code generating unit 45 is connected to the associating unit 42, and the associating unit 42 can revise the second type code of the numerical code as the identification code generated by the identification code generating unit 45. Further, the identification code generating unit 45 can record the number of revising times of the second type code of the numerical code in the associating unit 42, to generate the identification code according to the number of revising times.

[0076] The associating unit 42 associates the address information with the spare memory cell 44 through the identification code, such that the execution unit 43 can perform the read operation or the write operation on the spare memory cell 44.

[0077] Further, the memory device of the present disclosure also provides a third embodiment. With reference to FIG 6, a schematic structural diagram of the memory device according to a third embodiment of the present disclosure is illustrated. The third embodiment differs from the first embodiment in that the memory device also includes an ECC decoding unit 46.

[0078] The ECC decoding unit 46 is connected to the execution unit 43, the memory cell 41, and the associating unit 42.

[0079] The ECC decoding unit 46 is configured to decode the first ECC corresponding to the data to be read out in the read operation to restore data where an error likely occurs. Furthermore, the numerical code of the associating unit 42 may be revised based on a fact whether the ECC decoding unit 46 restores the data. The ECC decoding unit 46 is also configured to form a second ECC corresponding to data to be written in the write operation.

[0080] Specifically, in this embodiment, the command receiving unit receives a write command. When performing the write operation on the memory cell corresponding to the address information pointed to by the write command, the ECC decoding unit 46 forms an ECC corresponding to data to be written in the write operation, and stores the ECC into the memory cell 41 corresponding to the address information pointed to by the write command. After the write operation is completed, when a subsequent read operation is performed on the memory cell corresponding to the address information, the ECC decoding unit 46 decodes the ECC. It may be determined whether an error occurs in the data to be read out read by the read operation according to decoding of the ECC decoding unit 46, and then the numerical code of the associating unit 42 is revised.

[0081] Further, in this embodiment, it may be determined whether to revise the numerical code of the associating unit 42 based on a fact whether the ECC decoding unit 46 restores the data. Specifically, if the ECC decoding unit 46 decodes the ECC and restores the data, this means that an error occurs in the data to be read out read by the read operation. In this case, the numerical code corresponding to the address information of the memory cell is revised as a combination of the invalid marked value and the identification code in the associating unit 42. If the ECC decoding unit 46 decodes the ECC, but does not restore the data, this means that no error occurs in the data to be read out read by the read operation. In this case, the numerical code corresponding to the address information is revised as a combination of the valid marked value and the meaningless code in the associating unit 42, or the initial mark of the numerical code corresponding to the address information is retained.

[0082] In other embodiments of the present disclosure, the ECC decoding unit 46 decodes the ECC. Although the ECC decoding unit 46 does not restore the data, it may be still determined that an error occurs in the data to be read out read by the read operation according to decoding of the ECC decoding unit 46. In this case, the numerical code corresponding to the address information of the memory cell is revised as a combination of the invalid marked value and the identification code in the associating unit 42.

[0083] In the third embodiment, the execution unit 43 not only is connected to the ECC decoding unit 46, but also is connected to the memory cell 41. However, in a fourth embodiment of the present disclosure, with reference to FIG 7, a schematic structural diagram of the memory device according to the fourth embodiment, the execution unit 43 is connected to the ECC decoding unit 46, and the ECC decoding unit 46 is further connected to the memory cell 41. It is to be understood that different connection relationships may be selected ac-

cording to different needs.

[0084] The memory device of the present disclosure also provides a fifth embodiment. With reference to FIG 8, a schematic structural diagram of the memory device according to a fifth embodiment of the present disclosure is illustrated. The fifth embodiment differs from the third embodiment in that the memory device also includes a logic layer 100 and a plurality of memory layers 200 (only one memory layer is shown in FIG 8). The memory layers 200 may be DRAM chips, and the logic layer 100 may be a layer provided with a logic circuit, such as a control chip or an interposer. The plurality of memory layers 200 may be vertically stacked above or below the logic layer 100, but the present disclosure is not limited thereto. Furthermore, the plurality of memory layers 200 may be integrated together using other packaging methods.

[0085] The command receiving unit 40, the associating unit 42, the execution unit 43 and the ECC decoding unit 46 may be arranged in the logic layer 100. The memory cell 41 and the spare memory cell 44 are arranged in the memory layer 200. In another embodiment of the present disclosure, the associating unit 42 and the ECC decoding unit 46 may also be arranged in the memory layer 200.

[0086] In this embodiment, the logic layer 100 has at least one first data transmission port 47, and the memory layer 200 has at least one second data transmission port 48. Instructions and data are transmitted between the logic layer 100 and the plurality of memory layers 200 through the first data transmission port 47 and the second data transmission port 48.

[0087] Further, in the fifth embodiment, the execution unit 43 not only is connected to the ECC decoding unit 46, but also is connected to the memory cell 41 through the first data transmission port 47 and the second data transmission port 48. However, in the fifth embodiment of the present disclosure, with reference to FIG 9, a schematic structural diagram of the memory device according to the fifth embodiment, the execution unit 43 is connected to the ECC decoding unit 46, and the ECC decoding unit 46 is connected to the memory cell 41 through the first data transmission port 47 and the second data transmission port 48. It is to be understood that different connection relationships may be selected according to different needs.

[0088] What is mentioned above merely refers to some embodiments of the present disclosure. It is to be pointed out that to those of ordinary skill in the art, various improvements and embellishments may be made without departing from the principle of the present disclosure, and these improvements and embellishments are also deemed to be within the scope of protection of the present disclosure.

[0089] The ECC decoding unit 46 is configured to decode the first ECC corresponding to the data to be read out in the read operation to restore data where an error likely occurs. Furthermore, the numerical code of the associating unit 42 may be revised based on a fact whether the ECC decoding unit 46 restores the data. The ECC decoding unit 46 is also configured to form a second ECC corresponding to data to be written in the write operation.

[0090] Specifically, in this embodiment, the command receiving unit receives a write command. When performing the write operation on the memory cell corresponding to the address information pointed to by the write command, the ECC decoding unit 46 forms an ECC corresponding to data to be written in the write operation, and stores the ECC into the memory cell 41 corresponding to the address information pointed to by the write command. After the write operation is completed, when a subsequent read operation is performed on the memory cell corresponding to the address information, the ECC decoding unit 46 decodes the ECC. It may be determined whether an error occurs in the data to be read out read by the read operation according to decoding of the ECC decoding unit 46, and then the numerical code of the associating unit 42 is revised.

[0091] Further, in this embodiment, it may be determined whether to revise the numerical code of the associating unit 42 based on a fact whether the ECC decoding unit 46 restores the data. Specifically, if the ECC decoding unit 46 decodes the ECC and restores the data, this means that an error occurs in the data to be read out read by the read operation. In this case, the numerical code corresponding to the address information of the memory cell is revised as a combination of the invalid marked value and the identification code in the associating unit 42. If the ECC decoding unit 46 decodes the ECC, but does not restore the data, this means that no error occurs in the data to be read out read by the read operation. In this case, the numerical code corresponding to the address information is revised as a combination of the valid marked value and the meaningless code in the associating unit 42, or the initial mark of the numerical code corresponding to the address information is retained.

[0092] In other embodiments of the present disclosure, the ECC decoding unit 46 decodes the ECC. Although the ECC decoding unit 46 does not restore the data, it may be still determined that an error occurs in the data to be read out read by the read operation according to decoding of the ECC decoding unit 46. In this case, the numerical code corresponding to the address information of the memory cell is revised as a combination of the invalid marked value and the identification code in the associating unit 42.

[0093] In the third embodiment, the execution unit 43 not only is connected to the ECC decoding unit 46, but also is connected to the memory cell 41. However, in a fourth embodiment of the present disclosure, with reference to FIG 7, a schematic structural diagram of the memory device according to the fourth embodiment, the execution unit 43 is connected to the ECC decoding unit 46, and the ECC decoding unit 46 is further connected to the memory cell 41. It is to be understood that different connection relationships may be selected according to different needs.

[0094] The memory device of the present disclosure also provides a fifth embodiment. With reference to FIG 8, a schematic structural diagram of the memory device according to a fifth embodiment of the present disclosure is illustrated. The fifth embodiment differs from the third embodiment in that the memory device also includes a logic layer 100 and a plurality of memory layers 200 (only one memory layer is shown in FIG 8). The memory layers 200 may be DRAM chips, and the logic layer 100 may be a layer provided with a logic circuit, such as a control chip or an interposer. The plurality of memory layers 200 may be vertically stacked above or below the logic layer 100, but the present disclosure is not limited thereto. Furthermore, the plurality of memory layers 200 may be integrated together using other packaging methods.

[0095] The command receiving unit 40, the associating unit 42, the execution unit 43 and the ECC decoding unit 46 may be arranged in the logic layer 100. The memory cell 41 and the spare memory cell 44 are arranged in the memory layer 200. In another embodiment of the present disclosure, the associating unit 42 and the ECC decoding unit 46 may also be arranged in the memory layer 200.

[0096] In this embodiment, the logic layer 100 has at least one first data transmission port 47, and the memory layer 200 has at least one second data transmission port 48. Instructions and data are transmitted between the logic layer 100 and the plurality of memory layers 200 through the first data transmission port 47 and the second data transmission port 48.

[0097] Further, in the fifth embodiment, the execution unit 43 not only is connected to the ECC decoding unit 46, but also is connected to the memory cell 41 through the first data transmission port 47 and the second data transmission port 48. However, in the fifth embodiment of the present disclosure, with reference to FIG 9, a schematic structural diagram of the memory device according to the fifth embodiment, the execution unit 43 is connected to the ECC decoding unit 46, and the ECC decoding unit 46 is connected to the memory cell 41 through the first data transmission port 47 and the second data transmission port 48. It is to be understood that different connection relationships may be selected according to different needs.

[0098] What is mentioned above merely refers to some embodiments of the present disclosure. It is to be pointed out that to those of ordinary skill in the art, various improvements and embellishments may be made without departing from the scope of protection of the appended set of claims.

Claims

1. A method for reading and writing, comprising:

applying (S20) a read command to a memory device, the read command pointing to address information;

determining (S21) whether the address information pointed to by the read command is valid; and

reading (S22) data to be read out from a memory cell corresponding to the address information pointed to by the read command if the address information pointed to by the read command is valid;

wherein the method further comprises:

if an error occurs in the data to be read out, marking, in a lookup table, a first type code of a numerical code corresponding to the address information pointed to by the read command as an invalid marked value, revising a second type code as an identification code configured for identifying a spare memory cell, and storing the data to be read out into the spare memory cell,

wherein the identification code is generated according to a number of revising times of the second type code.

2. The method for reading and writing according to claim 1, further comprising:

marking the address information pointed to by the read command as invalid if the error occurs in the data to be read out; or

marking the address information pointed to by the read command as valid if no error occurs in the data to be read out;

wherein address information not marked as invalid is initially set as valid.

3. The method for reading and writing according to claim 2, wherein the reading data to be read out from the memory cell corresponding to the address information pointed to by the read command further comprises:

reading, from the memory cell corresponding to the address information pointed to by the read command, a first error correction code, ECC, corresponding to the data to be read out; and

wherein a method for determining whether an error occurs in the data to be read out comprises:

decoding the first ECC to determine whether the error occurs in the data to be read out.

4. The method for reading and writing according to claim 2, wherein address information of the memory cell and a numerical code corresponding to the address information are recorded in the lookup table, the numerical code being composed of a first type code and a second type code, the first type code being configured for marking whether the address information is valid, and the second type code being configured for recording the identification code of the

spare memory cell.

5. The method for reading and writing according to claim 4, further comprising: recording number of revising times of the second type code, and generating a corresponding identification code according to the number of revising times;
wherein the numerical code has an initial value; in the initial value, the first type code being a valid marked value, and the second type code being a meaningless code.

6. The method for reading and writing according to claim 4, comprising:

applying (S30) a write command to the memory device;
performing a write operation on a memory cell corresponding to address information pointed to by the write command if a mark of the address information pointed to by the write command is valid; and
stopping performing the write operation on the memory cell corresponding to the address information pointed to by the write command if the mark of the address information pointed to by the write command is invalid, and performing the write operation on the spare memory cell identified by the identification code corresponding to the address information pointed to by the write command.

7. The method for reading and writing according to claim 6, wherein

when applying the write command to the memory device, the numerical code is looked up from the lookup table by taking the address information pointed to by the write command as an index;
wherein the performing the write operation on the memory cell corresponding to the address information pointed to by the write command further comprises:
forming a second error correction code, ECC, corresponding to data to be written in the write operation, and writing the second ECC together with the data to be written into the memory cell corresponding to the address information pointed to by the write command.

8. The method for reading and writing according to claim 4, wherein the method further comprises: if a mark of the address information pointed to by the read command is invalid, performing a read operation on the spare memory cell identified by the identification code corresponding to the address information pointed to by the read command.

9. The method for reading and writing according to claim 1, further comprising: storing, when the error occurs in the data to be read out, corrected data into the spare memory cell if the data to be read out is corrected; and storing the data to be read out into the spare memory cell if the data to be read out is not corrected.

10. A memory device, comprising:

a command receiving unit (40), configured to receive a read command or a write command;
a memory cell (41), configured to correspond to address information pointed to by the read command or the write command;
a spare memory cell (44);
a determining unit, configured to determine whether the address information pointed to by the read command is valid; and
an execution unit (43), configured to perform a read operation or a write operation on the memory cell (41) or the spare memory cell (44) if the address information pointed to by the read command is valid,
wherein the memory device further comprises:

an associating unit, configured to if an error occurs in the data to be read out, mark, in a lookup table a first type code of a numerical code corresponding to the address information pointed to by the read command as an invalid marked value, revise a second type code as an identification code configured for identifying a spare memory cell, and store the data to be read out into the spare memory cell,
wherein the identification code is generated according to a number of revising times of the second type code.

11. The memory device according to claim 10, wherein the associating unit (42) is further configured to store mark information configured for recording whether the address information is valid or invalid;

wherein the associating unit (42) is a lookup table, and address information of the memory cell (41) and a numerical code corresponding to the address information are recorded in the lookup table;
wherein the numerical code is composed of a first type code and a second type code, the first type code is configured for marking whether the address information is valid, and the second type code is configured for recording the identification code of the spare memory cell (44).

12. The memory device according to claim 10, further

comprising an error correction code, ECC, decoding unit (46), wherein the ECC decoding unit (46) is configured to decode a first ECC corresponding to data to be read out in the read operation and to form a second ECC corresponding to data to be written in the write operation.

13. The memory device according to claim 10, wherein the execution unit (43) is further connected to the associating unit (42), and the execution unit (43) is configured to perform the read operation or the write operation on the memory cell (41) corresponding to the address information or on the spare memory cell (44), or to stop performing the read operation or the write operation on the memory cell (41) corresponding to the address information, based on a record of the associating unit (42).

Patentansprüche

1. Verfahren zum Lesen und Schreiben, umfassend:

Anwenden (S20) eines Lesebefehls auf eine Speichervorrichtung, wobei der Lesebefehl auf Adressinformationen hinweist;
Bestimmen (S21), ob die Adressinformationen, auf die der Lesebefehl hinweist, gültig sind; und
Lesen (S22) von auszulesenden Daten aus einer Speicherzelle, die den Adressinformationen entspricht, auf die der Lesebefehl hinweist, falls die Adressinformationen, auf die der Lesebefehl hinweist, gültig sind;
wobei das Verfahren ferner Folgendes umfasst:

falls ein Fehler in den auszulesenden Daten auftritt, Markieren eines ersten Typcodes eines Zahlencodes, der den Adressinformationen entspricht, auf die der Lesebefehl hinweist, in einer Lookup-Tabelle als ungültig markierten Wert, Überprüfen eines zweiten Typcodes als Identifikationscode, der zum Identifizieren einer überschüssigen Speicherzelle ausgestaltet ist, und Speichern der auszulesenden Daten in der überschüssigen Speicherzelle,
wobei der Identifikationscode gemäß einer Anzahl von Überprüfungen des zweite Typcodes erzeugt wird.

2. Verfahren zum Lesen und Schreiben nach Anspruch 1, ferner umfassend:

Markieren der Adressinformationen, auf die der Lesebefehl hinweist, als ungültig, falls der Fehler in den auszulesenden Daten auftritt; oder
Markieren der Adressinformationen, auf die der Lesebefehl hinweist, als gültig, falls kein Fehler in den auszulesenden Daten auftritt;
wobei Adressinformationen, die nicht als ungültig markiert sind, anfangs als gültig eingestellt werden.

3. Verfahren zum Lesen und Schreiben nach Anspruch 2, wobei die auszulesenden Lesedaten aus der Speicherzelle, die den Adressinformationen entspricht, auf die der Lesebefehl hinweist, ferner Folgendes umfassen:

Lesen eines ersten Fehlerkorrekturcodes, *Error Correction Code* - ECC, der den auszulesenden Daten entspricht, aus der Speicherzelle, die den Adressinformationen entspricht, auf die der Lesebefehl hinweist; und
wobei ein Verfahren zum Bestimmen, ob ein Fehler in den auszulesenden Daten auftritt, Folgendes umfasst: Decodieren des ersten ECC, um zu bestimmen, ob der Fehler in den auszulesenden Daten auftritt.

4. Verfahren zum Lesen und Schreiben nach Anspruch 2, wobei Adressinformationen der Speicherzelle und ein Zahlencode, der den Adressinformationen entspricht, in der Lookup-Tabelle aufgezeichnet werden, wobei der Zahlencode aus einem ersten Typcode und einem zweiten Typcode besteht, wobei der erste Typcode zum Markieren, ob die Adressinformationen gültig sind, ausgestaltet ist, und der zweite Typcode zum Aufzeichnen des Identifikationscodes der überschüssigen Speicherzelle ausgestaltet ist.

5. Verfahren zum Lesen und Schreiben nach Anspruch 4, ferner umfassend: Aufzeichnen der Anzahl der Überprüfungen des zweiten Typcodes und Erzeugen eines entsprechenden Identifikationscodes gemäß der Anzahl der Überprüfungen;
wobei der Zahlencode einen Anfangswert aufweist;
wobei in dem Anfangswert der erste Typcode ein gültig markierter Wert ist und der zweite Typcode ein bedeutungsloser Code ist.

6. Verfahren zum Lesen und Schreiben nach Anspruch 4, umfassend:

Anwenden (S30) eines Schreibbefehls auf die Speichervorrichtung;
Durchführen eines Schreibvorgangs auf einer Speicherzelle, die den Adressinformationen entspricht, auf die der Schreibbefehl hinweist, falls eine Markierung der Adressinformationen, auf die der Schreibbefehl hinweist, gültig ist; und
Anhalten der Durchführung des Schreibvorgangs auf der Speicherzelle, die den Adressinformationen entspricht, auf die der Schreibbefehl hinweist, falls die Markierung der Adressinformationen, auf die der Schreibbefehl hinweist,

ungültig ist, und Durchführen des Schreibvorgangs auf der überschüssigen Speicherzelle, die durch den Identifikationscode identifiziert wurde, der den Adressinformationen entspricht, auf die der Schreibbefehl hinweist.

7. Verfahren zum Lesen und Schreiben nach Anspruch 6, wobei

beim Anwenden des Schreibbefehls auf die Speichervorrichtung der Zahlencode in der Lookup-Tabelle nachgeschlagen wird, indem die Adressinformationen, auf die der Schreibbefehl hinweist, als Index herangezogen werden;
wobei das Durchführen des Schreibvorgangs auf der Speicherzelle, die den Adressinformationen entspricht, auf die der Schreibbefehl hinweist, ferner Folgendes umfasst:
Bilden eines zweiten Fehlerkorrekturcodes, ECC, der in dem Schreibvorgang zu schreibenden Daten entspricht, und Schreiben des zweiten ECC zusammen mit den auf der Speicherzelle, die den Adressinformationen entspricht, auf die der Schreibbefehl hinweist, zu schreibenden Daten.

8. Verfahren zum Lesen und Schreiben nach Anspruch 4, wobei das Verfahren ferner Folgendes umfasst: falls eine Markierung der Adressinformationen, auf die der Lesebefehl hinweist, ungültig ist, Durchführen eines Lesevorgangs auf der überschüssigen Speicherzelle, die durch den Identifikationscode identifiziert wurde, der den Adressinformationen entspricht, auf die der Lesebefehl hinweist.

9. Verfahren zum Lesen und Schreiben nach Anspruch 1, ferner umfassend: bei Auftreten des Fehlers in den auszulesenden Daten Speichern korrigierter Daten in der überschüssigen Speicherzelle, falls die auszulesenden Daten korrigiert sind; und Speichern der auszulesenden Daten in der überschüssigen Speicherzelle, falls die auszulesenden Daten nicht korrigiert sind.

10. Speichervorrichtung, umfassend:

eine Befehlsempfangseinheit (40), die dazu ausgestaltet ist, einen Lesebefehl oder einen Schreibbefehl zu empfangen;
eine Speicherzelle (41), die dazu ausgestaltet ist, Adressinformationen zu entsprechen, auf die der Lesebefehl oder der Schreibbefehl hinweist;
eine überschüssige Speicherzelle (44);
eine Bestimmungseinheit, die dazu ausgestaltet ist, zu bestimmen, ob die Adressinformationen, auf die der Lesebefehl hinweist, gültig sind; und
eine Ausführungseinheit (43), die dazu ausgestaltet ist, einen Lesevorgang oder einen Schreibvorgang auf der Speicherzelle (41) oder der überschüssigen Speicherzelle (44) durchzuführen, falls die Adressinformationen, auf die der Lesebefehl hinweist, gültig sind,
wobei die Speichervorrichtung ferner Folgendes umfasst:

eine Zuordnungseinheit, die dazu ausgestaltet ist, falls ein Fehler in den auszulesenden Daten auftritt, in einer Lookup-Tabelle einen ersten Typcode eines Zahlencodes, der den Adressinformationen entspricht, auf die der Lesebefehl hinweist, als ungültig markierten Wert zu markieren, einen zweiten Typcode als Identifikationscode zu überprüfen, der zum Identifizieren einer überschüssigen Speicherzelle ausgestaltet ist, und die auszulesenden Daten in der überschüssigen Speicherzelle zu speichern,
wobei der Identifikationscode gemäß einer Anzahl von Überprüfungen des zweiten Typcodes erzeugt wird.

11. Speichervorrichtung nach Anspruch 10, wobei die Zuordnungseinheit (42) ferner dazu ausgestaltet ist, Markierungsinformationen zu speichern, die zum Aufzeichnen, ob die Adressinformationen gültig oder ungültig sind, ausgestaltet sind;

wobei die Zuordnungseinheit (42) eine Lookup-Tabelle ist und die Adressinformationen der Speicherzelle (41) und ein Zahlencode, der den Adressinformationen entspricht, in der Lookup-Tabelle aufgezeichnet sind;
wobei der Zahlencode aus einem ersten Typcode und einem zweiten Typcode besteht, der erste Typcode zum Markieren, ob die Adressinformationen gültig sind, ausgestaltet ist und der zweite Typcode zum Aufzeichnen des Identifikationscodes der überschüssigen Speicherzelle (44) ausgestaltet ist.

12. Speichervorrichtung nach Anspruch 10, ferner umfassend eine Fehlerkorrekturcode-Decodiereinheit, ECC-Decodiereinheit (46), wobei die ECC-Decodiereinheit (46) dazu ausgestaltet ist, einen ersten ECC zu decodieren, der in dem Lesevorgang auszulesenden Daten entspricht, und einen zweiten ECC zu bilden, der in dem Schreibvorgang zu schreibenden Daten entspricht.

13. Speichervorrichtung nach Anspruch 10, wobei die Ausführungseinheit (43) ferner mit der Zuordnungseinheit (42) verbunden ist und die Ausführungseinheit (43) dazu ausgestaltet ist, den Lesevorgang

oder den Schreibvorgang auf der Speicherzelle (41), die den Adressinformationen entspricht, oder auf der überschüssigen Speicherzelle (44) durchzuführen oder die Durchführung des Lesevorgangs oder des Schreibvorgangs auf der Speicherzelle (41), die den Adressinformationen entspricht, basierend auf einer Aufzeichnung der Zuordnungseinheit (42) anzuhalten.

Revendications

1. Procédé de lecture et d'écriture, comprenant :

l'application (S20) d'une commande de lecture à un dispositif de mémoire, la commande de lecture pointant vers des informations d'adresse ;
la détermination (S21) de si les informations d'adresse vers lesquelles pointe la commande de lecture sont valides ; et
la lecture (S22) de données à lire à partir d'une cellule de mémoire correspondant aux informations d'adresse vers lesquelles pointe la commande de lecture si les informations d'adresse vers lesquelles pointe la commande de lecture sont valides ;
dans lequel le procédé comprend en outre :

si une erreur se produit dans les données à lire, le marquage, dans une table de consultation, d'un premier code de type d'un code numérique correspondant aux informations d'adresse vers lesquelles pointe la commande de lecture en tant que valeur marquée invalide, la révision d'un deuxième code de type en tant que code d'identification configuré pour identifier une cellule de mémoire de réserve, et le stockage des données à lire dans la cellule de mémoire de réserve,
dans lequel le code d'identification est généré en fonction d'un nombre de révisions du deuxième code de type.

2. Procédé de lecture et d'écriture selon la revendication 1, comprenant en outre :

le marquage des informations d'adresse vers lesquelles pointe la commande de lecture comme invalides si l'erreur se produit dans les données à lire ; ou
le marquage des informations d'adresse vers lesquelles pointe la commande de lecture comme valides si aucune erreur ne se produit dans les données à lire ;
dans lequel les informations d'adresse non marquées comme invalides sont initialement définies comme valides.

3. Procédé de lecture et d'écriture selon la revendication 2, dans lequel les données de lecture à lire à partir de la cellule de mémoire correspondant aux informations d'adresse vers lesquelles pointe la commande de lecture comprennent en outre :

la lecture, à partir de la cellule de mémoire correspondant aux informations d'adresse vers lesquelles pointe la commande de lecture, d'un premier code de correction d'erreur, *error correction code* - ECC, correspondant aux données à lire ; et
dans lequel un procédé pour déterminer si une erreur se produit dans les données à lire comprend : le décodage du premier ECC pour déterminer si l'erreur se produit dans les données à lire.

4. Procédé de lecture et d'écriture selon la revendication 2, dans lequel des informations d'adresse de la cellule de mémoire et un code numérique correspondant aux informations d'adresse sont enregistrées dans la table de consultation, le code numérique étant composé d'un premier code de type et d'un deuxième code de type, le premier code de type étant configuré pour marquer si les informations d'adresse sont valides, et le deuxième code de type étant configuré pour enregistrer le code d'identification de la cellule de mémoire de réserve.

5. Procédé de lecture et d'écriture selon la revendication 4, comprenant en outre : l'enregistrement du nombre de révisions du deuxième code de type, et la génération d'un code d'identification correspondant en fonction du nombre de révisions ;
dans lequel le code numérique a une valeur initiale ;
dans la valeur initiale, le premier code de type étant une valeur marquée comme valide, et le deuxième code de type étant un code dénué de sens.

6. Procédé de lecture et d'écriture selon la revendication 4, comprenant :

l'application (S30) d'une commande d'écriture au dispositif de mémoire ;
l'exécution d'une opération d'écriture sur une cellule de mémoire correspondant aux informations d'adresse vers lesquelles pointe la commande d'écriture si une marque des informations d'adresse vers lesquelles pointe la commande d'écriture est valide ; et
l'arrêt de l'exécution de l'opération d'écriture sur la cellule de mémoire correspondant aux informations d'adresse vers lesquelles pointe la commande d'écriture si la marque des informations d'adresse vers lesquelles pointe la commande d'écriture n'est pas valide, et l'exécution de l'opération d'écriture sur la cellule de

mémoire de réserve identifiée par le code d'identification correspondant aux informations d'adresse vers lesquelles pointe la commande d'écriture.

7. Procédé de lecture et d'écriture selon la revendication 6, dans lequel

lors de l'application de la commande d'écriture au dispositif de mémoire, le code numérique est recherché dans la table de consultation en prenant les informations d'adresse vers lesquelles pointe la commande d'écriture comme index ;
dans lequel l'exécution de l'opération d'écriture sur la cellule de mémoire correspondant aux informations d'adresse vers lesquelles pointe la commande d'écriture comprend en outre :
la formation d'un deuxième code de correction d'erreur, ECC, correspondant aux données à écrire dans l'opération d'écriture, et l'écriture du deuxième ECC conjointement avec les données à écrire dans la cellule mémoire correspondant aux informations d'adresse vers lesquelles pointe la commande d'écriture.

8. Procédé de lecture et d'écriture selon la revendication 4, dans lequel le procédé comprend en outre : si une marque des informations d'adresse vers lesquelles pointe la commande de lecture n'est pas valide, l'exécution d'une opération de lecture sur la cellule de mémoire de réserve identifiée par le code d'identification correspondant aux informations d'adresse vers lesquelles pointe la commande de lecture.

9. Procédé de lecture et d'écriture selon la revendication 1, comprenant en outre : le stockage, lorsque l'erreur se produit dans les données à lire, des données corrigées dans la cellule de mémoire de réserve si les données à lire sont corrigées ; et le stockage des données à lire dans la cellule de mémoire de réserve si les données à lire ne sont pas corrigées.

10. Dispositif de mémoire, comprenant :

une unité de réception de commande (40), configurée pour recevoir une commande de lecture ou une commande d'écriture ;
une cellule de mémoire (41), configurée pour correspondre aux informations d'adresse vers lesquelles pointe la commande de lecture ou la commande d'écriture ;
une cellule de mémoire de réserve (44) ;
une unité de détermination, configurée pour déterminer si les informations d'adresse vers lesquelles pointe la commande de lecture sont valides ; et
une unité d'exécution (43), configurée pour effectuer une opération de lecture ou une opération d'écriture sur la cellule de mémoire (41) ou la cellule de mémoire de réserve (44) si les informations d'adresse vers lesquelles pointe la commande de lecture sont valides,
dans lequel le dispositif de mémoire comprend en outre :

une unité d'association, configurée pour, si une erreur se produit dans les données à lire, marquer, dans une table de consultation, un premier code de type d'un code numérique correspondant aux informations d'adresse vers lesquelles pointe la commande de lecture en tant que valeur marquée invalide, réviser un deuxième code de type en tant que code d'identification configuré pour identifier une cellule de mémoire de réserve, et stocker les données à lire dans la cellule de mémoire de réserve, dans lequel le code d'identification est généré en fonction d'un nombre de révisions du deuxième code de type.

11. Dispositif de mémoire selon la revendication 10, dans lequel l'unité d'association (42) est en outre configurée pour stocker des informations de marque configurées pour enregistrer si les informations d'adresse sont valides ou invalides ;

dans lequel l'unité d'association (42) est une table de consultation, et les informations d'adresse de la cellule de mémoire (41) et un code numérique correspondant aux informations d'adresse sont enregistrées dans la table de consultation ;
dans lequel le code numérique est composé d'un premier code de type et d'un deuxième code de type, le premier code de type est configuré pour marquer si les informations d'adresse sont valides, et le deuxième code de type est configuré pour enregistrer le code d'identification de la cellule de mémoire de réserve (44).

12. Dispositif de mémoire selon la revendication 10, comprenant en outre une unité de décodage de code de correction d'erreur, ECC, (46), dans lequel l'unité de décodage d'ECC (46) est configurée pour décoder un premier ECC correspondant à des données à lire dans l'opération de lecture et pour former un deuxième ECC correspondant à des données à écrire dans l'opération d'écriture.

13. Dispositif de mémoire selon la revendication 10, dans lequel l'unité d'exécution (43) est en outre connectée à l'unité d'association (42), et l'unité d'exécution (43) est configurée pour effectuer l'opé-

ration de lecture ou l'opération d'écriture sur la cellule de mémoire (41) correspondant aux informations d'adresse ou sur la cellule de mémoire de réserve (44), ou pour arrêter l'exécution de l'opération de lecture ou de l'opération d'écriture sur la cellule de mémoire (41) correspondant aux informations d'adresse, sur la base d'un enregistrement de l'unité d'association (42).

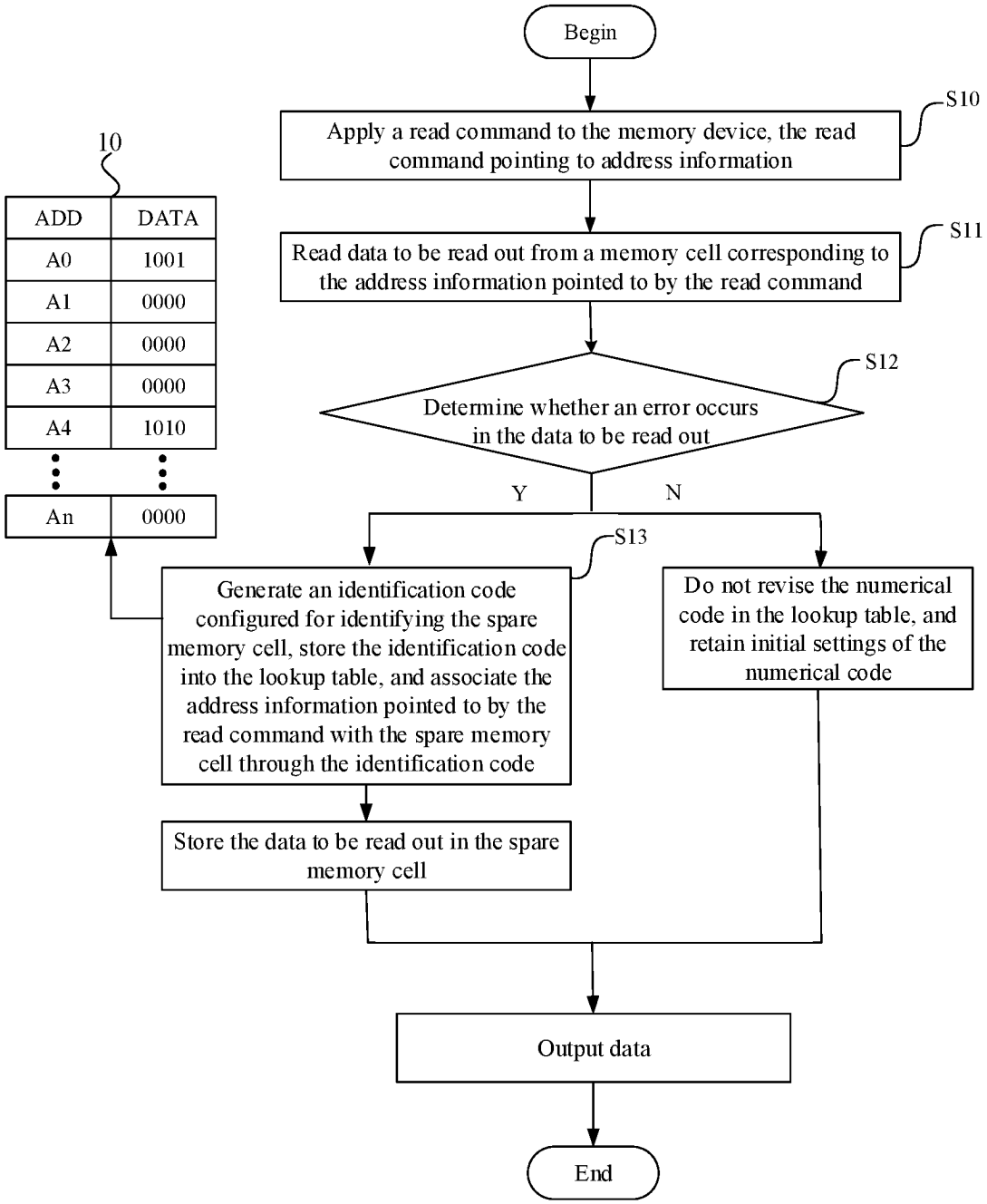
Begin
Apply a read command to the memory device, the read command pointing to address information
S10
Read data to be read out from a memory cell corresponding to the address information pointed to by the read command
S11
Determine whether an error occurs in the data to be read out
S12
Y
N
Generate an identification code configured for identifying the spare memory cell, store the identification code into the lookup table, and associate the address information pointed to by the read command with the spare memory cell through the identification code
S13
Do not revise the numerical code in the lookup table, and retain initial settings of the numerical code
Store the data to be read out in the spare memory cell
Output data
End
10
ADD
DATA
A0
1001
A1
0000
A2
0000
A3
0000
A4
1010
An
0000

FIG. 1

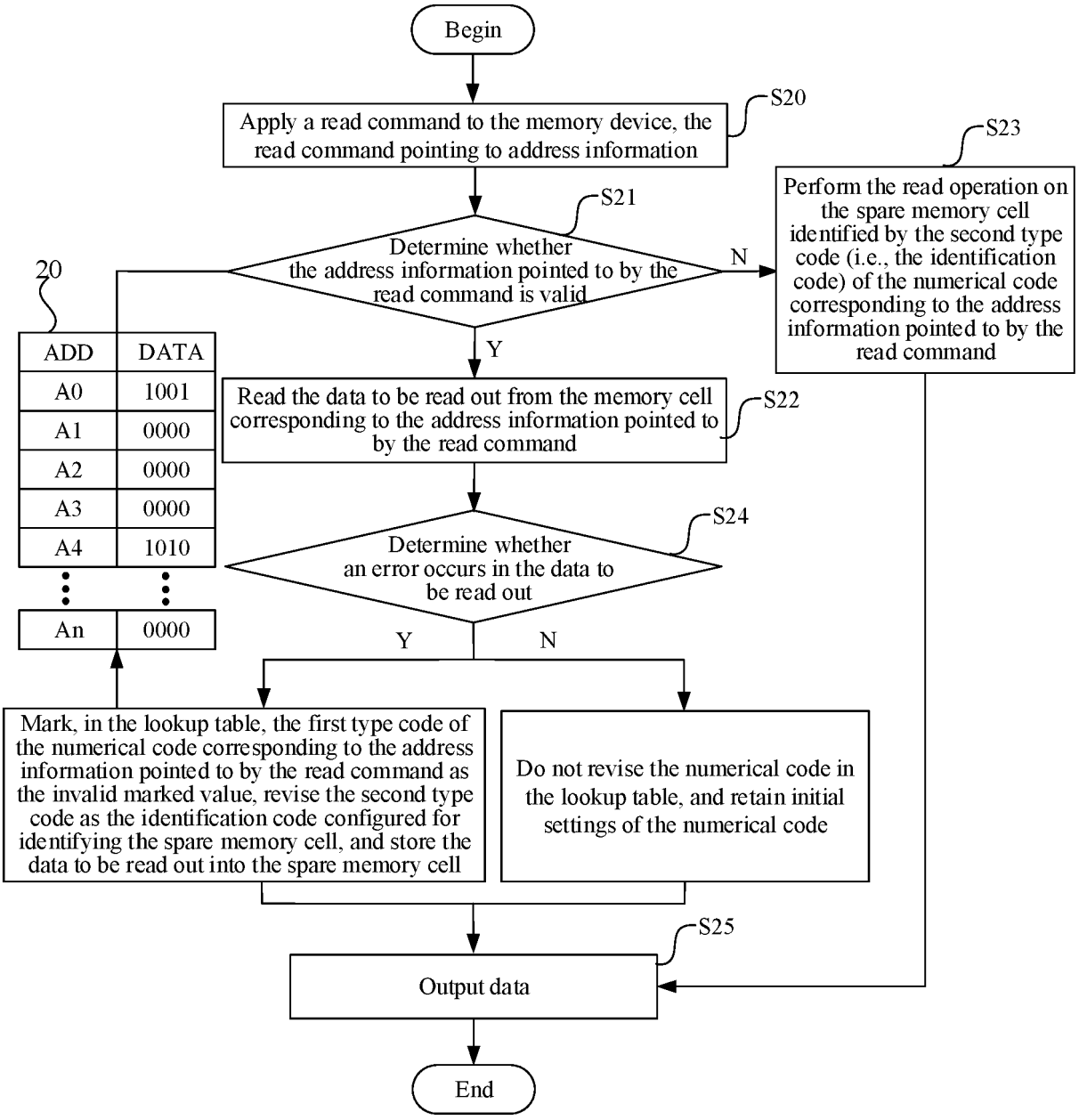
Begin
Apply a read command to the memory device, the read command pointing to address information
S20
Determine whether the address information pointed to by the read command is valid
S21
N
Y
Perform the read operation on the spare memory cell identified by the second type code (i.e., the identification code) of the numerical code corresponding to the address information pointed to by the read command
S23
Read the data to be read out from the memory cell corresponding to the address information pointed to by the read command
S22
Determine whether an error occurs in the data to be read out
S24
Y
N
Mark, in the lookup table, the first type code of the numerical code corresponding to the address information pointed to by the read command as the invalid marked value, revise the second type code as the identification code configured for identifying the spare memory cell, and store the data to be read out into the spare memory cell
Do not revise the numerical code in the lookup table, and retain initial settings of the numerical code
Output data
S25
End
20
ADD
DATA
A0
1001
A1
0000
A2
0000
A3
0000
A4
1010
An
0000

FIG. 2

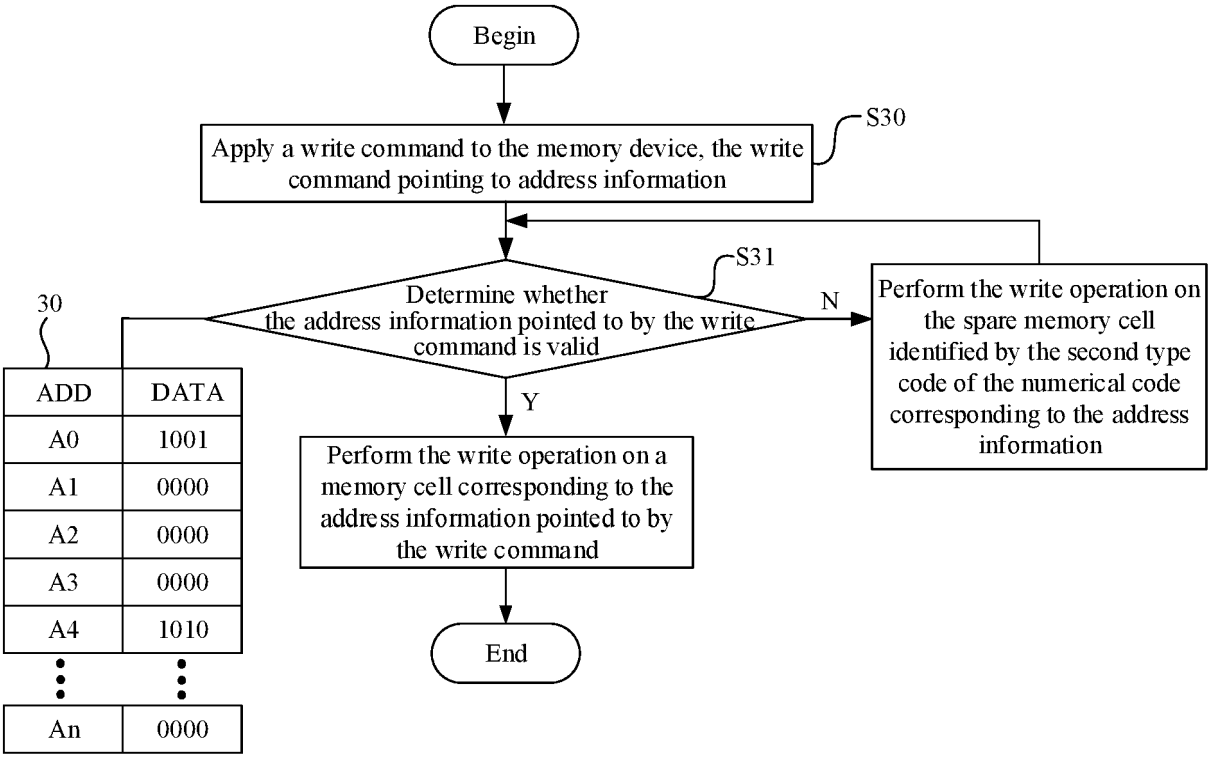
Begin
Apply a write command to the memory device, the write command pointing to address information
S30
Determine whether the address information pointed to by the write command is valid
S31
N
Perform the write operation on the spare memory cell identified by the second type code of the numerical code corresponding to the address information
Y
Perform the write operation on a memory cell corresponding to the address information pointed to by the write command
End
30
ADD
DATA
A0
1001
A1
0000
A2
0000
A3
0000
A4
1010
An
0000

FIG. 3

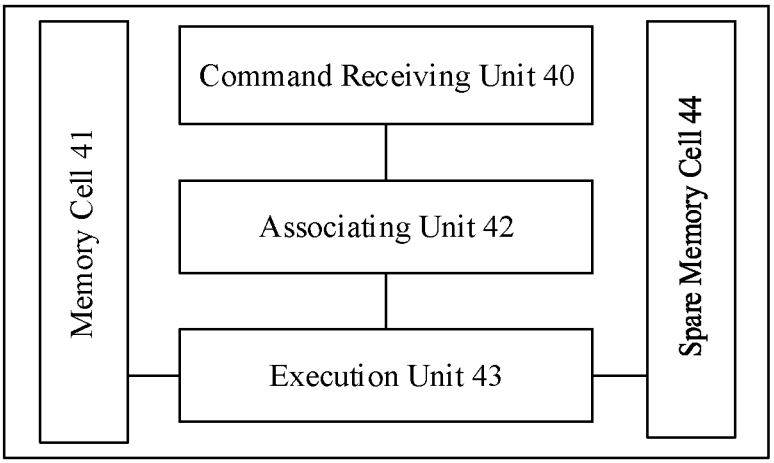
Command Receiving Unit 40
Associating Unit 42
Execution Unit 43
Memory Cell 41
Spare Memory Cell 44

FIG. 4

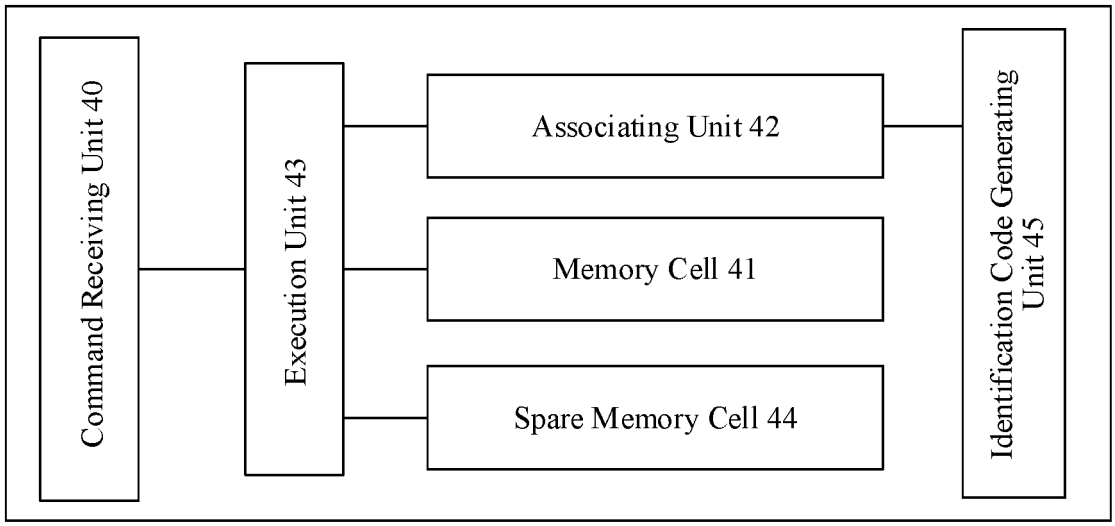
Command Receiving Unit 40
Execution Unit 43
Associating Unit 42
Memory Cell 41
Spare Memory Cell 44
Identification Code Generating Unit 45

FIG. 5

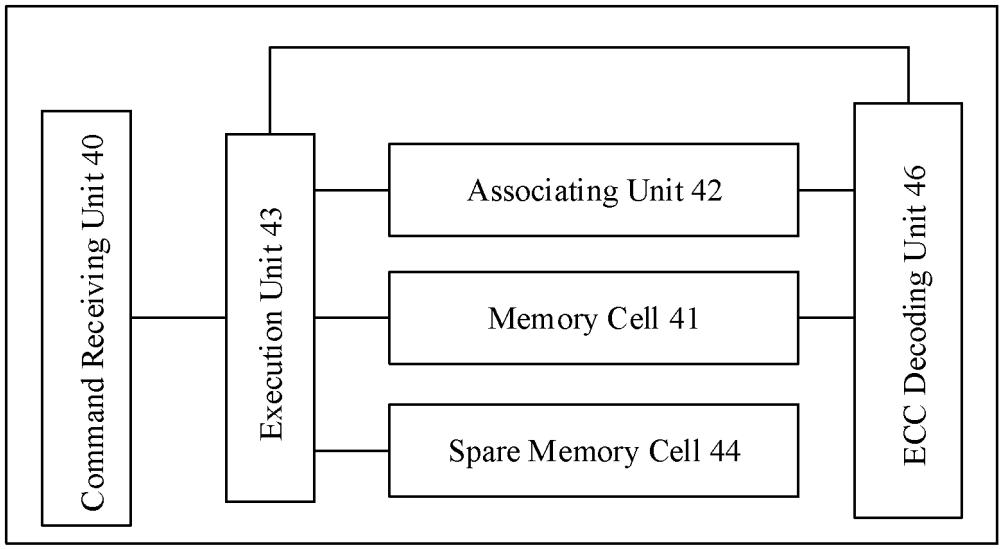
Command Receiving Unit 40
Execution Unit 43
Associating Unit 42
Memory Cell 41
Spare Memory Cell 44
ECC Decoding Unit 46

FIG. 6

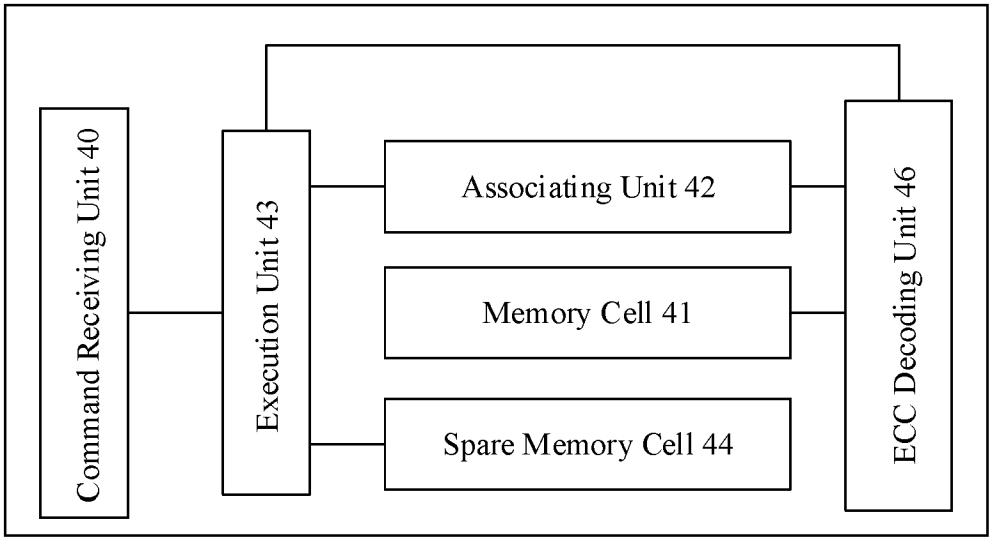
Command Receiving Unit 40
Execution Unit 43
Associating Unit 42
Memory Cell 41
Spare Memory Cell 44
ECC Decoding Unit 46

FIG. 7

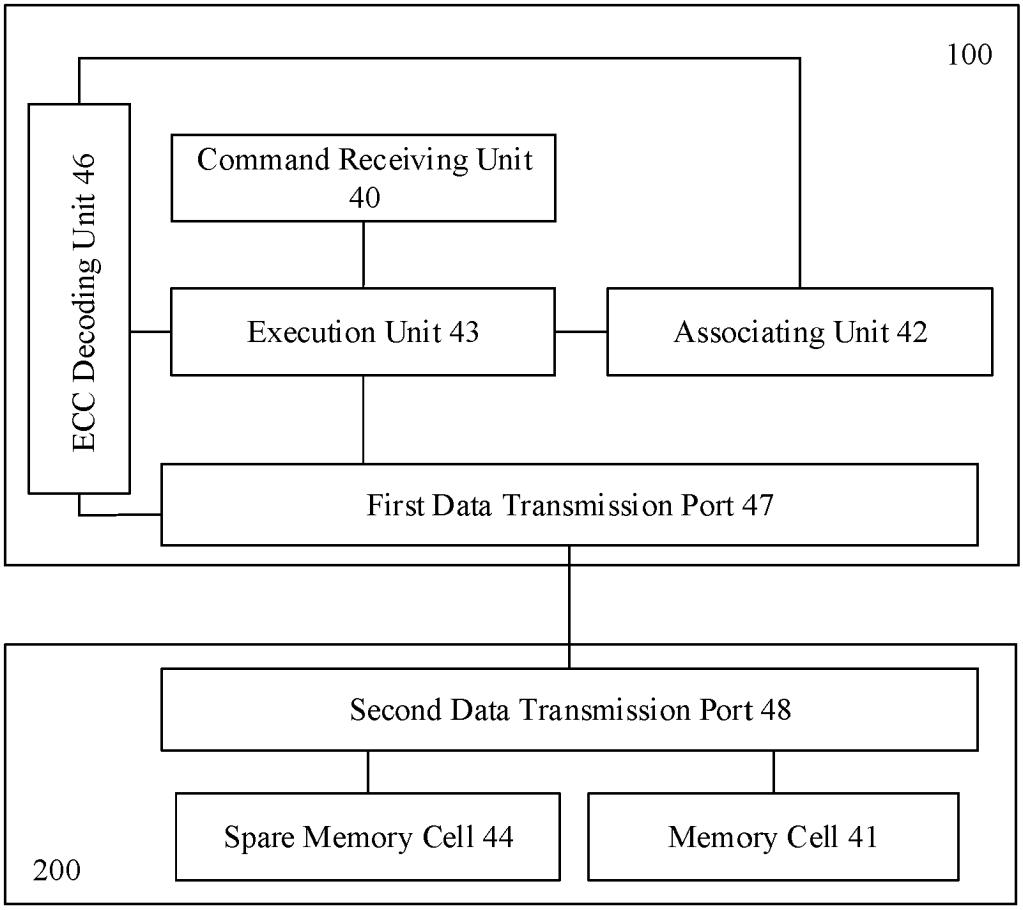
100
ECC Decoding Unit 46
Command Receiving Unit 40
Execution Unit 43
Associating Unit 42
First Data Transmission Port 47
Second Data Transmission Port 48
Spare Memory Cell 44
Memory Cell 41
200

FIG. 8

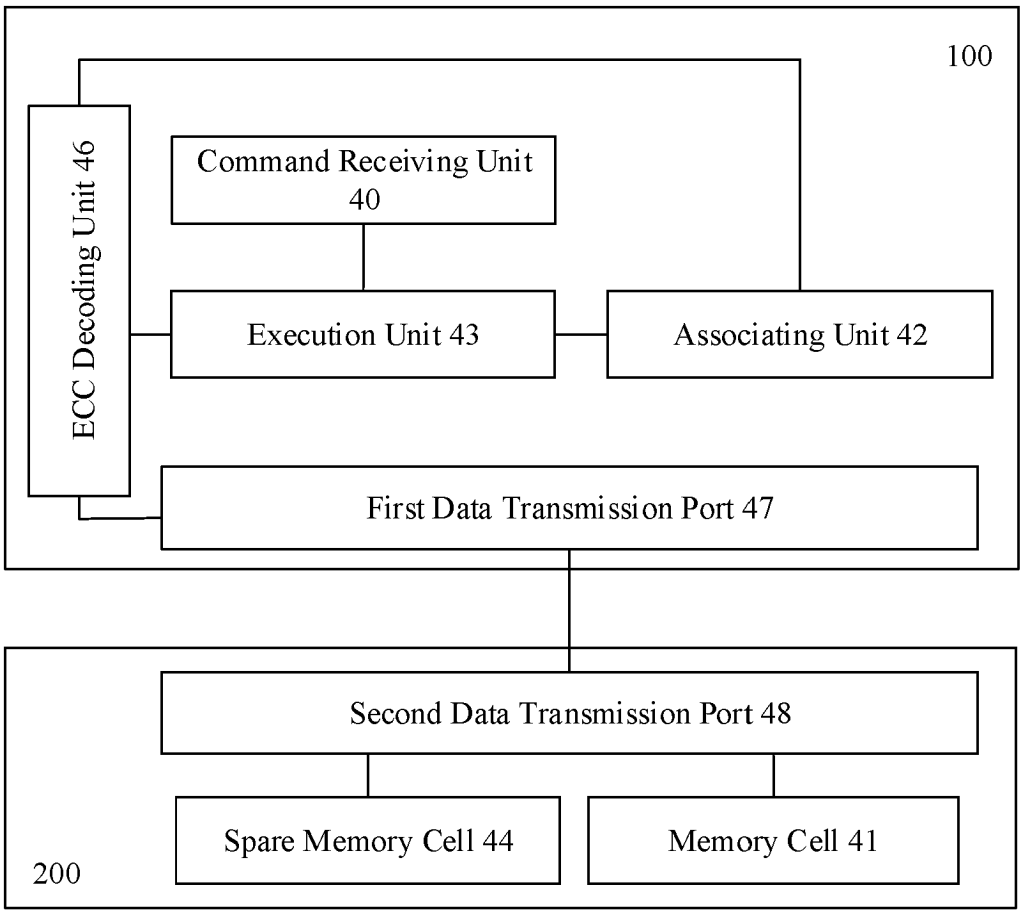
100
ECC Decoding Unit 46
Command Receiving Unit 40
Execution Unit 43
Associating Unit 42
First Data Transmission Port 47
Second Data Transmission Port 48
Spare Memory Cell 44
Memory Cell 41
200

FIG. 9

REFERENCES CITED IN THE DESCRIPTION

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