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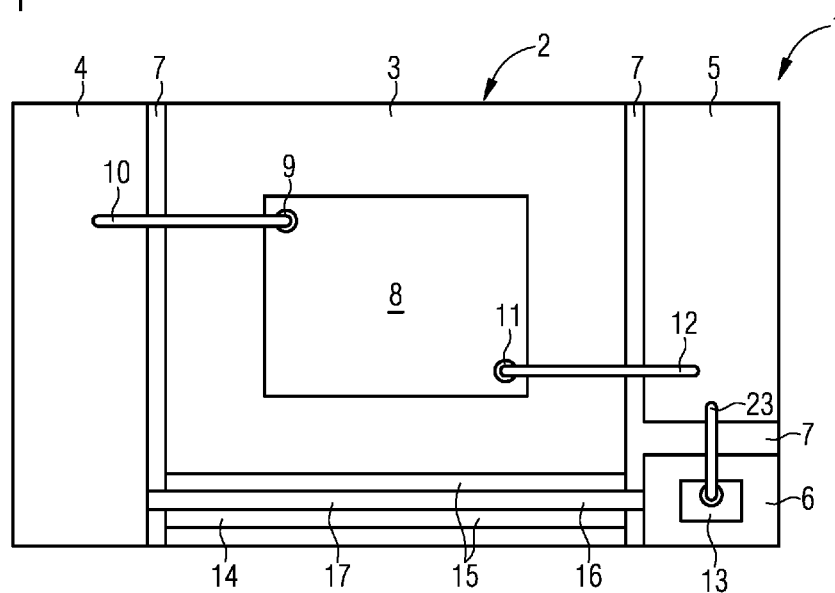
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(54) Title: OPTOELECTRONIC PACKAGE

FIG 1



(57) Abstract: The invention refers to an optoelectronic package comprising a carrier with a first conductive section, a second conductive section, a third conductive section and a fourth conductive section and a first insulating material arranged between the conductive sections. An optoelectronic semiconductor chip is arranged on a first top side of the first conductive section and electrically connected to a second top side of the second conductive section and a third top side of the third conductive section. The second conductive section and the third conductive section are arranged on opposite sides of the first conductive section. The fourth conductive section is arranged besides the third conductive section. A passive component is arranged electrically connected to the third conductive section and the fourth conductive section. The first insulating material is arranged between the conductive sections in a way that the first conductive section is electrically isolated from the second conductive section, from the third conductive section and from the fourth conductive section, and in a way that the third conductive section is electrically isolated from the second conductive section and from the fourth

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OPTOELECTRONIC PACKAGE**DESCRIPTION**

5 The invention refers to an optoelectronic package and a production method thereof.

Optoelectronic packages may comprise conductive sections which may act as conductors to provide electrical voltage for
10 an optoelectronic semiconductor chip and may also work as heat conducting means to allow heat occurring due to the operation of the optoelectronic semiconductor chip to be guided away from the optoelectronic semiconductor chip.

15 Conductive sections to allow for the electrical contact of the optoelectronic semiconductor chip may be arranged on opposite sides of the optoelectronic semiconductor chip.

Optoelectronic packages may further comprise passive components such as ESD-diodes. These ESD-diodes may prevent electrostatic discharges to reach the optoelectronic semiconductor chip. If the conductive sections for the supplying of the electrical voltage are arranged on opposite sides of the optoelectronic semiconductor chip, a passive component may be
20 arranged on top of one of these conductive sections. To electrically connect the passive component with the conductive section opposite of the optoelectronic semiconductor chip, a long bond wire may be used.

30 One disadvantage of such an optoelectronic package is that the long bond wire has to be placed within an area of the optoelectronic package that may be illuminated by light emitted from the optoelectronic semiconductor chip and therefore decreasing the yield of the optoelectronic package. Another
35 disadvantage of this approach is that arranging such long bond wires is difficult, and for some packages, the bond wire breaks, leading to destroyed optoelectronic components and therefore increased production costs.

An assignment of the invention is to provide an optoelectronic package in which no long bond wire is needed to allow for electric contact of the passive component, therefore increasing the yield and decreasing the production cost of the optoelectronic component.

The solution of these assignments is disclosed in the independent claims of this invention. Preferred embodiments are disclosed in the dependent claims.

An optoelectronic package comprises a carrier with a first conductive section, a second conductive section, a third conductive section and a fourth conductive section. A first insulating material is arranged between the conductive sections. An optoelectronic semiconductor chip is arranged on a first top side of the first conductive section. A first electrical contact of the optoelectronic semiconductor chip is electrically connected to a second top side of the second conductive section. This electrical contact may be established by a first bond wire. A second electrical contact of the optoelectronic semiconductor chip is electrically connected to a third top side of the third conductive section. This connection may be established by a second bond wire. The second conductive section and the third conductive section are arranged on opposite sides of the first conductive section. The fourth conductive section is arranged besides the third conductive section and therefore opposite to the second conductive section as well. A passive component is arranged electrically connected to the third conductive section and the fourth conductive section. The first insulating material is arranged between the conductive sections in a way that the first conductive section is electrically isolated from the second conductive section, from the third conductive section and from the fourth conductive section. Furthermore, the first insulating material is arranged in a way that the third conductive section is electrically isolated from the second conductive section and from the fourth conductive section.

The second conductive section and the fourth conductive section are electrically connected by a conducting material.

5 In one embodiment, a first trench is located within the first top side of the first conductive section and the first insulating material. The first trench extends from the second conductive section to the fourth conductive section. The first trench is partially filled with a second insulating material. A second trench is located within the second insulating material. The second trench extends from the second conductive section to the fourth conductive section and is
10 filled with the conductive material.

The passive component may comprise a bottom contact and may
15 be placed on the third conductive section or the fourth conductive section. A top side contact of the passive component may be connected to the fourth conductive section or the third conductive section respectively, particularly using a bond wire.

20

The conductive material filling the second trench is arranged in a way that the conductive material is not in electrical contact to the first conductive section due to the second insulating material partially filling the first trench. Therefore, the conductive material electrically connects the second conductive section to the fourth conductive section without electrically connecting these two conductive sections to the first conductive section. Therefore, the first contact of the optoelectronic semiconductor chip is electrically connected to the second conductive section and via the conductive material to the fourth conductive section and therefore also connected to the passive component.

30

Therefore, the long bond wire with its disadvantages is no
35 longer needed.

In one embodiment, the conductive sections are lead frame sections of a lead frame. Using this approach with lead frame

sections allows for an easy manufacturing process of the carrier with the lead frame sections embedded within the first insulating material.

5 In one embodiment, the first conductive section, the second conductive section and the third conductive section extend to an underside of the carrier. The underside of the carrier is arranged opposite to the semiconductor chip. Therefore, the first conductive section can be connected to a heat sink al-
10 lowing for heat transfer from the optoelectronic semiconductor chip during operation of the optoelectronic package. The second conductive section and the third conductive section may be used to electrically connect the optoelectronic semiconductor package and therefore the optoelectronic semicon-
15 ductor chip as well.

In one embodiment, the fourth conductive section extends to the underside of the carrier as well, providing another contacting possibility of the optoelectronic package. In one em-
20 bodiment, a bottom side of the fourth conductive section is arranged above the underside of the carrier and covered with the first insulating material. Therefore, the fourth conductive section is not accessible from the underside of the carrier, providing easier handling of the optoelectronic pack-
25 age.

The conductive sections extending to the underside of the carrier may be covered with solder pads to allow for soldering the package to another carrier, particularly a circuit
30 board.

In one embodiment, the passive component is an ESD-diode. Therefore, electrostatic discharges may be guided through the ESD-diode and not through the optoelectronic semiconductor
35 chip, preventing destruction of the optoelectronic semiconductor chip due to electrostatic discharges. The passive component may also be a back-biased diode to prevent destruction

of the optoelectronic semiconductor chip due to inverse electrode currents.

The conductive sections may comprise a metal, particularly copper. The first insulating material may be a plastic, a polymer, an epoxy-resin or a pre-preg. The second insulating material may comprise these materials as well. The first insulating material and the second insulating material may be uniformly formed from the same material.

In one embodiment, the second insulating material comprises epoxy resin or a pre-preg. These materials can be easily placed or printed within the first trench.

In one embodiment, the conductive material is silver paste. Silver paste can be easily placed within the second trench to allow for the electric contact between the second conductive section and the fourth conductive section.

In one embodiment, the optoelectronic semiconductor chip is embedded within a cover layer. The cover layer covers the first top side, the second top side, the third top side, the fourth top side and the passive component. This means that a top side of the carrier, on which the optoelectronic semiconductor chip is placed, is covered with the cover layer and therefore oxidation on the top sides of the conductive sections is reduced, as the conductive sections are covered by the cover layer. If the fourth conductive section does not extend to the underside of the carrier, the fourth conductive section is now fully covered by insulating material and therefore no longer accessible for contacting.

The cover layer may comprise a transparent silicone or may comprise converter particles capable of converting light emitted from the optoelectronic semiconductor chip to another wave length.

In one embodiment, the carrier comprises side walls comprising the first insulating material. The side walls extend to a plane above the optoelectronic semiconductor chip. Therefore, the optoelectronic semiconductor chip is arranged within a cavity formed by the side walls of the carrier. This cavity may be filled with the cover layer.

In one embodiment, the optoelectronic semiconductor chip is electrically connected to the second top side and the third top side using bond wires. The plane formed by the side walls of the carrier is located above the bond wires.

An optoelectronic package may be produced with a method comprising the steps explained in the following. A first conductive section, a second conductive section, a third conductive section and a fourth conductive section are placed. The second conductive section and the third conductive section are arranged on opposite sides of the first conductive section. The fourth conductive section is arranged besides the third conductive section and therefore also opposite to the second conductive section. Within the first conductive section, a first trench is induced. This first trench is later used to connect the second conductive section and the fourth conductive section and is therefore arranged in a way that the first trench extends from an area in the vicinity of the second conductive section to an area in the vicinity of the fourth conductive section. The inducing of the first trench within the first conductive section may be performed before or after the conductive sections are placed. Subsequently, a first insulating material is placed between the conductive sections in a way that the conductive sections are electrically isolated from one another and in a way that the first trench is extended to the second conductive section and the fourth conductive section. As an alternative, the first insulating material may be placed between the conductive sections and the first trench may be induced afterwards.

Subsequently, the first trench is filled with a second insulating material in a way that a second trench extending from the second conductive section to the fourth conductive section is formed. The second trench is not in contact with the first conductive section. Afterwards, a conductive material is filled into the second trench. Therefore, the second conductive section and the fourth conductive section are now electrically connected by the conductive material. Subsequently, an optoelectronic semiconductor chip is arranged on top of the first top side of the first conductive section. Afterwards, the optoelectronic semiconductor chip is electrically connected to the second conductive section and the third conductive section, particularly using bond wires. As a last step, a passive component is placed and electrically connected to the third conductive section and the fourth conductive section.

The conductive sections may be lead frame sections of a lead frame.

In one embodiment, the inducing of the first trench within the first conductive section is executed by using an etching process. Etching of lead frames is a well-known technique, so that the etching of the first conductive section is easily obtainable if the first conductive section is a lead frame section.

In one embodiment, the first insulating material and the second insulating material are identical. To place the first and the second insulating material, a casting mold is arranged around the conductive sections. The casting mold comprises a lug which can be placed within the first trench, partially filling the first trench during a molding process. The first and the second insulating material are then molded to form the carrier, and the parts of the first trench not filled by the lug are filled with the insulating material. After the casting mold is opened, the area where the lug has been during the molding process forms the second trench.

The above described features, properties and advantages of this invention as well as the method of obtaining them, will be more clearly and obviously understandable in the context of the following description of the embodiments, which are explained in more detail in the context of the Figures.

In schematic illustration show

- 10 Fig. 1 a top view of an optoelectronic package;
- Fig. 2 a cross section of the optoelectronic package;
- 15 Figs. 3 and 4 cross sections of a carrier;
- Fig. 5 a cross section of an optoelectronic package; and
- 20 Fig. 6 a cross section of conductive sections within a casting mold before a molding process.

Fig. 1 shows a top view of an optoelectronic package 1 comprising a carrier 2 with a first conductive section 3, a second conductive section 4, a third conductive section 5 and a fourth conductive section 6. A first insulating material 7 is arranged between the conductive sections 3, 4, 5, 6. An optoelectronic semiconductor chip 8 is arranged on a first top side of the first conductive section 3. A first electrical contact 9 of the optoelectronic semiconductor chip 8 is electrically connected to the second conductive section 4. The connection is established with a first bond wire 10. A second electrical contact 11 of the optoelectronic semiconductor chip 8 is electrically connected to the top side of the third conductive section 5 using a second bond wire 12. The second conductive section 4 and the third conductive section 5 are arranged on opposite sides of the first conductive section 3. The fourth conductive section 6 is arranged besides the third

conductive section 5 and therefore also opposite of the second conductive section 4. A passive component 13 is placed on top of the fourth conductive section 6 and connected to the third conductive section 5 using a third bond wire 23. The
5 passive component 13 comprises a bottom contact in direct electrical contact to the fourth conductive section 6. It is also possible that the passive component 13 is placed on top of the third conductive section 5 and connected to the fourth conductive section 6 with a bond wire. The first insulating
10 material 7 is arranged between the conductive sections 3, 4, 5, 6 in a way that the first conductive section 3 is electrically isolated from the second conductive section 4, from the third conductive section 5 and from the fourth conductive section 6 and in a way that the third conductive section 5 is
15 electrically isolated from the second conductive section 4 and from the fourth conductive section 6. A first trench 14 is located within the first top side of the first conductive section 3 and the first insulating material 7 in a way that the first trench 14 extends from the second conductive section 4 to the fourth conductive section 6. The first trench
20 14 is partially filled with a second insulating material 15. A second trench 16 is located within the second insulating material 15. The second trench 16 extends from the second conductive section 4 to the fourth conductive section 6. The second trench 16 is filled with a conductive material 17.
25 Therefore, the conductive material 17 establishes an electrical connection between the second conductive section 4 and the fourth conductive section 6 connecting the passive component 13 with the first electric contact 9 of the optoelectronic semiconductor chip 8 via the first bond wire 10, the
30 second conductive section 4, the conductive material 17 and the fourth conductive section 6.

The conductive material 17 may be arranged differently, particularly not within the second trench 16, but in a trench
35 within the first insulating material 7.

The conductive sections 3, 4, 5, 6 may comprise an electrical conductivity of 10 million Sievert per meter or more. The first conductive section 3 may comprise a heat conductivity of 50 Watt per meter and Kelvin or more. The conductive sections 3, 4, 5, 6 may comprise a metal with the stated electrical conductivity and heat conductivity, particularly copper.

The first insulating material 7 may comprise a plastic, a polymer, an epoxy resin or a pre-preg. The second insulating material 15 may comprise a plastic, a polymer, an epoxy resin or a pre-preg. The first insulating material 7 and the second insulating material 15 may be uniformly formed by the same material.

Fig. 2 shows a cross section of the optoelectronic package 1 of Fig. 1. The cross section extends through the first conductive section 3, the first trench 14, the second trench 16 and the optoelectronic semiconductor chip 8. The optoelectronic semiconductor chip 8 is placed on top of the first conductive section 3. The first conductive section 3 works as a heat sink to provide heat transfer from the optoelectronic semiconductor chip 8 to an underside 18 of the carrier 2. On the top side of the first conductive section 3, a first trench 14 partially filled with the second insulating material 15 is arranged. Within the second insulating material 15, the second trench 16 filled with the conductive material 17 is arranged. The conductive material 17 is electrically isolated from the first conductive section 3. This isolation works due to the second insulating material 15 arranged between the conductive material 17 and the first conductive section 3.

With a dashed line, a cover layer 19 covering the optoelectronic semiconductor chip 8 and the top side of the first conductive section 3 and therefore the second insulating material 15 and the conductive material 17 as well, is indicated. This cover layer 19 may form an optical element or may

comprise converter particles capable of converting a wavelength of radiation emitted from the optoelectronic semiconductor chip 8 to another wavelength.

- 5 In one embodiment, the conductive sections 3, 4, 5, 6 are lead frame sections of a lead frame. With this approach, the carrier 2 may easily be produced.

In one embodiment, the passive component 13 is an ESD-diode.

- 10 In one embodiment, the first insulating material 7 comprises a mold material, such as plastic, epoxy resin or pre-preg. In one embodiment, the second insulating material 15 comprises a plastic, epoxy resin or a pre-preg. In one embodiment, the conductive material 17 is silver paste.

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- Fig. 3 shows a cross section of the carrier 2 of Fig. 1. The cross section of Fig. 3 is perpendicular to the cross section of Fig. 2 and is guided through the first trench 14 and the second trench 16 respectively. The underside 18 of the carrier 2 comprises bottom sides of the first conductive section 3, the second conductive section 4 and the fourth conductive section 6. Oriented behind the fourth conductive section 6 and not shown in Fig. 3, the third conductive section 5 is arranged. Between the second conductive section 4 and the first conductive section 3, the first insulating material 7 is arranged. The first insulating material 7 is arranged between the first conductive section 3 and the fourth conductive section 6 as well. On a top side opposite of the underside 18 of the carrier 2, the first trench 14 partially filled with the second insulating material 15 extends from the second conductive section 4 to the fourth conductive section 6. Within the second insulating material 15, the second trench 16 is arranged and also extends from the second conductive section 4 to the fourth conductive section 6. The trench 16 is filled with the conductive material 17 and therefore electrically connecting the second conductive section 4 to the fourth conductive section 6.
- 20
- 25
- 30
- 35

In the carrier of Fig. 3, all four conductive sections 3, 4, 5, 6 extend to the underside 18 of the carrier and are therefore available for electrically and/or thermally connecting the conductive sections 3, 4, 5, 6.

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Fig. 4 shows another embodiment of the carrier 2 which is similar to the carrier of Fig. 3 except for the differences explained hereafter. The fourth conductive section 6 comprises a bottom side 24 which is arranged above the underside 18 of the carrier 2 and covered with the first insulating material 7. Therefore, the fourth conductive section 6 is not electrically and/or thermally accessible from the underside 18.

10

15 In the embodiment of Figs. 1 to 4, the conductive sections 3, 4, 5, 6 extend to edges of the carrier. It is also possible that the first insulating material 7 is arranged around the edges, forming an insulating edge around the conductive sections 3, 4, 5, 6.

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The conductive sections 3, 4, 5, 6 accessible from the underside 18 of the carrier may comprise solder pads which allow for soldering the package 1 to a carrier, particularly a circuit board.

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Fig. 5 shows a cross section through another embodiment of the invention. The carrier 2 in this embodiment is configured similar to the carrier of Fig. 2, insofar as no differences are described hereafter. The carrier 2 comprises additional first insulating material 7 arranged circumferential around the conductive sections 3, 4, 5, 6, particularly around and therefore on both sides of the first conductive section 3. The insulating material 7 at the edges of the carrier 2 is arranged in a way that the insulating material 7 forms side walls 25. The side walls 25 extend to a plane 26 above the optoelectronic semiconductor chip 8. Due to the side walls 25, a cavity above the optoelectronic semiconductor chip 8 is formed. This cavity is filled with the cover layer 19 up to

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the plane 26. The side walls 25 and therefore the plane 26 may be arranged in a way that the bond wires 10, 12, 23 are arranged below the plane 26 and therefore within the cover layer 19.

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The side walls 25 of the insulating material may be covered with a reflecting material.

10 The side walls 25 may be arranged in a way that the plane 26 is above the bond wires 10, 12, 23 of the package 1. Then, then, the bond wires 10, 12, 23 and the optoelectronic semiconductor chip 8 are arranged within the cavity provided by the side walls 25. If the cavity is filled with the cover layer 19, the cover layer 19 covers the bond wires 10, 12, 23
15 and the optoelectronic semiconductor chip 8.

To produce an optoelectronic package, the conductive sections 3, 4, 5, 6 may be arranged in a way as shown in Fig. 1. Afterwards, the first trench 14 may be induced within the first
20 conductive section 3. Subsequently, the first insulating material 7 may be arranged between the conductive sections 3, 4, 5, 6 in a way that the conductive sections 3, 4, 5, 6 are electrically isolated from one another and in way that the first trench 14 is extended to the second conductive section
25 4 and the fourth conductive section 6. Subsequently, the first trench 14 may be partially filled with a second insulating material 15 in a way that a second trench 16 extending from the second conductive section 4 to the fourth conductive section 6 is formed. The second trench 16 is thereby not in
30 contact with the first conductive section 3. Alternatively, it is possible to fully fill the first trench 14 with the second insulating material 15 and to subsequently form the second trench 16 within the second insulating material 15. The second trench 16 is subsequently filled with the conduc-
35 tive material 17. With this method, the carrier 2 is produced. Subsequently, the optoelectronic semiconductor chip 8 is placed on top of the first top side of the first conductive section 3 and electrically connected to the second con-

ductive section 4 and the third conductive section 5. Afterwards, the passive component 13 is placed and electrically connected to the third conductive section 5 and the fourth conductive section 6.

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Within this method, the inducing of the first trench 14 within the first conductive section 3 may be performed using an etching process.

10 The second conductive material 15 may be printed into the first trench 14.

It is possible that the first insulating material 7 and the second insulating material 15 are identical. In this case, 15 the insulating material 7, 15 may be placed by using a casting mold. The casting mold may comprise a lug which is placed within the first trench during a mold process.

To allow for the carrier 2 of Fig. 4, it is possible to thin 20 the fourth conductive section 6 before the first insulating material 7 is arranged. This thinning step may be performed by an etching process.

Fig. 6 shows a cross section of a casting mold 20 during such 25 a mold process. The casting mold 20 is arranged around the first conductive section 3. The first conductive section 3 comprises a first trench 14. A lug 21 of the casting mold 20 is partially arranged within the first trench 14, leaving a cavity 22 around the lug 21 within the first trench 14. Other 30 cavities 22 are arranged on the left and the right hand side of the first conductive section 3. During a subsequent mold process, insulating material 7, 15 may be placed within the cavities 22 and thus forming a uniform first insulating material around the conductive sections 3, 4, 5, 6 and within the 35 first trench 14.

Although the invention was described and illustrated in more detail using preferred embodiments, the invention is not lim-

ited to these. Variants of the invention may be derived by a person skilled in the art from the described embodiments without leaving the scope of the invention.

REFERENCE NUMERALS

	1	optoelectronic package
	2	carrier
5	3	first conductive section
	4	second conductive section
	5	third conductive section
	6	fourth conductive section
	7	first insulating material
10	8	optoelectronic semiconductor chip
	9	first electrical contact
	10	first bond wire
	11	second electrical contact
	12	second bond wire
15	13	passive component
	14	first trench
	15	second insulating material
	16	second trench
	17	conductive material
20	18	underside of the carrier
	19	cover layer
	20	casting mold
	21	lug
	22	cavity
25	23	third bond wire
	24	bottom side
	25	side wall
	26	plane

CLAIMS

1. An optoelectronic package (1) comprising a carrier (2) with a first conductive section (3), a second conductive section (4), a third conductive section (5) and a fourth conductive section (6) and a first insulating material (7) arranged between the conductive sections (3, 4, 5, 6), wherein an optoelectronic semiconductor chip (8) is arranged on a first top side of the first conductive section (3), wherein a first electrical contact (9) of the optoelectronic semiconductor chip (8) is electrically connected to a second top side of the second conductive section (4), wherein a second electrical contact (11) of the optoelectronic semiconductor chip (8) is electrically connected to a third top side of the third conductive section (5), wherein the second conductive section (4) and the third conductive section (5) are arranged on opposite sides of the first conductive section (3), wherein the fourth conductive section (6) is arranged besides the third conductive section (5), wherein a passive component (13) is arranged electrically connected to the third conductive section (5) and the fourth conductive section (6), wherein the first insulating material (7) is arranged between the conductive sections (3, 4, 5, 6) in a way that the first conductive section (3) is electrically isolated from the second conductive section (4), from the third conductive section (5) and from the fourth conductive section (6), in a way that the third conductive section (5) is electrically isolated from the second conductive section (4) and from the fourth conductive section (6), wherein a conductive material (17) electrically connects the second conductive section (4) and the fourth conductive section (6).
2. The optoelectronic package (1) according to claim 1, wherein a first trench (14) is located within the first top side of the first conductive section (3) and the first insulating material (7), wherein the first trench

(14) extends from the second conductive section (4) to the fourth conductive section (6), wherein the first trench (14) is partially filled with a second insulating material (15), wherein a second trench (16) is located within the second insulating material (15), wherein the second trench (16) extends from the second conductive section (4) to the fourth conductive section (6) and wherein the second trench (16) is filled with the conductive material (17).

3. The optoelectronic package (1) according to claim 1 or 2, wherein the conductive sections (3, 4, 5, 6) are lead frame sections of a lead frame.

4. The optoelectronic package (1) according to claims 1 to 3, wherein the first conductive section (3), the second conductive section (4) and the third conductive section (5) extend to an underside (18) of the carrier (2), wherein the underside (18) of the carrier (2) is arranged opposite to the optoelectronic semiconductor chip (8).

5. The optoelectronic package (1) according to claim 4, wherein the fourth conductive section (6) extends to the underside (18) of the carrier (2).

6. The optoelectronic package (1) according to claim 4, wherein a bottom side of the fourth conductive section (6) is arranged above the underside (18) of the carrier (2) and covered with the first insulating material (7).

7. The optoelectronic package (1) according to claims 1 to 6, wherein the passive component (13) is an ESD-diode.

8. The optoelectronic package (1) according to claims 1 to 7, wherein the second insulating material (15) comprises epoxy resin or a pre-preg.

9. The optoelectronic package (1) according to claims 1 to 8, wherein the conductive material (17) is silver paste.

10. The optoelectronic package (1) according to claims 1 to 9, wherein the optoelectronic semiconductor chip (8) is embedded within a cover layer (19), wherein the cover layer (19) covers the first top side, the second top side, the third top side, the fourth top side and the passive component (13).

11. The optoelectronic package (1) according to claims 1 to 10, wherein the carrier (2) comprises side wall (25)s comprising the first insulating material (7), wherein the side walls (25) extend to a plane above the optoelectronic semiconductor chip (8).

12. A method of production of an optoelectronic package (1), comprising the steps:

- Placing of a first conductive section, a second conductive section (4), a third conductive section (5) and a fourth conductive section (6), wherein the second conductive section (4) and the third conductive section (5) are arranged on opposite sides of the first conductive section (3), wherein the fourth conductive section (6) is arranged besides the third conductive section (5);
- Inducing of a first trench (14) within the first conductive section (3);
- Placing of a first insulating material (7) between the conductive sections (3, 4, 5, 6) in a way that the conductive sections (3, 4, 5, 6) are electrically isolated from one another and in a way that the first trench (14) is extended to the second conductive section (4) and the fourth conductive section (6);
- Partially filling of the first trench (14) with a second insulating material (15) in a way that a second trench (16) extending from the second conductive section (4) to the fourth conductive section (6) is

formed, wherein the second trench (16) is not in contact with the first conductive section (3);

- Filling of the second trench (16) with a conductive material (17);
- 5 - Arranging of an optoelectronic semiconductor chip (8) on top of a first top side of the first conductive section (3);
- Electrically connecting the optoelectronic semiconductor chip (8) to the second conductive section (4)
- 10 and the third conductive section (5);
- Placing of a passive component (13) and electrically connecting the passive component (13) to the third conductive section (5) and the fourth conductive section (6).

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13. The method of claim 12, wherein the inducing of the first trench (14) within the first conductive section (3) is executed by using an etching process.

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14. The method of claims 12 or 13, wherein the second insulating material (15) is printed into the first trench (14).

25

15. The method of claims 12 or 13, wherein the first insulating material (7) and the second insulating material (15) are identical, wherein a casting mold (20) is arranged around the conductive sections (3, 4, 5, 6), wherein the casting mold (20) comprises a lug (21) placed within the first trench (14) during a molding process and wherein

30 the first insulating material (7) and the second material are molded to form a carrier (2).

FIG 1

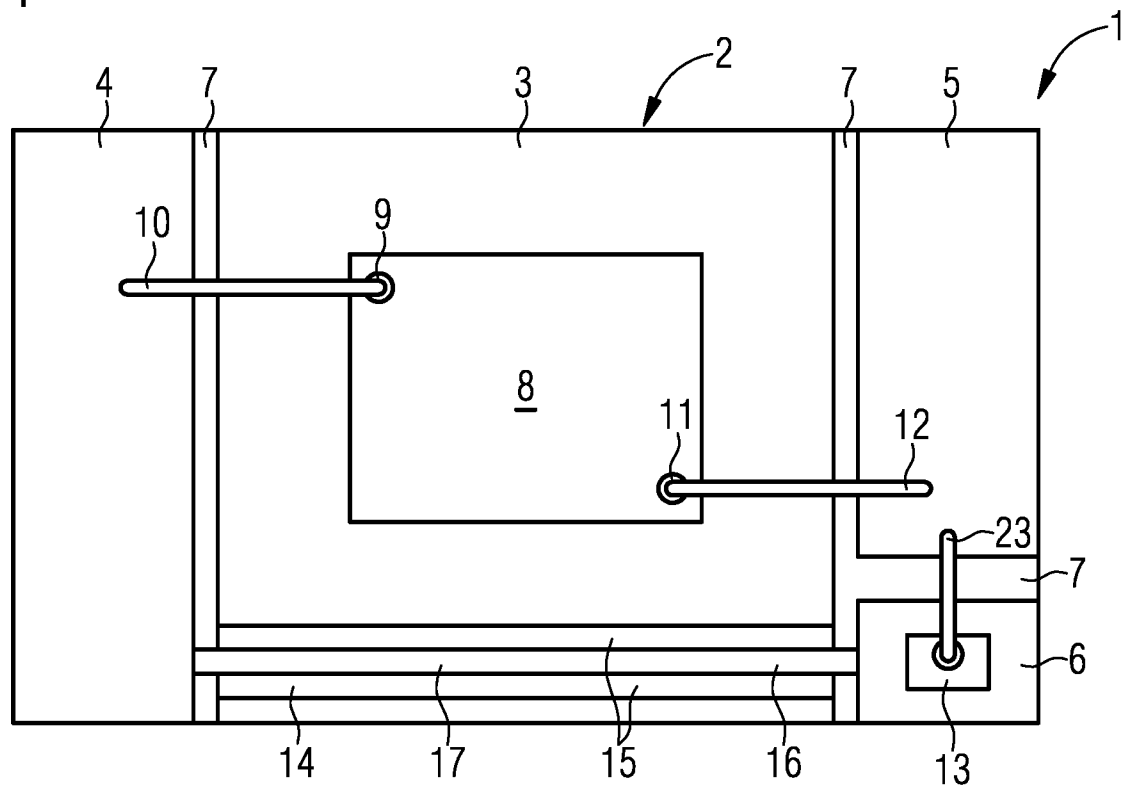


FIG 2

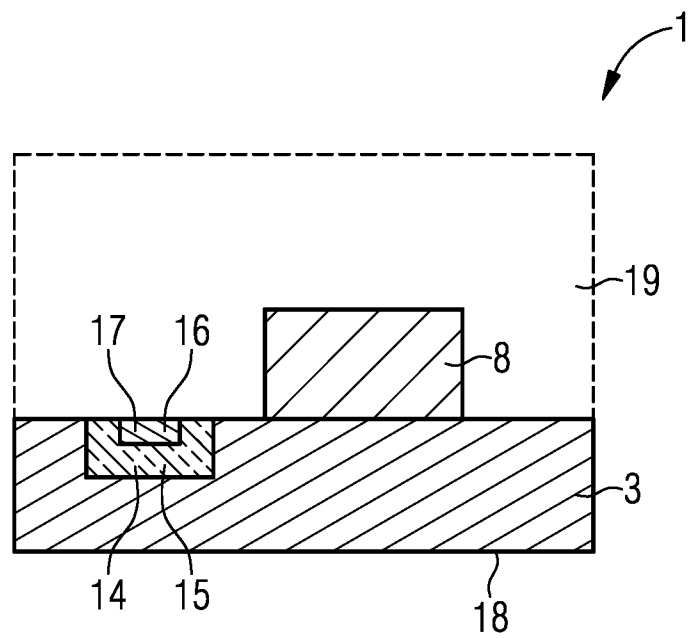


FIG 3

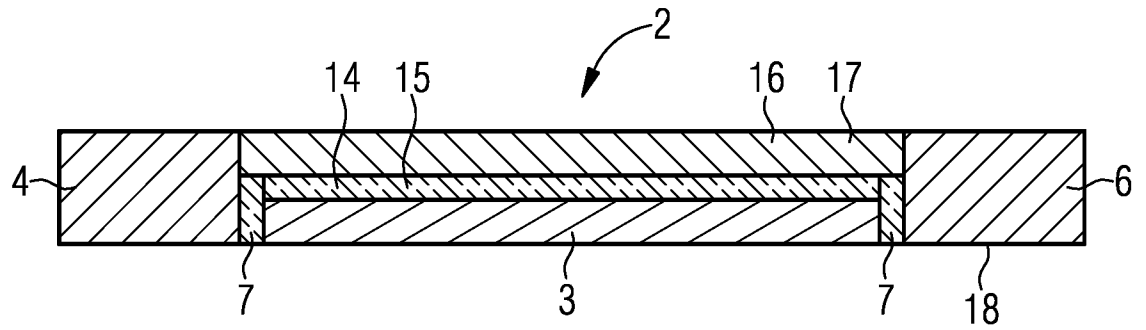


FIG 4

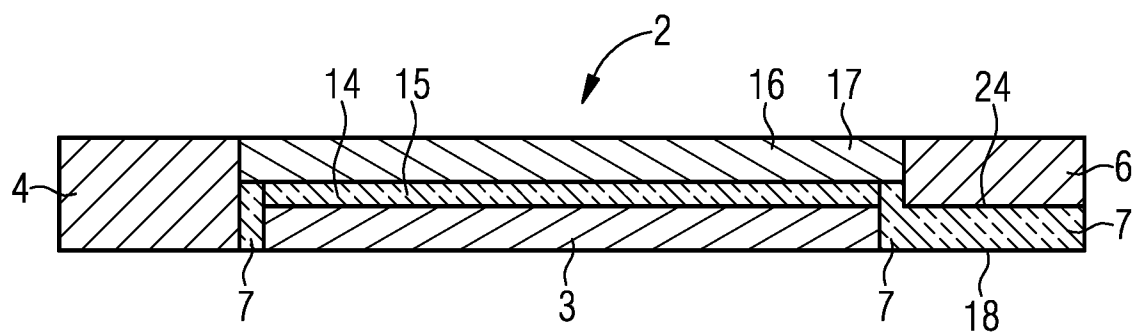


FIG 5

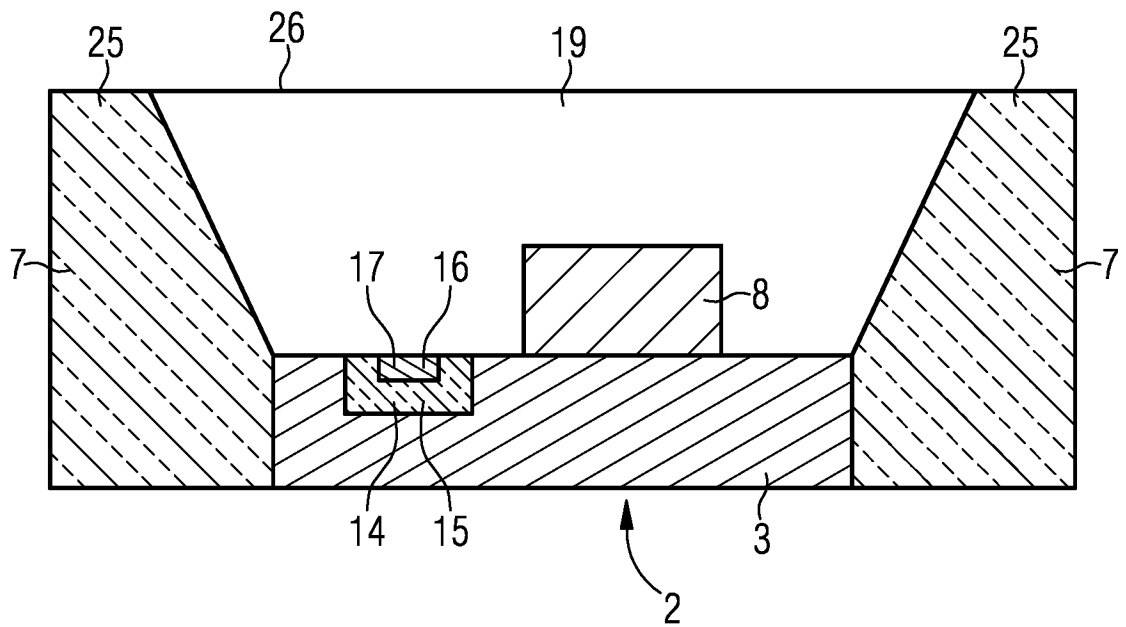
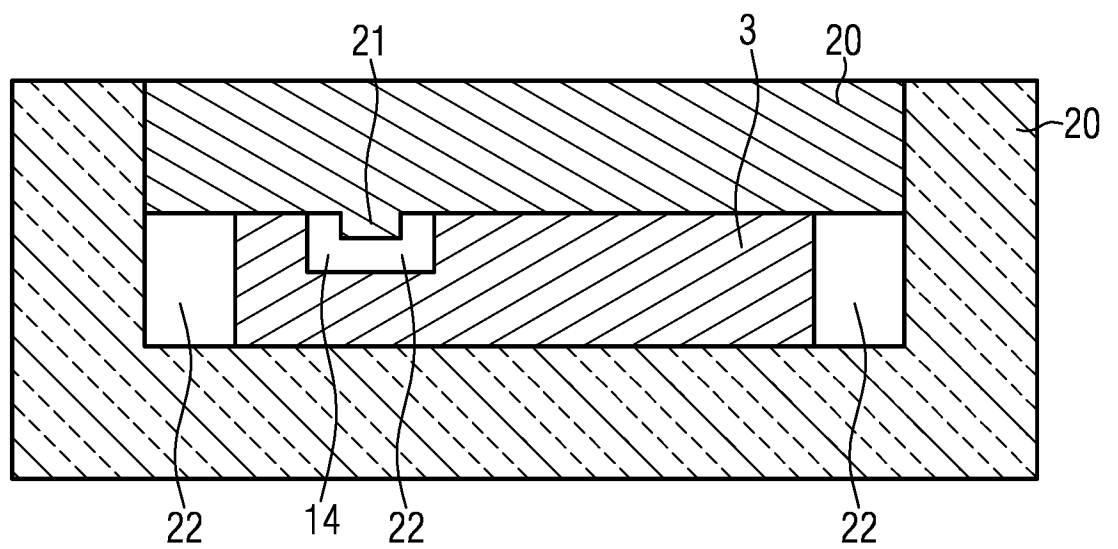


FIG 6



INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2017/083530

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L33/62 H01L25/16
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2007 116034 A (NICHIA KAGAKU KOGYO KK) 10 May 2007 (2007-05-10)	1,7,9-11
A	paragraphs [0012] - [0037], [0043] - [0048]; figure 3	2-6,8, 12-15
X	DE 10 2013 101262 A1 (OSRAM OPTO SEMICONDUCTORS GMBH [DE]) 14 August 2014 (2014-08-14)	1,3-8, 10,11
A	paragraphs [0061] - [0071]; figures 1a-c	2,9, 12-15
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A	paragraphs [0002] - [0043]; figures 4-7	
A	US 2011/127569 A1 (MINESHITA KENTARO [JP]) 2 June 2011 (2011-06-02)	1-15
	paragraphs [0032] - [0047]; figure 9	



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

18 May 2018

Date of mailing of the international search report

28/05/2018

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

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