(54) Title: SWITCHING REGULATOR CONTROL CIRCUIT
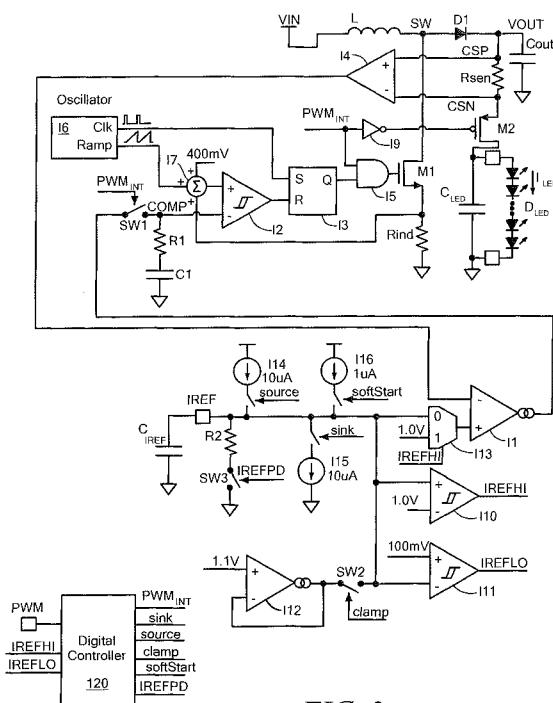
FIG. 3

(57) Abstract: A switching regulator control circuit includes a circuit configured to generate a control signal to control conduction of the regulator switch in response to a reference signal that is ramped to control a rate of change of the regulated output of the regulator and the control signal is gated in response to a PWM signal.

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— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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— *with international search report (Art. 21(3))*

SWITCHING REGULATOR CONTROL CIRCUIT

FIELD

[0001] This disclosure relates generally to switching regulators and, more particularly, to switching regulator control circuits.

BACKGROUND

[0002] Regulators, or converters, including a switch, sometimes referred to as a power switch, for transferring energy from an input, such as an AC or DC voltage or current source, to a regulated output are well known. In some regulators, sometimes referred to as switching regulators, the switch turns on and off to regulate the output. In other regulators, sometimes referred to as linear regulators, the switch operates in its active, or saturation region.

[0003] Common switching regulator configurations include Buck, Boost, Buck-Boost, flyback, SEPIC, Cúk, half bridge, and full bridge to name a few. As is also well known, various control methodologies for controlling conduction of the power switch can be applied to switching regulators, including Pulse Width Modulation (PWM) and Pulse Frequency Modulation (PFM), and for each of these control methodologies, various feedback and feed forward techniques are possible including voltage mode control and current mode control.

[0004] Switching regulators are often used to provide a regulated current to drive an LED load as may include one or multiple LEDs coupled in series and/or parallel. Such switching regulators control the intensity or brightness of the LEDs by selectively dimming the LEDs. In one type of LED dimming, sometimes referred to as analog dimming, the intensity of the LEDs is adjusted by adjusting the regulated LED current. Analog dimming may utilize an error amplifier which is responsive to a reference signal and to a feedback signal proportional to the regulator output to generate an error signal. The error signal is then used to generate a switch control signal to control conduction of the switch and the resulting regulated current. For example, the error signal may be compared to a ramp signal to generate the switch control signal with a duty cycle suitable for regulating the LED current at a desired level.

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[0005] In another type of LED dimming, sometimes referred to as PWM dimming, the intensity of the LEDs is adjusted by turning them off and on in response to a PWM signal at a variable duty cycle with a fixed DC current and frequency (typically 100Hz to 1KHz). The PWM signal may be externally provided or internally generated.

[0006] For LEDs, often PWM dimming is preferred over analog dimming because it minimizes the color shift that can occur when using analog dimming. On the other hand, analog dimming can be less complicated to implement than PWM dimming and PWM dimming pulses the LED current, which can cause visible flicker, audible noise, or EMI issues.

[0007] Figure 1 illustrates a Boost regulator driving an LED load with current mode control that permits both PWM dimming and analog dimming. Analog dimming is achieved by adjusting the reference of the error amplifier (I1) according to the voltage on an external pin. As illustrated in Figure 1, the IREF pin is the external input that can be used to control the error amplifier reference when the voltage is below 1.0V. When the IREF pin voltage is greater than 1.0V, comparator I10 changes the state of analog multiplexer ("mux") I13, running the error amplifier off of the internal reference, which may be more accurate than the voltage supplied on the IREF pin. This feature is sometimes implemented by adding an additional positive input to the error amplifier (I1) that overrides the internal reference when the external signal is less than the internal reference.

[008] For PWM dimming, the user controls the intensity of the LEDs by supplying a digital PWM signal into the PWM pin in Figure 1. As noted, some LED regulators may include the generation of the PWM signal on chip, in which case the user supplies an analog signal that is translated into a PWM duty cycle. Referring also the illustrative waveforms of Figure 2, when the PWM signal is low the SW node is tri-stated with AND gate I5 to cause the LED current to be disabled. In addition, many LED regulators also tri-state the COMP node by introducing switch SW1. This technique allows the control loop to quickly recover when the regulator is re-enabled on the PWM input rising edge. Without switch SW1 the error amplifier (I1) would have to slew the

COMP node to resume operation.

[009]   To provide an even faster LED turn on and turn off, some regulators introduce a

switch in series with the LEDs that is driven by the PWM input as illustrated by M2 in

5   Figure 1. Without M2, the turn off characteristic of the LED current would be exponential

because the output capacitor (Cout) will continue to supply current to the LEDs until the

dynamic resistance in the LEDs discharges Cout enough to turn off the diode component

of the LEDs. The dynamic resistance in the LEDs causes the output capacitor to more

slowly discharge, which results in the soft turn off characteristic and a small voltage ripple

10   across the output capacitor. This soft turn off characteristic makes the relationship

between the PWM pin duty cycle and the LED intensity non-linear, especially at low duty

cycles. On the other hand, turning the LED current instantaneously on and off can cause

EMI issues in some systems, since fast edges produce more harmonic noise further up in

the frequency domain which can be difficult to attenuate. This issue is especially

15   aggravated when there are wires between the LED driver and the LEDs, as shown in

Figure 1, because they act as an antenna for EMI emission.

SUMMARY

[0010] A switching regulator control circuit includes a circuit configured to generate a

20   control signal to control conduction of the regulator switch in response to a reference

signal that is ramped to control a rate of change (i.e., increase and/or decrease) of the

regulated output of the regulator and the control signal is gated in response to a PWM

signal. With this arrangement, in applications in which the regulated output is a regulated

current to drive an LED load, the LED is dimmed in response to a PWM signal, but in

25   conjunction with a controlled ramping the LED current in response to the reference signal.

With the described circuitry and techniques, EMI and other issues caused by

instantaneously turning on and off the switch are alleviated by slowly ramping the LED

current up when turning on the LEDs and down when turning off the LEDs in a well

controlled fashion. For example, the described arrangement reduces control loop

30   overshoot when the LEDs are turned back on after dimming. The described circuits and

methods reduce EMI while allowing for good low duty cycle performance.

[0011] Features may include one or more of the following. The PWM signal may be a

delayed version of an external digital signal. The regulated output may be a current and the reference signal ramped down to control the rate of decrease of the regulated output. The reference signal may be ramped at a rate established in part by a capacitor and/or at a user programmable rate. The reference signal may be provided with a first rate of increase

5   established by a first current source during a first, soft start time interval and with a second, faster rate of increase established by a second current source during a second time interval.

Also described is a method of dimming an LED including providing a PWM signal

10   to a switch to turn the switch on in response to an associated one of a rising edge and a falling edge of the PWM signal and to turn the switch off in response to the other one of the rising edge and the falling edge of the PWM signal. The LED current is ramped down in response to the one of the rising edge or the falling edge or the PWM signal associated with turning off the switch. The LED current may be ramped down by delaying turning

15   off the switch following a transition of the PWM signal. The delay may be established based on the reference signal crossing a predetermined threshold. The reference signal may be ramped at a rate established in part by a capacitor and/or at a user programmable rate. A soft start feature may be implemented. The ramping of the reference signal may be subject to a timeout feature. A second switch, coupled in series with the LED load, may be

20   controlled by a linear regulator in response to the reference signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The foregoing features of the disclosure, as well as the disclosure itself may be more fully understood from the following detailed description of the drawings, in which:

25   [0013] FIG. 1 is a schematic of a conventional switching regulator;

[0014] FIG. 2 shows several illustrative waveforms associated with the regulator of FIG. 1;

[0015] FIG. 3 is a schematic of a switching regulator having a control circuit with a ramp control feature;

30   [0016] FIG. 4 shows several illustrative waveforms associated with the regulator of FIG. 3;

[0017] FIG. 5 shows several additional illustrative waveforms associated with the regulator of FIG. 3;

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[0018] FIG. 6 is a flow diagram showing an illustrative process for timeout of the ramp control feature of FIG. 3;

[0019] FIG. 7 is a schematic of a switching regulator having a control circuit including an alternative ramp control feature; and

[0020] FIG. 8 shows several illustrative waveforms associated with the regulator of FIG. 7.

DETAILED DESCRIPTION

[0021] Referring to Figure 3, a switching regulator, including a switch M1 that conducts to transfer energy from an input source VIN to an output at which a regulated output is provided, further includes a circuit configured to generate a control signal to control conduction of the switch M1 and having a first input responsive to a reference signal (e.g., as provided at IREF), a second input responsive to a feedback signal proportional to the regulated output (e.g., as provided by I4), and an output at which the control signal is provided. The IREF reference signal is ramped to control a rate of change (i.e., increase and/or decrease) of the regulated output (I_{LED}) to implement a ramp control feature. The regulator control circuit further includes a logic circuit I5 coupled to the output of the circuit to gate the control signal in response to a PWM_{INT} signal.

[0022] More particularly, the regulator control circuit includes a current source (I14) and a current sink (I15) coupled to the IREF pin along with an external cap (C_{IREF}) to slowly ramp the IREF voltage. The LED current I_{LED} will slowly ramp with the IREF voltage at a rate established by a current source (I14, I16) or current sink (I15) and the value of the capacitor C_{IREF}, as will be described. The use of external cap C_{IREF} allows the user to program the ramp rate, typically on the order of 10u-100us. In addition to the IREF pin sink and source currents, the regulator also includes a 10%, IREFLO comparator (I11), 110% high impedance driver (I12), IREF pull down (SW3), and digital controller I20 to form the ramp control feature.

[0023] Referring also to the Figure 4 which shows illustrative waveforms associated with Figure 3, the ramp control feature is only active after the rising and falling edges of the PWM input. When the PWM input goes from low to high the IREF pin starts at 0V and

ramps up past the internal reference (here of 1.0V) at a rate determined by the IREF capacitance and the source current of source I14 (T1 to T2). As shown the LED current I_{LED} tracks the IREF pin voltage, slowly ramping up with IREF voltage.

[0024] When the IREF pin crosses the 1.0V internal reference, the comparator I10 trips (i.e., IREFHI=1) causing the mux I13 to toggle to hand off control from the IREF pin to the internal reference of 1.0V. Through the digital controller, the IREFHI signal also disables the source current I14 with the source signal and activates the 110% driver (I12) with the clamp signal. This prevents IREF from continuing to charge well past the 1.0V reference while ensuring that IREF does not drop below the 1.0V reference. The driver (I12) may be implemented with an OTA connected as a buffer to a 1.1V reference that only has a source and sink capability on the order of 10uA. This high impendence drive allows the user to easily override the driver, and pull the reference IREF below 1.0V to set an analog dim reference. Note that when the IREF pin is pulled below the IREFHI comparator I10, the 110% driver I12 is disabled with switch SW2. The system may also be designed to detect the analog dim mode of operation and disable the source and sink currents (I14 and I15) to provide better accuracy.

[0025] As shown in Figures 3 and 4, the PWM_{INT} signal causes the SW operation to resume, LED switch to close (M2), and COMP switch (SW1) to close on the rising edge of PWM_{INT}. However, with the addition of the ramp control feature, the LED current only jumps to the 10% level when the LED switch is closed (M2), due to the discharge characteristic, which will be explained in more detail later. As illustrated after SW, COMP, and LED operation are resumed at time T1, the ramp control feature begins to slowly ramp up the IREF pin resulting in a slow ramp up of the LED current (I_{LED}), LED voltage (VOUT) and the COMP voltage.

[0026] When the PWM input goes from high to low, the clamp is disabled and the IREF pin is discharged with the sink current (I15) starting at the 1.1V reference, and the LED current I_{LED} then begins to ramp down as it tracks the IREF voltage at the 1.0V handoff, as shown in Figure 4. In the prior art the LED switch (M2) would turnoff immediately with the PWM falling edge, but with the ramp control feature, the LED switch M2 must be closed while the LED current I_{LED} is being ramped down. This delay is implemented by

the digital controller (I20) via the PWM$_{INT}$ signal. After the PWM input falling edge, the PWM$_{INT}$ signal remains high until the IREF pin voltage reaches the 10% threshold (i.e., until the IREFLO signal transitions at time T4). Thus, it will be apparent that the PWM$_{INT}$ signal is a delayed version of the signal at the PWM input, where the delay corresponds to the time it takes the voltage at the IREF pin to fall to the 10% threshold (established by comparator I11) on the falling edge of the PWM signal and/or where the delay corresponds to the time it takes the voltage at the IREF pin to exceed the 10% threshold on the rising edge of the PWM signal. On the PWM$_{INT}$ falling edge (T4) the LED switch (M2) is opened, SW operation is halted, and the COMP node is tri-stated with switch SW1. The COMP node is tri-stated to save the control loop operating point while the output is not active so that when operation resumes, the control loop will resume regulation very quickly. In this case the operating point was at the 10% level so operation will also resume at the 10% level.

[0027] As discussed and illustrated in Figure 4, ramp down regulation (i.e., control of the rate of decrease of the LED current I$_{LED}$ via the IREF voltage) is halted when the IREF pin is less than the 10% threshold established by comparator I11. This non-zero threshold is selected because when LED current is ramping down, the system is relying on the LED string to discharge the output capacitor (Cout). As the current gets lower, the ability of the LEDs to discharge the output capacitance is reduced, which may cause the LED current to remain higher than the reference set by the IREF pin. In other words, the regulator in Figure 3 does not have any current sink capability due to diode D1, and therefore the fastest rate the LEDs can be discharge at is set by Cout and the V-I characteristic of the LEDs (D$_{LED}$). Due to the exponential V-I characteristic of LEDs, the rate that Cout discharges at decreases with current. Therefore, the 10% turnoff threshold is selected so that LEDs still have enough sink capability to approximately track the IREF voltage.

[0028] The 10% cutoff is also beneficial for the PWM input rising edge because the regulator cannot regulate LED current down to extremely low levels due to DCM (discontinuous conduction mode) operation and the SW node min duty cycle limit. For that reason, 10% is also selected as a point where the control loop can easily maintain the LED current. As shown in Figure 4, it is desirable that the control is resumed at the same

level (10%) that it was disabled at. This is because the LED voltage (VOUT) has been discharged to that level, and the COMP node is set to that level. Note that the COMP node has a step response on the PWM_{INT} falling and rising edges due to the zero introduced by R1 in the compensation network. Since COMP is slewing, a voltage is

5   developed across R1 that is eliminated when SW1 opens. When the controller is re-enabled the COMP node exhibits some overshoot to slew the inductor current up to the correct level.

[0029] To ensure that the control loop is able to maintain regulation at low IREF pin

10   voltages, it may be desirable to include a light load control technique in the regulator. One light load control technique is pulse skipping which can be implemented by introducing an offset in the current sense signal, as shown in Figure 3 with 400mV node on I7. Therefore, when the COMP voltage drops below the 400mV reference, the SW node will stop switching and resume when the COMP voltage rises above the 400mV

15   pedestal. This technique along with other light load control techniques, such as pulse frequency modulation, constant on time, etc. are well understood by those skilled in the art.

[0030] As illustrated in Figure 4, the 10% IREFLO threshold results in a small 10% step

20   in the LED current when the LED switch (M2) is open and closed. The small magnitude of this step should not cause significant EMI issues. However, the edge rate can be reduced with the addition of a small capacitor in parallel with the LEDs (C_{LED}). This capacitor (C_{LED}) should be at least one to several orders of magnitude smaller than the Cout capacitor.

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[0031] In LED drivers, it is important that the PWM input corresponds directly to the PWM dimming of the LEDs, which is a direct function of the light intensity. In most cases, the IREF ramp is insignificant compared to the LED on time at higher duty cycles, but at low duty cycles meeting this requirement becomes especially difficult and

30   important because the error term is much more significant compared to the LED on time. To meet this requirement with the ramp control feature, the control circuit is designed to provide the area under the curve when ramping up summed with the area when ramping down to be the same area as if the control feature were not present. To achieve this, the

IREF pin source and sink currents (I14 and I15) may be identical, and implemented with good relative accuracy. To cancel the delay introduced by the 10% IREFLO feature, the IREF driver (I12) reference is selected to be 10% above the reference handoff point (1.0V). This method relies on the IREF driver (I12) to be accurate relative to the 1.0V internal reference.

[0032] Depending on the crossover frequency set by the compensation network on the COMP pin, the LED current may not exactly track the IREF pin. This is especially true when a fast LED current slew rate is desired or a large output capacitor (Cout) or compensation capacitor (C1) is used. The current sink and source capability of the error amplifier can also impact the ability of the control loop to track the IREF voltage. In the situation when the LED current lags the IREF ramp rate, the IREF pin slew rate should be adjusted until the desired LED current ramp rate is achieved. Figure 5 illustrates how the system operates with fast LED current slew rates, where the LED current does not exactly track the IREF pin (the expected LED current is shown with dashed lines). As illustrated, the faster ramp and/or slower control loop results in a larger step in the LED current at the PWM_{INT} rising and falling edges.

[0033] To improve the tracking of the LED current with fast IREF pin ramp rates, the error amplifier could be altered to provide faster slewing of the COMP pin as may be achieved by increasing the transconductance of the error amplifier while IREFHI=0, which would in turn increase the crossover frequency of the control loop. In addition, the error amplifier source and sink capability could be altered. Large signal control techniques could also be used to slew the COMP pin when the difference between feedback input and the IREF input becomes too large. Similar to this approach would be to simply ramp the COMP pin in an open loop fashion. These methods may be extended even further when using a digital control loop.

[0034] To ensure that the ramp control feature is robust against faults and does not negatively impact the analog dim or PWM dim features, a ramp control timeout feature or other similar function may be implemented. A timeout feature may be especially important when IREF is ramping down because the ramp control feature delays the tri-stating of the SW node (forcing off M1) and the opening of the LED switch (M2) until

IREF crosses the IREFLO threshold. This delay will result in the PWM input being ignored when the IREF input is driven with a DC signal for analog dimming. A timeout also allows the user to disable the ramp control feature during PWM dimming by driving the IREF pin above the 1.0V reference. This is beneficial if the ramp control feature is

5   not desirable because floating the IREF pin may not fully eliminate the ramp control impact due to the parasitic capacitance on the IREF pin.

[0035] Figure 6 details the operation of an illustrative ramp control timeout feature. The ramp control timeout is only monitored on the PWM falling edge, and the timeout timer

10   starts when the PWM input goes low. The timer is reset when IREF crosses the IREFLO threshold (IREFLO=1), and ramp control operation continues as normal. Otherwise if the timer reaches its final count before IREFLO=1 then the ramp control feature is disabled. The feature remains disabled until the IREF signal is driven below the IREFLO threshold. Ramp control operation will resume naturally when the IREF pin is no longer driven

15   externally because the sink current will ramp the IREF pin down when the PWM signal goes low.

[0036] It will be appreciated that other circuitry and techniques can be used to disable the ramp control feature. For example, other pins may be used directly to disable the ramp

20   control feature, such as a mode pin or even a serial interface.

[0037] During startup and fault conditions, the IREF pin is initialized to a startup state. This is done in Figure 3 with SW3 and the IREFPD signal that comes from the digital controller I20, to pull down on the IREF pin.

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[0038] The ramp control architecture lends itself to including a soft start feature, such as the implementation shown in Figure 3. The reference signal IREF is provided with a first rate of increase (i.e., ramps up at a first rate) established by a current source I16 to implement the soft start feature during a first, soft start time interval and is provided with a

30   second, faster rate of increase established by a current source I14 to implement the ramp control feature during a second time interval. The respective current source control signals (source and soft start) are provided by the digital controller, as shown.

[0039] In the illustrated embodiment, the ramp control feature is implemented with 10uA sink and source currents (I14 and I15), whereas the soft start ramp is implemented with a 1uA current source (I16). This results in a soft start ramp that is 10x slower the ramp control rate. Other ratios may be used. Upon startup, during the first time interval, after the UVLO (under voltage lock out) fault clears or any other faults, the IREF pull down (SW3) is released and the 1uA soft start current (I16) will be used to charge the IREF pin with the ramp control current sources disabled (I14 and I15). During the second time interval, as commences after the IREF pin crosses the IREFHI threshold, the soft start feature will be disabled, and the ramp control driver and current sources will be re-engaged as described above.

[0040] Figure 3 implements the soft start feature by simply ramping the reference of the error amplifier I1. Due to the fact the LEDs will not conduct current until there is a few volts across them, the current sense voltage (CSP-CSN) will remain at zero until VOUT reaches a few volts. As a result, the error amplifier will drive the COMP pin as hard as possible because the 0V current sense voltage (CSP-CSN) is not tracking the soft start ramp. This may result in some overshoot when the LEDs finally do begin to conduct. Fortunately this overshoot will occur at very low LED currents, and at that point the LED current will begin to track the soft start ramp. Other soft start circuits and techniques are also possible. One example is to change the feedback signal of the error amplifier from the current sense amplifier I4 to a resistor divider across VOUT until the LEDs begin to conduct.

[0041] The ramp control feature can also be implemented using other circuitry and/or techniques in addition to or in place of the presented circuitry and techniques. One additional technique is illustrated in Figure 7, which turns the PMOS LED switch (M2) into a linear regulator with the addition of amplifier I21. The reference of the linear regulator (I21 and M2) is the IREF signal. This linear regulator technique does not suffer the limitations of the LED string discharging the output capacitor (Cout) explained earlier because M2 can control the LED current independent of the voltage across Cout. Therefore in Figure 7 the IREFLO threshold has been changed to 5% (50mV) to take advantage of this higher performance technique. In addition, the reference for driver I12 has been changed to 105% (1.05V) to properly cancel out the delay. Note that it is still

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beneficial to have a non-zero IREFLO threshold to be tolerant of errors in the circuitry and relax the design requirements of the linear regulator.

[0042] When adding an additional control loop to regulate the LED current, as done in Figure 7, it is important that the multiple loops do not negatively interact with one another. In this case, the switching regulator must simply supply enough current to support the current need of linear regulator I21. As shown in Figure 7 and 8, this requirement is met by tri-stating COMP pin with the IREFHI signal so that the switching regulator continues to run as if the LEDs were continuing to sink the full regulation current. As a result, when ramping down the LED current, the output voltage (VOUT) will rise up as the output capacitor is charged with the excess current, as illustrated in Figure 8. Then when the LED current is ramped up, the switching regulator disabled, by shifting the PWM_{INT} signal as shown in Figure 8, so that excess charge in the output capacitor (Cout) is depleted as the LED current is ramped up. When the IREF voltage crosses the 1.0V handoff point, the linear regulator will naturally drive the LED switch (M2) into the triode region because the switching regulator will take over regulation by supplying less current than demanded by the linear regulator.

[0043] To ensure the design is robust against errors, it may be beneficial to add an offset between the error amplifier (I1) reference and the linear regulator to ensure the switching regulator provides enough current for all cases. Other techniques may also be used to ensure the switching regulator provides enough current to the linear regulator, such as multiplexing the error amplifier feedback from the current sense amplifier (I4) to a resistor divider monitoring the output voltage to regulator VOUT at a level just above the regulation point.

[0044] All references cited herein are hereby incorporated herein by reference in their entirety.

[0045] Having described preferred embodiments, it will now become apparent to one of ordinary skill in the art that other embodiments incorporating their concepts may be used. It will be appreciated that the proposed ramp control circuitry and techniques can be applied any linear or switching regulator topology including but not limited to Buck,

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Boost, Buck-Boost, SEPIC, Cúk, half-bridge, full bridge, and linear regulators. Furthermore the described circuitry and techniques are not limited to mixed signal systems but can be applied using digital, analog, or software methods, such as a digital to analog converter or charge pump to replace the current sources and external capacitor on

5   the IREF pin. The rate of the IREF pin could be defined by other parameters such as input voltage, output voltage, light intensity, or any other fixed or variable parameter. The ramp up and down characteristic does not need to be linear; for example, it can have an exponential characteristic or even a discontinuity in the shape if desired. The described circuitry and techniques can be implemented with any control loop including current

10   mode control (as discussed and illustrated), voltage mode control, constant on time control, constant off time control, or any other analog and/or digital control scheme. In addition, the proposed circuitry and techniques are not limited to application in regulators that regulate current, and can be applied to regulators that instead regulate voltage, power, or other parameter. Furthermore, it will be appreciated that a regulator of the type

15   described herein may operate in different dimming modes in conjunction and/or in addition to the dimming described herein that utilizes the ramp control feature.

[0046] It is felt therefore that these embodiments should not be limited to disclosed embodiments, but rather should be limited only by the spirit and scope of the appended

20   claims.

CLAIMS

1.   A switching regulator control circuit for controlling a switching regulator comprising a switch that conducts to transfer energy from an input source to an output at which a regulated output is provided, the switching regulator control circuit comprising:

        a circuit configured to generate a control signal to control conduction of the switch
5   and having a first input responsive to a reference signal, a second input responsive to a feedback signal proportional to the regulated output, and an output at which the control signal is provided, wherein the reference signal is ramped to control a rate of change of the regulated output; and

        a logic circuit coupled to the output of the circuit to gate the control signal in
10   response to a PWM signal.

2.   The switching regulator control circuit of claim 1 wherein the regulated output is a current and the reference signal is ramped down to control the rate of decrease of the regulated output.

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3.   The switching regulator control circuit of claim 1 wherein the PWM signal is a delayed version of an external digital signal.

4.   The switching regulator control circuit of claim 1 wherein the reference signal is
20   ramped at a rate established in part by a capacitor.

5.   The switching regulator control circuit of claim 1 wherein the reference signal is ramped at a user programmable rate.

25   6.   The switching regulator control circuit of claim 5 wherein the reference signal is ramped in accordance with a user selected capacitance.

7.   The switching regulator control circuit of claim 1 wherein the reference signal is provided with a first rate of increase established by a first current source during a first, soft
30   start time interval and is provided with a second, faster rate of increase established by a second current source during a second time interval.

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8.   In a switching regulator adapted to provide an LED current to drive an LED, a method of dimming the LED comprising:

providing a PWM signal to a switch to turn the switch on in response to an associated one of a rising edge and a falling edge of the PWM signal and to turn the switch off in response to the other one of the rising edge and the falling edge of the PWM signal; and

ramping down the LED current in response to the one of the rising edge or the falling edge of the PWM signal associated with turning the switch off.

9.   The method of claim 8 wherein ramping down the LED current comprises delaying turning off the switch for a time interval following the one of the rising edge or the falling edge of the PWM signal.

10.   The method of claim 8 wherein ramping down the LED current comprises delaying turning off a second switch coupled in series with the LED for a time interval following the one of the rising edge or the falling edge of the PWM signal.

11.   The method of claim 10 further comprising providing a second control signal to the second switch to operate the second switch as a linear regulator.

12.   The method of claim 8 wherein the LED current is ramped down at a user programmable rate.

13.   The method of claim 12 wherein the rate at which the LED current is ramped down is selectable in accordance with selection of a capacitance.

14.   The method of claim 8 further comprising stopping ramping down the LED current in response to a timeout condition.

15.   The method of claim 8 wherein the timeout condition comprises a reference signal falling to below a predetermined voltage level.

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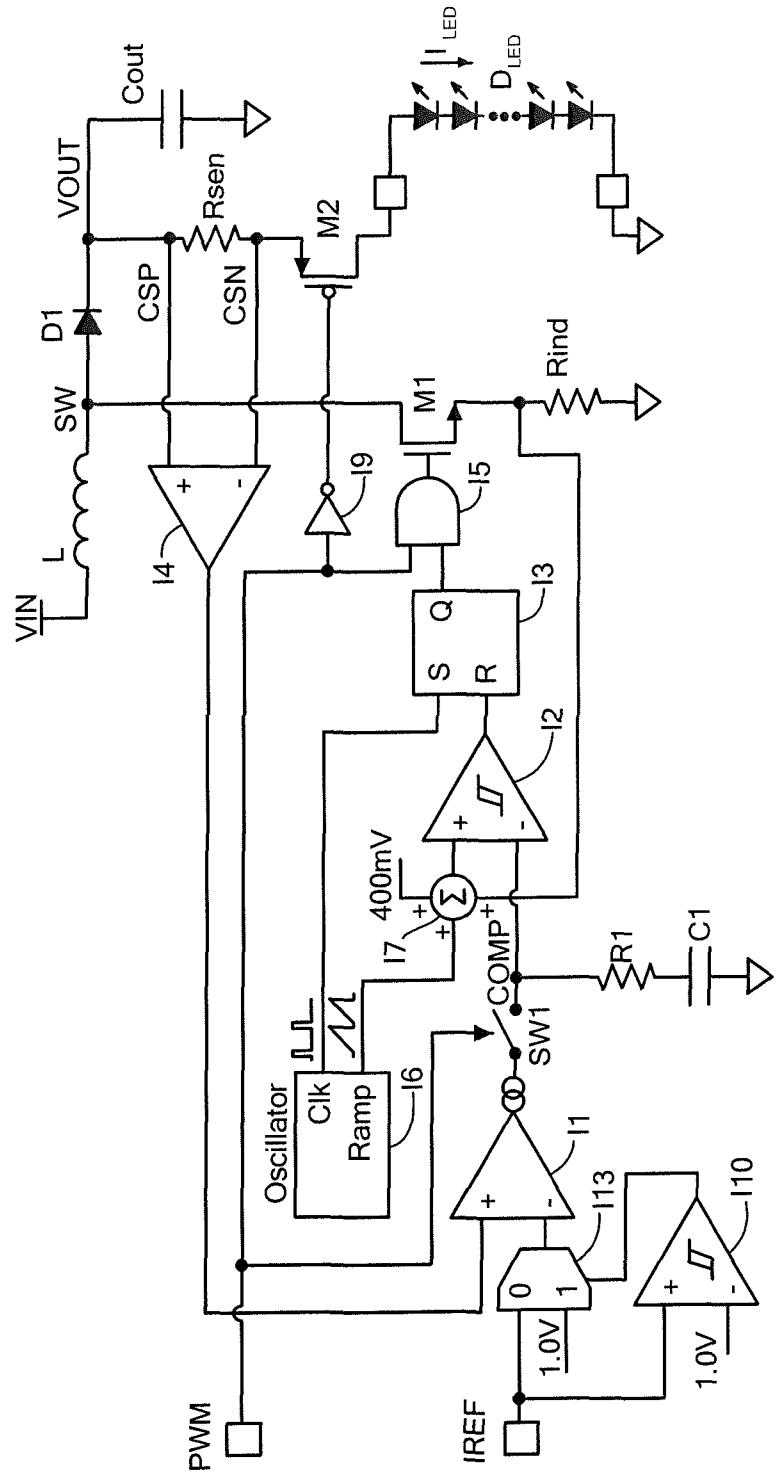
FIG. 1
PRIOR ART

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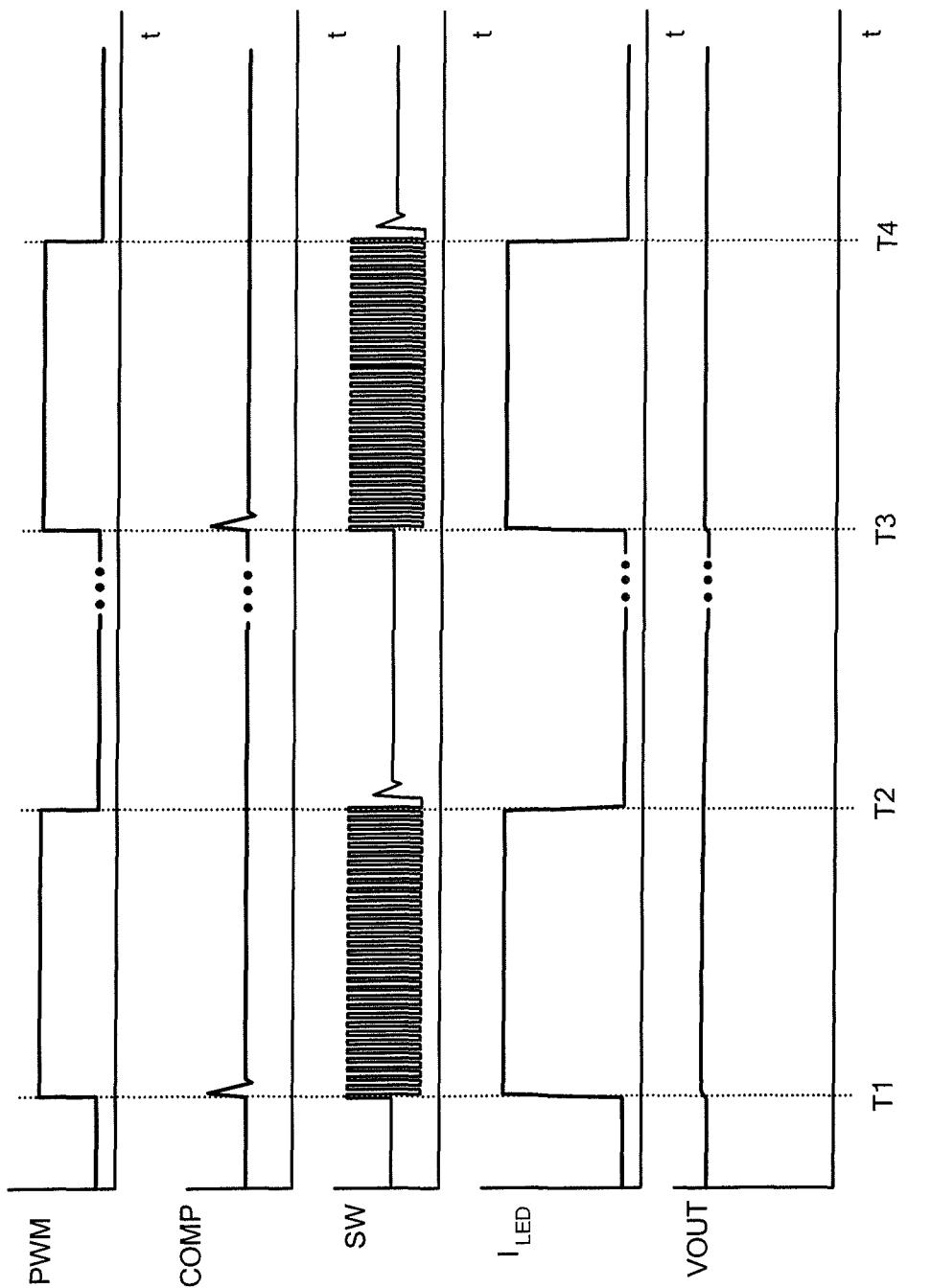
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PRIOR ART

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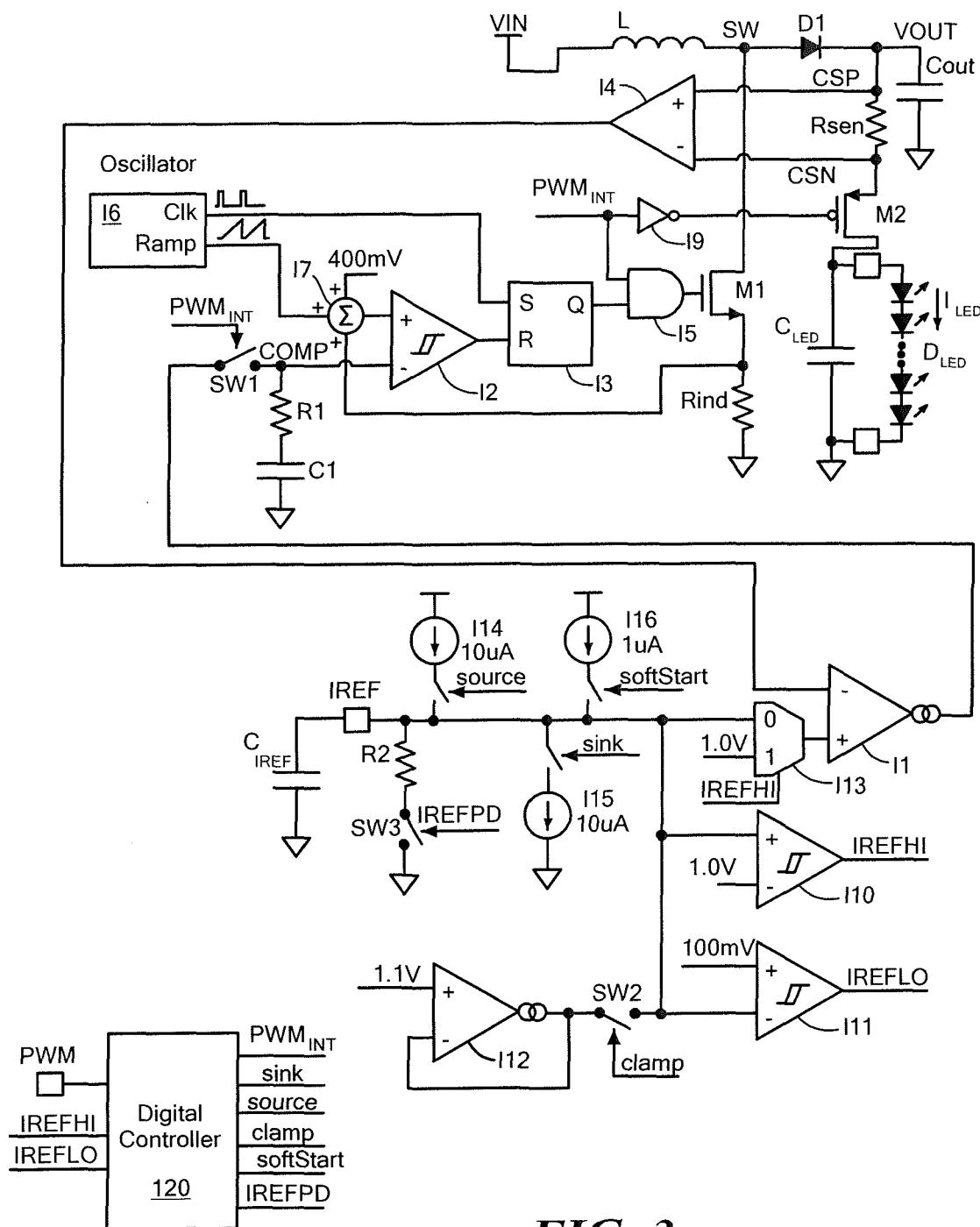
FIG. 3

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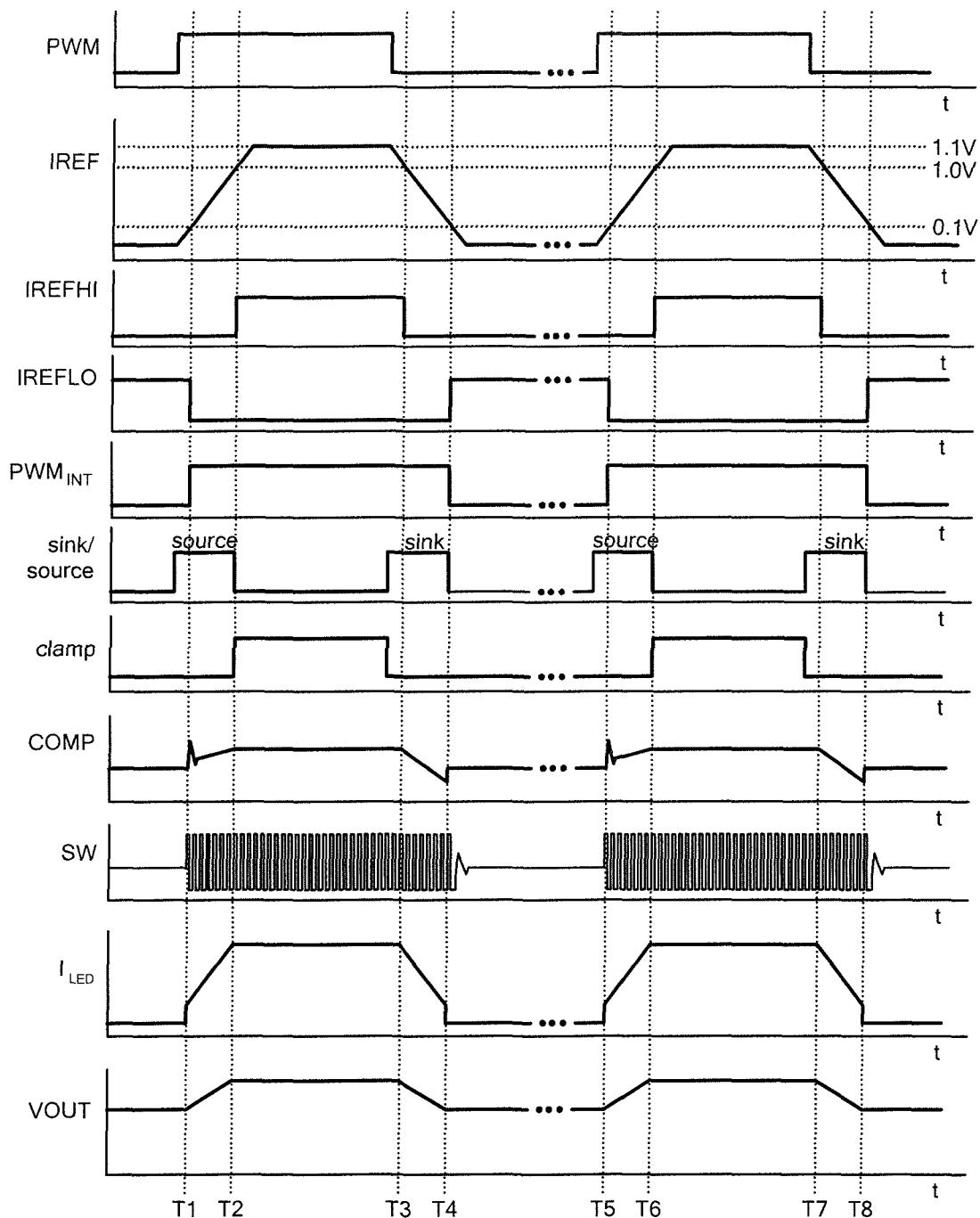
FIG. 4

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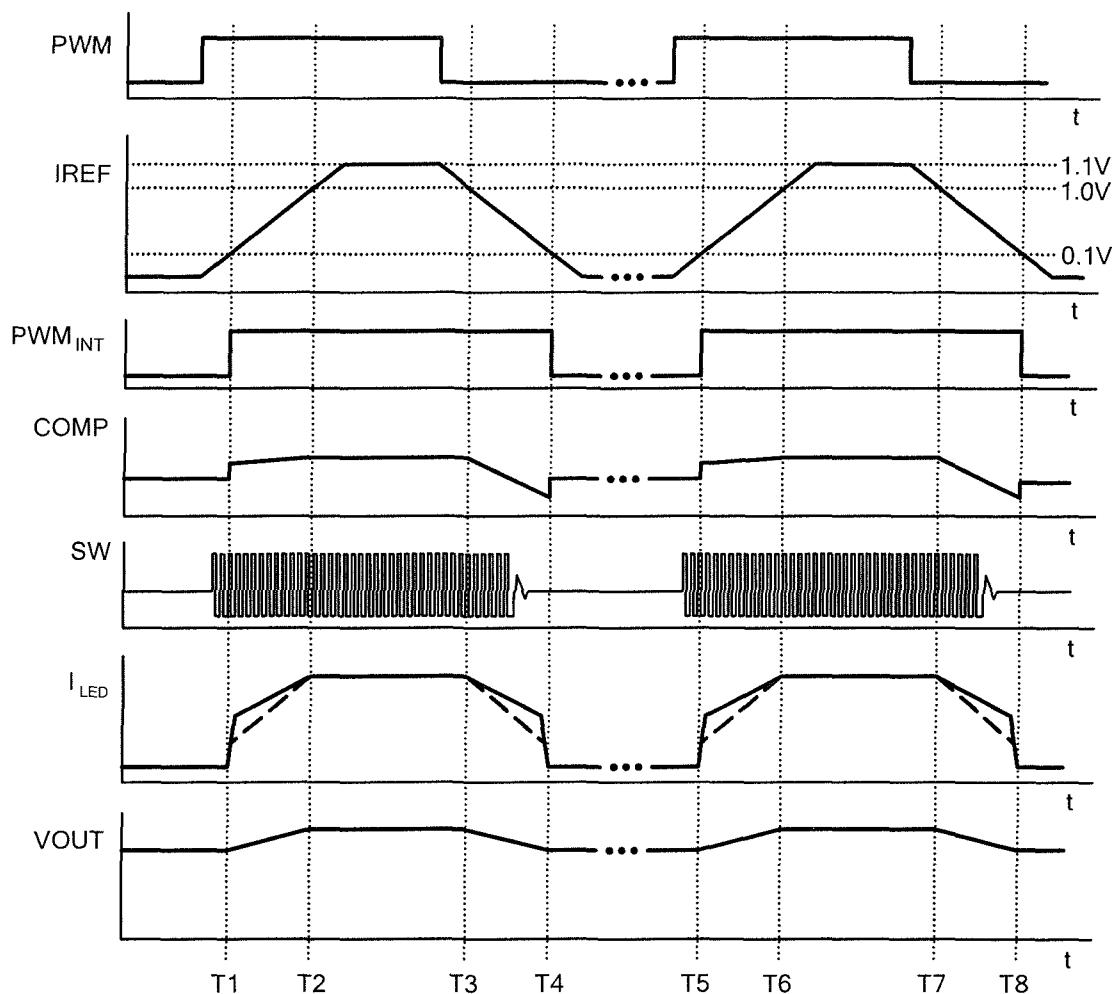
FIG. 5

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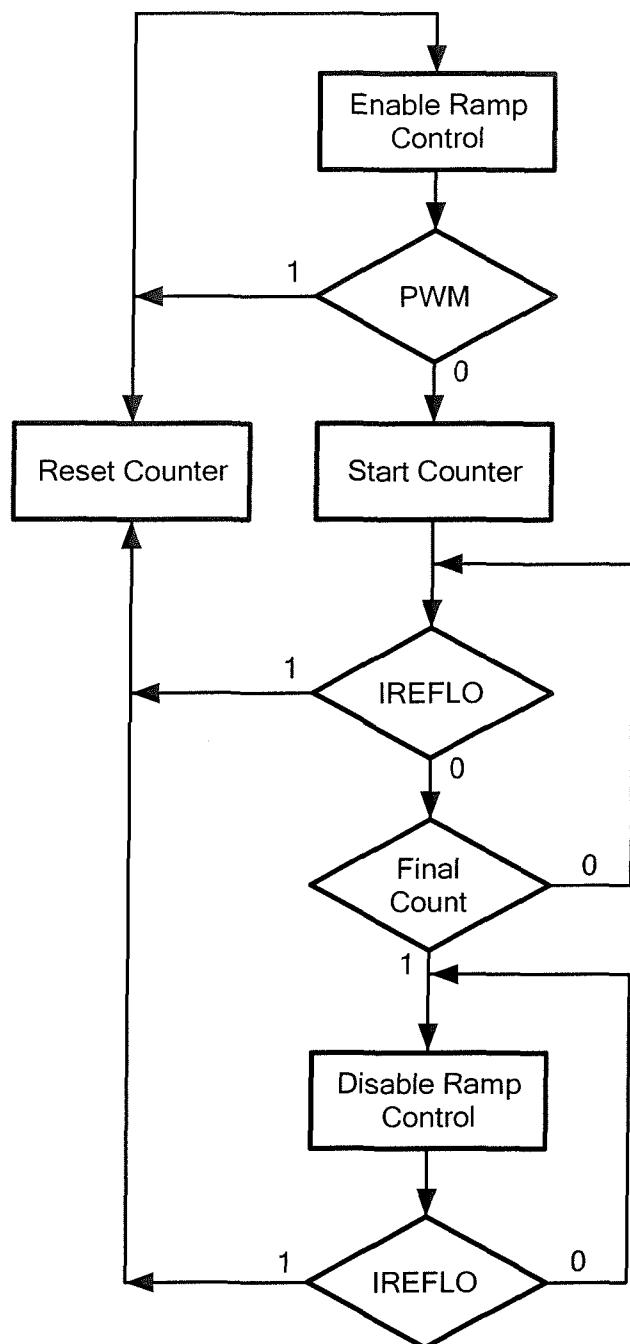
FIG. 6

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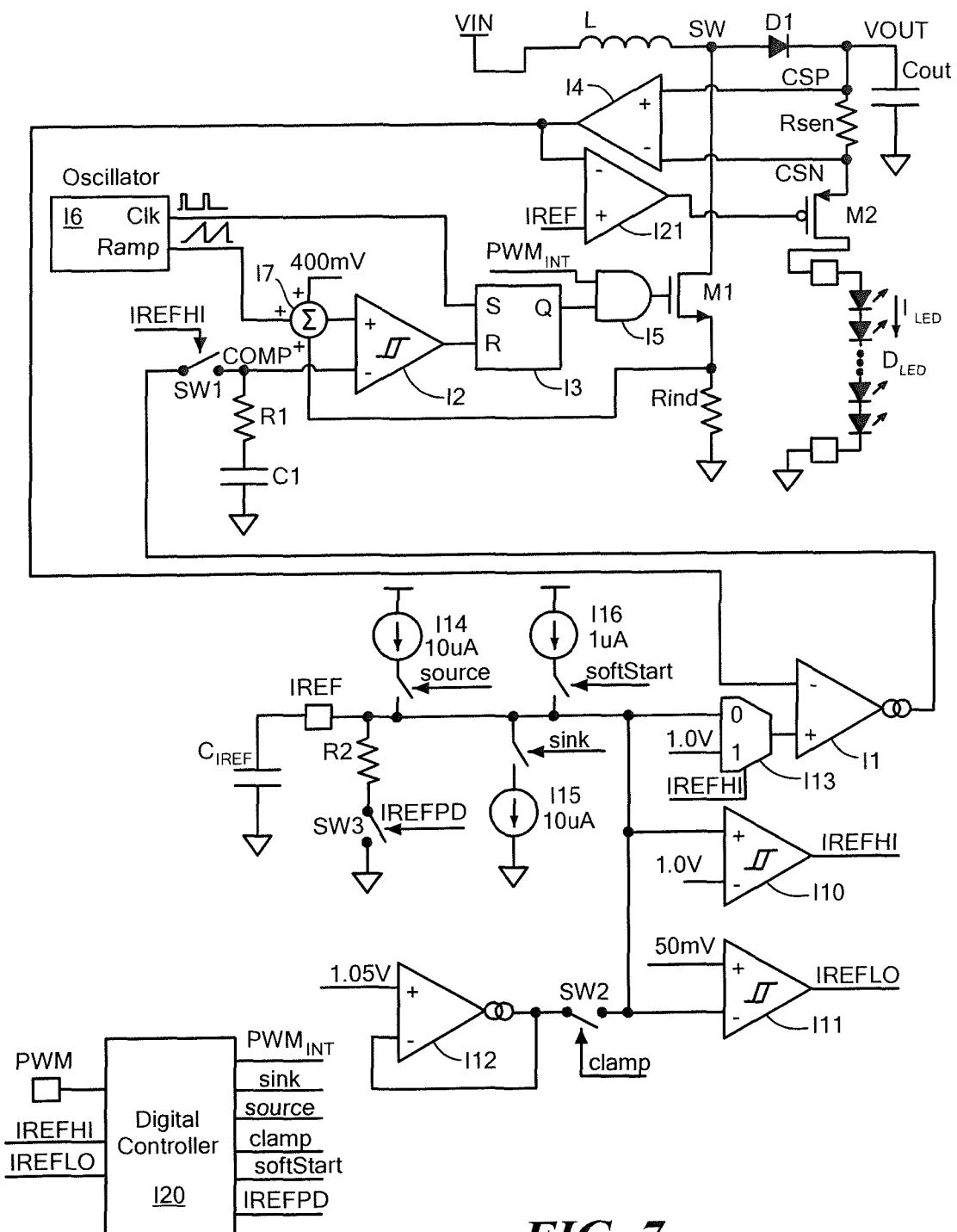
FIG. 7

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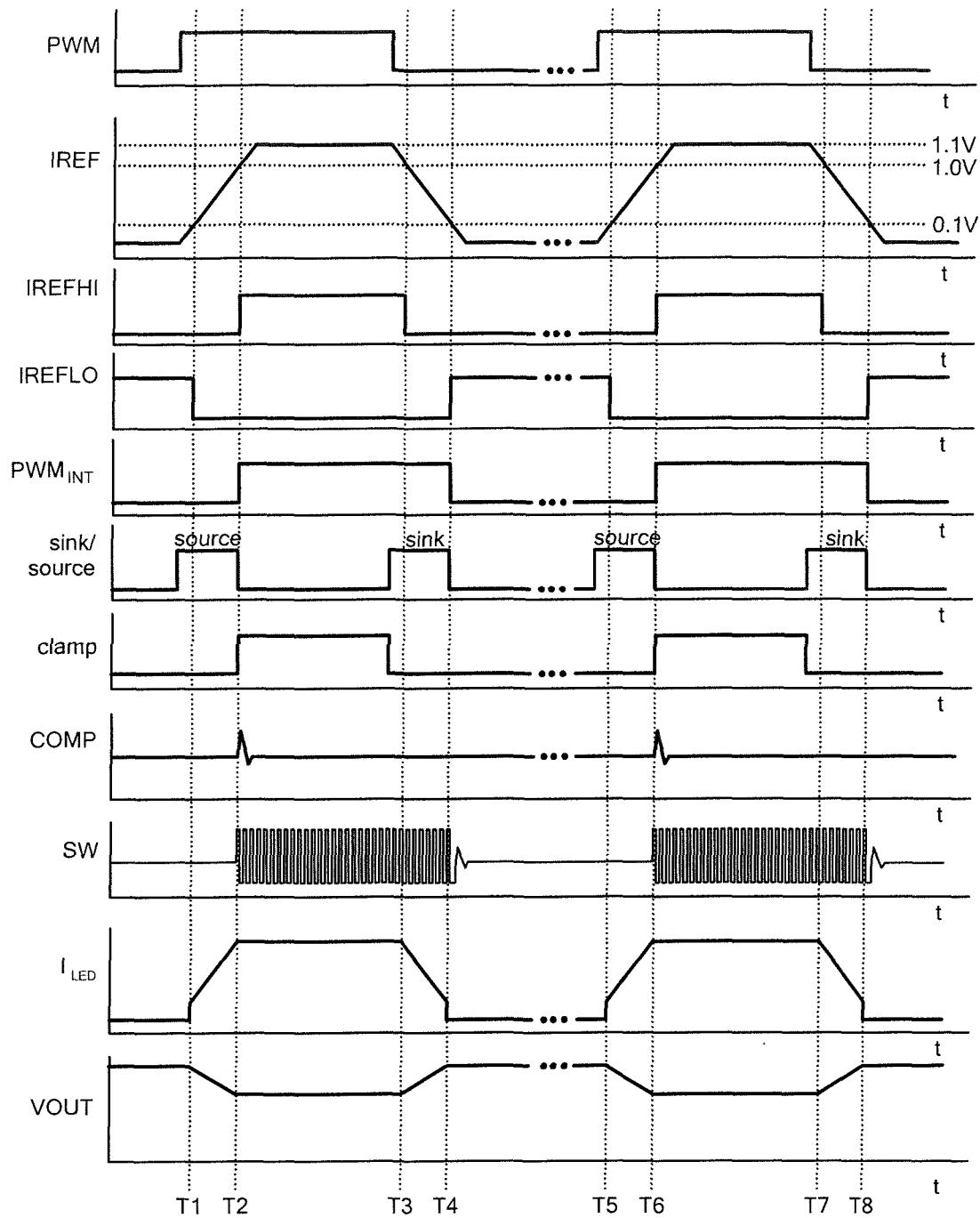
FIG. 8

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

INV. H05B33/08
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H05B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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Y	paragraph [0024] - paragraph [0040]; figures 1,2 -----	2-7,9-15
X	US 2010/289424 A1 (CHANG RONALD [US] ET AL) 18 November 2010 (2010-11-18)	1,8
Y	paragraph [0001] - paragraph [0077]; figures 2-5 -----	2-7,9-15
Y	EP 2 723 146 A1 (LINEAR TECHN INC [US]) 23 April 2014 (2014-04-23)	4,7
A	paragraph [0024] - paragraph [0029]; figures 4-7 -----	1,8
A	US 2008/084196 A1 (LACOMBE DAVID K [US] ET AL) 10 April 2008 (2008-04-10) paragraph [0005] - paragraph [0036] -----	1-15

| | Further documents are listed in the continuation of Box C. | [X] | See patent family annex. |

Date of the actual completion of the international search	Date of mailing of the international search report
13 August 2015	20/08/2015

| Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016 | Authorized officer Henderson, Richard |

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Form PCT/ISA/210 (second sheet) (April 2005)

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