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— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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(54) **Title**: EMBEDDED SIGE PROCESS FOR MULTI-THRESHOLD PMOS TRANSISTORS

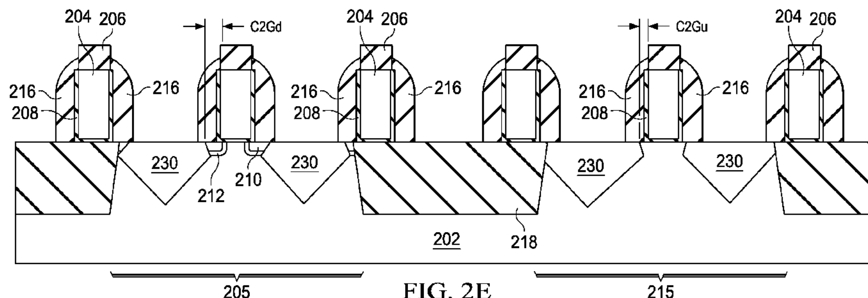

FIG. 2E

(57) **Abstract**: In described examples of an integrated circuit and method having a first PMOS transistor (205) with extension (210) and pocket implants (212) and with SiGe source and drains (230) and having a second PMOS transistor (215) without extension and without pocket implants and with SiGe source and drains (230), the distance (C2Gd) from the SiGe source and drains (230) to the gate of the first PMOS transistor (205) is greater than the distance (C2Gu) from the SiGe source and drains (230) to the gate of the second PMOS transistor (215), and the turn on voltage of the first PMOS transistor (205) is at least 50 mV higher than the turn on voltage of the second PMOS transistor (215).

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EMBEDDED SIGE PROCESS FOR MULTI-THRESHOLD PMOS TRANSISTORS

[0001] This relates generally to integrated circuits, and more particularly to PMOS transistors with silicon germanium source and drain diffusions.

BACKGROUND

[0002] Techniques to embed SiGe source/drain regions have been used for CMOS devices to increase compressive stress in the channel region of PMOS devices to improve device performance by improving hole mobility. In such process flows, following gate stack and source/drain extension formation, a cavity is formed in the source/drain regions of the PMOS device. Cavity formation is generally accomplished by a multi-step dry etch process, followed by a wet etch process.

[0003] The first dry etch step is a first anisotropic dry etch used to etch through a deposited hardmask layer (e.g., silicon nitride) to begin etching of a cavity in the substrate (e.g., silicon), followed by an isotropic dry lateral etch (dry lateral etch) that expands the cavity including laterally toward the PMOS transistor channel, followed by a second anisotropic dry etch to define the bottom wall of the cavity.

[0004] The multi-step dry etch is generally followed by a wet crystallographic etch, which forms a "diamond-shaped" cavity. The wet etchant for the crystallographic etch has crystal orientation selectivity to the substrate material, such as an etchant comprising tetramethyl ammonium hydroxide (TMAH), which is used to etch the substrate beginning with the U-shaped recesses provided by the multi-step dry etch processing. During the wet crystallographic etching process, the etch rate of the <111> crystal orientation is less than that of other crystal orientations such as <100>. As a result, the U-shaped recess becomes a diamond-shaped recess.

[0005] FIG. 1A is a depiction showing an in-process PMOS transistor just prior to the formation of SiGe (silicon germanium) source and drain diffusions. The PMOS transistor is shown having a gate stack including a gate electrode 104 on a substrate 102 such as silicon, with a sidewall spacer 116 on the walls of the gate stack and a hard mask layer (e.g., silicon nitride) 106 on the gate electrode 104. P-type source and drain extensions 110 and n-type halo or pockets 112 are formed self-aligned to an offset spacer 108 dielectric, such as silicon dioxide or

silicon nitride. The p-type extensions 110 electrically connect the PMOS transistor channel to the deep source drains to which contacts are formed. The n-type pockets 112 increase the doping in the PMOS transistor channel 114 and set the PMOS transistor turn on voltage (vtp).

[0006] FIG. 1B shows the PMOS transistor immediately after completing multi-step dry cavity etch processing. Typically, the first dry etch step is a first anisotropic dry etch used to etch through a deposited hardmask layer (eg. silicon nitride) and to begin etching a cavity into the substrate 102. This is followed by an isotropic dry lateral etch step that expands the cavity laterally 118 toward the PMOS transistor channel 114. This etch is typically followed by a second anisotropic dry etch to define the bottom wall of the cavity 120.

[0007] FIG. 1C shows a depiction of an in-process PMOS transistor after the wet crystallographic cavity etch forms diamond-shaped recesses 122. The C2G (cavity to gate space) is the distance from the edge of the cavity to the edge of the transistor gate.

[0008] Following the wet crystallographic etch, boron doped SiGe is grown epitaxially in the diamond-shaped recesses to form the PMOS embedded SiGe source/drain regions. The embedded SiGe regions are spaced close enough to the outer edge of the PMOS transistor channel, so that they impart a high amount of compressive stress to the channel. However, the SiGe regions are not too close to the outer edge of the PMOS transistor channel, so that dopant diffusion from the in-situ doping in the SiGe runs into the PMOS channel and alters the PMOS threshold voltage (vtp).

[0009] Integrated circuits often require PMOS transistors with a low turn on voltage (LVPMOS) for high performance circuits in addition to the core PMOS transistors. Typically, one pattern and implantation step is used to set the vt of the core PMOS transistors, and a second pattern and implantation step is used to set the lower vtp of the LVPMOS transistors.

SUMMARY

[0010] In described examples, an integrated circuit is formed with a first PMOS transistor with extension and pocket implants and with SiGe source and drains and with a second PMOS transistor without extension and without pocket implants and with SiGe source and drains. The distance from the SiGe source and drains to the gate of the first PMOS transistor is greater than the distance from the SiGe source and drains to the gate of the second PMOS transistor. The turn on voltage of the first PMOS transistor is higher than the turn on voltage of the second PMOS transistor. Described examples include a method for forming an integrated circuit with a

first PMOS transistor with extension and pocket implants and with SiGe source and drains and with a second PMOS transistor without extension and without pocket implants and with SiGe source and drains. The distance from the SiGe source and drains to the gate of the first PMOS transistor is greater than the distance from the SiGe source and drains to the gate of the second PMOS transistor, and the turn on voltage of the first PMOS transistor is higher than the turn on voltage of the second PMOS transistor

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] FIG. 1A-1C (prior art) are cross-sections of the formation of SiGe source and drains on a PMOS transistor.

[0012] FIG. 2A through FIG. 2E are cross sections of an integrated circuit with an embodiment low voltage PMOS transistor depicted in successive stages of fabrication.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0013] The figures are not drawn to scale, and they are provided merely to illustrate example embodiments. Several aspects are described below with reference to example applications for illustration. Numerous specific details, relationships and methods are set forth to provide an understanding. One skilled in the relevant art, however, will readily recognize that embodiments can be practiced without one or more of the specific details or with other methods. In other instances, well-known structures or operations are not shown in detail to avoid obscuring. Some acts may occur in different orders and/or concurrently with other acts or events. Furthermore, not all illustrated acts or events are required to implement a methodology.

[0014] For the purposes of this description, the term "C2Gd" refers to the SiGe cavity to gate space for a PMOS transistor with extension and pocket doping. The term "C2Gu" refers to the SiGe cavity to gate space for a LVPMOS transistor without extension and pocket doping (undoped).

[0015] FIG. 2E shows a portion of an integrated circuit with a core PMOS 205 and low voltage PMOS (LVPMOS) 215 transistor with SiGe source and drains formed according to embodiments. The LVPMOS transistor 215 with a lower vtp is formed with no additional lithography or implantation steps. The core PMOS transistor 205 has source and drain extensions 210 and pockets 212. The LVPMOS transistor 215 does not have source and drain extensions and does not have pockets. Also, the SiGe cavity to gate space (C2Gd) on the core PMOS transistor is greater than the SiGe cavity to gate space (C2Gu) of the LVPMOS transistor.

The lack of pocket doping and the smaller SiGe cavity to gate space on the LVPMOS transistor results in a transistor with a lower turn on voltage. The smaller cavity SiGe to gate space on the LVPMOS transistor also enables the source and drain diffusions of the LVPMOS transistor to electrically connect to the transistor channel without increased series resistance.

[0016] A method for forming a core PMOS transistor and a LVPMOS transistor with SiGe source and drain diffusions using only one extension pattern and implantation step is illustrated in steps in an integrated circuit manufacturing flow depicted in FIGS. 2A through 2E.

[0017] FIG. 2A shows a cross section through PMOS transistor gates 204 in an integrated circuit. PMOS transistor gates 204 with a dielectric capping layer 206 are formed on an n-type substrate 202. The n-type substrate may be an nwell formed in a p-type substrate. Shallow trench isolation (STI) 218 electrically isolates the core PMOS transistor 205 from the LVPMOS transistor 215. A core PMOS extension photoresist pattern 224 is formed on the integrated circuit blocking the extension implant 226 and the pocket implant 228 from the LVPMOS transistor 215 and opening the core PMOS transistor 205 to the extension 226 and pocket 228 implants. The p-type extension implant 226 may be self-aligned to an offset spacer 208 (dielectric such as SiO_2 or Si_3N_4) forming the core PMOS source and drain extensions 210. The n-type halo or pocket implant 228 may be implanted self-aligned to an offset spacer 208 to adjust the doping of the core PMOS transistor channel 114 to set the turn on voltage (vtp). After performing the extension and halo implants, photoresist pattern 224 is removed.

[0018] FIG. 2B shows the integrated circuit after SiGe spacer sidewalls 216 are formed on the PMOS transistor gates 204. The SiGe spacer sidewalls 216 and the dielectric capping layer 206 completely enclose the gate 204 to prevent epitaxial growth of SiGe on the gate 204 material. In an example embodiment, the SiGe spacer sidewalls are about 20 nm of silicon nitride.

[0019] FIG. 2C shows the integrated circuit after a multi-step dry etch forms the U-shaped cavities 220A (for the core PMOS transistor 205) and 220B (for the LVPMOS transistor 215) in the substrate 202. For example, the first dry etch step may be a first anisotropic dry etch used to etch through a deposited hardmask layer (e.g., silicon nitride) and to begin etching the cavities 220A and 220B into the substrate 202. This may be followed by an isotropic dry lateral etch step that expands the cavity laterally toward the channel. This etch may be followed by a second anisotropic dry etch to define the bottom wall of the cavities 220A and 220B. At this point, U-shaped cavities 220A and 220B are both similarly aligned to the spacers 216.

[0020] As shown in FIG. 2D, a wet crystallographic etch is used to etch along crystallographic planes in the substrate 202 to produce "diamond-shaped" cavities 222A and 222B. The wet etchant for the crystallographic etch has crystal orientation selectivity to the substrate material, such as an etchant comprising tetramethyl ammonium hydroxide (TMAH), which is used to etch the substrate beginning with the U-shaped recesses 220A and 220B (FIG. 2C) provided by the multi-step dry etch processing. During the wet crystallographic etching process, the etch rate of the <111>crystal orientation is less than that of other crystal orientations such as <100>. As a result, the U-shaped recesses 220A and 220B become diamond-shaped.

[0021] Because boron doping retards the wet crystallographic etch, the lightly doped silicon (no extension and pocket implant) where the LVPMOS 215 transistor is being formed etches faster than the silicon by PMOS transistor 205 that is more heavily doped by the extension implant 226. As a result, cavity 220B extends further under spacers 216 than cavity 220A at the surface/top of the cavities. In an example embodiment with a sidewall 216 thickness of about 20 nm and a boron extension doping of 1.2 E14 /cm2, the cavity to gate space (C2Gu) with the lightly doped substrate on the LVPMOS transistor 215 is about 5 nm compared to 15 nm for the cavity to gate space (C2Gd) with the boron doped extension on the core PMOS transistor 205. The smaller C2Gu on the LVPMOS transistor enables the p-type SiGe to connect to the LVPMOS transistor 215 channel without an extension implant. Also, the stress is increased because the SiGe will be closer to the transistor channel on the LVPMOS transistor 215, additionally improving the performance of the LVPMOS transistor. The combination of the SiGe being closer to the transistor channel plus the lack of a pocket implant lowers the turn on voltage of the LVPMOS transistor. In an example embodiment, the turn on voltage of the LVPMOS transistor 215 is about 200 mV lower than the turn on voltage of the core PMOS transistor 205.

[0022] Referring now to FIG. 2E, p-doped SiGe 230 is epitaxially grown to fill the diamond shaped cavities 222A and 222B on the core PMOS 205 and LVPMOS 215 transistors, respectively. The p-doped SiGe is sufficiently close (C2Gu) to the channel of the LVPMOS transistor to electrically connect the p-type SiGe to the channel of the LVPMOS transistor 215 without a p-type extension implant, whereas the p-type doped SiGe is too far (C2Gd) from the channel of the core PMOS transistor to form an electrical connection. Additional processing to

add deep source and drain diffusions, silicide, contacts and interconnect levels may then be performed to complete the integrated circuit.

[0023] If desired, dopant may be implanted at low energy to fine tune the LVPMOS transistor 215 turn on voltage when the nwell dopant is implanted.

[0024] Core PMOS 205 and LVPMOS 215 transistors with SiGe source and drains are simultaneously formed using only one extension and pocket patterning and implantation step. This saves significant cost and cycle time over the conventional method that requires separate patterning and implantation steps for the core PMOS 205 and LVPMOS 215 transistors.

[0025] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. An integrated circuit, comprising:

a first PMOS transistor with source and drain extensions and with pockets, the first PMOS transistor having SiGe source and drains with a first SiGe cavity to gate distance; and

a second PMOS transistor without source and drain extensions and without pockets, the second PMOS transistor having SiGe source and drains with a second SiGe cavity to gate distance;

wherein the second SiGe cavity to gate distance is smaller than the first SiGe cavity to gate distance, and wherein a turn on voltage of the second PMOS transistor is lower than the turn on voltage of the first PMOS transistor.

2. The integrated circuit of claim 1, wherein the turn on voltage of the second PMOS transistor is at least 50 mV lower than the turn on voltage of the first PMOS transistor.

3. The integrated circuit of claim 1, wherein the turn on voltage of the second PMOS transistor is about 200 mV lower than the turn on voltage of the first PMOS transistor.

4. The integrated circuit of claim 1, wherein the first SiGe cavity to gate distance is approximately three times the second SiGe cavity to gate distance.

5. The integrated circuit of claim 1, further comprising SiGe spacer sidewalls on a gate of the first PMOS transistor and on a gate of the second PMOS transistor, wherein the SiGe spacer sidewalls are approximately 20 nm, and wherein the first SiGe cavity to gate distance is approximately 15 nm, and wherein the second SiGe cavity to gate distance is approximately 5 nm.

6. A process of forming an integrated circuit, comprising:

forming a first PMOS transistor gate of a first PMOS transistor with source and drain extension implants and with pocket implants self-aligned to the first PMOS transistor gate;

forming a second PMOS transistor gate without source and drain extension implants and without pocket implants;

forming SiGe spacer sidewalls on the first and second PMOS transistor gates;

dry etching first U-shaped cavities self-aligned to the SiGe spacer sidewalls in source and drain regions of the first PMOS transistor and second U-shaped cavities self-aligned to the SiGe spacer sidewalls in source and drain regions of the second PMOS transistor; and

converting the first and second U-shaped cavities to first and second diamond shaped cavities, respectively, using a wet crystallographic etch, wherein the distance from the first diamond shaped cavity to the gate of the first PMOS transistor is greater than the distance from the second diamond shaped cavity to the gate of the second PMOS transistor;

wherein a turn on voltage of the first PMOS transistor is at least 50 mV higher than a turn on voltage of the second PMOS transistor.

7. The process of claim 6, wherein the turn on voltage of the first PMOS transistor is about 200 mV higher than the turn on voltage of the second PMOS transistor.

8. The process of claim 6, wherein the SiGe spacer sidewalls are approximately 20 nm.

9. The process of claim 6, wherein the SiGe spacer sidewalls are approximately 20 nm, and wherein the distance from the first diamond shaped cavity to the gate of the first PMOS transistor is approximately 15 nm, and wherein the distance from the second diamond shaped cavity to the gate of the second PMOS transistor is approximately 5 nm.

10. The process of claim 6, wherein the wet crystallographic etch uses tetramethyl ammonium hydroxide.

11. A process of forming an integrated circuit, comprising:

forming a first PMOS gate of a first PMOS transistor and a second PMOS gate of a second PMOS transistor;

forming a photoresist pattern exposing an area for the first PMOS transistor and covering an area for the second PMOS transistor;

using the photoresist pattern, implanting source and drain extension regions in the first PMOS transistor without implanting source and drain extension regions in the second PMOS transistor;

using the photoresist pattern, implanting pocket regions in the first PMOS transistor without implanting pocket region into the second PMOS transistor;

removing the photoresist pattern;

forming SiGe spacer sidewalls on the first and second PMOS gates; and

without forming source and drain extension regions in the second PMOS transistor, forming a first SiGe cavity in the first PMOS transistor and a second SiGe cavity in the second PMOS transistor, wherein a first SiGe cavity to gate spacing of the first PMOS transistor is greater than a second SiGe cavity to gate spacing of the second PMOS transistor;

wherein a turn on voltage of the first PMOS transistor is at least 50 mV higher than a turn on voltage of the second PMOS transistor.

12. The process of claim 11, wherein the turn on voltage of the first PMOS transistor is about 200 mV higher than the turn on voltage of the second PMOS transistor.

13. The process of claim 11, wherein the SiGe spacer sidewalls are about 20 nm.

14. The process of claim 11, wherein the SiGe spacer sidewalls are approximately 20 nm, and wherein the first SiGe cavity to gate spacing is approximately 15 nm, and wherein the second SiGe cavity to gate spacing is approximately 5 nm.

15. The process of claim 11, wherein the first SiGe cavity and the second SiGe cavity are diamond shaped and are formed by:

dry etching first U-shaped cavities self-aligned to the SiGe spacer sidewalls in source and drain regions of the first PMOS transistor and second U-shaped cavities self-aligned to the SiGe spacer sidewalls in source and drain regions of the second PMOS transistor; and

performing a wet crystallographic etch to convert the first and second U-shaped cavities to first and second diamond shaped cavities, respectively, wherein the wet crystallographic etch laterally etches the second U-shaped cavity faster than the first U-shaped cavity at the surface to form the first SiGe cavity to gate spacing of the first PMOS transistor greater than the second SiGe cavity to gate spacing of the second PMOS transistor.

16. The process of claim 15, wherein the wet crystallographic etch uses tetramethyl ammonium hydroxide.

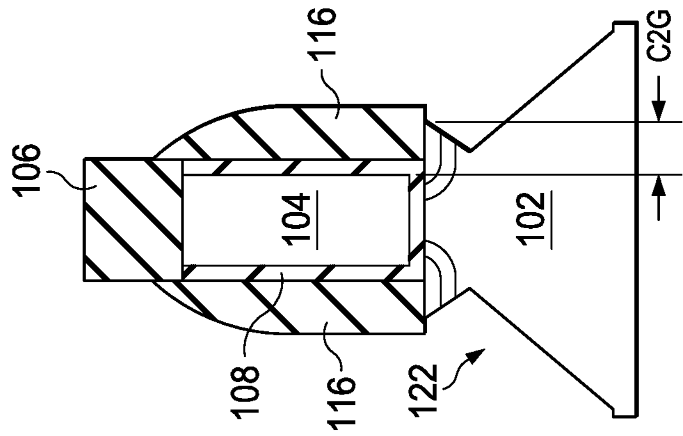

FIG. 1C
(PRIOR ART)

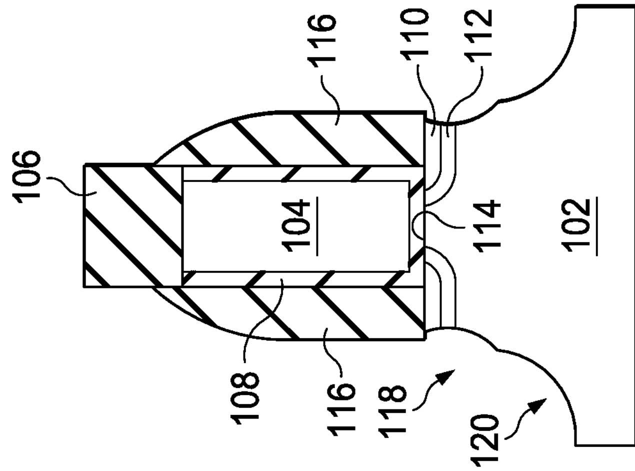

FIG. 1B
(PRIOR ART)

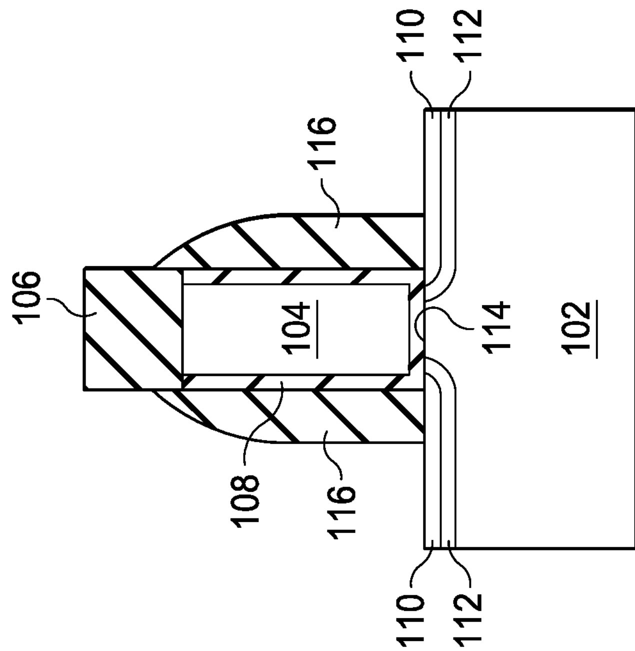

FIG. 1A
(PRIOR ART)

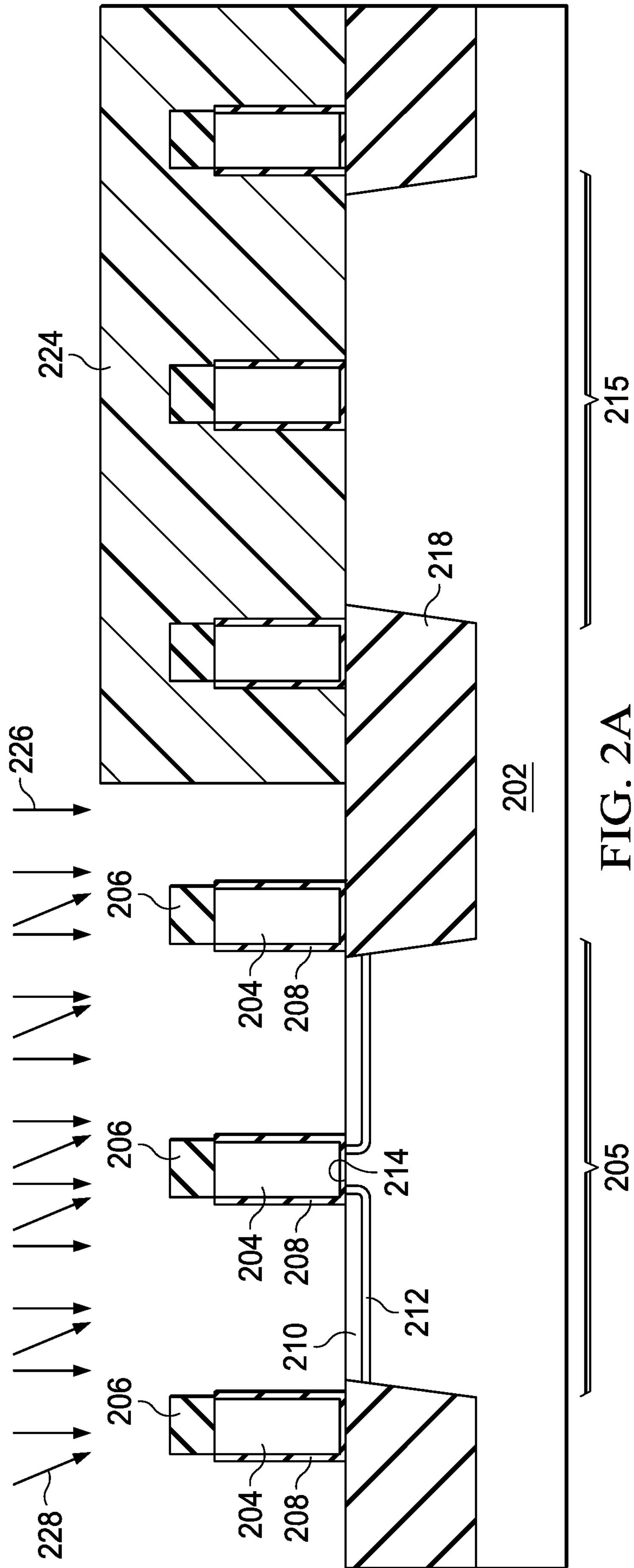

FIG. 2A

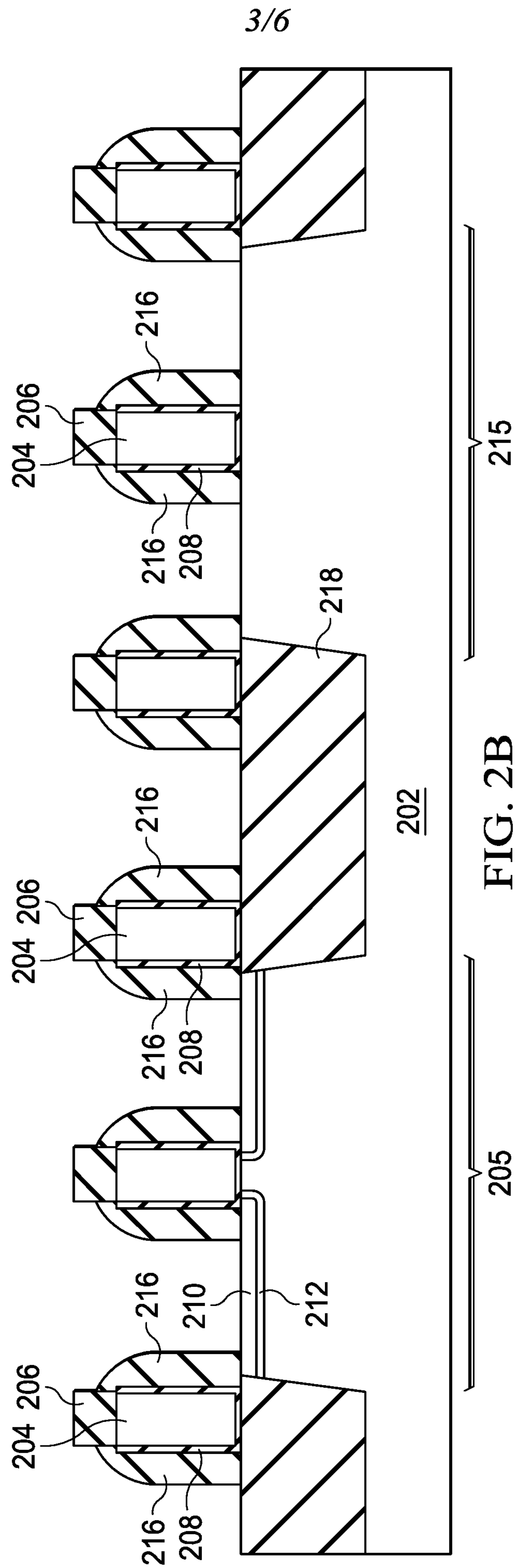

FIG. 2B

204 206 208 216 210 212 220A 220B 218 215 205 202

FIG. 2C

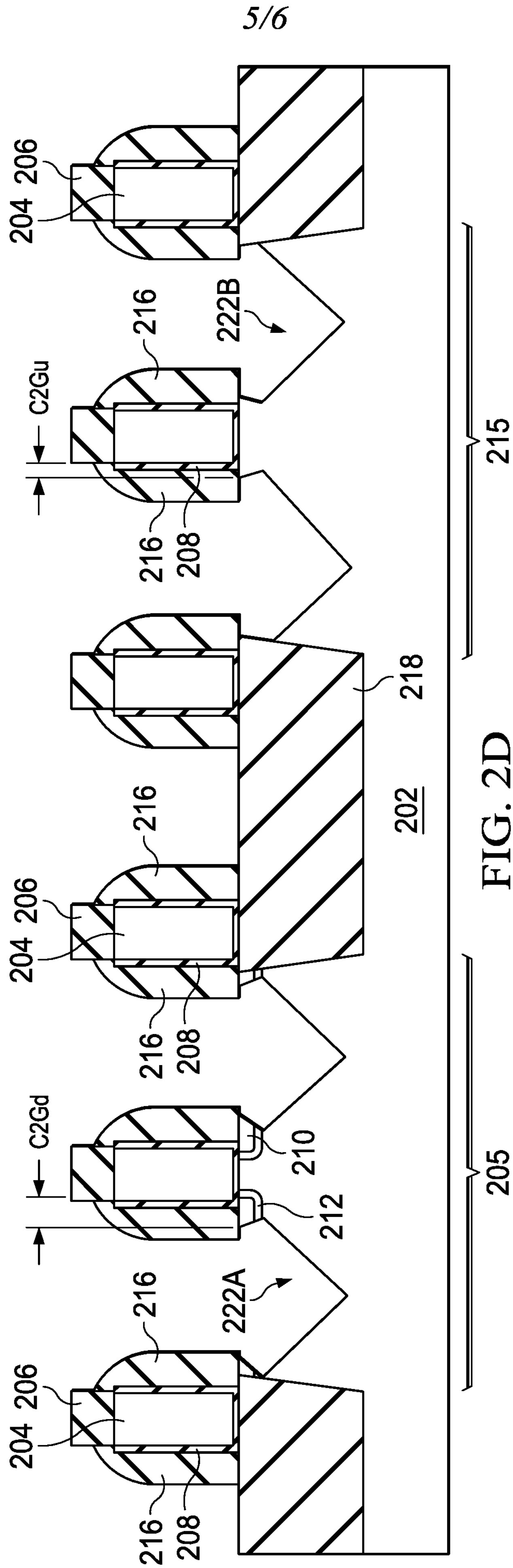

FIG. 2D

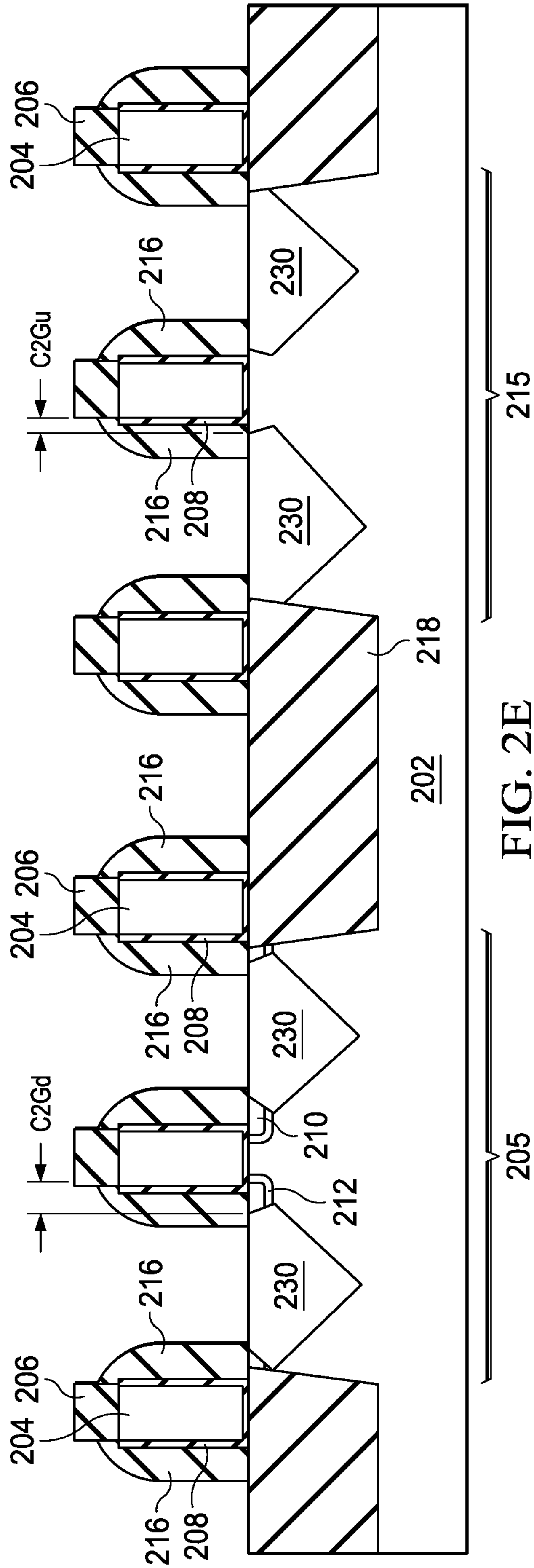

FIG. 2E

INTERNATIONAL SEARCH REPORT	International application No. PCT/US 2016/050409

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/06 *(2006.01)*
H01L 21/8232 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 27/04-27/08, 21/8232

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2015/0031178 A1 (TEXAS INSTRUMENTS INCORPORATED) 29.01.2015	1-16
A	US 2014/0346565 A1 (SEMICONDUCTOR MANUFACTURING INTERNATIONAL (SHANGHAI) CORPORATION) 27.11.2014	1-16
A	US 2015/0214116 A1 (GLOBALFOUNDRIES INC.) 30.07.2015	1-16
A	US 2009/0179236 A1 (TEXAS INSTRUMENTS INCORPORATED) 16.07.2009	1-16
A	WO 2015/027141 A1 (TEXAS INSTRUMENTS INCORPORATED) 26.02.2015	1-16

☐ Further documents are listed in the continuation of Box C.   ☐ See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
08 December 2016 (08.12.2016)	15 December 2016 (15.12.2016)

Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37	Authorized officer I. Baginskaya Telephone No. (499) 240-25-91