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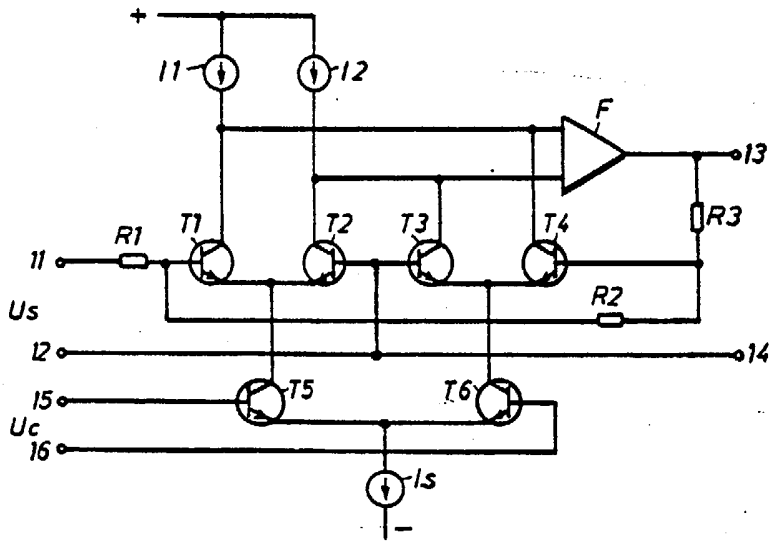

(57) **Abstract**

A gain control circuit includes at least a first (T1, T2) and a second (T3, T4) transistor differential amplifier the input circuits of which are connected in parallel to a signal voltage source. The gain control is performed by distributing a constant current (Is) between these differential amplifiers as a function of a control quantity (Uc) for setting the transconductance of the stages in a complementary way. The two differential amplifiers are provided with negative feed back (F, R1, R2, R3) but with different feed back factors. As the transistors in the differential amplifiers carrying signals of the same phase are interconnected the output signal from the automatic gain control circuit the output signal from the gain control circuit will consist of a superposition of the output signals of the two differential amplifiers.

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GAIN CONTROL CIRCUIT

FIELD OF THE INVENTION

The present invention relates to a gain control circuit suitable to be implemented in a monolitic technique and substantially intended to be used in line and microphone amplifiers for telephone instruments.

DESCRIPTION OF PRIOR ART

It is known to use differential amplifier stages in gain control circuits intended to be included in amplifiers designed in an integrated technique. By means of these stages it is possible to design temperature stable amplifiers. Gain control circuits of this type are for example described in the USA patent publication 3 684 974 or in the German patent publication 2 262 580.

A gain control circuit according to the above patent publications is working according to the current sharing principle implying that the signal current is shared by one or more differential stages the shares being determined by a control current. The controlled signal voltage is taken out across one (or more) load impedances where the current share determined by the control voltage is transformed into an output voltage.

SUMMARY OF THE INVENTION

The gain control circuits previously known are intended as volume controls in radio sets and audio amplifiers. Therefore, they must have a large control range whereas the total gain and a possible drift of the gain is of minor importance. It is also obvious that gain control circuits of this type cannot be used in telephone instruments with their great demands of the nominal attenuation as well as of the control range. The tolerated deviation from the specified attenuation value is of magnitude ± 0.1 dB when the control range is 6 dB.

The object of the present invention is to achieve a gain control circuit which fulfils the above requirements which includes at least a

first and a second transistor differential amplifier the inputs of which are connected in parallel to a signal source and the characteristics of the invention appear from the attached patent claims. A gain control circuit according to the invention thoroughly fulfils the demands for a defined amplification required in an amplifier for telephone purposes at the same time as low noise, low distortion and low power consumption are obtained.

BRIEF DESCRIPTION OF THE DRAWING

The invention will be more fully described with reference to the accompanying drawing, where

Fig 1 shows a gain control circuit according to the invention with an unbalanced output and

Fig 2 shows a similar circuit with a balanced output.

PREFERRED EMBODIMENTS

The circuit shown in Fig 1 includes a first differential stage with the transistors T1 and T2, a second differential stage with the transistors T3 and T4 and a third differential stage with the transistors T5 and T6. A signal is applied across the input terminals 11 and 12. The input 11 is connected through the resistor R1 to the base of the transistor T1 and through the resistor R1 + R2 to the base of the transistor T4. The base electrodes of the transistors T2 and T3 are interconnected and connected to the input 12 and the output 14. The collectors in the transistors T1 and T4 are connected to a constant current source I1 and to an input of an amplifier F while the collectors of the transistors T2 and T3 are connected to a constant current source I2 and the second input of the amplifier F. The interconnected emitters of the transistors T1 and T2 are connected to the collector of the transistor T5 in the third differential amplifier. The collector of the transistor T6 in the same differential amplifier is connected in the same way to the emitters of the transistors T3 and T4. The emitters of the transistors T5 and T6 are connected to a constant current source Is. The base electrodes of the transistors T5 and T6 are connected to

a DC control voltage Uc. There is a negative feed back from the output of the amplifier F through the resistor R2 to the base circuit of the transistor T4 (directly) and the transistor T1 (through R2). Thus the differential amplifiers T1, T2 and T3, T4 have different negative feed back factors.

The circuit operates in the following way. The sharing of the constant current Is between the transistors T5 and T6 can be controlled through the DC voltage Uc. This implies that the emitters in the differential amplifiers T1, T2 and T3, T4 receive corresponding currents. It is well known that the amplification of a differential stage increases with the emitter current. If, for example, the greater part of the current Is is sent through the transistors T1, T2 while the transistors T3, T4 carry a very small current the differential amplifier T1, T2 will amplify the input signal with maximum amplification while the contribution from T3, T4 is negligible. The negative feed-back circuit including the amplifier F gives a loop amplification which is proportional to $\frac{R3 + R2}{R1}$. On the other hand if the greater part of the current Is is sent through the differential amplifier T3, T4 this amplifier will amplify the input signal and the amplification will be proportional to $\frac{R3}{R2 + R1}$ i e it will be lower than in the first case. These two extreme cases determine the limits for the control range. Other current sharings give gains between these limits. An analysis of the circuit gives the following expression for the total gain A of the circuit

$$A = \frac{A1(1 + \beta 2) + A2(1 + \beta 1)}{(1 + \beta 1)(1 + \beta 2) + A1 \cdot \beta 1)(1 + \beta 2) + A2(1 + \beta 1)}$$

where A1 is the gain of the differential amplifier T1, T2, A2 is the gain in the differential amplifier T3, T4 and $\beta 1$ and $\beta 2$ is the negative feed back factor for the corresponding negative feed back network R3 + R2; R1 and R3; R2 + R1 respectively.

In an embodiment the negative feed back network was so dimensioned that the amplifier had the gains 20dB and 26 dB at the limits of the control voltage. For all intermediate values of the DC voltage signal the gain was kept within the limits required for telephone amplifiers and the gain control was stable within given tolerances.

Fig 2 shows a modified gain control circuit according to the invention with the negative feed back amplifier F1 where both the input and the output are balanced. In this case collectors of the transistors T1 and T3 are connected together as well as the collectors of the transistors T2 and T4. The input 11 is connected to the base of the transistor T1 through the resistor R4 and to the base of the transistor T3 through the resistor R4 + R5. One output of the amplifier F1 is connected as well to the output 13, as to the base of the transistor T3 through the resistor R6. In a similar way the input 12 is connected to the base of the transistor T2 through the resistor R7 and to the base of the transistor T4 through the resistor R7 + R8 while the second output of the amplifier F1 is connected as well to the output 14, as to the base of the transistor T4 through the resistor R8. The bases of the transistors T2 and T3 are not connected together in this case. The circuit according to Fig 2 essentially works in the same way as described in Fig 1, the only difference being that also the negative feed back circuit is balanced.

What we claim is:

1 A gain control circuit including at least a first (T1, T2) and a second (T3, T4) transistor-differential amplifier, the input circuits of which are connected in parallel to a signal voltage source, characterized in that the transistors in the differential amplifiers (T1-T4) carrying signal currents having equal phase are connected together and to the input side of an amplifier (F) having at least one input, that a current source (Is, T5, T6) is arranged to feed emitter currents to said differential circuits (T1, T2; T3, T4), the quotient of said emitter currents depending on a control signal (Uc) applied to the current source (Is, T5, T6) the output of the amplifier (F) being connected to the input of said first and second differential amplifiers through a negative feed back network (e g R1, R2, R3), so dimensioned that said two differential amplifiers together with said negative feed back network have different loop gain for the same emitter current.

2 A gain control circuit according to claim 1, characterized in that the input and output circuits of the amplifier (F) and the negative feed back network (R4, R5, R6; R7, R8, R9) are balanced.

Fig. 1

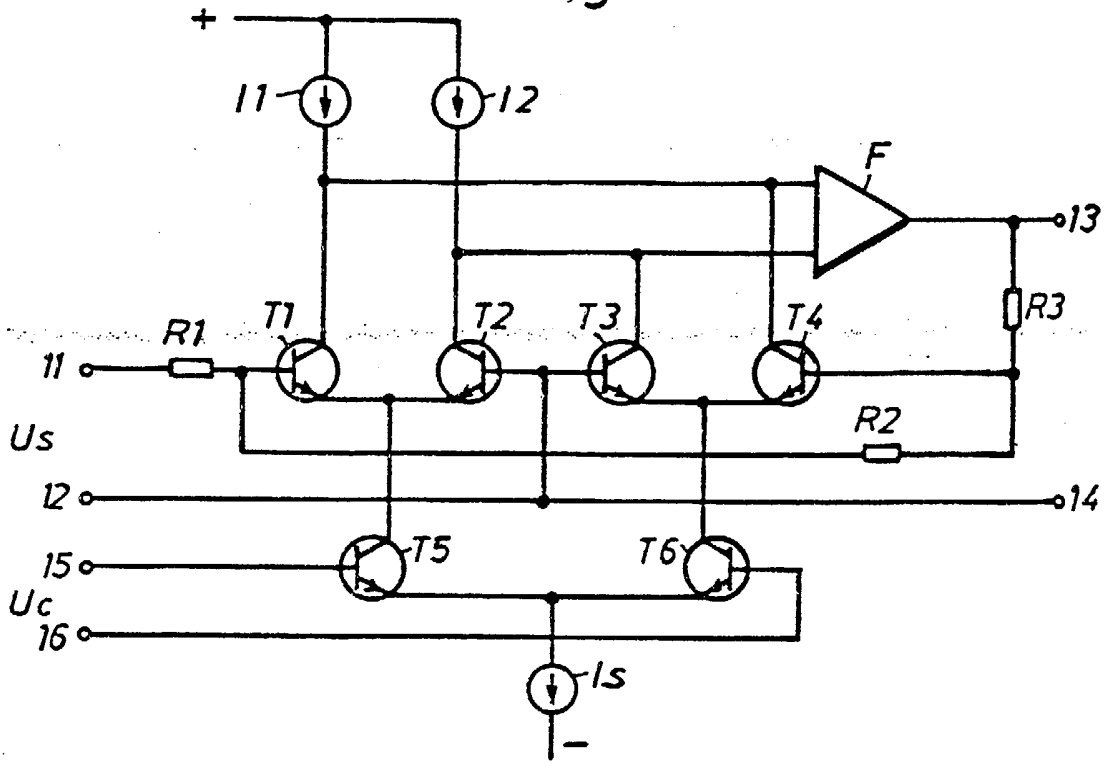
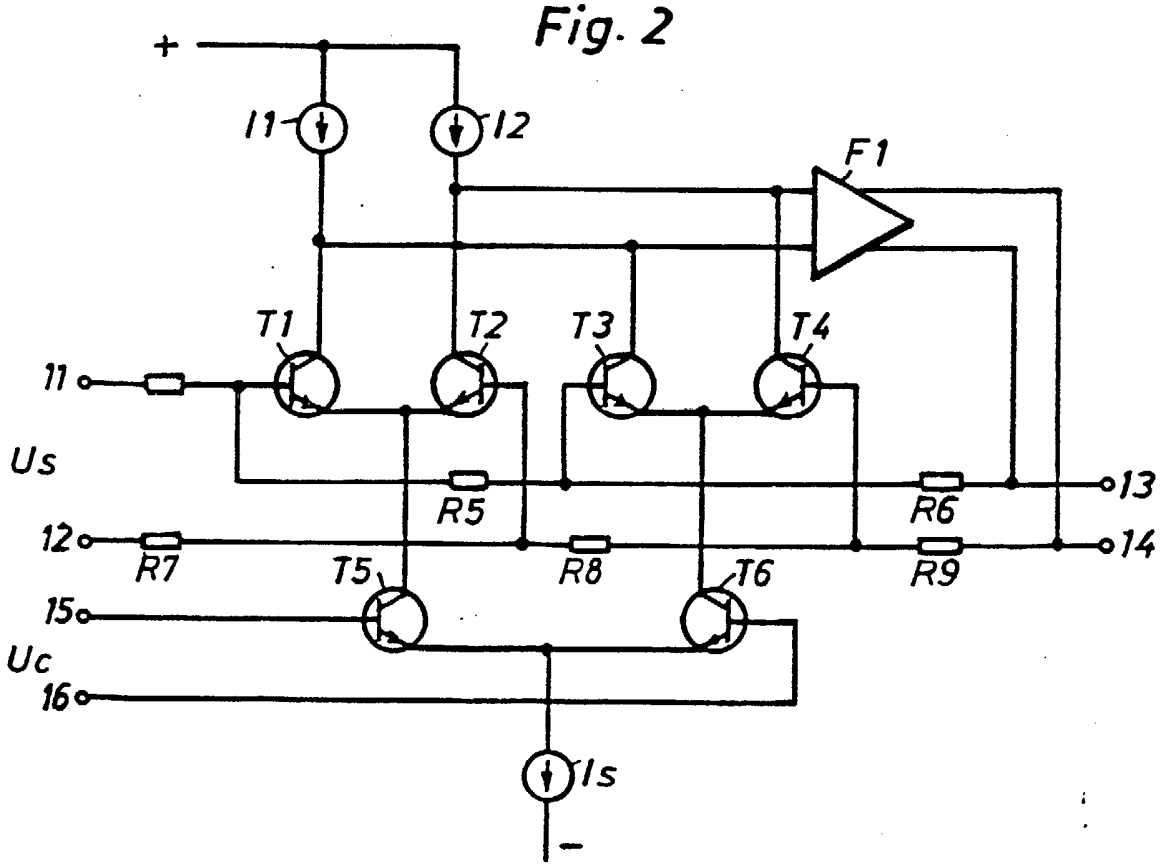


Fig. 2



INTERNATIONAL SEARCH REPORT

International Application No PCT/SE80/00047

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC [3]

H 03 F 1/34, 3/45, H 04 M 1/60

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
IPC [5]	H 03 F 1/34, 3/45; H 04 M 1/60, 1/62
Deutsche Kl	21a [2]: 18/05, 18/08, 34/03
US Cl	179/1A, 1F, 81; 330/30, 69, 261

Documentation Searched other than Minimum Documentation to the Extent that such Documents are included in the Fields Searched [6]

SE, NO, DK, FI classes as above

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
A	SE, C, 352 791 published 1973, January 8, Honeywell Inc.	1
A	US, A, 4 052 679 published 1977, October 4, Sanyo Electric Co Ltd.	1

* Special categories of cited documents: [15]

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IV. CERTIFICATION

Date of the Actual Completion of the International Search [1]	Date of Mailing of this International Search Report [1]
1980-04-21	1980-04-28
International Searching Authority [1]	**Signature of Authorized Officer [20]**
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