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(71) Applicant: SPIRE MANUFACTURING INC. [US/US]; 49016 Milmot Drive, Fremont, California 94538 (US).

(72) Inventors: DAU, Hai; 408 Saturn Park Court, San Ramon, California 94582 (US). WENG, Lim; BLK 132, Bedok North Street 2, Unit# 13-79, Singapore 460132 (SG). SHANMUGAM, Kathandan; Blk 30, Balam Road, Unit # 07-28, Singapore 370030 (SG). BUI, Christine; 6830 Eagle Ridge Drive, Gilroy, California 95020 (US).

(74) Agent: GONZALES, Mark; 5538 Civic Terrace Avenue, Newark, California 94660 (US).

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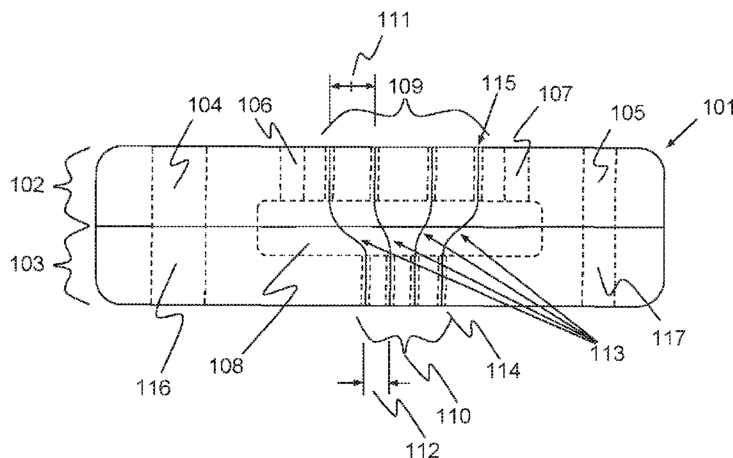


Fig. 1

(57) Abstract: In one embodiment, the present invention includes an interface apparatus for semiconductor testing. The interface apparatus includes a housing. The housing includes a lower housing substrate and an upper housing substrate. The lower housing substrate has a plurality of apertures arranged according to a fine pitch, and the upper housing substrate has a plurality of apertures arranged according to a coarse pitch. A plurality of wires passes through the plurality of apertures from the lower housing substrate to the upper housing substrate. Each wire has plated conductive ends emanating from opposing sides of the housing. The plurality of apertures of the lower housing substrate corresponds to the plurality of apertures of the upper housing substrate. The interface apparatus transforms a pattern having a course pitch to a pattern having a fine pitch.

WO 2017/053910 A1

Interface Apparatus for Semiconductor Testing and Method of Manufacturing Same

CROSS REFERENCE TO RELATED APPLICATIONS

5 **[0001]** This application is an application of U.S. patent application no. 14/864,823 titled "Interface Apparatus for Semiconductor Testing and Method of Manufacturing Same", filed September 24, 2015.

BACKGROUND

[0002] The present invention relates to an electrical/mechanical interface apparatus, and in 10 particular, to interface apparatus for semiconductor testing and method of manufacturing same.

[0003] The pads on semiconductor devices are getting smaller. Traditional cantilever probes need to scrub the pad and with smaller areas, the scrub may extend into the die area potentially causing damage to the device.

15 **[0004]** An alternative solution is the vertical probe. However interfacing these vertical probe contactors to tester equipment has become more difficult as the pitch between device pads becomes less than 100 microns.

[0005] Thus, there is a need for interface apparatus for semiconductor testing and method of manufacturing same.

20 ## SUMMARY

[0006] Embodiments of the present invention include an interface apparatus for semiconductor testing. The interface apparatus includes a first housing substrate, a second housing substrate, and a plurality of wires. The first housing substrate has a first plurality of apertures arranged according to a first pitch. The second housing substrate mates to the first 25 housing substrate and has a second plurality of apertures arranged according to a second pitch. The plurality of wires passes through the first and second plurality of apertures. Each wire has plated conductive ends emanating from opposing sides of the housing. The first plurality of apertures corresponds to the second plurality of apertures, and the first pitch is less than the second pitch.

30 **[0007]** In one embodiment the interface apparatus further includes a recessed portion in at least one of the first and second housing substrates thereby providing an internal volume within the housing.

[0008] In another embodiment, the plated conductive ends are all plated with the same material and with the same tolerance of thickness.

[0009] Embodiments of the present invention include a method of manufacturing an interface apparatus. The method includes drilling, passing, attaching, and cutting. The drilling includes drilling a first plurality of apertures through a first housing substrate. The first plurality of apertures is arranged according to a first pitch. The drilling includes drilling a second plurality of apertures through a second housing substrate. The second plurality of apertures is arranged according to a second pitch. The passing includes passing a plurality of wires through the first and second plurality of apertures. The attaching includes attaching the first housing substrate to the second housing substrate thereby forming a complete housing. The cutting includes cutting wire ends protruding out from the first and the second housing substrates. The first plurality of apertures corresponds to the second plurality of apertures, and the first pitch is less than the second pitch.

[0010] In one embodiment the attaching further includes injecting epoxy into an internal volume of the housing. The internal volume formed from a recessed portion in at least one of the first and second housing substrates.

[0011] In another embodiment, the method further includes plating. The plating may occur without masking and without a fixture.

[0012] Embodiments of the present invention include a system of interfacing a vertical probe assembly with an automated tester. The system includes an interface apparatus. The interface apparatus includes a first housing substrate, a second housing substrate, and a plurality of wires. The first housing substrate has a first plurality of apertures arranged according to a first pitch. The second housing substrate mates to the first housing substrate and has a second plurality of apertures arranged according to a second pitch. The plurality of wires passes through the first and second plurality of apertures. Each wire has plated conductive ends emanating from opposing sides of the housing. The first plurality of apertures corresponds to the second plurality of apertures, and the first pitch is less than the second pitch. The system also includes a PCB which has a plurality of conductive pads. The plurality of conductive pads couple with the plurality of wires positioned within the second plurality of apertures.

[0013] In one embodiment the system further comprises a recessed portion in at least one of the first and second housing substrates thereby providing an internal volume within the housing.

[0014] The following detailed description and accompanying drawings provide a better understanding of the nature and advantages of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] Figs. 1 illustrates an apparatus according to one embodiment of the present invention.

[0016] Fig. 2 illustrates a method of manufacturing a interface apparatus according to another embodiment of the present invention.

[0017] Figs. 3A-D illustrate an upper housing substrate according to yet another embodiment of the invention. Fig. 3A illustrates a contact side of the upper housing substrate. Fig. 3B illustrates a side view of the upper housing substrate. Fig. 3C illustrates an internal view of the upper housing substrate, and Fig. 3D illustrates two 3-dimensional views of the upper housing substrate.

[0018] Figs. 4A-D illustrate a lower housing substrate according to another embodiment of the invention. Fig. 4A illustrates a contact side of the lower housing substrate. Fig. 4B illustrates a side view of the upper housing substrate. Fig. 4C illustrates an internal view of the lower housing substrate, and Fig. 3D illustrates two 3-dimensional views of the lower housing substrate.igs. 4A-D illustrate a lower housing substrate according to another embodiment of the invention.

[0019] Figs. 5A-D illustrate a printed circuit board (PCB) configured to attach an interface apparatus according to yet another embodiment of the invention. Fig. 5A illustrates a contact side of the PCB. Fig. 5B illustrates a side view of the PCB. Fig. 5C illustrates a detail of an area of Fig. 5A and Fig. 5D illustrates two 3-dimensional views of the PCB.

[0020] Figs. 6A-C illustrate a system of interfacing a tester with a vertical probe contactor according to another embodiment of the invention. Fig. 6A illustrates a contactor side of the system. Fig. 6B illustrates a side view of the system. Fig. 6C illustrates a 3-dimensional view of the system.

DETAILED DESCRIPTION

[0021] Described herein are techniques for interface apparatus and method for manufacturing same. In the following description, for purposes of explanation, numerous examples and specific details are set forth in order to provide a thorough understanding of the present invention. It will be evident, however, to one skilled in the art that the present invention as defined by the claims may include some or all of the features in these examples alone or in combination with other features described below, and may further include modifications and equivalents of the features and concepts described herein.

[0022] Figs. 1 illustrates an apparatus 100 according to one embodiment of the present invention. Apparatus 100 includes a housing 101 comprising an upper housing substrate 102, a lower housing substrate 103, and a plurality of wires 113 passing through plurality of apertures 109-110. Each wire has plated conductive ends emanating from opposing sides housing 101 (e.g. 114-115). Plurality of apertures 114 corresponds to plurality of apertures 115. For every aperture of the plurality of apertures 114, there is a corresponding aperture of plurality of apertures 115 which the same wire of the plurality of wires 113 are threaded through.

[0023] Plurality of apertures 109 has a pitch 111 and plurality of apertures 110 has a pitch of 112. Pitch 112 is less than pitch 111. In some embodiments pitch 112 may be less than or equal to 250 microns. In some embodiments pitch 111 may be greater than or equal to 300 microns. Apparatus 100 interfaces between a course pitch provided by plurality of apertures 109 and a fine pitch provided by plurality of apertures 110. This may allow a technology of greater than 250 micrometers capability to interface with another technology which has less than 100 micrometers capability. For example, a printed circuit board (PCB) (not shown) may have a pattern which may be interfaced to a vertical probe contactor.

[0024] Apparatus 100 also has an internal volume 108 which is recessed on both housing substrate 102-103. In another embodiment, only one of the housing substrates (i.e. housing substrate 102 or 103) may include a recessed portion to provide the internal volume. Holes 106-107 may be used to inject epoxy into the internal volume 108. In another embodiment, there may be a plurality of epoxy holes to aid in injecting an even flow of epoxy into internal volume 108. This plurality of epoxy holes may be arrayed along a periphery of the plurality of apertures 102 or 103 in order to provide a complete adhesion of the plurality of wires 113 within plurality of apertures 102-103.

[0025] Apparatus 100 also has alignment holes 104-105 and 116-117 that may be used to align housing substrate 102 to housing substrate 103 prior to attaching them with an epoxy injection as described above. Alignment holes 104-105 and 116-117 may also be used to align apparatus 100 to a PCB. For example, plurality of apertures 109 may be arranged in a ball grid array (BGA) pattern so that solder balls or a thick solder paste may be distributed on a conductive BGA pattern on a PCB, and the alignment holes 104-105 and 116-117 may be used to align apparatus 100 to a PCB so that heat may be applied and apparatus 100 may be soldered to the PCB. In one embodiment, the alignment holes 104-105, 116-117 may be used to align a contactor to the apparatus 100 and a PCB (i.e. mechanically interface a contactor to a PCB) and the plurality of apertures 109-110 may electrically interface between the contactor and the PCB.

[0026] The plated conductive ends (e.g. 114-115) may be all plated with the same material and with the same tolerance of thickness. This may be accomplished if all the wire ends are plated at the same time. For example, a lot of similar apparatus such as apparatus 100 may be plated together: first by bathing the lot in nickel; and then by bathing the lot in gold. In one embodiment, housing 101 is ceramic such that only the wire ends will adhere to the nickel and gold (respectively).

[0027] Fig. 2 illustrates a method of manufacturing 200 an interface apparatus according to another embodiment of the present invention.

[0028] At 201, drill a first plurality of apertures through a first housing substrate. The first plurality of apertures is arranged according to a first pitch.

[0029] At 202, drill a second plurality of apertures through a second housing substrate. The second plurality of apertures is arranged according to a second pitch.

[0030] At 203, align the first and second housing substrate to each other. This may be accomplished by having a fixture which has steal dowels which go through the alignment holes on the first and second housing.

[0031] At 204, place temporary spacers between the first and second housing substrates. This may be used to allow enough space to thread the plurality of wires into the respective pluralities of apertures found in the first and second housing substrates.

[0032] At, 205, pass a plurality of wires through the pluralities of apertures according to a correspondence between the first and second plurality of apertures.

[0033] At 206, attach the first and second housing substrates. This forms a single housing. The attaching may include injecting epoxy into an internal volume of the housing. The internal volume may be formed from a recessed portion in at least one of said first and second housing substrates.

5 [0034] At 207, cut the wire ends of the plurality of wires protruding out from the first and second housing substrates.

[0035] At 207, lap the wire ends.

[0036] At 208, plate the wire ends. The plating may include gold plating over an initial nickel plating. The plating may occur without masking and without a fixture. For example, 10 in one embodiment, the housing may be made of ceramic such that the entire unit may be placed into a plating bath. This would insure that all the wire ends were plated with the same tolerance of thickness and the same material. This operation does not need masking because the plating material would not adhere to the ceramic portions of the unit.

[0037] Figs. 3A-D illustrate an upper housing substrate 300 according to yet another 15 embodiment of the invention. Fig. 3A illustrates a contact side of upper housing substrate 300 showing alignment holes 314-315, epoxy injection holes 301-313, and plurality of apertures 316. The plurality of apertures 316 is in a BGA pattern in this embodiment.

[0038] Fig. 3B illustrates a side view of upper housing substrate 300.

[0039] Fig. 3C illustrates an internal view of upper housing substrate 300 showing 20 alignment holes 314-315 and plurality of apertures 316.

[0040] Fig. 3D illustrates two 3-dimensional views of upper housing substrate 300. Upper housing substrate 300 includes a recessed portion 317 in which a plurality of wires and an epoxy may reside.

[0041] Figs. 4A-D illustrate a lower housing substrate 400 according to another 25 embodiment of the invention. Fig. 4A illustrates a contact side of lower housing substrate 400 showing plurality of apertures 401-402 and alignment holes 403-404.

[0042] Fig. 4B illustrates a side view of upper housing substrate 400.

[0043] Fig. 4C illustrates an internal view of lower housing substrate 400 showing plurality of apertures 401-402 and alignment holes 403-404.

[0044] Fig. 4D illustrates two 3-dimensional views of lower housing substrate 400. Lower housing substrate 400 includes plurality of apertures 401-402 and a recessed portion 405 in which a plurality of wires and an epoxy may reside.

[0045] Figs. 5A-D illustrate a printed circuit board 500 (PCB) configured to attach an
5 interface apparatus according to yet another embodiment of the invention. Fig. 5A illustrates a contact side of PCB 500 showing alignment holes 502-503 and a plurality of conductive pads 501. Area 504 shows the contact area where an interface apparatus may be attached.

[0046] Fig. 5B illustrates a side view of PCB 500. PCB 500 includes a plurality of pins to interface to a test plate. PCB 500 may be a daughter board configured as a contactor
10 interface board. In one embodiment, PCB 500 may be a general interface board which may be used on a family of test plates in order to quickly replace the vertical probes on a test system.

[0047] Fig. 5C illustrates a detail of area 504 of Fig. 5A showing alignment holes 502-503 and conductive pads 501. In one embodiment, conductive pads 501 may have a solder mask.
15 In another embodiment, the plurality of conductive pads 501 may be arranged in a BGA pattern and bumped with solder balls (e.g. solder ball 505). The plurality of conductive pads 501 may have positions to couple with a plurality of wires positioned within a plurality of apertures also arranged in the same BGA pattern.

[0048] Fig. 5D illustrates two 3-dimensional views of PCB 500. Contactor side 506 may
20 be where an interface apparatus may be attached. PCB 500 may be attached to a tester though a test plate from the tester side 507 side.

[0049] Figs. 6A-C illustrate a system 600 of interfacing a tester with a vertical probe contactor according to another embodiment of the invention. Fig. 6A illustrates a contactor side of system 600 showing interface apparatus 604 attached to PCB 601. Interface apparatus
25 604 includes a plurality of conductive ends 608-609 and alignment holes 606-607. System 600 is a dual site interface system designed to contact 2 die simultaneously. Other configurations of multisite arrangements are also possible in other embodiments. Alignment holes 606-607 may be used to align a contactor to interface apparatus 604.

[0050] Fig. 6B illustrates a side view of system 600. Fig. 6B shows PCB 601 having a
30 plurality of pins 605 on the tester side of system 600 and an interface apparatus 604 attached

on the contactor side of system 600. Interface apparatus 604 includes an upper housing substrate 602 and a lower housing substrate 603.

[0051] Fig. 6C illustrates a 3-dimensional view of system 600. Fig. 6C shows the contactor side 610 of system 600. Interface apparatus 604 is shown attached to PCB 601. In other
5 embodiments, interface apparatus 604 may be attached directly to a test plate which interfaces to a tester. In another embodiment, interface apparatus 604 may be attached to a swap block which couples to test instruments through a pogo tower and general interface PCB.

[0052] The above description illustrates various embodiments of the present invention along
10 with examples of how aspects of the present invention may be implemented. The above examples and embodiments should not be deemed to be the only embodiments, and are presented to illustrate the flexibility and advantages of the present invention. Based on the above disclosure, other arrangements, embodiments, implementations and equivalents will be evident to those skilled in the art and may be employed without departing from the spirit and
15 scope of the invention.

WHAT IS CLAIMED IS:

1 1. An interface apparatus for semiconductor testing, said interface
2 apparatus comprising:
3 a housing including
4 a first housing substrate having a first plurality of apertures arranged
5 according to a first pitch, and
6 a second housing substrate mated to said first housing substrate and
7 having a second plurality of apertures arranged according to a second pitch; and
8 a plurality of wires passing through said first and second plurality of apertures,
9 each wire of said plurality of wires having plated conductive ends emanating from opposing
10 sides of said housing,
11 wherein said first plurality of apertures corresponds to said second plurality of
12 apertures, and wherein said first pitch is less than said second pitch.

1 2. The interface apparatus of claim 1 further comprising a recessed
2 portion in at least one of said first and second housing substrates thereby providing an
3 internal volume within said housing.

1 3. The interface apparatus of claim 2 wherein said internal volume includes
2 an epoxy.

1 4. The interface apparatus of claim 1 wherein the second plurality of
2 apertures is arranged according to a ball grid array pattern.

1 5. The apparatus of claim 1 further comprising alignment holes on both
2 said first and said second housing substrates

1 6. The apparatus of claim 1 wherein said plated conductive ends are all
2 plated with the same material and with the same tolerance of thickness.

1 7. A method of manufacturing an interface apparatus, said method
2 comprising:
3 drilling a first plurality of apertures through a first housing substrate, said first
4 plurality of apertures arranged according to a first pitch;
5 drilling a second plurality of apertures through a second housing substrate,
6 said second plurality of apertures arranged according to a second pitch;

7 passing a plurality of wires through said first and second plurality of apertures;
8 attaching said first housing substrate to said second housing substrate thereby
9 forming a housing; and
10 cutting a wire ends protruding out from said first and said second housing
11 substrates,
12 wherein said first plurality of apertures corresponds to said second plurality of
13 apertures, and wherein said first pitch is less than said second pitch.

1 8. The method of claim 7 wherein said attaching further includes
2 injecting epoxy into an internal volume of said housing, said internal volume formed from a
3 recessed portion in at least one of said first and second housing substrates.

1 9. The method of claim 8 wherein said injecting occurs through a
2 plurality of holes in said second housing substrate, said plurality of holes placed on a
3 periphery of said second plurality of apertures.

1 10. The method of claim 7 further comprising placing temporary spacers
2 between said first and second housing substrates.

1 11. The method of claim 10 further comprising aligning said first and said
2 second housing substrate.

1 12. The method of claim 7 further comprising:
2 lapping said wire ends; and
3 plating said wire ends.

1 13. The method of claim 12 wherein said plating occurs without masking
2 and without a fixture.

1 14. The method of claim 12 further comprising:

2 bumping a plurality of conductive pads of a printed circuit board (PCB), said
3 plurality of conductive pads having a position to couple with said plurality of wires
4 positioned within said second plurality of apertures; and
5 soldering said housing to said PCB by heating a solder of said bumping.

1 15. The system of interfacing a vertical probe assembly with an automated
2 tester, said system comprising:

3 an interface apparatus comprising,
4 . a housing including
5 a first housing substrate having a first plurality of apertures
6 arranged according to a first pitch, and
7 a second housing substrate mated to said first housing substrate
8 and having a second plurality of apertures arranged according to a
9 second pitch, and
10 a plurality of wires passing through said first and second plurality of
11 apertures, each wire of the plurality of wires having plated conductive ends
12 emanating from opposing sides of said housing,
13 wherein said first plurality of apertures corresponds to said second
14 plurality of apertures, and wherein said first pitch is less than said second
15 pitch; and
16
17 a PCB having a plurality of conductive pads, said plurality of conductive pads
18 coupled with said plurality of wires positioned within said second plurality of apertures.

1 16. The system of claim 15 further comprising a recessed portion in at
2 least one of said first and second housing substrates thereby providing an internal volume
3 within said housing.

1 17. The system of claim 16 wherein said internal volume includes an epoxy.

1 18. The system of claim 15 wherein the second plurality of apertures is
2 arranged according to a ball grid array pattern.

1 19. The system of claim 15 further comprising alignment holes on both
2 said first and said second housing substrates.

1 20. The system of claim 15 wherein said plated conductive ends are all
2 plated with the same material and with the same tolerance of thickness.

100

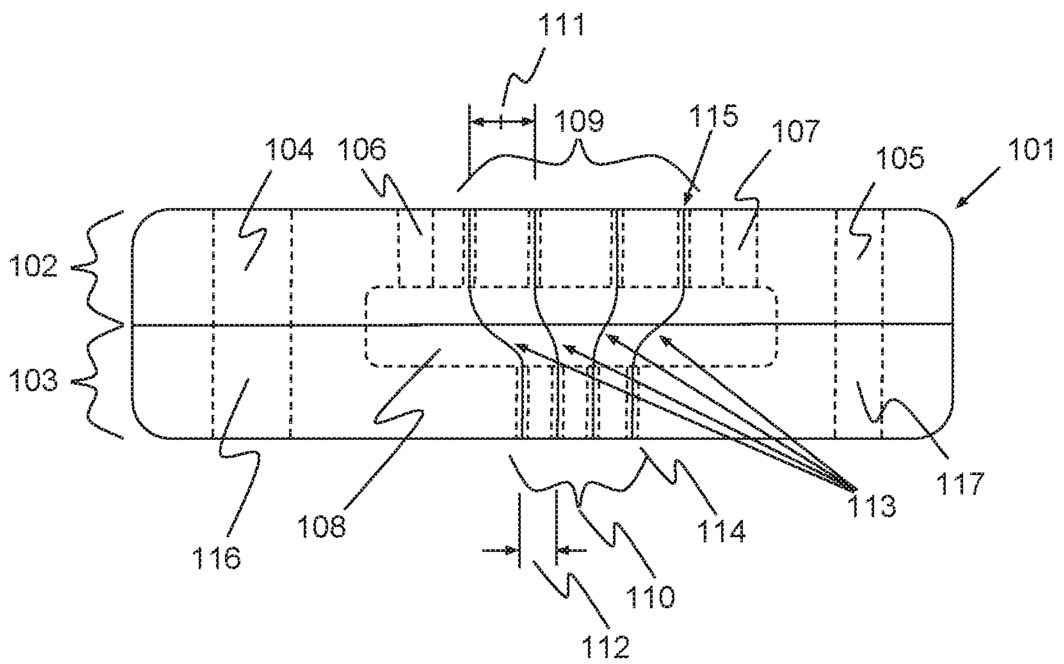


Fig. 1

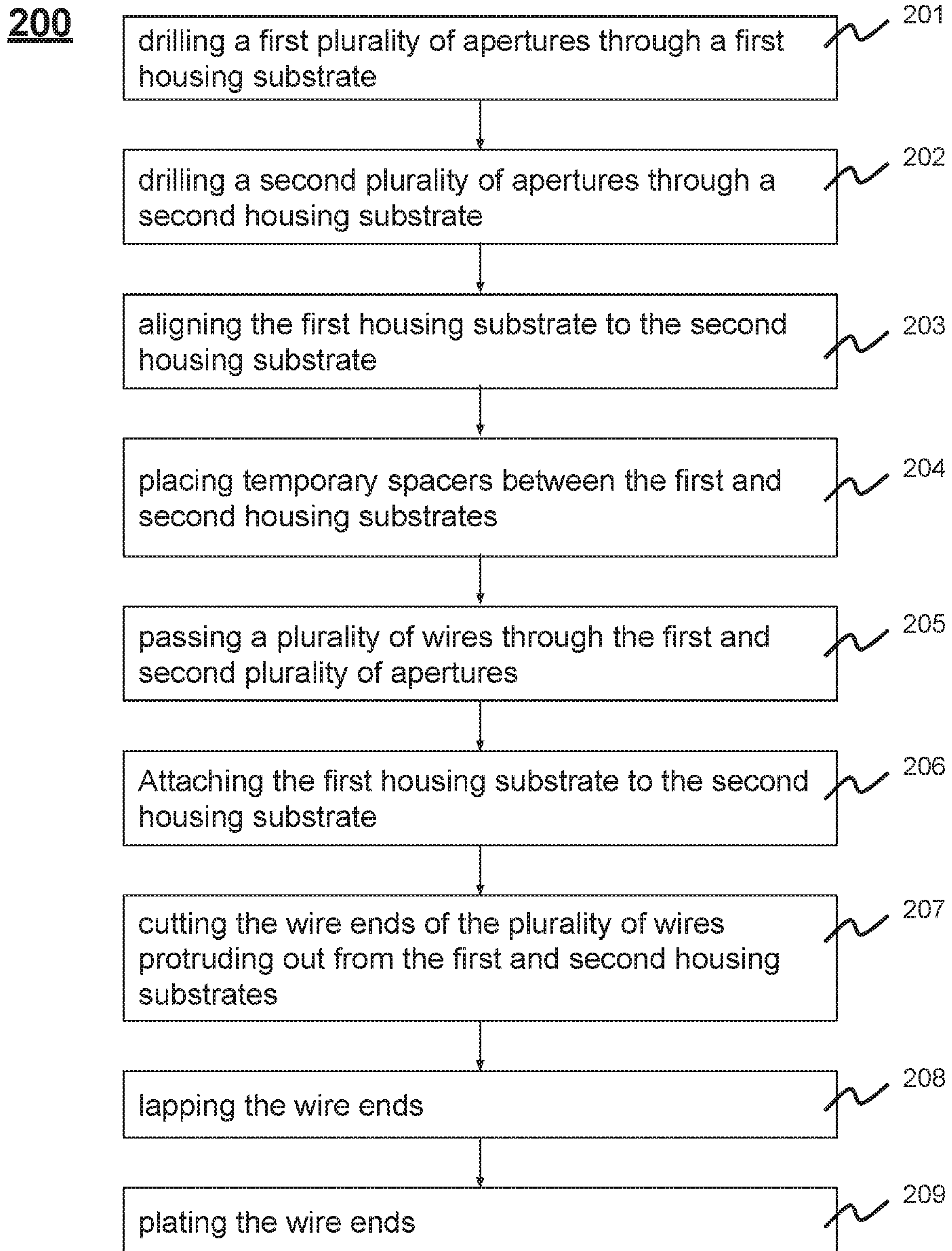


Fig. 2

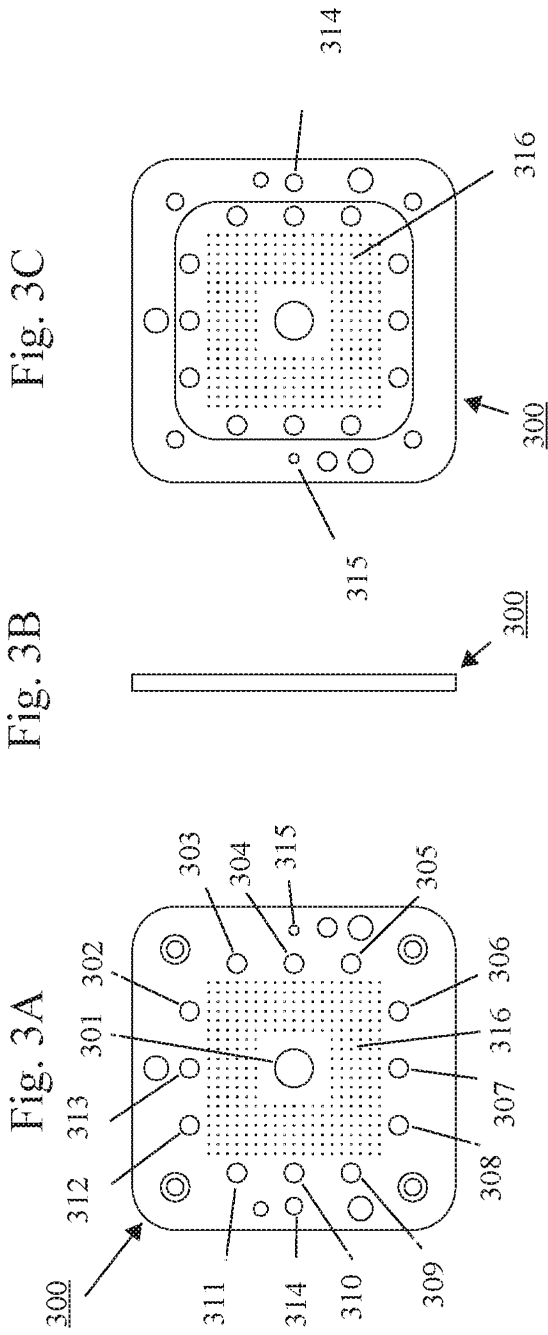


Fig. 3A

Fig. 3B

Fig. 3C

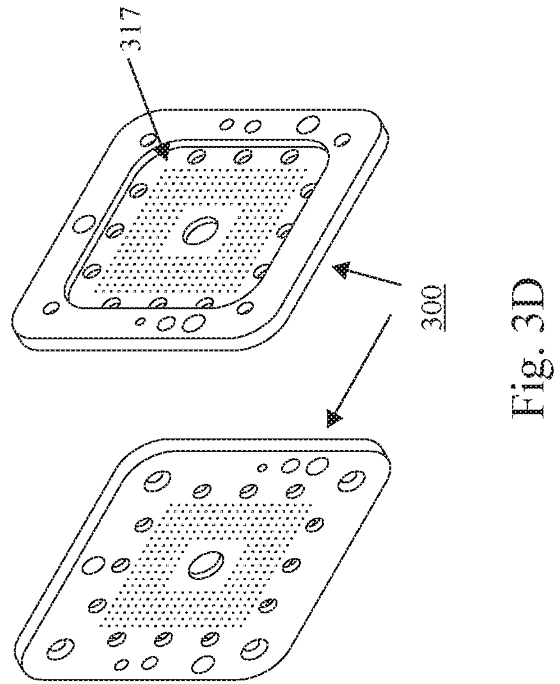


Fig. 3D

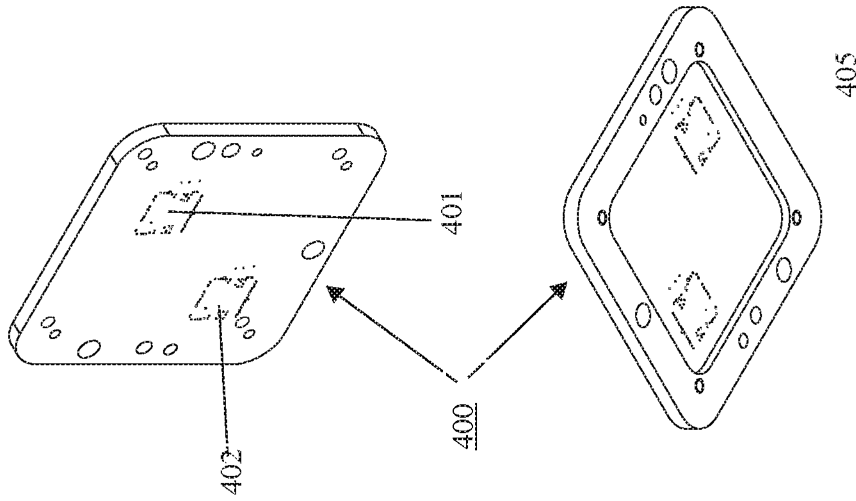


Fig. 4D

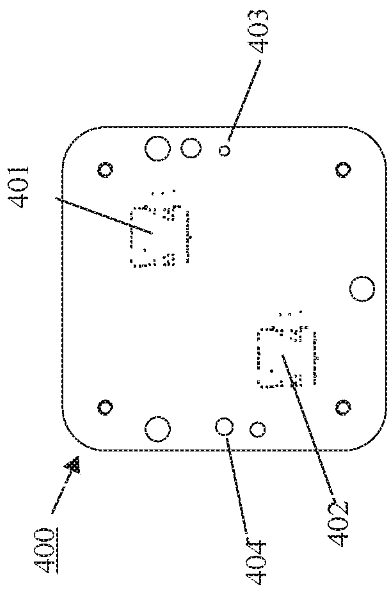


Fig. 4A

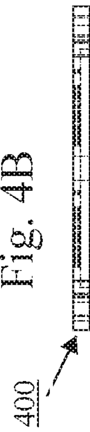


Fig. 4B

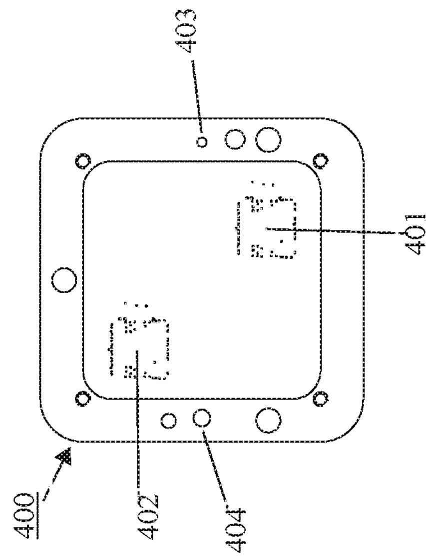


Fig. 4C

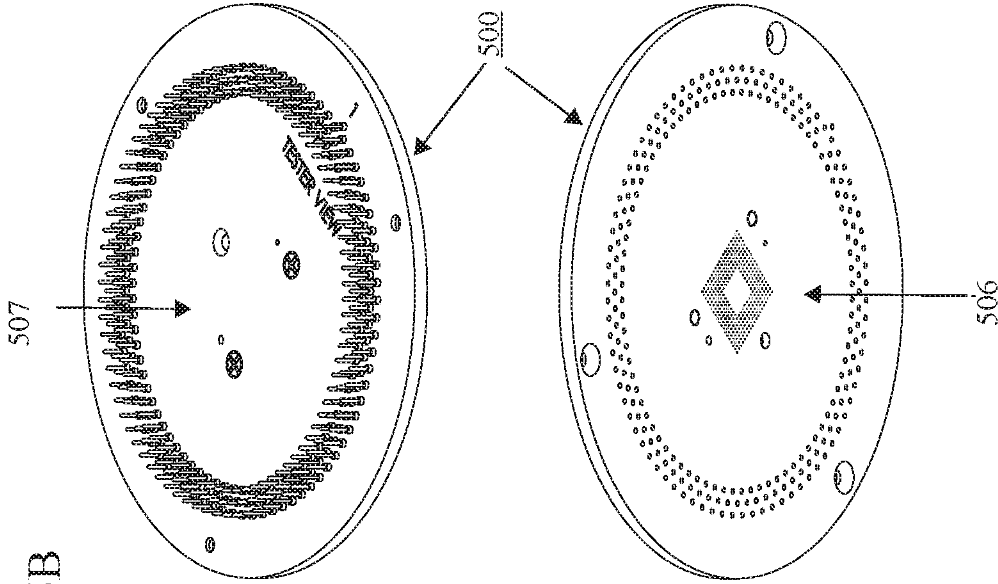


Fig. 5B
507
500
TESTER VIEW
506

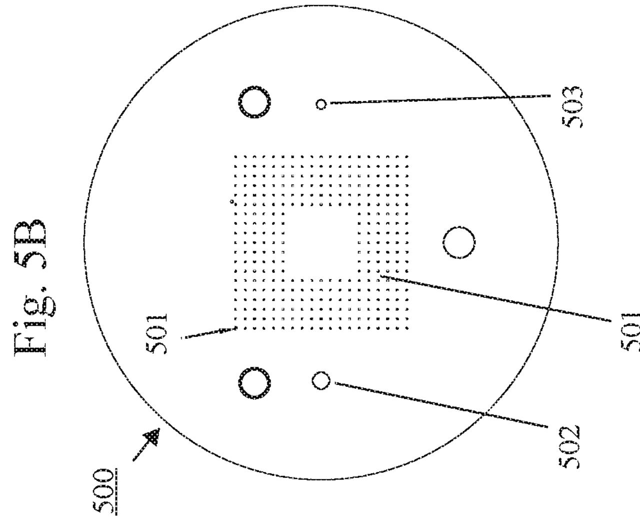


Fig. 5B
500
501
501
502
503

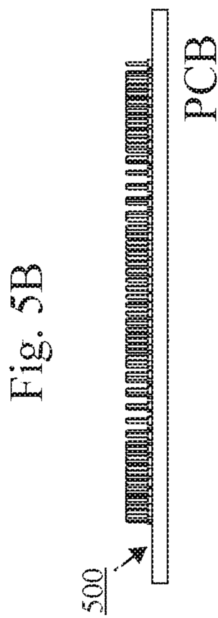


Fig. 5B
500
PCB

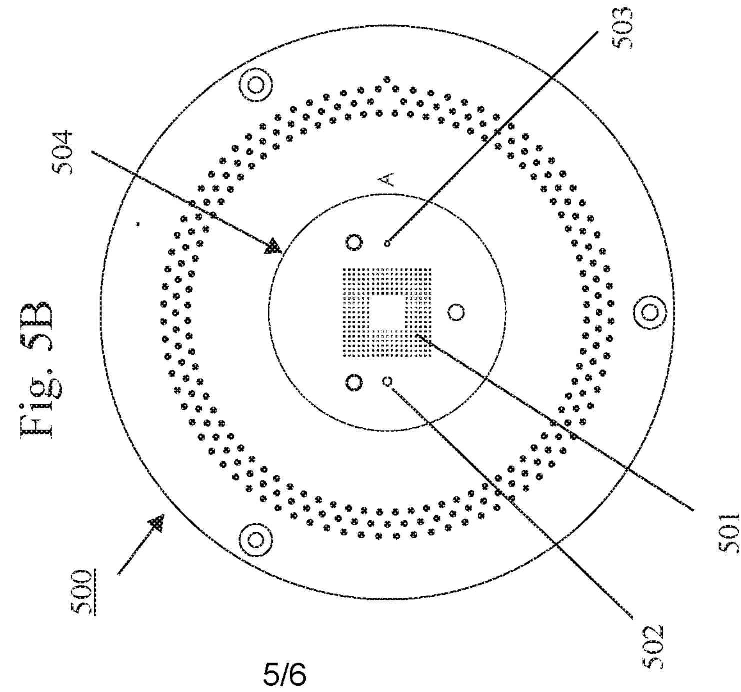


Fig. 5B
500
504
A
503
501
502

Fig. 6C

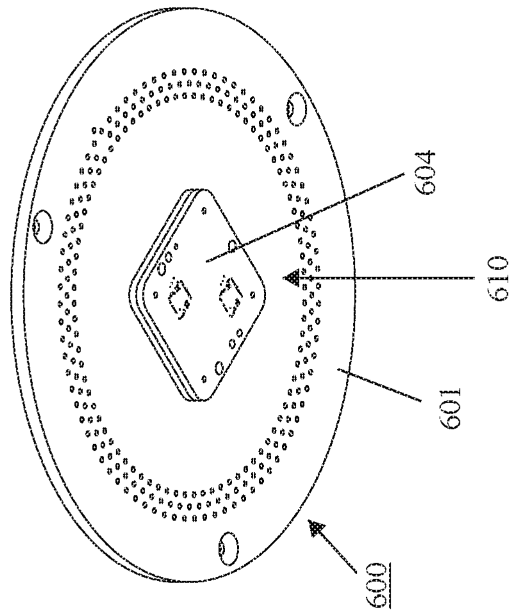
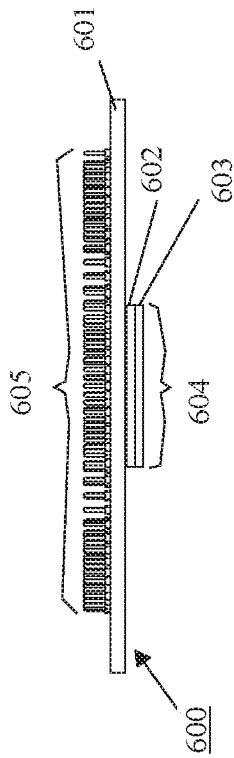


Fig. 6B



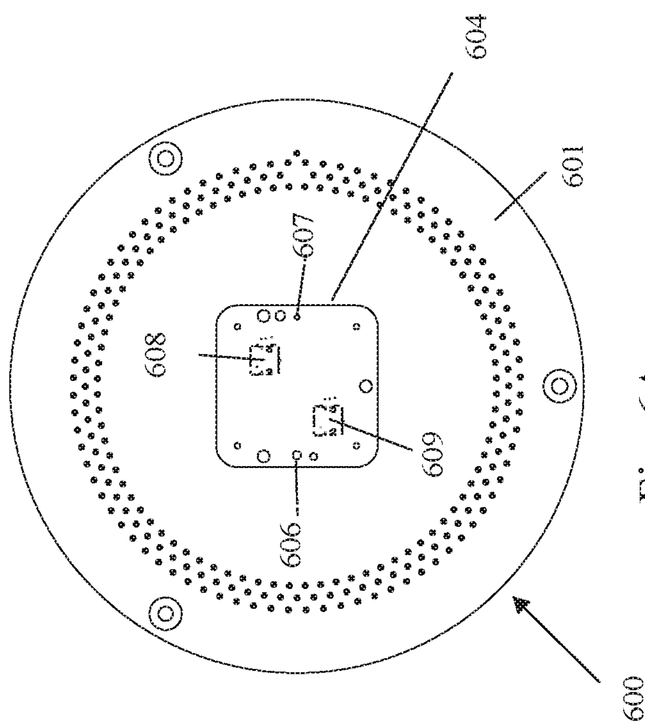


Fig. 6A

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/053603

A. CLASSIFICATION OF SUBJECT MATTER

G01R 1/073(2006.01)i, G01R 3/00(2006.01)i, G01R 31/28(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G01R 1/073; G01R 1/067; G01R 31/26; G01R 31/28; G01R 1/06; G01R 31/02; G01R 3/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: test, probe, semiconductor, aperture, pitch, wire

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2013-0082728 A1 (WANG) 04 April 2013 See abstract, paragraphs [24]-[30] and figures 4A-6D.	7-11
Y		1-6,12-20
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☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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09 January 2017 (09.01.2017)	**09 January 2017 (09.01.2017)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
KIM, Yeon Kyung
Telephone No. +82-42-481-3325

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
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