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Beffa

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(54) **METHOD FOR SORTING INTEGRATED CIRCUIT DEVICES**

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This patent is subject to a terminal disclaimer.

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Related U.S. Application Data

(60) Continuation of application No. 09/941,092, filed on Aug. 28, 2001, now Pat. No. 6,373,011, which is a continuation of application No. 09/713,912, filed on Nov. 15, 2000, now Pat. No. 6,365,861, which is a division of application No. 09/520,067, filed on Mar. 7, 2000, now Pat. No. 6,350,959, which is a continuation of application No. 09/133,338, filed on Aug. 13, 1998, now Pat. No. 6,100,486, which is a division of application No. 08/785,353, filed on Jan. 17, 1997, now Pat. No. 5,927,512.

(51) **Int. Cl.**
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(52) **U.S. Cl.** **209/571**; 209/573; 324/158.1; 324/765

(58) **Field of Classification Search** 209/571, 209/573; 324/158.1, 759, 764, 765; 700/96, 700/108, 109, 121
See application file for complete search history.

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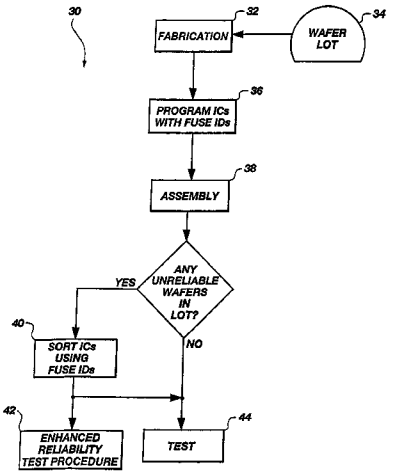
(57) **ABSTRACT**

A method for sorting integrated circuit (IC) devices of the type having a substantially unique identification (ID) code, such as a fuse ID, including automatically reading the ID code of each of the IC devices and sorting the IC devices in accordance with their automatically read ID codes, is disclosed.

3 Claims, 8 Drawing Sheets



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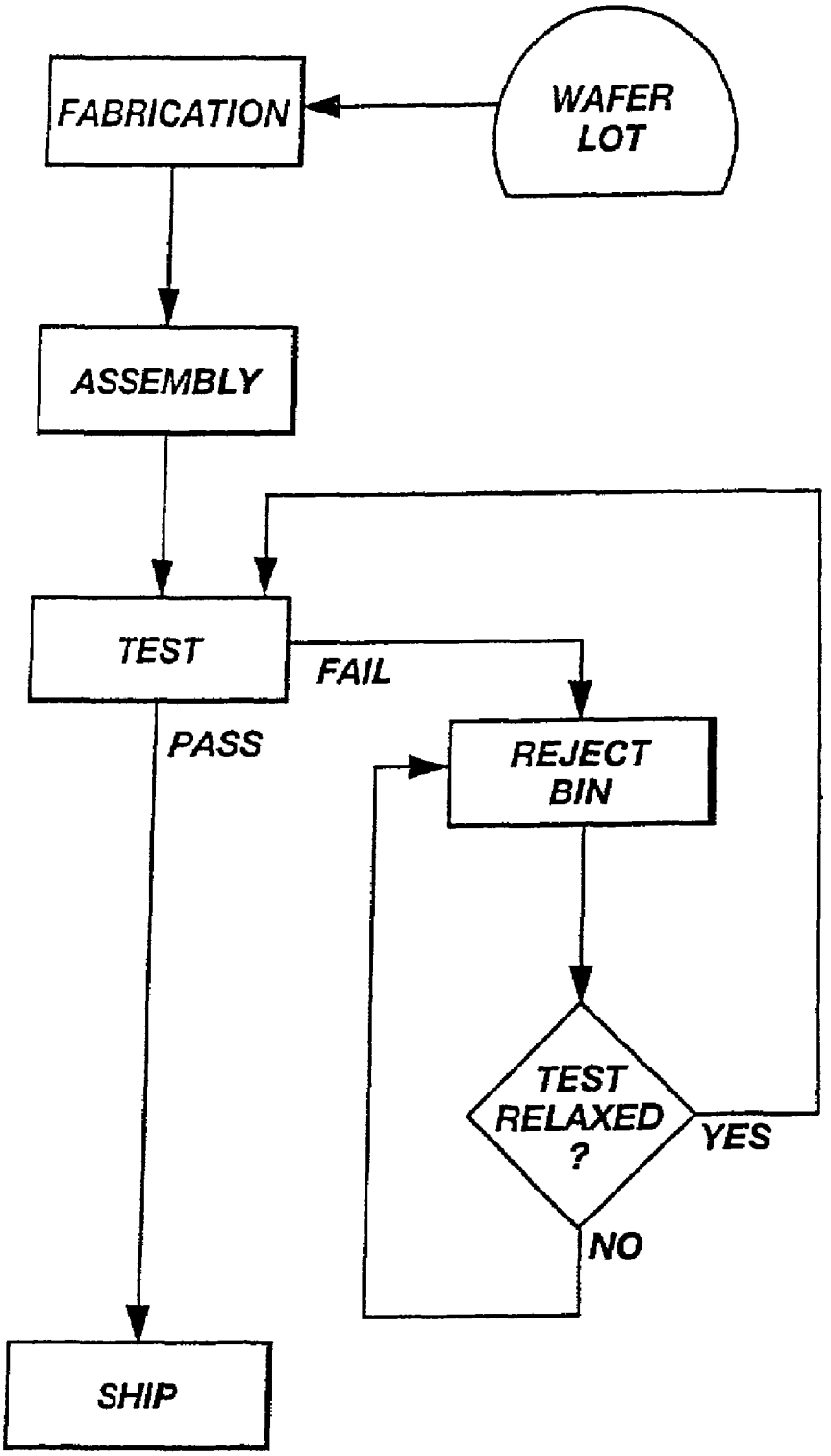


Fig. 1
(PRIOR ART)

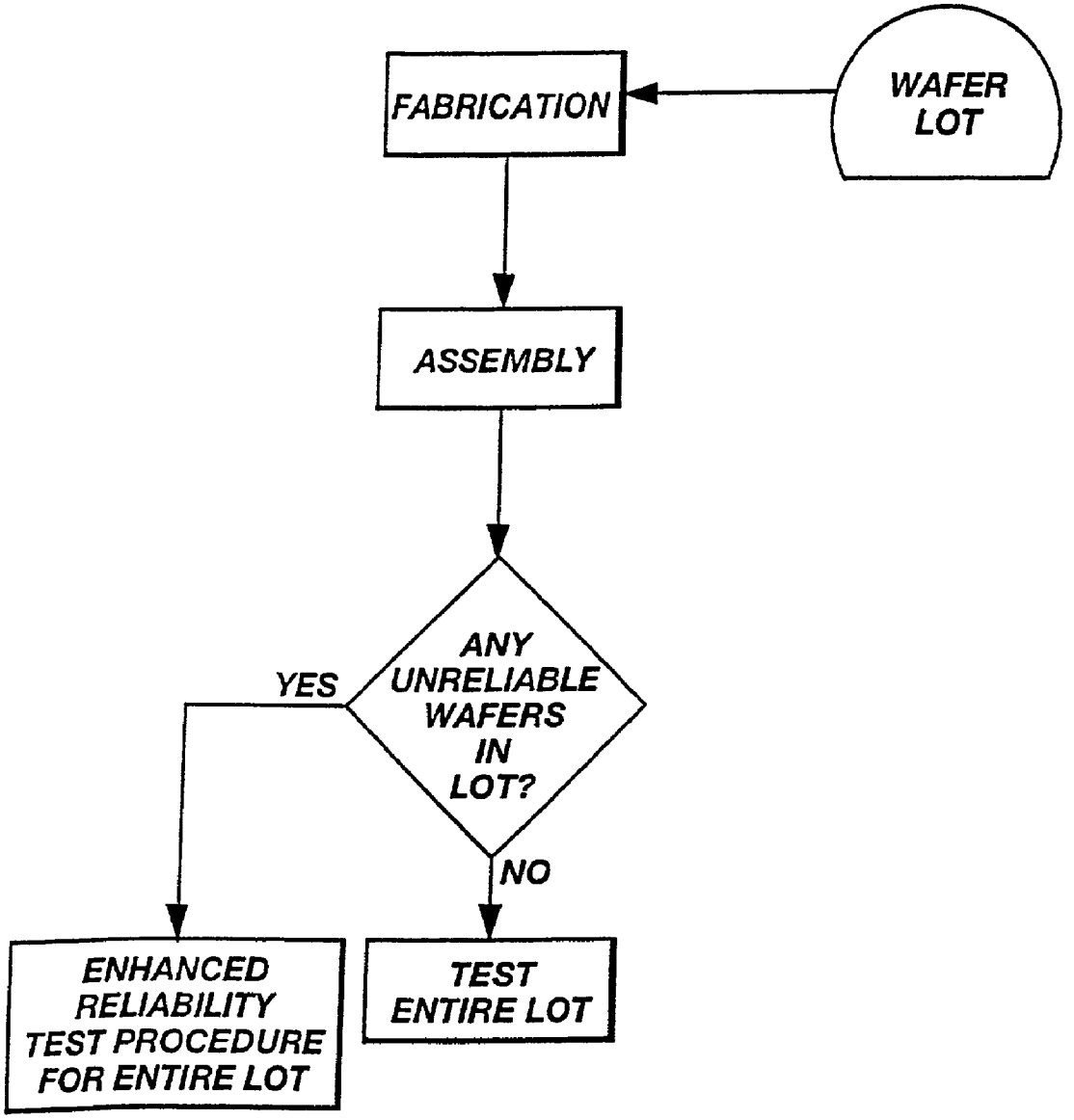


Fig. 2
(PRIOR ART)

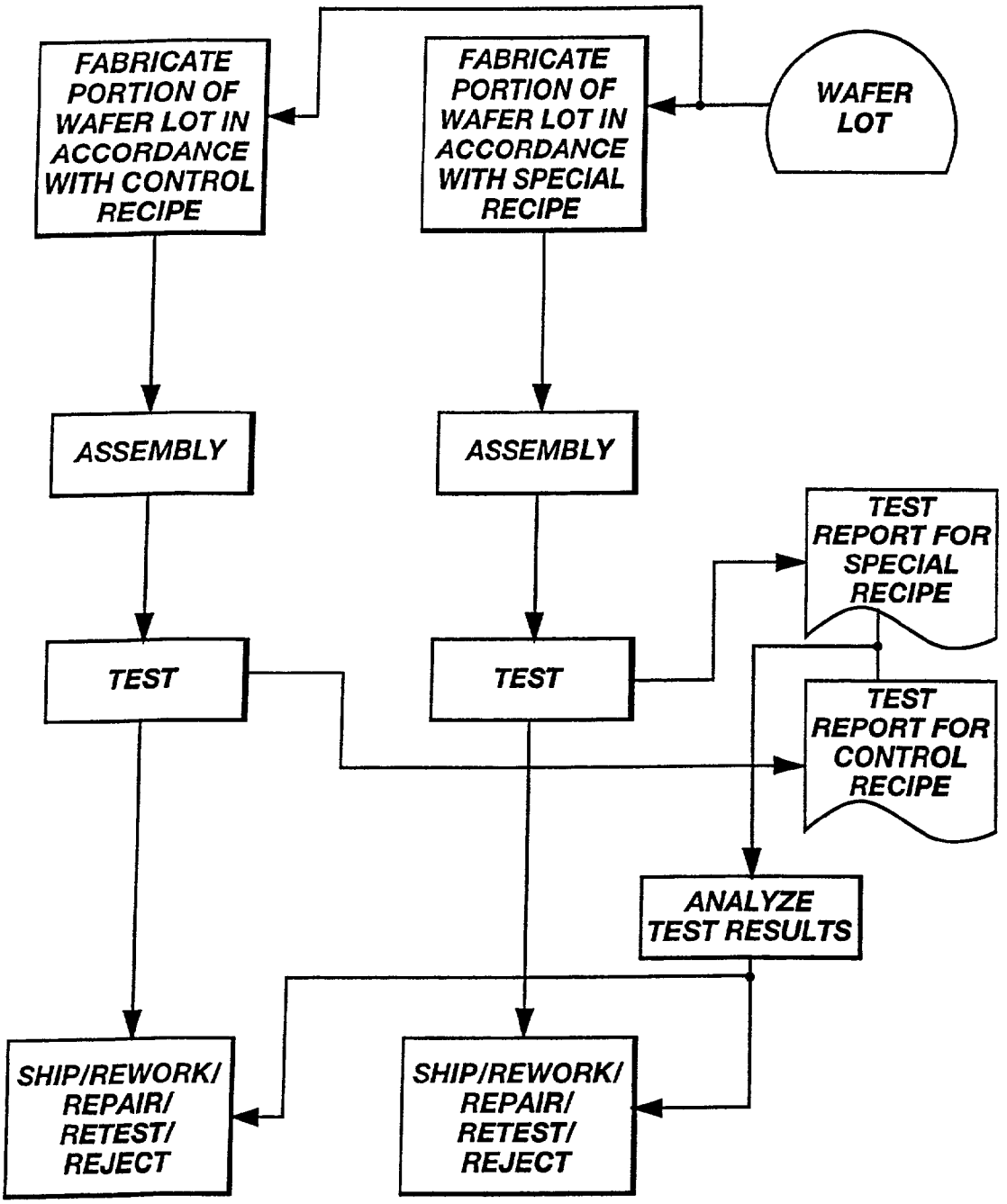


FIG. 3
(PRIOR ART)

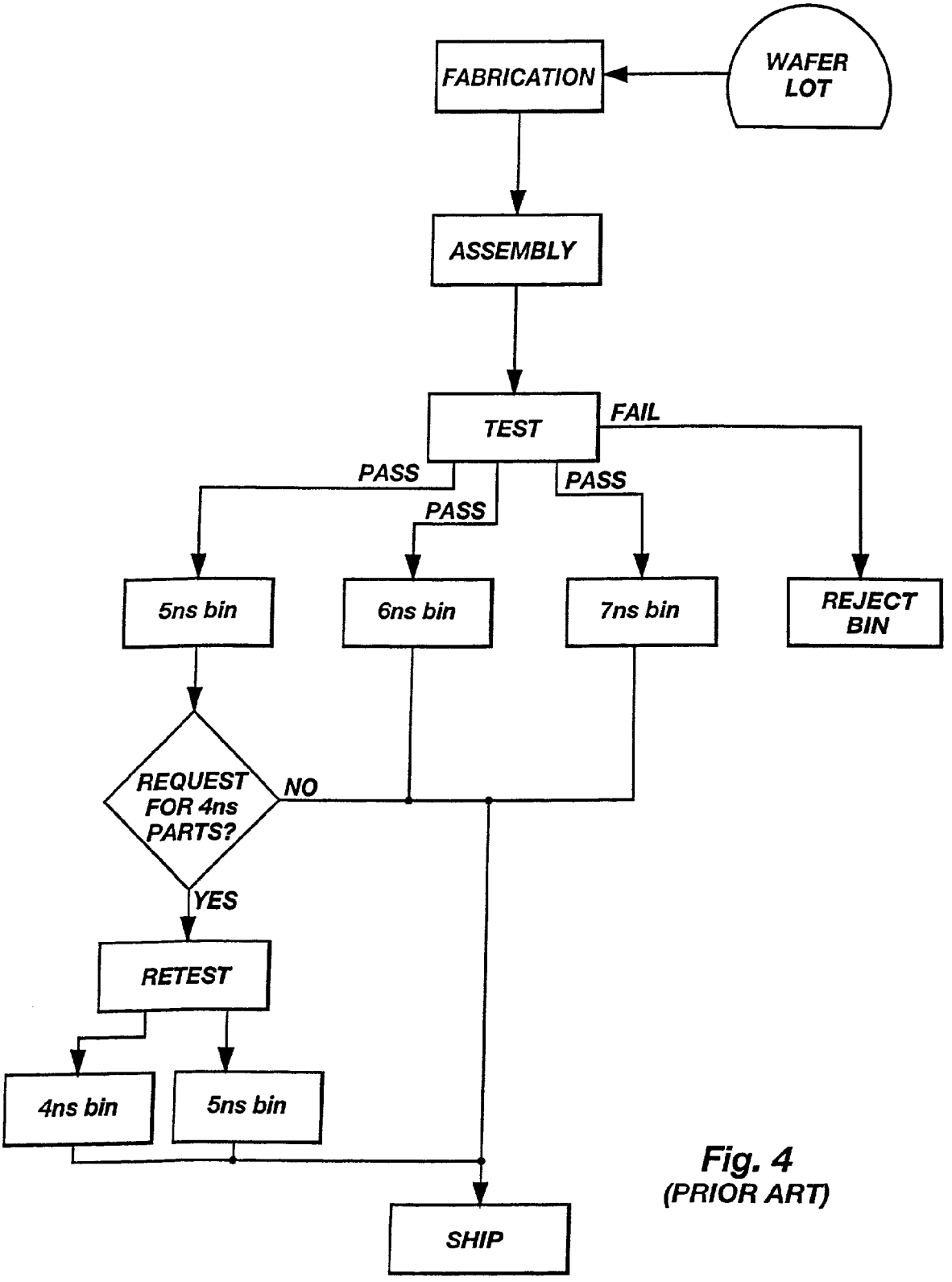


Fig. 4
(PRIOR ART)

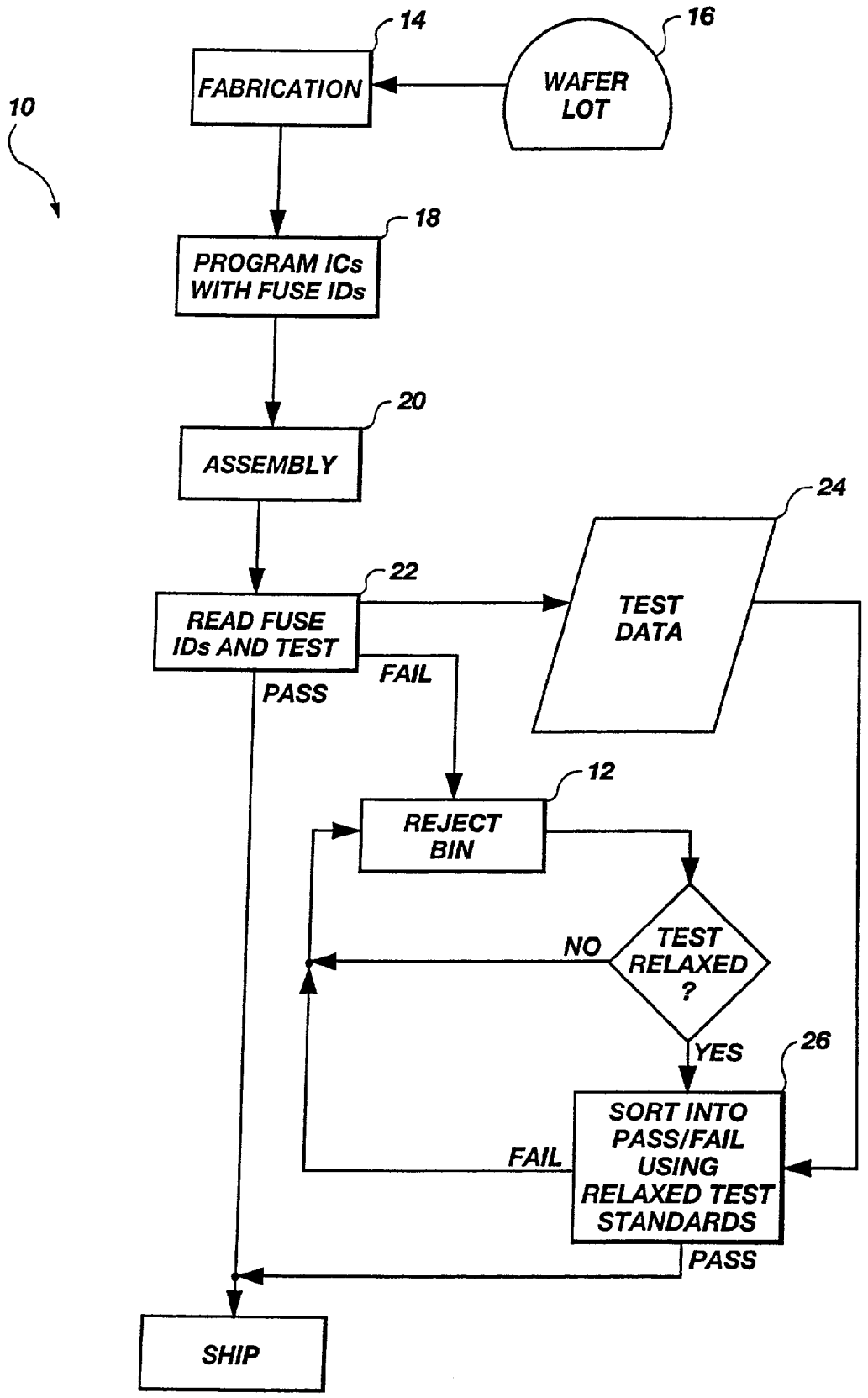

10
14
FABRICATION
16
WAFER LOT
18
PROGRAM ICs WITH FUSE IDs
20
ASSEMBLY
24
TEST DATA
22
READ FUSE IDs AND TEST
PASS
FAIL
12
REJECT BIN
NO
TEST RELAXED ?
YES
26
SORT INTO PASS/FAIL USING RELAXED TEST STANDARDS
FAIL
PASS
SHIP

Fig. 5

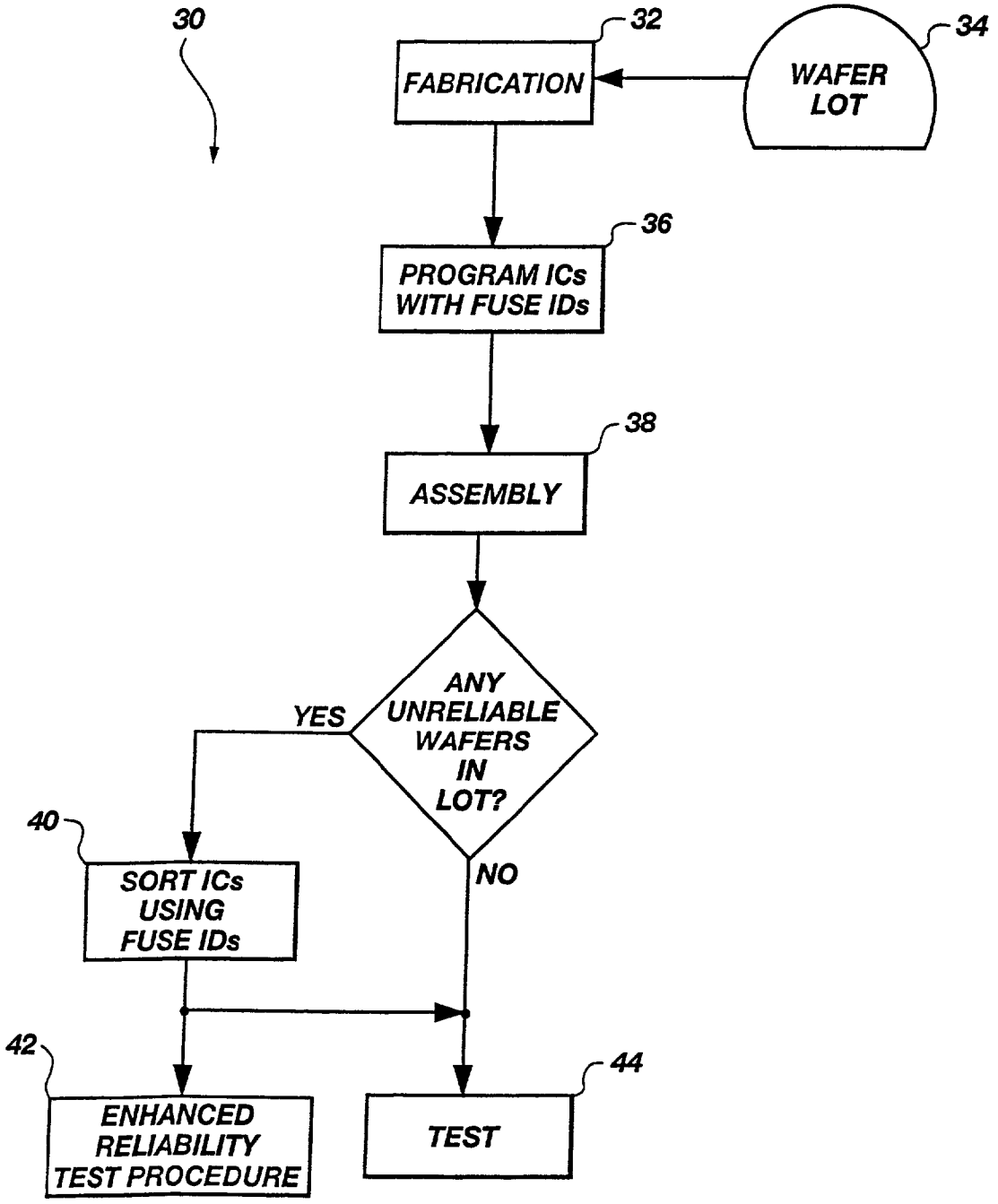

30
32
FABRICATION
34
WAFER LOT
36
PROGRAM ICs WITH FUSE IDs
38
ASSEMBLY
ANY UNRELIABLE WAFERS IN LOT?
YES
NO
40
SORT ICs USING FUSE IDs
42
ENHANCED RELIABILITY TEST PROCEDURE
44
TEST

Fig. 6

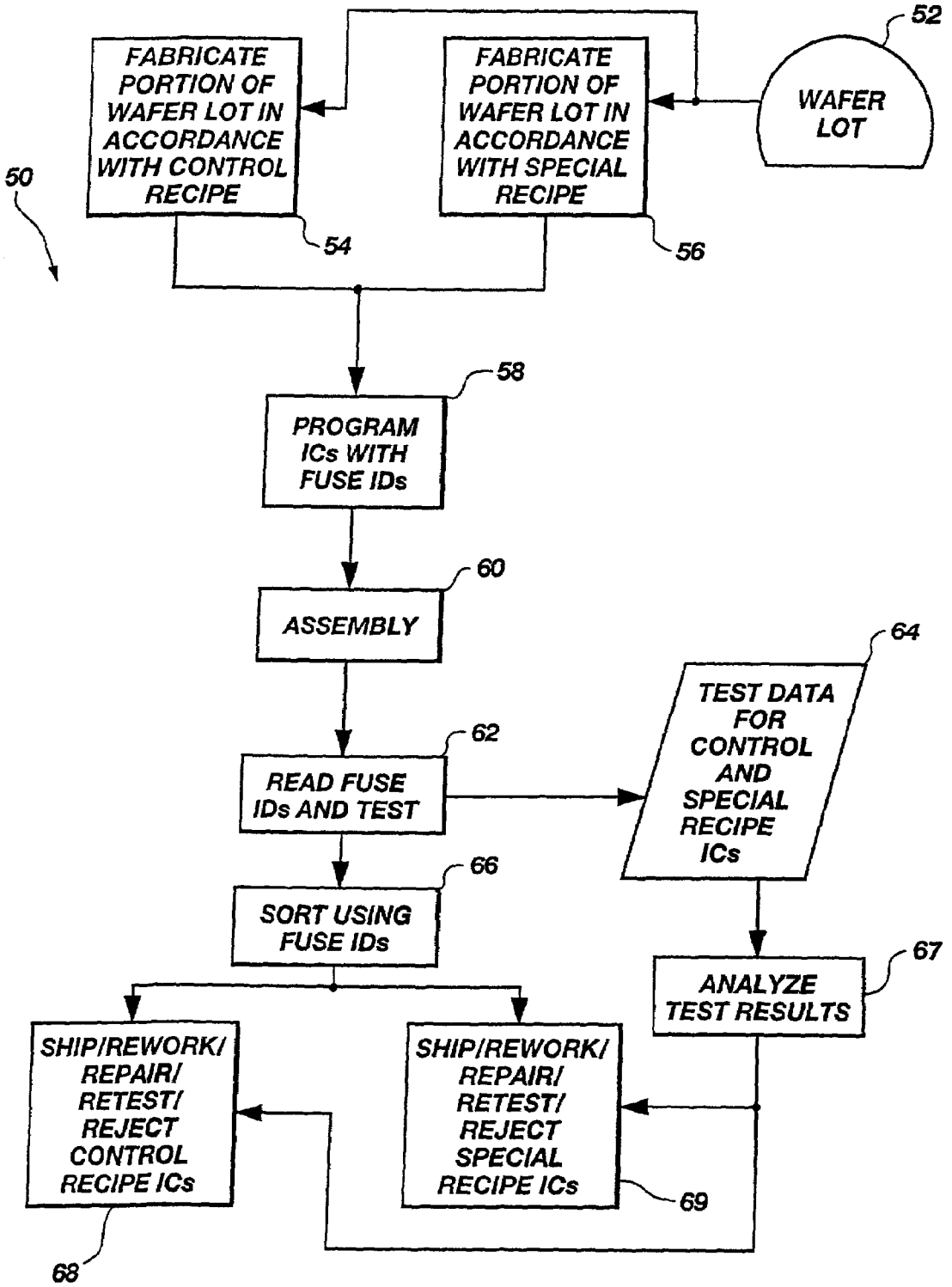

50
52
WAFER LOT
FABRICATE PORTION OF WAFER LOT IN ACCORDANCE WITH CONTROL RECIPE
54
FABRICATE PORTION OF WAFER LOT IN ACCORDANCE WITH SPECIAL RECIPE
56
58
PROGRAM ICs WITH FUSE IDs
60
ASSEMBLY
62
READ FUSE IDs AND TEST
64
TEST DATA FOR CONTROL AND SPECIAL RECIPE ICs
66
SORT USING FUSE IDs
67
ANALYZE TEST RESULTS
SHIP/REWORK/ REPAIR/ RETEST/ REJECT CONTROL RECIPE ICs
68
SHIP/REWORK/ REPAIR/ RETEST/ REJECT SPECIAL RECIPE ICs
69

Fig. 7

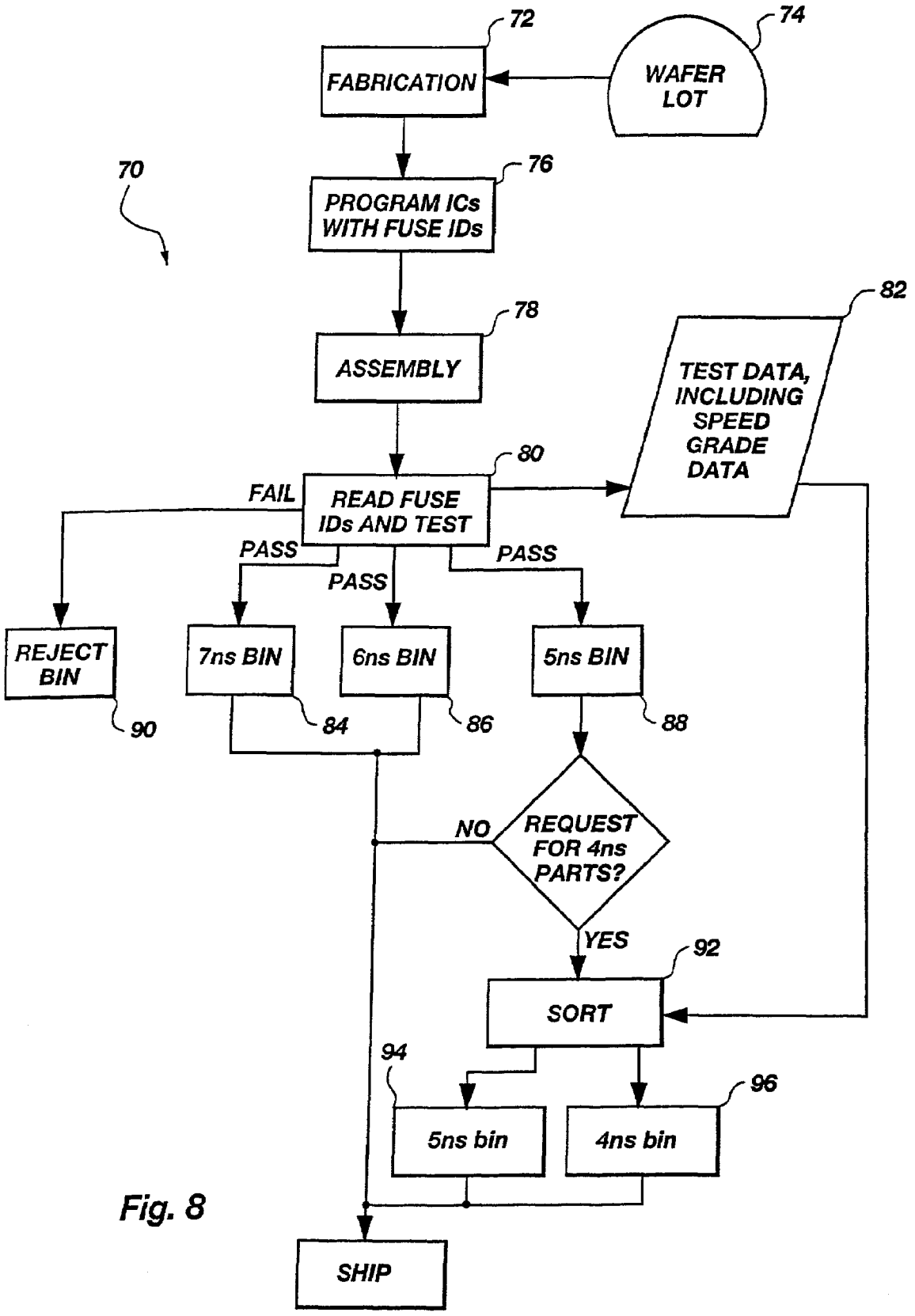

70
72
FABRICATION
74
WAFER LOT
76
PROGRAM ICs WITH FUSE IDs
78
ASSEMBLY
82
TEST DATA, INCLUDING SPEED GRADE DATA
80
READ FUSE IDs AND TEST
FAIL
PASS
PASS
PASS
REJECT BIN
90
7ns BIN
84
6ns BIN
86
5ns BIN
88
NO
REQUEST FOR 4ns PARTS?
YES
92
SORT
94
5ns bin
96
4ns bin
SHIP

Fig. 8

METHOD FOR SORTING INTEGRATED CIRCUIT DEVICES

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of application Ser. No. 09/941,092, filed Aug. 28, 2001, now U.S. Pat. No. 6,373,011 B1, issued Apr. 16, 2002, which is a continuation of application Ser. No. 09/713,912, filed Nov. 15, 2000, now U.S. Pat. No. 6,365,861 B1, issued Apr. 2, 2002, which is a division of application Ser. No. 09/520,067, filed Mar. 7, 2000, now U.S. Pat. No. 6,350,959 B1, issued Feb. 26, 2002, which is a continuation of application Ser. No. 09/133,338, filed Aug. 13, 1998, now U.S. Pat. No. 6,100,486, issued Aug. 8, 2000, which is a division of application Ser. No. 08/785,353, filed Jan. 17, 1997, now U.S. Pat. No. 5,927,512, issued Jul. 27, 1999.

The present application is also related to: application Ser. No. 08/591,238, filed Jan. 17, 1996, now abandoned; application Ser. No. 08/664,109, filed Jun. 13, 1996, now U.S. Pat. No. 5,895,962, issued Apr. 20, 1999; a divisional application having Ser. No. 09/133,336, filed Aug. 13, 1998, now U.S. Pat. No. 6,147,316, issued Nov. 14, 2000; a application having Ser. No. 08/822,731, filed Mar. 24, 1997, now U.S. Pat. No. 5,856,923, issued Jan. 5, 1999; a application having Ser. No. 08/806,442, filed Feb. 26, 1997, now U.S. Pat. No. 5,915,231, issued Jun. 22, 1999; a application having Ser. No. 08/871,015, filed Jun. 6, 1997, now U.S. Pat. No. 5,907,492, issued May 25, 1999; and a application having Ser. No. 08/801,565 filed Feb. 17, 1997, now U.S. Pat. No. 5,844,803, issued Dec. 1, 1998.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates in general to integrated circuit (IC) manufacturing and, more specifically, to methods in IC manufacturing processes for sorting IC devices using identification (ID) codes, such as fuse IDs, in the devices.

2. State of the Art

Integrated circuits (ICs) are small electronic circuits formed on the surface of a wafer of semiconductor material, such as silicon, in an IC manufacturing process referred to as "fabrication." Once fabricated, ICs are electronically probed to evaluate a variety of their electronic characteristics, cut from the wafer on which they were formed into discrete IC dice or "chips," and then assembled for customer use using various well-known IC packaging techniques, including lead frame packaging, Chip-On-Board (COB) packaging, and flip-chip packaging.

Before being shipped to customers, packaged ICs are generally tested to ensure they will function properly once shipped. Testing typically involves a variety of known test steps, such as pre-grade, burn-in, and final, which test ICs for defects and functionality and grade ICs for speed. As shown in FIG. **1**, ICs that pass the described testing are generally shipped to customers, while ICs that fail the testing are typically rejected.

The testing standards for a particular IC product are sometimes relaxed as the product "matures," such that ICs previously rejected under strict testing standards may pass the relaxed testing standards. Consequently, reject bins containing previously rejected ICs are sometimes "culled" for ICs that are shippable under relaxed testing standards by testing the rejected ICs again using the relaxed testing standards. Unfortunately, while this culling process does retrieve shippable ICs from reject bins, it makes inefficient use of expensive and often limited testing resources by diverting those resources away from testing untested ICs in order to retest previously rejected ICs. Therefore, there is a need in the art for an improved method of culling or sorting such reject bins for shippable ICs.

Similarly, as shown in FIG. **2**, all the ICs from the wafers in a wafer lot typically undergo enhanced reliability testing that is more extensive and strict than normal testing when any of the wafers in the lot are deemed to be unreliable because of fabrication or other process errors. Since a wafer lot typically consists 50 or more wafers, many of the ICs that undergo the enhanced reliability testing do not require it because they come from wafers that are not deemed unreliable. Performing enhanced reliability testing on ICs that do not need it is inefficient because such testing is typically more time-consuming and uses more resources than normal testing. Therefore, there is a need in the art for a method of sorting ICs from a wafer lot into those ICs that require enhanced reliability testing and those that do not.

Likewise, as shown in FIG. **3**, a new or special "recipe" for fabricating ICs on wafers is sometimes tested by fabricating some wafers from a wafer lot using the special recipe and other wafers from the wafer lot using a control recipe. ICs from the wafers then typically undergo separate assembly and test procedures so that the test results of ICs fabricated using the special recipe are not mixed with the test results of ICs fabricated using the control recipe, and vice versa. Test reports from the separate test procedures are then used to evaluate the special recipe and to determine whether the ICs are to be shipped to customers, reworked, repaired, retested, or rejected. Unfortunately, because the ICs undergo separate test and assembly procedures, undesirable variables, such as differences in assembly and test equipment, are introduced into the testing of the special recipe. It would be desirable, instead, to be able to assemble and test the ICs using the same assembly and test procedures, and to then sort the ICs and their test results into those ICs fabricated using the special recipe and those ICs fabricated using the control recipe. Therefore, there is a need in the art for a method of identifying individual ICs fabricated using a special or control recipe and sorting the ICs based on their fabrication recipe.

As described above, ICs are typically tested for various characteristics before being shipped to customers. For example, as shown in FIG. **4**, ICs may be graded in test for speed and placed in various bins (e.g., 5 nanoseconds (ns), 6 ns, and 7 ns bins) according to their grading. If a customer subsequently requests a more stringent speed grade (e.g., 4 ns), ICs in one of the bins (e.g., a 5 ns bin) are retested and thereby sorted into ICs that meet the more stringent speed grade (e.g., 4 ns bin) and those that do not (e.g., 5 ns bin). While this conventional process sorts the ICs into separate speed grades, it makes inefficient use of expensive and often limited testing resources by diverting those resources away from testing untested ICs in order to retest previously tested ICs. Therefore, there is a need in the art for an improved method of culling or sorting bins for ICs that meet more stringent standards, such as a higher speed grading.

As described in U.S. Pat. Nos. 5,301,143, 5,294,812, and 5,103,166, some methods have been devised to electronically identify individual ICs. Such methods take place "off" the manufacturing line and involve the use of electrically retrievable ID codes, such as so-called "fuse IDs," programmed into individual ICs to identify the ICs. The programming of a fuse ID typically involves selectively blowing an arrangement of fuses and anti-fuses in an IC so that when the fuses or anti-fuses are accessed, they output a selected ID code. Unfortu-

nately, none of these methods address the problem of identifying and sorting ICs "on" a manufacturing line.

BRIEF SUMMARY OF THE INVENTION

An inventive method for sorting integrated circuit (IC) devices of the type to have a substantially unique identification (ID) code, such as a fuse ID, including automatically reading the ID code of each of the IC devices and sorting the IC devices according to their automatically read ID codes. The inventive method can be used in conjunction with an IC manufacturing process that includes providing semiconductor wafers, fabricating the ICs on each of the wafers, causing each of the ICs to store its ID code, separating each of the ICs from its wafer to form an IC die, assembling the IC dice into IC devices, and testing the IC devices. The method can also be used in conjunction with Single In-line Memory Module (SIMM), Dual In-line Memory Module (DIMM), and other multi-chip module (MCM) manufacturing processes.

In another embodiment, an inventive method for recovering IC devices from a group of IC devices that have previously been rejected in accordance with a test standard that has since been relaxed includes: storing test results that caused each of the IC devices in the group to be rejected in connection with an ID code, such as a fuse ID, associated with each device; automatically reading the ID code from each of the IC devices; accessing the test results stored in connection with each of the automatically read ID codes; comparing the accessed test results for each of the IC devices with the relaxed test standard; and sorting the IC devices according to whether their accessed test results pass the relaxed test standard in order to recover any of the IC devices having test results that pass the relaxed test standard.

By sorting the IC devices in accordance with their previously stored test results and their ID codes, the above-described inventive method eliminates the need to retest the IC devices after the test standard is relaxed in order to cull shippable IC devices from the rejected devices.

In still another embodiment, a method for sorting a group of IC devices in accordance with a first IC standard, such as a speed standard, that have previously been sorted in accordance with a second IC standard, such as a speed standard is less stringent than the first IC standard, includes storing test results that caused each of the IC devices in the group to be sorted into the group in connection with ID codes, such as fuse IDs, of the devices, automatically reading the ID code from each of the IC devices, accessing the test results stored in connection with each of the automatically read ID codes, comparing the accessed test results for each of the IC devices with the first IC standard, and sorting the IC devices according to whether their test results pass the first IC standard.

In a further embodiment, an inventive back-end test method for separating IC devices in need of enhanced reliability testing from a group of IC devices undergoing back-end test procedures includes: storing a flag in connection with an ID code, such as a fuse ID, associated with each of the IC devices in the group indicating whether each IC device is in need of enhanced reliability testing; automatically reading the ID code of each of the IC devices in the group; accessing the enhanced reliability testing flag stored in connection with each of the automatically read ID codes; and sorting the IC devices in accordance with whether their enhanced reliability testing flag indicates that they are in need of enhanced reliability testing.

Thus, the inventive method described above provides an advantageous method for sorting ICs from the same wafer lot into those ICs that require enhanced reliability testing and those that do not.

In a still further embodiment, an inventive method in an IC manufacturing process for testing different fabrication process recipes includes the following: providing first and second pluralities of semiconductor wafers; fabricating a first plurality of ICs on each of the first plurality of wafers in accordance with a control recipe; fabricating a second plurality of ICs on each of the second plurality of wafers in accordance with a test recipe; causing each of the ICs on each of the wafers to permanently stOre a substantially unique ID code, such as a fuse ID; separating each of the ICs on each of the wafers from its wafer to form one of a plurality of IC dice; assembling each of the IC dice into an IC device; automatically reading the ID code from the IC in each of the IC devices; testing each of the IC devices; and sorting each of the IC devices in accordance with the automatically read ID code from the IC in each of the IC devices indicating that the IC is from one of the first and second pluralities of ICs.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

FIG. **1** is a flow diagram illustrating a conventional procedure in an integrated circuit (IC) manufacturing process for culling shippable ICs from a reject bin;

FIG. **2** is a flow diagram illustrating a conventional procedure in an IC manufacturing process for directing ICs to enhanced reliability testing;

FIG. **3** is a flow diagram illustrating a conventional procedure in an IC manufacturing process for testing a new or special fabrication process recipe;

FIG. **4** is a flow diagram illustrating a conventional procedure in an IC manufacturing process for speed sorting ICs;

FIG. **5** is a flow diagram illustrating a procedure in an integrated circuit (IC) manufacturing process for culling shippable ICs from a reject bin in accordance with the present invention;

FIG. **6** is a flow diagram illustrating a procedure in an IC manufacturing process for directing ICs to enhanced reliability testing in accordance with another embodiment of the present invention;

FIG. **7** is a flow diagram illustrating a procedure in an IC manufacturing process for testing a new or special fabrication process recipe in accordance with still another embodiment of the present invention; and

FIG. **8** is a flow diagram illustrating a procedure in an IC manufacturing process for speed sorting ICs in accordance with a further embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

As shown in FIG. **5**, an inventive method for sorting integrated circuit (IC) devices is embodied in a method **10** in an IC manufacturing process for culling shippable ICs from a reject bin **12**. It will be understood by those having skill in the field of this invention that the present invention is applicable to sorting any IC devices, including Dynamic Random Access Memory (DRAM) ICs, Static Random Access Memory (SRAM) ICs, Synchronous DRAM (SDRAM) ICs, processor ICs, Single In-line Memory Modules (SIMMs), Dual In-line Memory Modules (DIMMs), and other Multi-Chip Modules (MCMs).

The method **10** includes the step of fabricating **14** ICs on wafers from a wafer lot **16**. ICs fabricated on the wafers are

then programmed in a program step **18** in the manner described above with a fuse identification (ID) unique to each IC. The fuse ID may identify a wafer lot ID, the week the ICs were fabricated, a wafer ID, a die location on the wafer, and a fabrication facility ID. It will be understood, of course, that the present invention includes within its scope ICs having any ID code, including those having fuse IDs. It will also be understood that the ID code for each IC need not be unique, but instead may only specify the wafer the IC comes from, for example.

Once programmed, the ICs proceed through an assembly step **20** to a test step **22** where the fuse IDs are automatically read and stored in association with test data **24** generated in the test step **22**. Although the fuse IDs are typically read electronically, it will be understood that they may also be read optically if the fuse ID consists of "blown" laser fuses that are optically accessible. It will also be understood that the test data **24** may include data such as the following: data identifying the testing equipment that tested the ICs, operating personnel who operated the testing equipment, and the set-up of the equipment when the ICs were tested; and data indicating the time and date the ICs were tested, the yield of shippable ICs through the test step **22**, and test results for the ICs from the various stages of the test step **22**.

ICs that pass the test step **22** are typically shipped to customers, while those that fail the test step **22** are directed to the reject bin **12**. At a point in time when test standards of the test step **22** have been relaxed as described above, the ICs in the reject bin **12** are sorted in a sort step **26** by reading the fuse ID of each IC, accessing the test data **24** associated with the fuse ID, and comparing the accessed test data **24** with the relaxed test standards. Those ICs that fail even the relaxed test standards are directed back to the reject bin **12**, while those ICs that pass the relaxed test standards are typically shipped to customers. The method **10** thus successfully culls shippable ICs from the reject bin **12** without retesting the ICs.

As shown in FIG. **6**, the inventive sorting method is also embodied in a back-end (i.e., after fabrication) test method **30** for separating ICs in need of enhanced reliability testing from a group of ICs undergoing back-end test procedures. ICs typically require enhanced reliability testing because the wafer they come from is unreliable as a result of fabrication errors and other unintended manufacturing process deviations.

The method **30** includes the step **32** of fabricating ICs on wafers from a wafer lot **34**. ICs fabricated on the wafers are then programmed in a program step **36** in the manner described above with a fuse identification (ID) unique to each IC. The fuse ID may identify a wafer lot ID, the week the ICs were fabricated, a wafer ID, a die location on the wafer, and a fabrication facility ID. It will be understood, of course, that the present invention includes within its scope ICs having any ID code, including those having fuse IDs. It will also be understood that the ID code for each IC need not be unique, but instead may only specify the wafer the IC comes from, for example.

Once programmed, the ICs proceed through an assembly step **38**. At this point in the IC manufacturing process, it is not uncommon for a number of wafers to have been identified as being unreliable for the reasons stated above. The fuse IDs of the ICs that come from these unreliable wafers may then be associated with a stored flag indicating the ICs come from unreliable wafers. If any wafers in the wafer lot **34** have been identified as being unreliable, the ICs proceed to a sort step **40**, where their fuse IDs are automatically read so the ICs can be sorted into those flagged as coming from the unreliable wafers that require processing through an enhanced reliability testing step **42** and those not flagged as coming from the unreliable wafers that may proceed through a standard test step **44**. Of course, those ICs that pass either the standard test step **44** or the enhanced reliability testing step **42** are typically shipped to customers, while those that fail these steps are directed to a reject bin (not shown).

Thus, the present invention provides a method **30** that directs those ICs needing enhanced reliability testing to the enhanced reliability testing step **42**, while allowing those that do not require enhanced reliability testing to proceed through the standard testing step **44**.

As shown in FIG. **7**, the inventive sorting method is further embodied in a method **50** for testing different fabrication process recipes. Such testing is typically done in accordance with a Special Work Request (SWR) from an engineer or technician.

The method **50** includes fabricating some of the wafers from a wafer lot **52** in a fabrication step **54** in accordance with a control process recipe that is typically the normal process recipe in use in the IC manufacturing process at the time. The remainder of the wafers from the wafer lot **52** is fabricated in another fabrication step **56** in accordance with a special or test process recipe. The special or test process recipe may change a variety of variables in the fabrication process, including doping, the thickness of IC layers, etc.

Once the ICs are fabricated in the fabrication steps **54** and **56**, the ICs are then programmed in a program step **58** in the manner described above with a fuse identification (ID) unique to each IC. The fuse ID may identify a wafer lot ID, the week the ICs were fabricated, a wafer ID, a die location on the wafer, and a fabrication facility ID. It will be understood, of course, that the present invention includes within its scope ICs having any ID code, including those having fuse IDs. It will also be understood that the ID code for each IC need not be unique, but instead may only specify the wafer the IC comes from, for example.

Once programmed, ICs proceed through an assembly step **60** to a test step **62** where the fuse IDs are automatically read and stored in association with test data **64** generated for both the control recipe ICs and the special or test recipe ICs in the test step **62**. Although the fuse IDs are typically read electronically, it will be understood that they may also be read optically if the fuse ID consists of "blown" laser fuses that are optically accessible. It will also be understood that the test data **64** may include data such as the following: data identifying the testing equipment that tested the ICs, operating personnel who operated the testing equipment, and the set-up of the equipment when the ICs were tested; and data indicating the time and date the ICs were tested, the yield of shippable ICs through the test step **62**, and test results for the ICs from the various stages of the test step **62**.

Once the test data **64** is generated, the data **64** may be analyzed **67** to determine those ICs that are shippable and those that are not, and to determine any differences in test results between the control recipe ICs and the special or test recipe ICs. The ICs are sorted in a sort step **66** so they may be shipped, reworked, repaired, retested, or rejected in accordance with the analysis of the test results.

By sorting the control recipe **68** and special or test recipe **69** ICs at the end of the IC manufacturing process, the method **50** is able to assemble and test the ICs together and thus eliminate unintended variables introduced into the process of testing the special or test recipe by the conventional method of assembling and testing the ICs separately. The inventive method **50** thus provides more reliable test results.

As shown in FIG. **8**, the inventive method for sorting IC devices is also embodied in a method **70** in an IC manufac-

turing process for sorting IC devices in accordance with an IC standard, such as speed, that is more stringent than an IC standard that the devices were previously sorted in accordance with. It will be understood that although the method of FIG. **8** will be described with respect to speed sorting, the method is applicable to all situations in which ICs previously sorted in accordance with an IC standard, such as speed, need to be sorted in accordance with another, more stringent IC standard. Such IC standards may include, for example, access time, data setup time, data hold time, standby current, refresh current, and operating current.

The method **70** includes the step **72** of fabricating ICs on wafers from a wafer lot **74**. ICs fabricated on the wafers are then programmed in a program step **76** in the manner described above with a fuse identification (ID) unique to each IC. The fuse ID may identify a wafer lot ID, the week the ICs were fabricated, a wafer ID, a die location on the wafer, and a fabrication facility ID. It will be understood, of course, that the present invention includes within its scope ICs having any ID code, including those having fuse IDs.

Once programmed, the ICs proceed through an assembly step **78** to a test step **80** where the fuse IDs are automatically read and stored in association with test data **82** generated in the test step **80**. Although the fuse IDs are typically read electronically, it will be understood that they may also be read optically if the fuse ID consists of "blown" laser fuses that are optically accessible. It will also be understood that the test data **82** includes speed grading data for each IC, as described above, and may include data such as the following: data identifying the testing equipment that tested the ICs, operating personnel who operated the testing equipment, and the set-up of the equipment when the ICs were tested; and data indicating the time and date the ICs were tested, the yield of shippable ICs through the test step **80**, and test results for the ICs from the various stages of the test step **80**.

ICs that pass the test step **80** are typically directed to speed graded bins **84**, **86**, and **88**, while those that fail the test step **80** are directed to a reject bin **90**. The speed graded bins **84**, **86**, and **88** typically each contain ICs of varying speeds. For example, the bin **88** may contain a variety of 5.0 ns, 4.5 ns, 4.0 ns, 3.5 ns, etc. parts, the bin **86** may contain a variety of 6.0 ns, 5.5 ns, 5.1 ns, etc. parts, and the bin **84** may contain a variety of 7.0 ns, 6.5 ns, 6.1 ns, etc. parts.

On occasion, customers request ICs that meet a more stringent speed standard (e.g., 4 nanoseconds (ns)) than any of the ICs in the various bins **84**, **86**, and **88** have been graded for. While bin **88**, for example, may contain ICs that will meet the more stringent speed standard, the bin **88** cannot be used to supply the customer's request because the ICs in the bin **88** have only been graded (i.e., are guaranteed to meet or exceed) a lower speed standard (e.g., 5 ns). Therefore, the present inventive method **70** sorts the ICs in a sort step **92** by reading the fuse ID of each IC, accessing the test data **82**, including the speed grading data, associated with the fuse ID, and comparing the accessed speed grading data with the more stringent speed standard (e.g., 4 ns). Those ICs that fail the more stringent speed standard are directed to a speed graded bin **94**, while those ICs that pass the more stringent speed standard are directed to another speed graded bin **96** where they can be used to fill the customer's request. The inventive method **70** thus sorts the ICs in accordance with a more stringent IC standard, such as speed, than they were previously sorted in accordance with the present invention without having to retest the ICs, and thus without reusing valuable testing resources to retest ICs.

Although the present invention has been described with reference to particular embodiments, the invention is not limited to these described embodiments. For example, while the various steps of the embodiments of the inventive sorting method have been described as occurring in a particular order, it will be understood that these steps need not necessarily occur in the described order to fall within the scope of the present invention. Thus, the invention is limited only by the appended claims, which include within their scope, all equivalent methods that operate according to the principles of the invention as described.

What is claimed is:

1. A testing method for an integrated circuit of an integrated circuit device of a plurality of integrated circuit devices comprising:

establishing an enhanced reliability testing flag for an integrated circuit device resulting from fabrication errors and manufacturing deviations from a manufacturing process for an integrated circuit device of a plurality of integrated circuit devices;

storing an enhanced reliability testing flag in the integrated circuit device associated with a unique identification code of each integrated circuit device of the plurality of integrated circuit devices for indicating whether each integrated circuit device requires enhanced reliability testing;

automatically reading the unique identification code of each integrated circuit device of the plurality of integrated circuit devices when each integrated circuit device of the plurality of integrated circuit devices forms a portion of a wafer;

accessing the enhanced reliability testing flag stored for the unique identification code of each integrated circuit device of the plurality of integrated circuit devices;

sorting the plurality of integrated circuit devices in accordance with whether their enhanced reliability testing flag indicates they are in need of the enhanced reliability testing; and

performing the enhanced reliability testing for each integrated circuit device of the plurality of integrated circuit devices requiring the enhanced reliability testing.

2. A reliability testing method for an integrated circuit of an integrated circuit device of a plurality of integrated circuit devices comprising:

establishing an enhanced reliability testing flag for an integrated circuit device resulting from fabrication errors and manufacturing deviations from a manufacturing process for an integrated circuit device of a plurality of integrated circuit devices;

storing an enhanced reliability testing flag in the integrated circuit device associated with a unique identification code of each integrated circuit device of the plurality of integrated circuit devices for indicating whether each integrated circuit device requires further reliability testing;

automatically reading the unique identification code of each integrated circuit device of the plurality of integrated circuit devices;

accessing the enhanced reliability testing flag stored for each unique identification code of each integrated circuit device of the plurality of integrated circuit devices;

sorting the plurality of integrated circuit devices in accordance with whether their enhanced reliability testing flag indicates they are in need of the further reliability testing; and

performing the further reliability testing for each integrated circuit device of the plurality of integrated circuit devices requiring the further reliability testing.

3. A manufacturing method for an integrated circuit of an integrated circuit device of a plurality of integrated circuit devices comprising:

establishing an enhanced reliability testing flag for an integrated circuit device resulting from fabrication errors and manufacturing deviations from a manufacturing process for an integrated circuit device of a plurality of integrated circuit devices;

storing an enhanced reliability testing flag in the integrated circuit device associated with a unique identification code of each integrated circuit device of the plurality of integrated circuit devices for indicating whether each integrated circuit device requires further reliability testing;

automatically reading the unique identification code of each integrated circuit device of the plurality of integrated circuit devices;

accessing the enhanced reliability testing flag stored for each unique identification code of each integrated circuit device of the plurality of integrated circuit devices;

sorting the plurality of integrated circuit devices in accordance with whether their enhanced reliability testing flag indicates they are in need of the further reliability testing; and

performing the further reliability testing for each integrated circuit device of the pluratity of integrated circuit devices requiring the further reliability testing.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,446,277 B2
APPLICATION NO. : 10/092185
DATED : November 4, 2008
INVENTOR(S) : Beffa

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

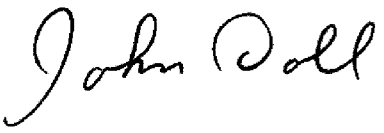
On the Title Pg Item -56-, under "U.S. Patent Documents", line 7, after "4,510,673 A" insert -- * --.

On the Title Pg Item -56-, under "U.S. Patent Documents", line 7, after "Shils et al." insert -- 438/15 --.

In column 10, line 12, in Claim 3, delete "plurality" and insert -- plurality --, therefor.

Signed and Sealed this

Third Day of March, 2009



JOHN DOLL
Acting Director of the United States Patent and Trademark Office