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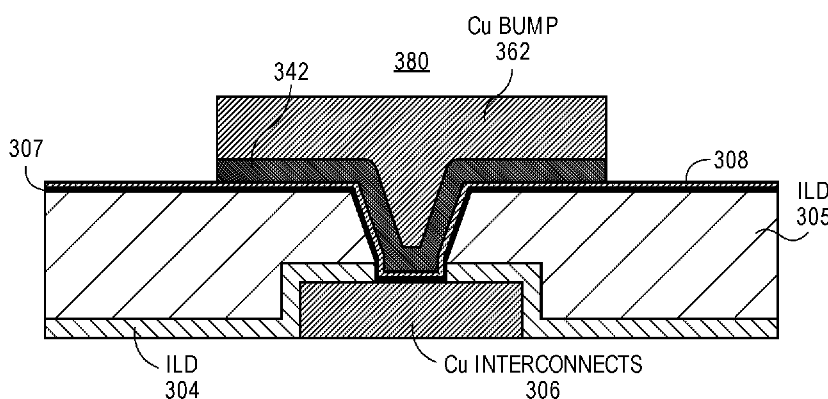

FIG. 3E

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(57) Abstract: Embodiments of the invention include a microelectronic device that includes a layer dielectric material that includes a feature with a depression. A Nickel barrier layer is formed in the depression of the feature and a first conductive layer is formed in the depression of the feature. The microelectronic device can optionally include a second conductive layer formed below the depression of the feature.

MICROELECTRONIC DEVICES AND METHODS FOR ENHANCING INTERCONNECT RELIABILITY PERFORMANCE USING AN IN-SITU NICKEL BARRIER LAYER

5 ## FIELD OF THE INVENTION

Embodiments of the present invention relate generally to the manufacture of semiconductor devices. In particular, embodiments of the present invention relate to microelectronic devices and methods for enhancing interconnect reliability performance using an in-situ nickel barrier layer.

10

BACKGROUND OF THE INVENTION

Copper pillar and bump interconnects manufactured at the wafer-level are used in Flip Chip assembly processes, which typically utilize tin-based solder to connect die to package.
15 While the solder is a softer, conductive material that can be reflowed upon application of heat, at elevated temperatures it tends to react with copper to form intermetallic compounds (IMC). IMCs have poor thermomechanical and electrical properties, and can compromise the electrical and reliability performance of a packaged semiconductor device. Solder can consume some or all of the 1st layer interconnect copper, which is why taller copper bumps are required to prevent
20 IMC formation in the underlying interconnect layers. Taller copper structures act as a sacrificial layer to solder, however, these taller copper structures also introduce higher mechanical stress upon any underlying ILD material layers at the wafer and die level, which can lead to other device failure modes.

25 ## BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a cross-sectional image of Solder-capped Copper bump in a packaged die 100 after aggressive reliability testing.

Figure 2 illustrates a process for enhancing interconnect reliability performance using an in-situ nickel barrier layer for back end metallization, e.g., forming copper interconnects for
30 microelectronic devices (e.g., integrated circuit chips) in accordance with one embodiment.

Figures 3A-3E illustrate cross-sectional drawings of a microelectronic device (e.g., 300, 320, 340, 360, 380) that is fabricated in accordance with the operations of the process of Figure 2 in accordance with one embodiment.

FIGS. 4A-4F illustrate paired-simulated reflow experiments in accordance with certain
35 embodiments.

Figures 5A-5C illustrate cross-sectional images of microelectronic devices 500, 520, and 540 having copper bump layers post resist strip in accordance with certain embodiments.

Figure 6 illustrates a computing device 900 in accordance with one embodiment.

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DETAILED DESCRIPTION OF THE INVENTION

Described herein are microelectronic devices that are designed to enhance interconnect reliability performance without impacting electrical performance using an in-situ nickel barrier layer. In the following description, various aspects of the illustrative implementations will be 10 described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. However, it will be apparent to those skilled in the art that embodiments of the present invention may be practiced with only some of the described aspects. For purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the illustrative implementations. However, it will be 15 apparent to one skilled in the art that embodiments of the present invention may be practiced without the specific details. In other instances, well-known features are omitted or simplified in order to not obscure the illustrative implementations.

Various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding embodiments of the present invention, however, the order 20 of description should not be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation.

Electronic connections between the electronic devices (e.g., transistors) in an integrated circuit (IC) chip are currently typically created using copper metal or alloys of copper metal. Devices in an IC chip can be placed not only across the surface of the IC chip but devices can 25 also be stacked in a plurality of layers on the IC chip. Electrical interconnections between electronic devices that make up the IC chip are built using vias and trenches that are filled with conducting material. Layer(s) of insulating materials, frequently, low-k dielectric materials, separate the various components and devices in the IC chip.

The substrate on which the devices of the IC circuit chip are built is, for example, a silicon 30 wafer or a silicon-on-insulator substrate. Silicon wafers are substrates that are typically used in the semiconductor processing industry, although embodiments of the invention are not dependent on the type of substrate used. The substrate could also be comprised of germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, gallium antimonide, and or other Group III-V materials either alone or in combination with silicon or

silicon dioxide or other insulating materials. IC devices that make up the chip are built on the substrate surface. At least one dielectric layer is deposited on the substrate. Dielectric materials include, but are not limited to, silicon dioxide (SiO_2), low-k dielectrics, silicon nitrides, and or silicon oxynitrides. The dielectric layer optionally includes pores or other voids to further reduce
5 its dielectric constant. Typically, low-k films are considered to be any film with a dielectric constant smaller than that of SiO_2 which has a dielectric constant of about 4.0. Low-k films having dielectric constants of about 1 to about 2.7 are typical of current semiconductor fabrication processes. The production of integrated circuit device structures often also includes placing a silicon dioxide film or layer, or capping layer on the surface of low-k (low dielectric
10 constant) ILD (inter-layer dielectric) films. Low-k films can be, for example, boron, phosphorous, or carbon doped silicon oxides. Carbon-doped silicon oxides can also be referred to as carbon-doped oxides (CDOs) and organo-silicate glasses (OSGs). To form electrical interconnects, dielectric layers are patterned to create one or more trenches and or vias within which metal interconnects will be formed. The terms trenches and vias are used herein because
15 these are the terms commonly associated with the features that are used to form metal interconnects. In general, a feature used to form a metal interconnect is a depression having any shape formed in a substrate or layer deposited on the substrate. The feature is filled with conducting interconnect material. The trenches and or vias may be patterned (created) using conventional wet or dry etch semiconductor processing techniques. Dielectric materials are used
20 to isolate electrically metal interconnects from the surrounding components. Barrier layers are used between the metal interconnects and the dielectric materials to prevent metal (such as copper) migration into the surrounding materials. Device failure can occur, for example, in situations in which copper metal is in contact with dielectric materials because the copper metal can ionize and penetrate into the dielectric material. Barrier layers placed between a dielectric
25 material, silicon, and or other materials and the copper interconnect can also serve to promote adhesion of the copper to the other material(s).

The present design adds a barrier layer to stop solder migration to the underlying interconnect layers and thus enables shorter bumps and less mechanical stress within the ILD. In this present design, an in-situ method creates conformally plated (through photoresist) Nickel
30 film that is formed within a thick via beneath the copper bump. Nickel is a widely used material in the semiconductor industry in first layer interconnect and packaging applications, due to its ability to act as an effective diffusion barrier to solder. Nickel will prevent the IMC from forming in underlying interconnect structures, which will enable shorter copper bumps (e.g., up to 30-40% thinner bumps) without impacting electrical or reliability performance. The present

design also improves (reduces) mechanical stress on the ILD stack due to a reduction of the thickness of the bump. The present design is customizable to future technologies with reduced copper bump dimensions, and will enable decrease of bump height and critical dimensions (CD), and thus less Cu volume.

5 Nickel is widely used in the semiconductor industry in 1st layer interconnect and packaging applications, and is a known to act as a good diffusion barrier to Sn based solders. The basic principle of the present design is that a Nickel barrier layer is added in situ and at wafer level above underlying interconnect layers with Nickel electrolytic (e.g., Nickel atomic weight % of at least 95%) or electro-less plating (e.g., Nickel atomic weight % of at least 80%) using a 10 plate-through-photoresist process. In one example, the Ni barrier layer has a minimum thickness of 1-2 microns. In other examples, the Ni barrier layer has a minimum thickness of less than 1 micron. The Ni barrier is formed with no extra barrier-seed or lithography layer, and does not affect downstream fab operations. While copper has excellent current carrying properties, which makes it a viable material for interconnect layers, in the current Flip Chip assembly processes, 15 copper in the first layer interconnect layer reacts with solder to form IMC during reliability testing. Thus to protect from solder, and prevent IMC formation in the underlying, current-carrying interconnect layers, taller Copper Bumps (e.g., 8-12 microns) are required.

Figure 1 illustrates a cross-sectional image of Solder-capped Copper bumps in a packaged die 100 after aggressive reliability testing. Figure 1 shows results of aggressive 20 reliability tests that shows complete Copper consumption of the bump, exposing underlying interconnect layers and causing device failure modes due to electrical opens due to IMC/void formation.

The present design enables shorter copper bumps (e.g., less than 8-12 microns), and thus less mechanical stress within the ILD stack, and better reliability performance. In 25 addition, the Ni barrier is created in fab using a plate-through photoresist option which does not require an extra barrier-seed or lithography layer. Since a final device structure includes a buried Ni layer capped with Cu, the first layer interconnect would appear in accordance with conventional first layer interconnects. Therefore, there is no impact to Fab end of line electrical test, Sort, and packaging processes since copper remains at the 30 top of the bump.

This present design provides a new approach towards forming shorter copper pillars and bumps above underlying interconnect layers through the addition of a Nickel-plated barrier layer immediately before the bump layer is filled with copper. This prevents IMC proliferation into the underlying interconnect layers and formation of electrical opens. A

general flow of the fab process during a formation of a bump layer is outlined in Figures 2 and 3.

Figure 2 illustrates a process for enhancing interconnect reliability performance using an in-situ nickel barrier layer for back end metallization, e.g., forming copper interconnects for transistor devices for microelectronic devices (e.g., integrated circuit chips) in accordance with one embodiment. Figures 3A-3E illustrate cross-sectional drawings of a microelectronic device (e.g., 300, 320, 340, 360, 380) that is fabricated in accordance with the operations of the process of Figure 2 in accordance with one embodiment. In Figure 3A, a depression (e.g., trench or via 302) that is to be filled with a conducting metal to form an electrically conducting interconnect of a microelectronic device is provided at operation 201. The trench or via is a depression that is typically formed in a dielectric layer, such as ILD layers 304 and 305 through an etching process used in the semiconductor industry. The ILD layers and interconnect are formed on a substrate of the device. The walls and bottom of the trench or via (the side(s) of the depression) can optionally be coated with a thin barrier layer 307. The thin barrier layer is deposited by ALD, CVD, or PVD, for example. An optional barrier layer (e.g., Titanium containing layer 307, Tantalum containing layer 307) and an optional seed layer (e.g., Copper seed layer 308) are deposited (e.g., deposited on exposed upper surfaces of ILD 304, 305, and underlying interconnect layer 306) at operation 202. The seed layer is deposited by ALD, PVD, or CVD, for example. At operation 204, lithography is performed with a photoresist layer (e.g., photoresist layer 322) being applied to a surface of the device (e.g., device 320 of Figure 3B). Light is used to transfer a pattern from a photomask (e.g., interconnect photomask) to the photoresist layer, which is light-sensitive. Chemical treatments then cause a portion of the photoresist layer to be removed. These removed portions correspond to opening 324 (and other openings) of this layer. A resist surface treatment occurs at operation 206. The openings are then filled with metal (e.g., in-situ Nickel barrier layer 342, copper layer) through a deposition process (e.g., electroplating, electroless plating) at operation 208. In one example, the Nickel barrier layer is plated through openings in the photoresist at operation 208. Then, a Copper layer (e.g., copper layer 362) is plated through these same openings in the same photoresist layer at operation 210. The Copper layer is disposed on the Nickel barrier layer.

In another example, a first Copper layer is plated through openings in the photoresist and then the Nickel barrier layer is plated through the same openings in the photoresist at operation 208. Then, a second Copper layer is plated through the same openings in the same photoresist layer at operation 210. The second Copper layer is disposed on the Nickel barrier layer.

In another example, a first Copper layer is plated through openings in the photoresist at operation 208 and then the Nickel barrier layer is plated through the same openings in the photoresist at operation 210. The Nickel barrier layer is disposed on the first Copper layer.

A resist strip, etch, and clean are performed at operation 212 to generate a device (e.g., device 380). Annealing the microelectronic device provides an electrical interconnect structure having a Nickel barrier layer that prevents solder migration to underlying interconnect layers. In general, an electrodeposition process comprises the deposition of a metal onto a semiconductor substrate from an electrolytic solution that comprises ions of the metal to be deposited. In one example, a negative bias is placed on the substrate. The electrolyte solution can be referred to as a plating bath or an electroplating bath. The positive ions of the metal are attracted to the negatively biased substrate. The negatively biased substrate reduces the ions and the metal deposits onto the substrate. In another example, electroless plating, which is also known as chemical or auto-catalytic plating, is a non-galvanic plating process that involves several simultaneous reactions in an aqueous solution. These reactions occur without the use of external electrical power.

A fabrication end of line (EOL) electronic test and sort are performed on a wafer level at operation 214. A fabrication EOL packaging is performed at operation 216 with die of the wafer being packaged with packaging materials. An upper level metallic interconnect layer contacts solder during the packaging.

FIGS. 4A-4F illustrate paired-simulated reflow experiments in accordance with certain embodiments. Figure 4A illustrates a cross-sectional image of a microelectronic device 400 having a conventional copper (Cu) bump deposition with a Cu thickness of 1X for the Copper layer 410. Figure 4C illustrates a cross-sectional image of a microelectronic device 430 having a conventional copper (Cu) bump deposition with a Cu thickness of 2X for the Copper layer 411. Figure 4Eillustrates a cross-sectional image of a microelectronic device 440 having a reduced thickness copper (Cu) bump deposition for the Copper layer 412 with a novel in-situ nickel layer 420. Quick Turn Reliability Tests (QTRT) are performed on these microelectronic devices in which bumps capped with solder layers 401-403 are subjected to an elevated temperature condition in order to simulate solder reflow conditions in a reliability test.

Figures 4B, 4D, and 4F illustrate cross-sectional images of microelectronic devices 450, 460, and 470 after the reflow of the solder layers 404-406. Copper consumption can be observed with the QTRT in Figure 4B for the conventional bump deposition with 1X Cu thickness for the Copper layer 413. In this case, IMC is formed down to the ILD 452

within an underlying via layer, which could lead to increased resistance and/or electrical open type failure modes. The Copper layer 414 remains as a continuous film throughout the bump and underlying VIA layer in the conventional bump deposition with 2X Cu thickness as illustrated in Figure 4D and the Copper layer 415 is completely consumed
5 down to the Nickel layer 421 in the novel method with 1X Ni deposition layer, 1X Cu deposition layer of Figure 4F. However, the overall thickness of the Nickel layer in Figure 4F is greater than the Copper layer thickness left in Figure 4D. The Nickel layer remains intact as an underlying barrier layer as demonstrated in Figure 4F and thus provides protection of the underlying interconnect layers with maintained electrical continuity from
10 die to package. In principle this could help enable shorter copper bumps with matched or better electrical test and reliability data as compared to the conventional method, as well as reduced stress on the ILD stack.

Figures 5A-5C illustrate cross-sectional images of microelectronic devices 500, 520, and 540 having copper bump layers post resist strip in accordance with certain
15 embodiments. The interconnect structure 500 includes ILD (inter-layer dielectric) films 510 and 512, optional barrier layer 507 (e.g., Titanium containing layer, Tantalum containing layer), optional seed layer 508 (e.g., Copper seed layer 508), Nickel layer 504, optional Copper bump layer 502, and Copper interconnect 506. In one example, if the structure 500 does not includes the Copper bumper layer 502, then the Nickel layer 504 has a thicker
20 deposition. The interconnect structure 520 includes ILD (inter-layer dielectric) films 530 and 532, optional barrier layer 527 (e.g., Titanium containing layer, Tantalum containing layer), optional seed layer 528 (e.g., Copper seed layer 528), Nickel layer 514, Copper bump layer 512, Copper layer 516, and Copper interconnect 518. The interconnect structure 540 includes ILD (inter-layer dielectric) films 550 and 552, optional barrier layer 547 (e.g.,
25 Titanium containing layer, Tantalum containing layer), optional seed layer 548 (e.g., Copper seed layer 548), Nickel layer 544, Copper bump layer 542, and Copper interconnect 548. With the approach of the novel process of Figure 2, the Nickel barrier layer can be selectively added to the bottom (Figure 5A), middle (Figure 5B), or top of the Cu bump (Figure 5C). Each Cu or Ni layer within the stack would require a single plating step, all
30 using the same plate-through photoresist layer.

It will be appreciated that, in a system on a chip embodiment, the die may include a processor, memory, communications circuitry and the like. Though a single die is illustrated, there may be none, one or several dies included in the same region of the wafer.

In one embodiment, the microelectronic device may be a crystalline substrate formed using

a bulk silicon or a silicon-on-insulator substructure. In other implementations, the microelectronics device may be formed using alternate materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, indium gallium arsenide, gallium
5 antimonide, or other combinations of group III-V or group IV materials. Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation upon which a semiconductor device may be built falls within the scope of embodiments of the present invention.

Figure 6 illustrates a computing device 900 in accordance with one embodiment of the
10 invention. The computing device 900 houses a board 902. The board 902 may include a number of components, including but not limited to at least one processor 904 (e.g., microelectronic device 300, 320, 340, 360, 380, 440, 470, 500, 520, 540, etc.) and at least one communication chip 906. The at least one processor 904 is physically and electrically coupled to the board 902. In some implementations, the at least one communication chip 906 is also physically and
15 electrically coupled to the board 902. In further implementations, the communication chip 906 is part of the processor 904. In one example, the communication chip 906 (e.g., microelectronic device 300, 320, 340, 360, 380, 440, 470, 500, 520, 540, etc.) includes an antenna unit 920.

Depending on its applications, computing device 900 may include other components that may or may not be physically and electrically coupled to the board 902. These other components
20 include, but are not limited to, volatile memory (e.g., DRAM 910, 911), non-volatile memory (e.g., ROM 912), flash memory, a graphics processor 916, a digital signal processor, a crypto processor, a chipset 914, an antenna unit 920, a display, a touchscreen display 930, a touchscreen controller 922, a battery 932, an audio codec, a video codec, a power amplifier 915, a global positioning system (GPS) device 926, a compass 924, a gyroscope, a speaker, a camera 950, and
25 a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

The communication chip 906 enables wireless communications for the transfer of data to and from the computing device 900. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that
30 may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 906 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), WiGig, IEEE 802.20, long term evolution

(LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 900 may include a plurality of communication chips 906. For instance, a first communication chip 906 may be dedicated to shorter range wireless communications such as Wi-Fi, WiGig, and Bluetooth and a second communication chip 906 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, 5G, and others.

The at least one processor 904 of the computing device 900 includes an integrated circuit die packaged within the at least one processor 904. In some implementations of embodiments of the invention, the integrated circuit die of the processor includes one or more devices, such as microelectronic devices (e.g., microelectronic device 300, 320, 340, 360, 380, 440, 470, 500, 520, 540, etc.) in accordance with implementations of embodiments of the invention. The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

The communication chip 906 also includes an integrated circuit die packaged within the communication chip 906. In accordance with another implementation of embodiments of the invention, the integrated circuit die of the communication chip includes one or more microelectronic devices (e.g., microelectronic device 300, 320, 340, 360, 380, 440, 470, 500, 520, 540, etc.).

The following examples pertain to further embodiments. Example 1 is a microelectronic device that includes a layer of dielectric material having a feature with a depression, a Nickel barrier layer formed in the depression of the feature by plating through a photoresist layer, and a first conductive layer formed in the depression of the feature by plating through the photoresist layer.

In example 2, the subject matter of example 1 can optionally include a second conductive layer formed below the depression of the feature. The Nickel barrier layer prevents migration of solder to the second conductive layer.

In example 3, the subject matter of any of examples 1-2 can optionally include a barrier layer and a seed layer formed in the depression of the feature and disposed above the second conductive layer.

In example 4, the subject matter of example 3 can optionally include the Nickel barrier layer being disposed on the seed layer.

In example 5, the subject matter of any of examples 1-4 can optionally include the first conductive layer being disposed on the Nickel barrier layer.

In example 6, the subject matter of any of examples 1-4 can optionally include the Nickel barrier layer being disposed on the first conductive layer. The Nickel barrier layer prevents migration of solder to the first conductive layer.

In example 7, the subject matter of any of examples 1-6 can optionally include the first and second conductive layers each comprising a Copper layer.

Example 8 is a microelectronic device comprising a layer of dielectric material that includes a feature with a depression, a Nickel barrier layer formed in the depression of the feature by plating through a photoresist layer, a first conductive layer formed in the depression of the feature by plating through the photoresist layer, and a second conductive layer formed in the depression of the feature by plating through the photoresist layer.

In example 9, the subject matter of example 8 can optionally include a third conductive layer formed below the depression of the feature. The Nickel barrier layer prevents migration of solder to the second and third conductive layers.

In example 10, the subject matter of any of examples 8-9 can optionally include a barrier layer and a seed layer formed in the depression of the feature and disposed above the third conductive layer.

In example 11, the subject matter of any of examples 8-10 can optionally include the Nickel barrier layer being disposed on the second conductive layer, which is disposed on the seed layer.

In example 12, the subject matter of any of examples 8-11 can optionally include the first conductive layer being disposed on the Nickel barrier layer.

In example 13, the subject matter of any of examples 8-12 can optionally include the first, second, and third conductive layers each comprising a Copper layer.

In example 14, the subject matter of any of examples 8-13 can optionally include a printed circuit board that is attached to the first conductive layer of the substrate with solder.

Example 15 is a method that comprises providing a microelectronic device having a layer of dielectric material that includes a feature with a depression, forming a photoresist layer with openings, forming a Nickel barrier layer in the openings by plating through the photoresist layer, and forming a first conductive layer in the openings by plating through the photoresist layer.

In example 16, the subject matter of example 15 can optionally include the Nickel barrier layer preventing migration of solder to an underlying second conductive layer.

In example 17, the subject matter of any of examples 15-16 can optionally include forming a barrier layer and a seed layer in the depression of the feature with the barrier and seed layers being disposed above the second conductive layer.

In example 18, the subject matter of any of examples 15-17 can optionally include the Nickel barrier layer being disposed on the seed layer.

In example 19, the subject matter of any of examples 15-18 can optionally include the first conductive layer being disposed on the Nickel barrier layer.

In example 20, the subject matter of any of examples 15-18 can optionally include the Nickel barrier layer being disposed on the first conductive layer. The Nickel barrier layer prevents migration of solder to the first conductive layer.

CLAIMS

What is claimed is:

1. A microelectronic device comprising:
5 a layer of dielectric material that includes a feature with a depression;
a Nickel barrier layer formed in the depression of the feature; and
a first conductive layer formed in the depression of the feature.

2. The microelectronic device of claim 1, further comprising:
10 a second conductive layer formed below the depression of the feature, wherein the Nickel barrier layer prevents migration of solder to the second conductive layer.

3. The microelectronic device of claim 2 further comprising:
a barrier layer and a seed layer formed in the depression of the feature and disposed
15 above the second conductive layer.

4. The microelectronic device of claim 3 wherein the Nickel barrier layer is disposed on the seed layer.

20 5. The microelectronic device of claim 4, wherein the first conductive layer is disposed on the Nickel barrier layer.

6. The microelectronic device of claim 1, wherein the Nickel barrier layer is disposed on the first conductive layer, wherein the Nickel barrier layer prevents migration of solder to the
25 first conductive layer.

7. The microelectronic device of claim 1, wherein the first and second conductive layers each comprise a Copper layer.

30 8. A microelectronic device comprising:
a layer of dielectric material that includes a feature with a depression;
a Nickel barrier layer formed in the depression of the feature;
a first conductive layer formed in the depression of the feature; and
a second conductive layer formed in the depression of the feature.

9. The microelectronic device of claim 8, further comprising:

a third conductive layer formed below the depression of the feature, wherein the Nickel barrier layer prevents migration of solder to the second and third conductive layers.

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10. The microelectronic device of claim 9 further comprising:

a barrier layer and a seed layer formed in the depression of the feature and disposed above the third conductive layer.

10 11. The microelectronic device of claim 10 wherein the Nickel barrier layer is disposed on the second conductive layer, which is disposed on the seed layer.

12. The microelectronic device of claim 8, wherein the first conductive layer is disposed on the Nickel barrier layer.

15

13. The microelectronic device of claim 8, wherein the first, second, and third conductive layers each comprise a Copper layer.

14. The microelectronic device of claim 8, further comprising:

20 a printed circuit board that is attached to the first conductive layer of the substrate with solder.

15. A method comprising:

providing a microelectronic device having a layer of dielectric material that includes

25 a feature with a depression;

forming a Nickel barrier layer in the depression of the feature; and

forming a first conductive layer in the depression of the feature.

16. The method of claim 15, wherein the Nickel barrier layer prevents migration of solder to an

30 underlying second conductive layer.

17. The method of claim 16 further comprising:

forming a barrier layer and a seed layer in the depression of the feature and disposed above the second conductive layer.

18. The method of claim 17 wherein the Nickel barrier layer is disposed on the seed layer.

19. The method of claim 15, wherein the first conductive layer is disposed on the Nickel
5 barrier layer.

20. The method of claim 15, wherein the Nickel barrier layer is disposed on the first conductive layer, wherein the Nickel barrier layer prevents migration of solder to the first conductive layer.
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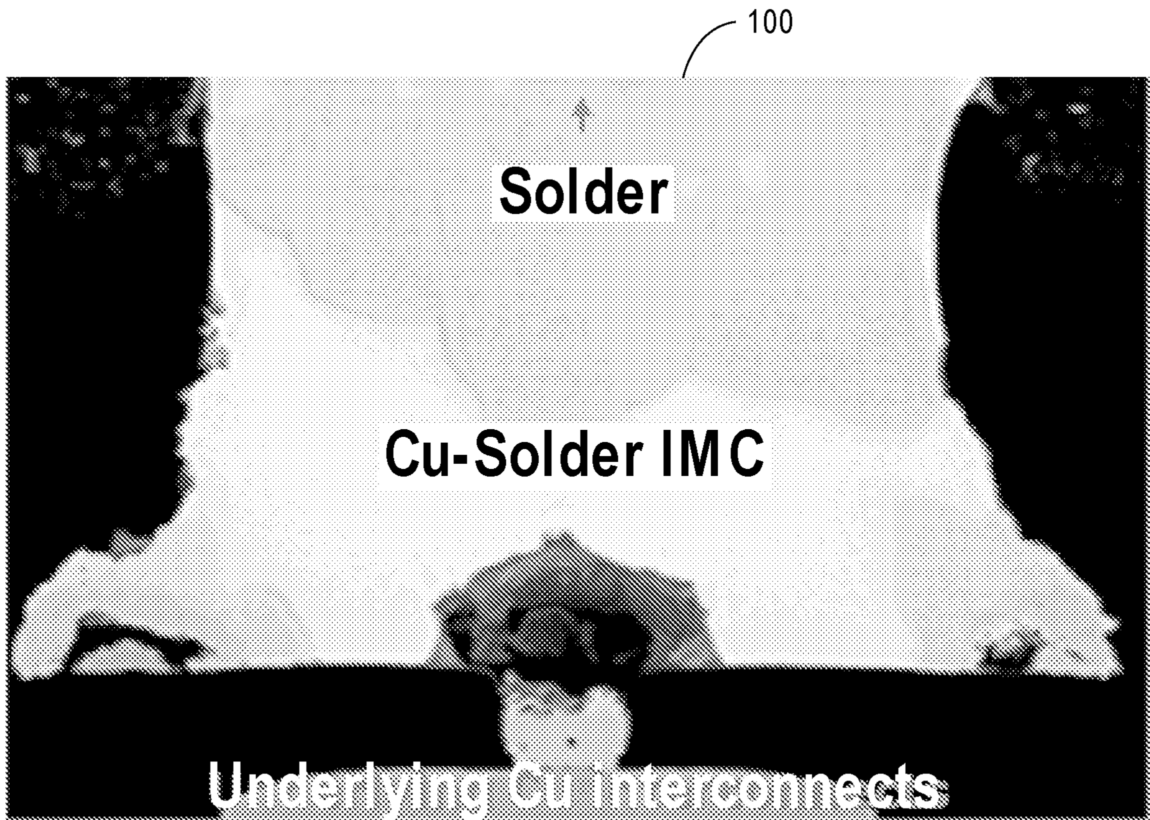

FIG. 1

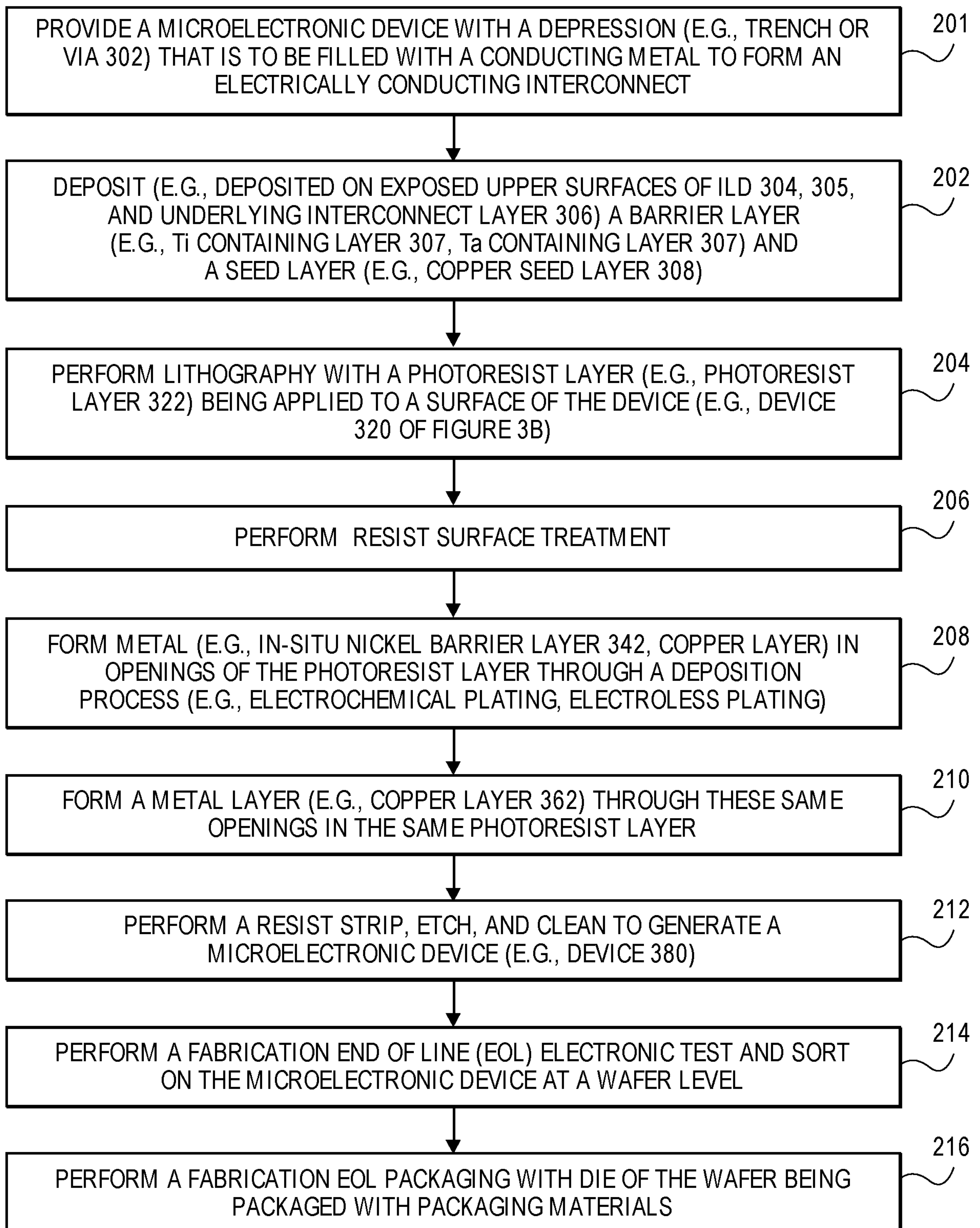

FIG. 2

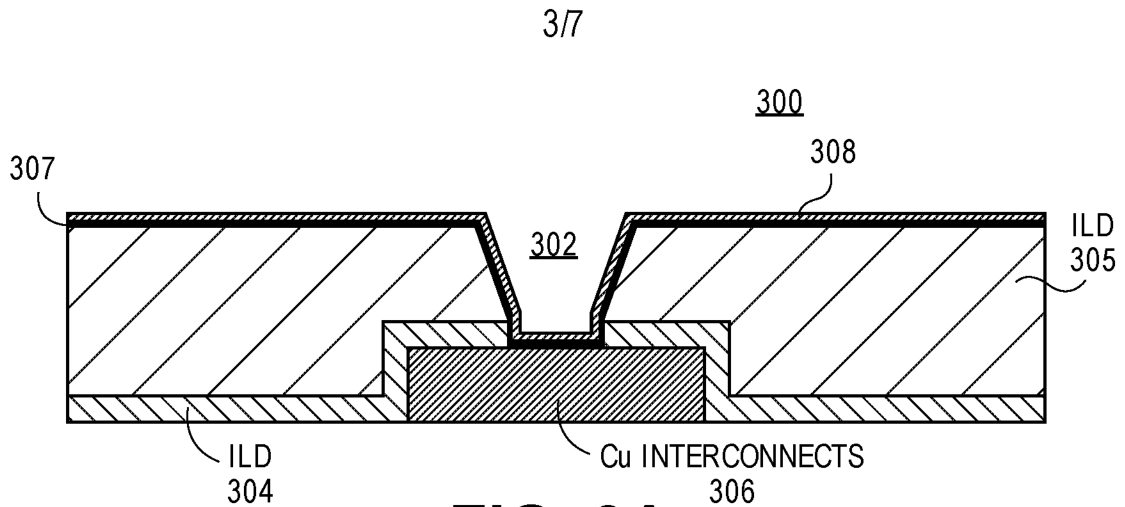

FIG. 3A

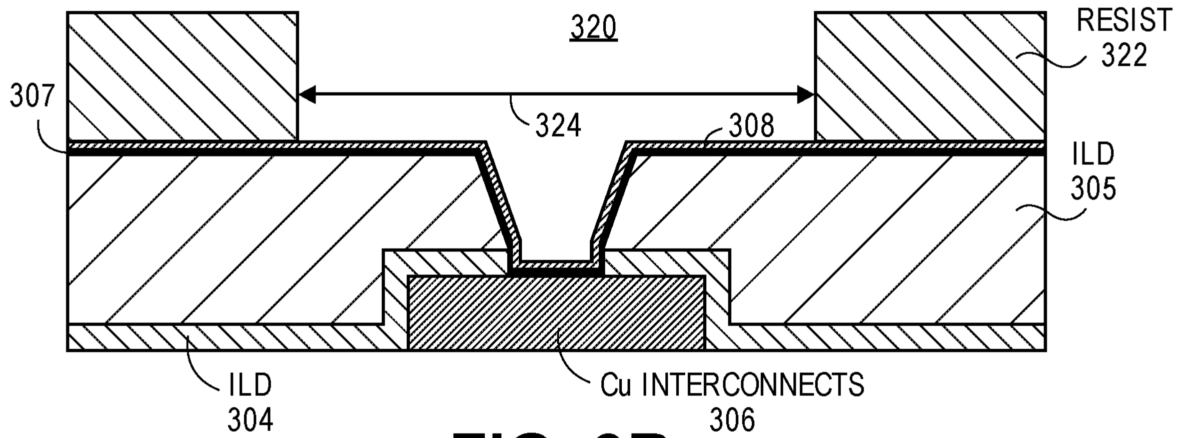

FIG. 3B

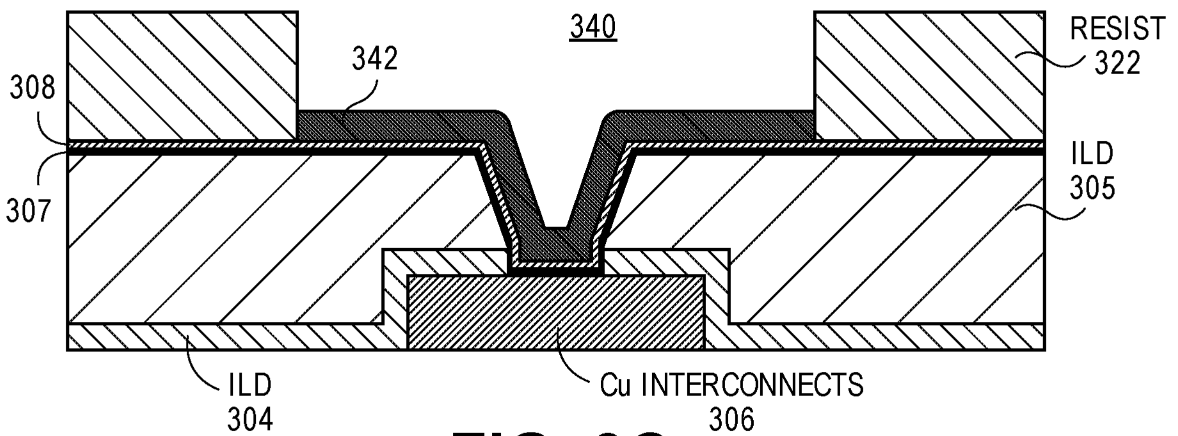

FIG. 3C

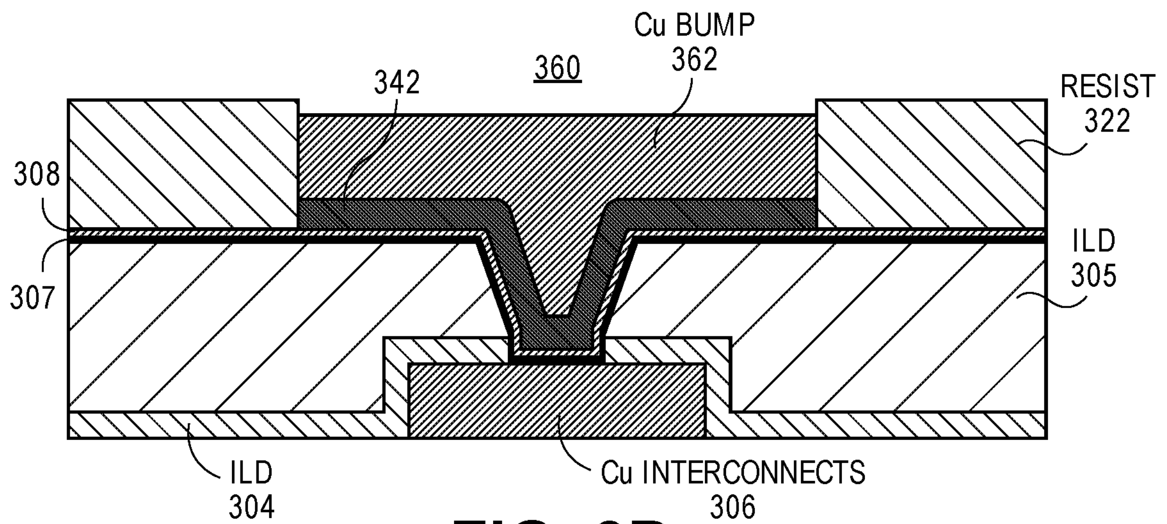

FIG. 3D

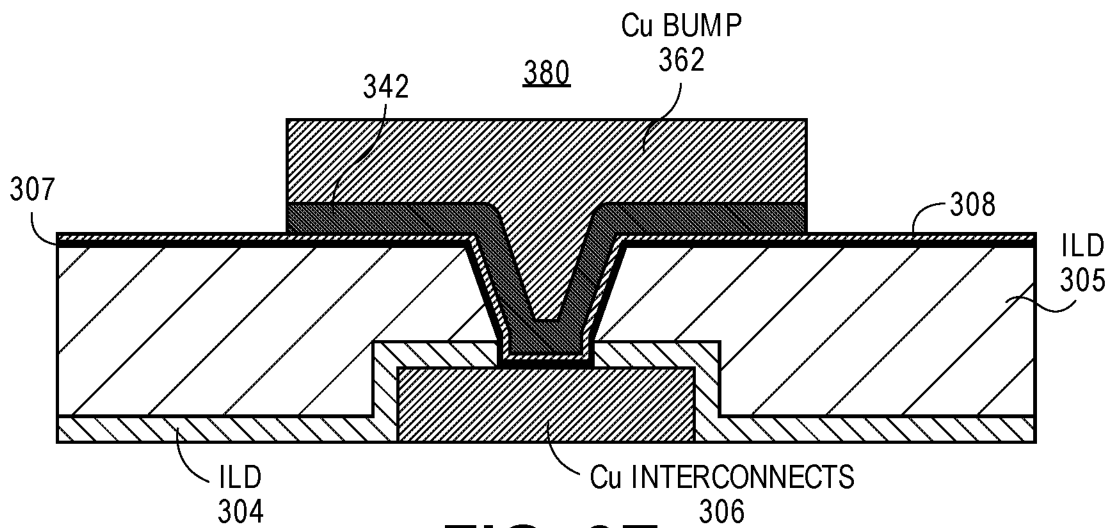

FIG. 3E

No reflow

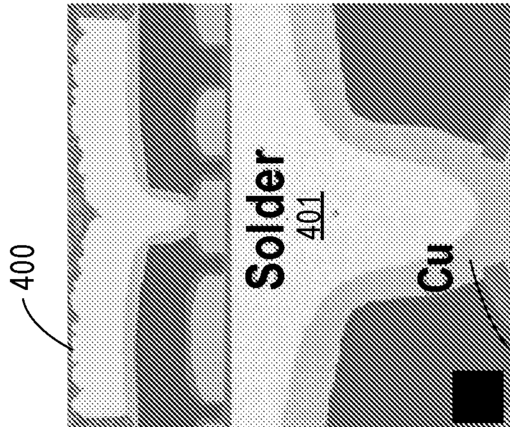

FIG. 4A

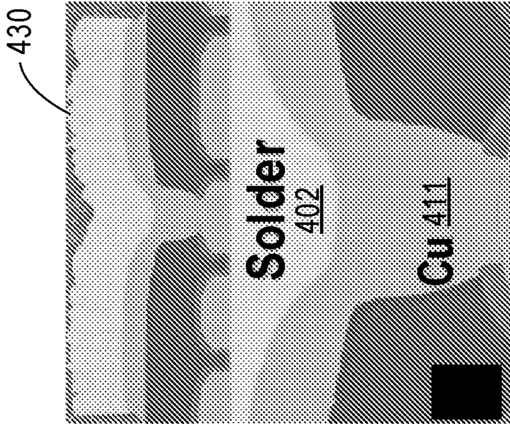

FIG. 4C

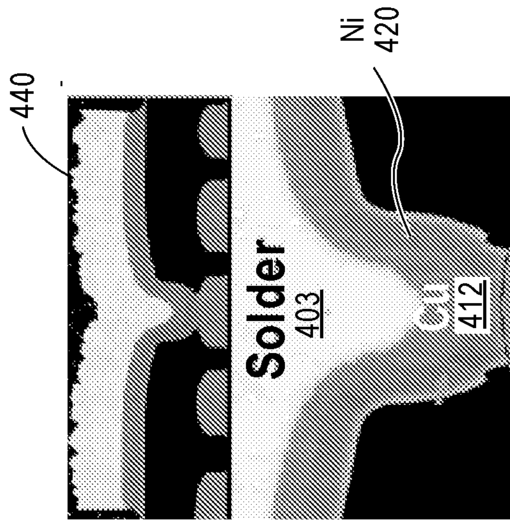

FIG. 4E

After QTRT reflow

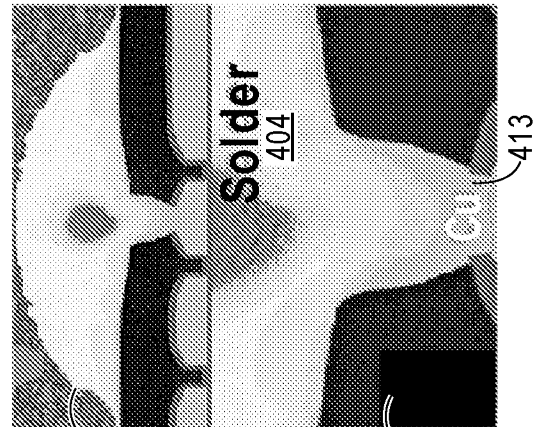

FIG. 4B

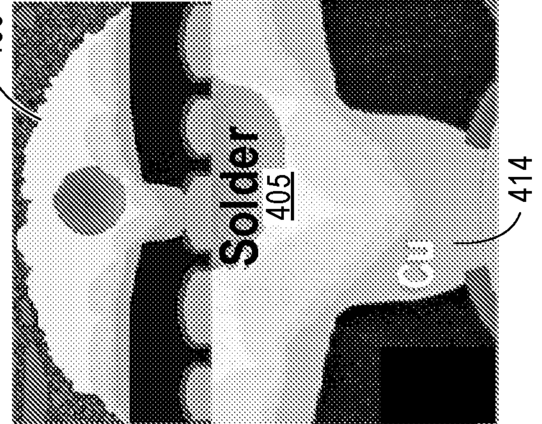

FIG. 4D

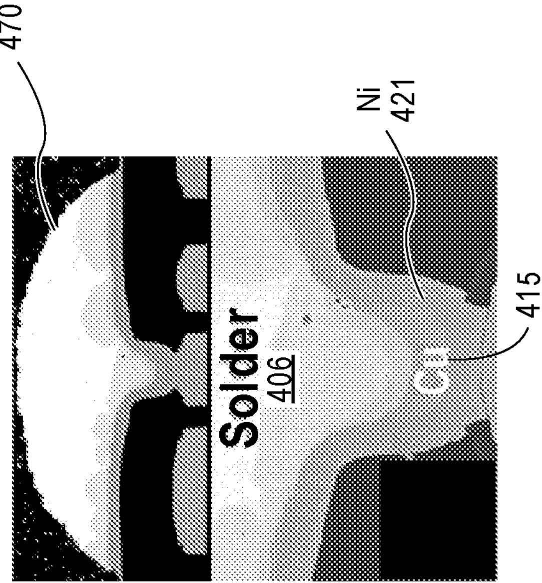

FIG. 4F

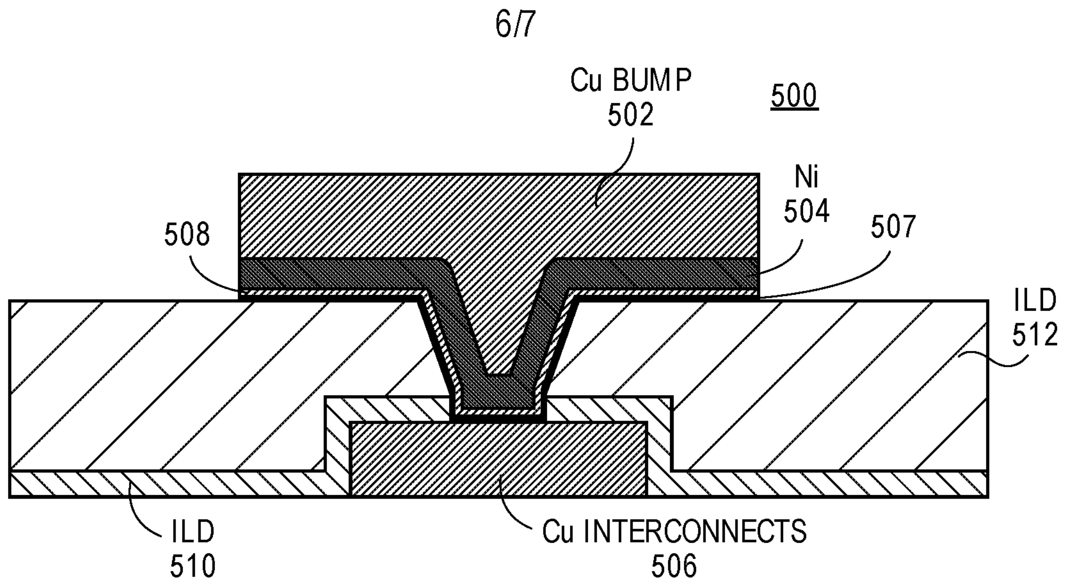

FIG. 5A

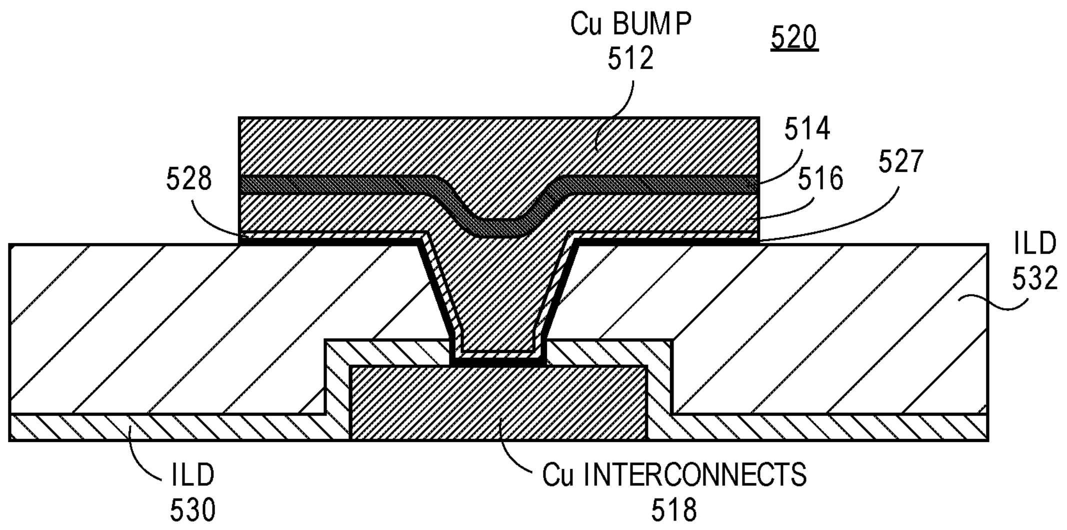

FIG. 5B

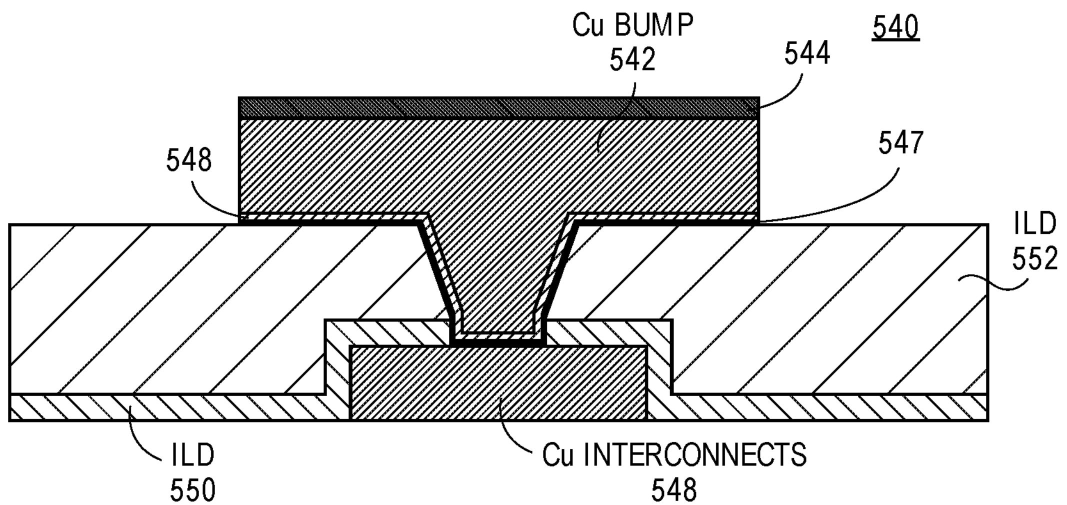

FIG. 5C

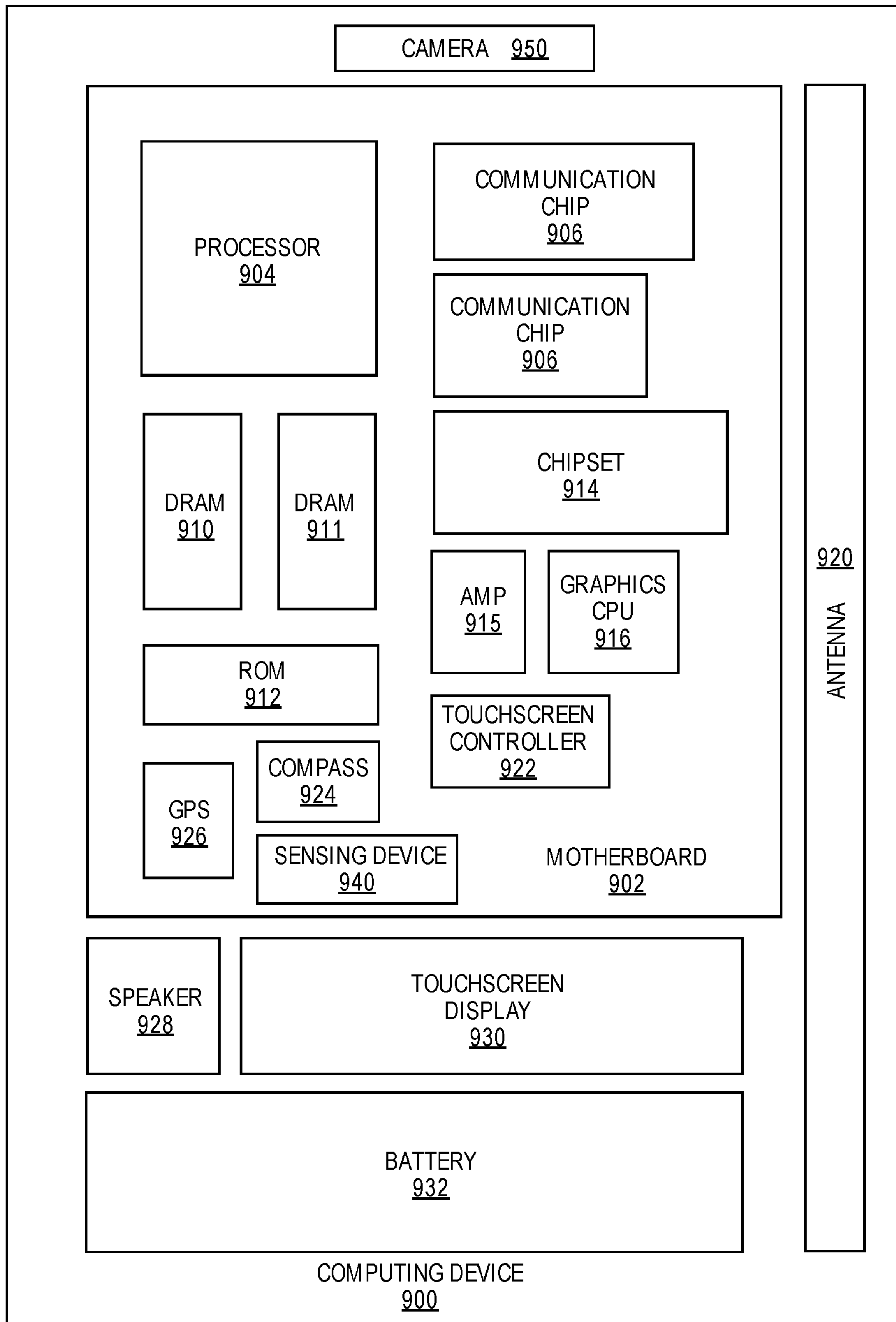

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/055031

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/768(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/768; H01L 21/60; H01L 23/00; H01L 23/48; H01L 23/498; H01L 21/44; H01L 21/48

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: nickel barrier, copper, depression, dielectric, interconnect, bump

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y		6-14,20
Y	US 2011-0101527 A1 (MING-DA CHENG et al.) 05 May 2011 See paragraphs [0020]-[0030], [0049], claim 19 and figures 1A-1C.	6-14,20
A	US 2005-0208748 A1 (KAMALESH K. SRIVASTAVA et al.) 22 September 2005 See claim 1 and figures 1(a)-1(d).	1-20
A	US 2006-0030139 A1 (J. DANIEL MIS et al.) 09 February 2006 See claim 47 and figure 4.	1-20
A	US 2014-0227831 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.) 14 August 2014 See claim 1 and figures 1-6.	1-20

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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Date of the actual completion of the international search
27 June 2017 (27.06.2017)

Date of mailing of the international search report
28 June 2017 (28.06.2017)

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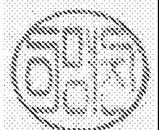

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