(12) UK Patent (19) GB (11) 2 118 394 B

(54) Title of invention

Integrated circuit arrangement comprising means for generating a current

(51) INT CL⁴; **H03F 1/00**
H01L 27/04

(21) Application No
8309726

(22) Date of filing
11 Apr 1983

(30) Priority data

(31) **3213838**

(32) **15 Apr 1982**

(33) **Fed Rep of Germany (DE)**

(43) Application published
26 Oct 1983

(45) Patent published
29 Aug 1985

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(52) Domestic classification
H3T 2B8 2T2X 3X 4D 5E AX
H1K 11D1 11D3 11D 1AA9 1CA 1FJ GAX

(56) Documents cited
None

(58) Field of search
H3T

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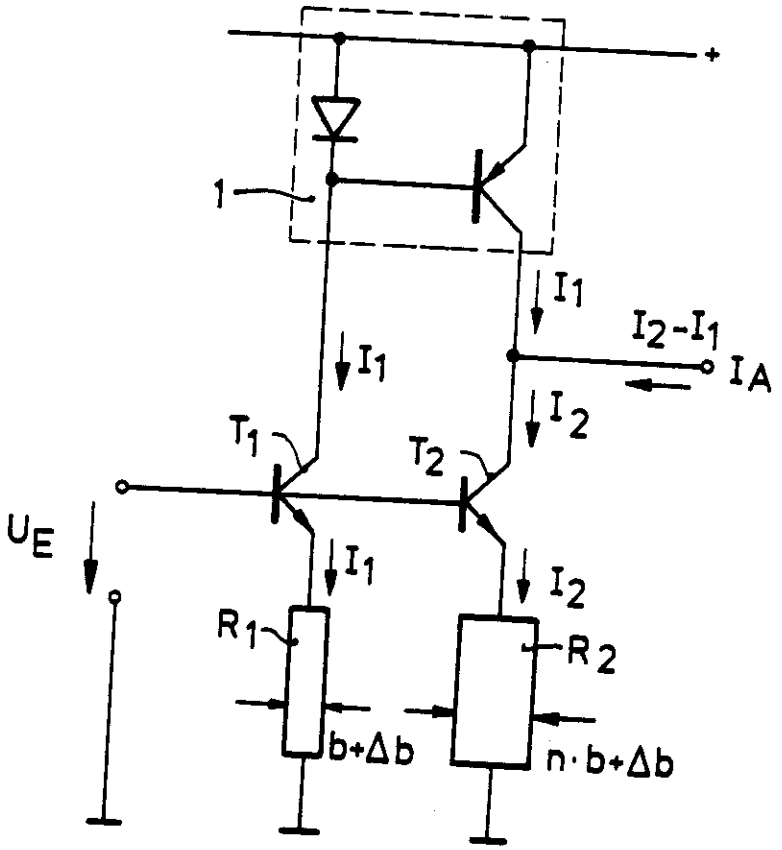
GB 2 118 394 B


+
1
I1
I2-I1
IA
I1
I2
T1
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UE
I1
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R1
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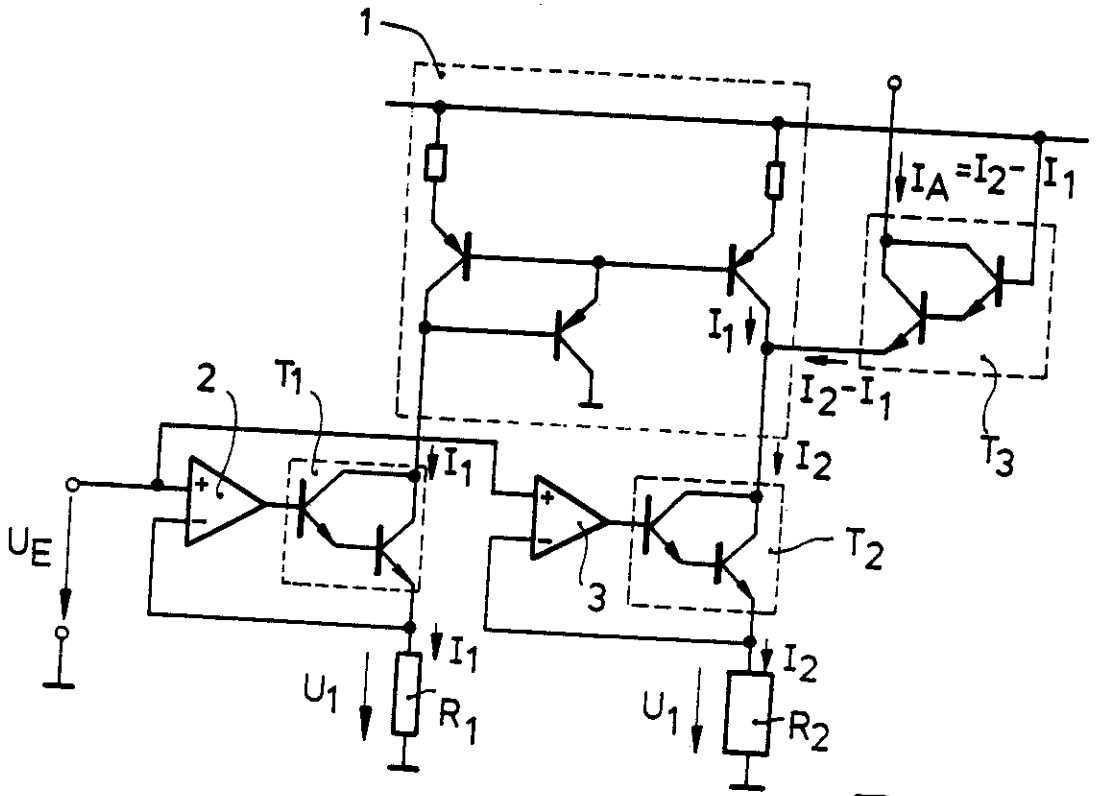
b+Δb
n·b+Δb

Fig.1


1
IA=I2-I1
I1
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3
I1
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R2

Fig.2

"INTEGRATED CIRCUIT ARRANGEMENT COMPRISING MEANS FOR GENERATING A CURRENT".

The invention relates to an integrated circuit arrangement comprising means for generating a current which produces a voltage drop across a reference resistor, which voltage drop is determined by an input voltage. Such means are generally referred to as a voltage-current converter.

In an integrated circuit the accuracy of a voltage-current conversion obtained by means of a reference resistor of predetermined value depends on the spread in the resistance of this reference resistor. The spread in this resistance mainly depends on the resistance per unit area of the layer of material forming the resistor and on the spread in width of the resistance track.

In a monolithic integrated semiconductor circuit the resistance per unit area depends on the quotient of the specific resistance of the doped zone forming the resistor and the thickness of this doped zone. The spread in width of the resistance track depends on the tolerances in the process which determines the structure of the doped zone (photolithography, etching for example). Therefore, unless special measures are taken it is well-nigh impossible to effect a voltage current conversion with a small spread within an integrated circuit.

It is an object of the invention to construct an integrated circuit arrangement of the type set forth in the opening paragraph which operates as a voltage-current converter in such a way that the accuracy of the voltage current conversion can be substantially independent of the spread in width of the resistance track and thus need be significantly influenced only by the (comparatively small) spread of the resistance per unit area.

According to the invention a second current is generated in a circuit branch which is arranged in parallel with the reference resistor, which second current produces a voltage drop, determined

by the same input voltage, across a second reference resistor which is arranged in the said branch, which second resistor has, compared with the first-mentioned said reference resistor, the same resistance per unit area, the same length and a different width, the difference between the currents flowing through said reference resistor forming the output current of the arrangement.

In a circuit thus constructed comprising two resistors to each of which the input voltage or a voltage derived therefrom is applied, the current components resulting from the spread in width will, provided the resistors are jointly manufactured, i.e. manufactured during the same processing steps, normally be equal and cancel each other when the difference between the currents is formed because the absolute spread in width of the two resistors will normally be the same.

Preferably, the difference between the currents flowing through the resistors is formed by means of a current mirror.

In order to isolate the currents flowing through the two resistors from each other it is advantageous to arrange the resistors in the emitter lines of respective transistors whose bases are driven by the input voltage.

If in such a circuit the bases are driven by the input voltage directly the difference between the input voltage and the base-emitter voltage of the transistors will appear across the resistors. It is therefore effective to drive the bases of the said transistors via respective operational amplifiers, which compensate for the base-emitter voltages of these transistors.

In order to minimize the base currents, and consequently the difference between the collector and emitter currents of the said transistors these transistors are preferably Darlington transistors or replaced by field-effect transistors.

Preferably, the said resistors are formed by doped zones in the semiconductor body in which the arrangement is formed.

Embodiments of the invention will now be described, by way of example, with reference to the drawing. In the drawing:

Figure 1 is the circuit diagram of a first embodiment of the

invention and

Figure 2 is the circuit diagram of a second embodiment of the invention.

In Figure 1 an integrated circuit in the form of a voltage-current converter for generating an output current I_A includes means for generating currents I_1 and I_2 which produce voltage drops across reference resistors R_1 and R_2 respectively, these voltage drops both being determined by an input voltage U_E. The reference resistors R_1 and R_2 are jointly manufactured and have the same resistance per unit area, the same length, but different widths. The resistor R_1 has a width $b + \Delta b$, whilst the resistor R_2 has a width $n \cdot b + \Delta b$, Δb being the same for both resistors because of the joint manufacture. Both resistors are formed by doped zones in the semiconductor body of the integrated current. The two resistors receive the input voltage U_E via the transistors T_1 and T_2, the resistors being arranged in the emitter lines and the input voltage being applied to the bases of these transistors. The collector currents of the transistors T_1 and T_2 are supplied by a current mirror 1. The complexity of this current mirror depends on the required accuracy of the conversion ratio. The difference between the two currents I_1 and I_2 forms the output current I_A, these currents I_1 and I_2 producing the same voltage drop, i.e. the input voltage U_E less the base-emitter voltages of transistors T_1 and T_2 respectively, across the resistors R_1 and R_2 respectively. Since the absolute spread in width of the two resistors is the same, the current components therein resulting from the spread in width (actual width minus nominal width of the resistors) for the same input voltage U_E coupled to each are themselves equal and cancel each other when the difference of the currents is formed.

If R_S = the layer resistance of R_1 and R_2
l = the resistor length of R_1 and R_2
b = the width of the resistor R_1
$n \cdot b$ = the width of the resistor R_2
Δb = the spread in resistor width,

the following relationships are valid:

$R_1 = R_S \cdot \frac{1}{b + \Delta b}$ and $R_2 = R_S \cdot \frac{1}{n \cdot b + \Delta b}$.

This means that the input voltage U_E produces a current $I_1 = U_E \cdot \frac{b + \Delta b}{R_S \cdot 1}$ in the resistor R_1 and a current $I_2 = U_E \cdot \frac{n \cdot b + \Delta b}{R_S \cdot 1}$ in the resistor R_2 (assuming for simplicity that all of the voltage U_E occurs across each resistance). The current difference, which forms the output current $I_A = I_2 - I_1 = U_E \cdot \frac{(n-1)b}{R_S \cdot 1}$, no longer contains the spread in width Δb, but only the nominal width b, i.e. the output current I_A no longer depends on the spread in width of the resistors R_1 and R_2.

As in the circuit shown in Figure 1 instead of the input voltage U_E the difference between this voltage and the base-emitter voltage of the respective transistor T_1 or T_2 appears across the resistors R_1 and R_2, it may be necessary to compensate for these base-emitter voltages if this is required in view of the desired accuracy of the circuit. Figure 2 is the circuit diagram of a second embodiment of the invention in which this is done. For this purpose the bases of the two transistors T_1 and T_2 are driven in the circuit of Figure 2 by the input voltage U_E via operational amplifiers 2 and 3 respectively. The output of each operational amplifier is connected to the base of the associated transistor. The input voltage U_E is applied to the non-inverting input of each operational amplifier, whilst the inverting input of each operational amplifier is connected to the emitter of the associated transistor. In this way the full input voltage U_E appears across the resistors R_1 and R_2; the base-emitter voltages are thus compensated for.

The principle of operation of the circuit shown in Figure 2 is identical to that of the circuit shown in Figure 1. However, the current mirror is more complex, so that the accuracy of the conversion ratio is higher. Moreover the output current I_A is taken from the junction point of the current mirror 1 and the transistor T_2 by means of a transistor T_3, which is a Darlington transistor.

The transistors T_1 and T_2 are also Darlington transistors in order to minimise the base currents of these two transistors, and consequently the difference between the collector current and the emitter current of each transistor. For this purpose the two transistors T_1 and T_2 may alternatively be field-effect transistors.

CLAIMS:

1. An integrated circuit arrangement comprising means for generating a current which produces a voltage drop across a reference resistor, which voltage drop is determined by an input voltage characterised in that a second current is generated in a circuit branch which is arranged in parallel with the reference resistor, which second current produces a voltage drop, determined by the same input voltage, across a second resistor which is arranged in the said branch, which second resistor has, compared with the first-mentioned said reference resistor, the same resistance per unit area, the same length and a different width, the difference between the currents flowing through said reference resistors forming the output content of the arrangement.

2. An arrangement as claimed in Claim 1, characterised in that the difference between the currents flowing through the resistors is formed by means of a current mirror.

3. An arrangement as claimed in Claim 1 or 2, characterised in that the resistors are arranged in the emitter lines of respective transistors whose bases are driven by the input voltage.

4. An arrangement as claimed in Claim 3, characterised in that the bases of the said transistors are driven via respective operational amplifiers which compensate for the base-emitter voltages of these transistors.

5. An arrangement as claimed in Claim 3 or 4, characterised in that the said transistors are Darlington transistors.

6. A modification of an arrangement as claimed in Claim 4, characterised in that the said transistors are replaced by field-effect transistors.

7. An arrangement as claimed in any of the preceding Claims, characterised in that the said resistors are formed by doped zones in the semiconductor body in which the arrangement is formed.

8. An integrated circuit arrangement substantially as described herein with reference to Figure 1 or Figure 2 of the drawing.

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RENEWAL DETAILS

PATENT No 2118394 11-4-83

RENEWAL DATE ~~27-10-1978~~ -
5th year renewal fee due 11 April 1987

RENEWAL FEE PAID FOR ..... YEAR ON .....

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FOR THE COMPTROLLER

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Publication No.
2118394 A dated 26 October 1983

Patent Granted: WITH EFFECT FROM SECTION 25(1) 28 AUG 1985

Application No.
8309726 filed on 11 April 1983

Priority claimed:
15 April 1982 in Germany (Federal Republic of) doc: 3213836

Title:
Integrated circuit arrangement comprising means for generating a current

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Classified to:
H3T H1K

Examination requested 21 DEC 1983

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Printed by the Patent Office at St. Mary Cray, 02 SEP 83