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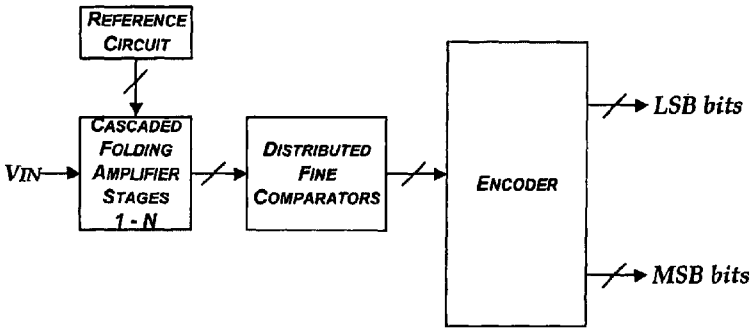


*FIG. 2A*

(57) Abstract: A system, apparatus and method for a folding analog-to-digital converter (ADC) are described. The general architecture of the folding ADC includes an array (1 - N) of cascaded folding amplifier stages, a distributed array of fine comparators, and an encoder. Each folding amplifier stage includes folding amplifiers that are configured to receive inputs from a prior stage, and also generate output signals for the next stage. The folding amplifiers output signals for a given stage are evaluated by a corresponding comparator stage, which may include multiple comparators, and also optionally coupled to an interpolator. The outputs of the comparators from all stages are collectively evaluated by the encoder, which generates the output of the folding ADC. Unlike conventional folding ADCs that require fine and coarse channels, the presently described folding ADC provides conversion without the need for a coarse channel. The encoder can also be arranged to facilitate recursive error correction.

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## AMENDED CLAIMS
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1. An analog-to-digital converter (ADC) apparatus that is arranged for operation as a folding ADC with a unified architecture using a fine channel without a coarse channel, wherein the apparatus is configured to convert an analog input signal (VIN) to a digital output signal (DOUT), the apparatus comprising:

a plurality (N) of folding amplifier stages (STAGE 1 through STAGE N), wherein the folding amplifier stages are arranged in a cascaded configuration such that a bus of input terminals for a subsequent folding amplifier stage is coupled to a bus of output terminals for a preceding folding amplifier stage in the cascaded configuration, wherein each folding amplifier stage includes a corresponding folding factor;

a plurality (N) of fine comparator stages (STAGE 1 through STAGE N), wherein the fine comparator stages are arranged in a distributed configuration where each of the fine comparator stages is associated with a corresponding one of the plurality of folding amplifier stages, wherein each of the fine comparator stages includes a bus of input terminals that is coupled to the bus of output terminals for the corresponding folding amplifier stage, and wherein each of the fine comparator stages includes a bus of output terminals; and

an encoder that includes a bus of input terminals, wherein the bus of input terminals in the encoder is correspondingly coupled to the bus of output terminals from each of the fine comparator stages, wherein the encoder is arranged to evaluate all outputs from the fine comparator stages to determine the digital output signal.

2. The apparatus of claim 1, wherein the folding factors for the plurality of folding amplifier stages are the same as one another.

3. The apparatus of claim 1, wherein the folding factors for the plurality of folding amplifier stages are different from one another.

4. The apparatus of claim 1, further comprising a track and hold circuit that includes an input terminal that is arranged to receive the analog input signal (VIN) and an output terminal that is coupled to a first one of the plurality of amplifier stages (STAGE 1).

5. The apparatus of claim 1, further comprising:

a reference circuit that is arranged to generate a plurality of reference signals and to provide the reference signals to a bus of output terminals;

a first amplifier stage (STAGE 0) that includes a bus of input terminals and a bus of output terminals, wherein the bus of input terminals from the first amplifier stage (STAGE 0) is coupled to the bus of output terminals from the reference circuit, wherein the bus of output terminals from the first amplifier stage (STAGE 0) is coupled to the bus of input terminals for a first one of the plurality of folding amplifier stages (STAGE 1), and wherein the first amplifier stage (STAGE 0) is arranged to combine the analog input signal (VIN) with the plurality of reference signals to provide voltage amplification; and

a first fine comparator stage (STAGE 0) that includes a bus of input terminals that is coupled to the bus of output terminals from the first amplifier stage (STAGE 0), wherein the first fine comparator stage includes one or more outputs that are coupled to the encoder.

6. The apparatus of claim 1, wherein the plurality of folding amplifier stages are arranged as fully differential amplifier stages such that each bus of input terminals in the amplifier stages corresponds to a differential input signal and each bus of output terminals in the amplifier stages corresponds a differential output signal.

7. The apparatus of claim 6, wherein each of the plurality of fine comparator stages is arranged to evaluate the differential output signals from the corresponding one of the folding amplifier stages.

8. The apparatus of claim 1, wherein the plurality of folding amplifier stages are arranged as single-ended amplifier stages such that each bus of input terminals in the amplifier stages corresponds to a single-ended input signal and each bus of output terminals in the amplifier stages corresponds a single-ended output signal.

9. The apparatus of claim 8, wherein each of the plurality of fine comparator stages is arranged to evaluate the single-ended output signals from the corresponding one of the folding amplifier stages.

10. The apparatus of claim 8, further comprising a reference circuit that is arranged to generate a plurality of reference levels for each of the plurality of folding amplifier stages.

11. The apparatus of claim 1, further comprising a plurality (N) of interpolator stages (STAGE 1 through STAGE N), wherein the bus of output terminals from each of the folding amplifier stages (STAGE 1 through STAGE N) is coupled to a corresponding one of the plurality of interpolator stages (STAGE 1 through STAGE N).

12. The apparatus of claim 1, further comprising a plurality (N-1) of interpolator stages (STAGE 1 through STAGE N-1), wherein the bus of output terminals from a corresponding one of the folding amplifier stages (STAGE 1 through STAGE N-1) is coupled to a corresponding one of the plurality of interpolator stages.

13. The apparatus of claim 1, each of the plurality (N) of folding amplifier stages comprising an array of individual amplifiers, wherein:

each individual amplifier includes an input terminal that is coupled to the bus of input terminals for the corresponding folding amplifier stage;

each individual amplifier includes an output terminal; and

a polarity of each of the individual amplifiers is configured such that groups of the individual amplifiers have output terminals that are coupled in common to the bus of output terminals for the corresponding folding amplifier stage and such that the groups of the individual amplifiers are configured to have an alternating polarity to achieve the folding factor for the corresponding folding amplifier stage.

14. The apparatus of claim 13, wherein the individual amplifiers are either fully differential amplifiers or single-ended amplifiers.

15. The apparatus of claim 13, further comprising a plurality (N-1) of interpolator stages (STAGE 1 through STAGE N-1), wherein the bus of output terminals from a corresponding one of the folding amplifier stages (STAGE 1 through STAGE N-1) is coupled to a corresponding one of the plurality of interpolator stages, wherein each of the groups of the individual amplifiers for a corresponding one of the plurality

of folding amplifier stages is coupled to a different input of the corresponding interpolator stage.

16. The apparatus of claim 13, each of the plurality (N) of fine comparator stages comprising an array of individual comparators, wherein:

each individual comparator includes an input terminal that is coupled to a corresponding one of the output terminals for the corresponding group of individual amplifiers for the corresponding folding amplifier stage;

each individual comparator includes an output terminal; and

the output terminals of the individual comparators are coupled to the bus of input terminals for the encoder.

17. The apparatus of claim 16, wherein the individual comparators are either fully differential comparators or single-ended comparators.

18. The apparatus of claim 1, wherein each of the plurality (N) of fine comparator stages is arranged to provide an output that is cyclically coded such that upward trending codes are different from downward trending codes.

19. The apparatus of claim 1, wherein the encoder is arranged to evaluate a group of outputs from each of the plurality (N) of fine comparator stages to identify cyclical codes such that upward trending codes are different from downward trending codes.

20. The apparatus of claim 1, wherein the encoder is arranged to evaluate comparator outputs of a selected stage (STAGE K) of the plurality (N) of fine comparator stages and also evaluate comparator outputs of a preceding stage (STAGE K-1)

of the plurality of fine comparator stages to identify a fold associated with the selected stage (STAGE K) of the plurality (N) of fine comparator stages.

21. The apparatus of claim 1, wherein the encoder is arranged to recursively correct comparator output values for each prior stage (STAGE K-1) of the plurality (N) of fine comparator stages based on an evaluation of comparator output values for each current stage (STAGE K) of the plurality (N) of fine comparator stages.

22. The apparatus of claim 1, wherein the encoder is arranged to convert the digital output signal (DOUT) to base-2.

23. The apparatus of claim 1, further comprising a plurality of sample and hold stages, wherein each of the sample and hold stages is associated with one of the folding amplifier stages, wherein each of the sample and hold stages includes a bus of input terminals that is coupled to the bus of output terminals for the corresponding folding amplifier stage, and wherein each of the sample and hold stages includes a bus of output terminals that is coupled to the subsequent folding amplifier stage.

24. The apparatus of claim 23, each of the plurality of sample and hold stages comprising an array of individual sample and hold circuits, wherein each individual sample and hold circuit includes an input terminal that is coupled to the bus of output terminals for the corresponding folding amplifier stage.

25. The apparatus of claim 24, wherein the individual sample and hold stages are either fully differential sample and hold stages or single-ended sample and hold stages.

26. An analog-to-digital converter (ADC) system that is arranged for operation as a folding ADC with a unified architecture using a fine channel without a coarse channel, wherein the system is configured to convert an analog input signal (VIN) to a digital output signal (DOUT), the system comprising:

a reference circuit that is arranged to provide a plurality of reference signals;

a first amplifier stage (STAGE 0) that is arranged to generate a plurality of output signals in response to the plurality of reference signals and also in response to the input signal (VIN);

a plurality (N) of folding amplifier stages (STAGE 1 through STAGE N) and corresponding interpolator stages (STAGE 1 through STAGE N) arranged in a cascaded configuration such that outputs from a preceding folding amplifier stage are coupled to inputs of a succeeding folding amplifier stage through the corresponding interpolator stage, wherein the first amplifier stage (STAGE 0) precedes a first one of the folding amplifier stages (STAGE 1);

a last folding amplifier stage (STAGE N+1) that follows a last one of the plurality of folding amplifier stages (STAGE N), wherein outputs of the last one of the plurality of folding amplifiers stages (STAGE N) are coupled to inputs of the last folding amplifier stage (STAGE N+1) through the corresponding interpolator stage;

a first fine comparator stage (STAGE 0) that is arrange to generate a coded output signal in response to the output signals of the first amplifier stage (STAGE 0);

a plurality (N) of additional fine comparator stages (STAGE 1 through STAGE N) that are each associated with a corresponding one of the plurality of folding amplifier stages (STAGE 1 through STAGE N), where each of the plurality of

additional fine comparator stages is arranged to generate a corresponding coded output signal in response to output signals from the corresponding one of the plurality of folding amplifier stages;

a last fine comparator stage (STAGE N+1) that is arrange to generate a last coded output signal in response to output signals of the last folding amplifier stage (STAGE N+1); and

an encoder that is arranged to collectively evaluate the coded output signals from the first fine comparator stage, the additional fine comparator stages and the last fine comparator stage such that the digital output signal (DOUT) is determined by evaluation of fine comparator stage outputs without evaluating separated coarse channel results.

27. The system of claim 26, wherein the encoder is arranged to evaluate the coded output signals of a selected one of the fine comparator stages (STAGE K) and also evaluate the coded output signals of a preceding one (STAGE K-1) of the fine comparator stages to identify a fold associated with the selected one of the fine comparator stages (STAGE K).

28. The system of claim 26, wherein the encoder is arranged to recursively correct the coded output signals for each prior fine comparator stage (STAGE K-1) based on an evaluation of the coded output signals for each current fine comparator stage (STAGE K).

29. The system of claim 26, wherein the encoder is arranged to convert the digital output signal (DOUT) to base-2.

30. The system of claim 26, further comprising:

a first sample and hold stage that is coupled between the first amplifier stage (STAGE 0) and the corresponding interpolator stage;

a plurality (N) of sample and hold stages (STAGE 1 through STAGE N), where each of the plurality of sample and hold stages is coupled between a corresponding one of the plurality of folding amplifier stages and the corresponding interpolator stage; and

an additional sample and hold stage that is coupled between the last folding amplifier stage and the last fine comparator stage.

31. An analog-to-digital converter (ADC) method that is arranged for operation as a folding ADC with a unified architecture using a fine channel without a coarse channel, wherein the method converts an analog input signal (VIN) to a digital output signal (DOUT), the method comprising:

coupling reference signals and the analog input signal (VIN) to an input of a first stage (STAGE 0) amplifier;

coupling an output of the first stage amplifier to an input of a first stage (STAGE 0) fine comparator;

selecting each of a plurality of folding amplifier stages (STAGE 1 through STAGE N) in succession beginning from STAGE 1, and for each selected amplifier stage (STAGE X):

coupling outputs from a previous stage (STAGE X - 1) amplifier to inputs of a current stage (STAGE X) amplifier, and

coupling outputs of the current stage (STAGE X) amplifier to inputs of a current stage (STAGE X) fine comparator; and

evaluating outputs of each stage (STAGE 0 through STAGE N) fine comparator with an encoder process, wherein the encoder process determines the digital output signal (DOUT) from the collective outputs of the fine comparators without evaluating separated coarse channel results.

32. The method of claim 31, the encoder process comprising identifying a final conversion value for the digital output signal (DOUT) by evaluating the outputs from the fine comparators for each of the stages (STAGE 0 through STAGE N), identifying a fine conversion value for each of the evaluated outputs from the fine comparators, and identifying a fold associated with each of the evaluated outputs from the fine comparators.

33. The method of claim 31, wherein the encoding process is arranged to convert the digital output signal (DOUT) to base-2.

34. The method of claim 31, the encoder process comprising:

selecting each fine comparator stage in succession beginning from STAGE 1 as a currently selected stage, and for each currently selected stage (STAGE K):

evaluating the outputs from the fine comparators for the currently selected stage (STAGE K) and cyclically encoding a fine conversion value, and

evaluating the outputs from the fine comparators for the previously selected stage (STAGE K-1) and identifying a fold for the currently selected stage (K); and

identifying a final conversion value for the digital output signal (DOUT) from the identified folds and the cyclically encoded fine conversion values for the stages.

35. The method of claim 31, the encoder process comprising:

selecting each fine comparator stage in succession beginning from STAGE 1 as a currently selected stage, and for each currently selected stage (STAGE K):

evaluating the outputs from the fine comparators for the currently selected stage (STAGE K) and cyclically encoding a fine conversion value,

evaluating the outputs from the fine comparators for the previously selected stage (STAGE K-1) and identifying a fold for the currently selected stage (K), and

recursively correcting the fine conversion value for the currently selected stage (STAGE K) based on the fine conversion values for each of the previously selected stages (STAGE K-1 through STAGE 0); and

identifying a final conversion value for the digital output signal (DOUT) from the identified folds and the cyclically encoded fine conversion values for the stages.

36. The method of claim 31, further comprising sampling the outputs from the current stage (STAGE X) with a sample and hold stage for one or more of the selected amplifier stages.

37. The method of claim 36, wherein coupling the outputs from the previous stage (STAGE X - 1) amplifier to the inputs of the current stage (STAGE X) amplifier further comprises coupling the outputs from the sample and hold stage from the previous stage (X-1) to the inputs of the current stage (STAGE X) amplifier.

38. The method of claim 36, wherein coupling the outputs from the previous stage (STAGE X - 1) amplifier to the inputs of the current stage (STAGE X) fine comparators further comprises coupling the outputs from the sample and hold stage from the previous stage (X-1) to the inputs of the current stage (STAGE X) fine comparator.

39. An analog-to-digital converter apparatus comprising:

at least two folding amplifier stages arranged in a cascaded configuration, each folding amplifier stage having a folding factor;

at least two comparator stages, each comparator stage configured to receive an output of one of the amplifier stages; and

an encoder configured to determine a digital output signal based on outputs of the comparator stages.

40. The apparatus of Claim 39, further comprising:

a non-folding amplifier stage configured to receive an analog input signal; and

an additional comparator stage configured to receive an output of the non-folding amplifier stage.

41. The apparatus of Claim 40, further comprising:

a reference circuit configured to provide a reference signal to the non-folding amplifier stage.

42. The apparatus of Claim 39, further comprising:

at least two interpolator stages, each interpolator stage coupled to an input of one of the folding amplifier stages.

43. The apparatus of Claim 39, further comprising:

at least two sample and hold circuits, each sample and hold circuit configured to receive the output of one of the amplifier stages;

wherein each comparator stage is coupled to one of the sample and hold circuits.

44. The apparatus of Claim 39, wherein the folding factors of the folding amplifier stages are equal to one another.

45. The apparatus of Claim 39, wherein the folding factors of the folding amplifier stages are different from one another.

46. The apparatus of Claim 39, wherein:

each folding amplifier stage comprises a fully differential amplifier stage configured to receive a differential input signal and to generate a differential output signal; and

each comparator stage is configured to receive the differential output signal from a corresponding one of the folding amplifier stages.

47. The apparatus of Claim 39, wherein:

each folding amplifier stage comprises a single-ended amplifier stage configured to receive a single-ended input signal and to generate a single-ended output signal; and

each comparator stage is configured to receive the single-ended output signal from a corresponding one of the folding amplifier stages.

48. The apparatus of Claim 39, wherein each folding amplifier stage comprises an array of individual amplifiers.

49. The apparatus of Claim 48, wherein:

each individual amplifier includes an input terminal coupled to a bus of input terminals for the corresponding folding amplifier stage;

each individual amplifier includes an output terminal coupled to a bus of output terminals for the corresponding folding amplifier stage; and

a polarity of each individual amplifier is configured such that alternating groups of the individual amplifiers have alternating polarities to achieve the folding factor for the corresponding folding amplifier stage.

50. A method for converting an analog input signal into a digital output signal, the method comprising:

processing the analog input signal using multiple folding amplifier stages arranged in a cascaded configuration, each folding amplifier stage having a folding factor;

receiving outputs from the folding amplifier stages at multiple comparator stages;

providing outputs from the comparator stages to an encoder; and

generating the digital output signal using the encoder based on the outputs of the comparator stages.

51. The method of Claim 50, further comprising:

processing the analog input signal using a non-folding amplifier stage coupled to a first of the folding amplifier stages;

receiving an output from the non-folding folding amplifier stage at an additional comparator stage; and

providing an output from the additional comparator stage to the encoder.

52. The method of Claim 51, further comprising:

providing a reference signal to the non-folding amplifier stage.

53. The method of Claim 50, wherein generating the digital output signal comprises using an encoding process to determine the digital output signal based on the outputs of the comparator stages without evaluating separated coarse channel results.

54. The method of Claim 53, wherein the encoding process comprises identifying a final conversion value for the digital output signal by:

evaluating the outputs from the comparator stages;

identifying a conversion value for each of the evaluated outputs; and

identifying a fold associated with each of the evaluated outputs.

55. The method of Claim 53, wherein the encoding process comprises:

selecting each of the comparator stages in succession;

for a currently-selected comparator stage:

evaluating the output from the currently-selected comparator stage and cyclically encoding a conversion value; and

evaluating the output from a previously-selected comparator stage and identifying a fold for the currently-selected comparator stage; and

identifying a final conversion value for the digital output signal from the identified folds and the cyclically encoded conversion values.

56. The method of Claim 53, wherein the encoding process comprises:

selecting each of the comparator stages in succession;

for a currently-selected comparator stage:

evaluating the output from the currently-selected comparator stage and cyclically encoding a conversion value;

evaluating the output from a previously-selected comparator stage and identifying a fold for the currently-selected comparator stage; and

recursively correcting the conversion value for the currently-selected comparator stage based on at least one conversion value for at least one previously-selected comparator stage; and

identifying a final conversion value for the digital output signal from the identified folds and the cyclically encoded conversion values.

57. The method of Claim 50, further comprising:

sampling the outputs from the folding amplifier stages with sample and hold stages;

wherein receiving the outputs from the folding amplifier stages at the comparator stages comprises receiving outputs from the sample and hold stages at the comparator stages.

58. An analog-to-digital converter system comprising:

a first amplifier stage configured to receive an analog input signal;

a reference circuit configured to provide a reference signal to the first amplifier stage;

at least two folding amplifier stages arranged in a cascaded configuration, a first of the folding amplifier stages coupled to the first amplifier stage, each folding amplifier stage having a folding factor;

at least three comparator stages, each comparator stage configured to receive an output of one of the amplifier stages; and

an encoder configured to determine a digital output signal based on outputs of the comparator stages.