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# (54) Title: A METAL-SEMICONDUCTOR-METAL (MSM) HETEROJUNCTION DIODE

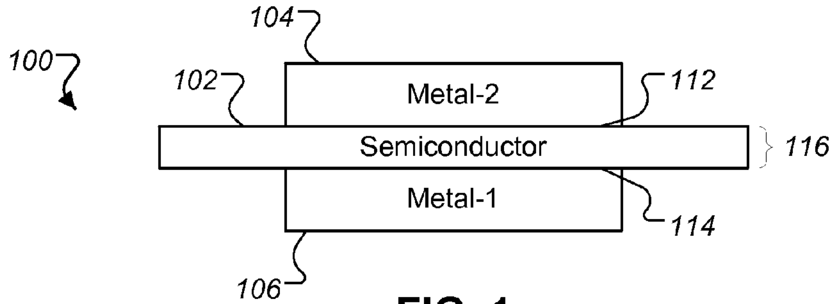

FIG. 1

**(57) Abstract**: In one aspect, a diode comprises: a semiconductor layer having a first side and a second side opposite the first side, the semiconductor layer having a thickness between the first side and the second side, the thickness of the semiconductor layer being based on a mean free path of a charge carrier emitted into the semiconductor layer; a first metal layer deposited on the first side of the semiconductor layer; and a second metal layer deposited on the second side of the semiconductor layer.

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## AMENDED CLAIMS

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1. A diode, comprising:

a semiconductor layer having a first side and a second side opposite the first side, the semiconductor layer having a thickness between the first side and the second side, the thickness of the semiconductor layer being based on a mean free path of a charge carrier emitted into the semiconductor layer;

a first metal layer deposited on the first side of the semiconductor layer; and

a second metal layer deposited on the second side of the semiconductor layer;

wherein the thickness of the semiconductor layer that is based on the mean free path of the charge carrier increases an amount of ballistic transport of the charge carrier through the semiconductor layer, relative to an amount of ballistic transport of the charge carrier through another semiconductor layer with another thickness that is independent of the mean free path of the charge carrier.

2. The diode of claim 1, wherein the thickness of the semiconductor layer is comparable to or less than the mean free path of the charge carrier emitted into the semiconductor layer.

3. The diode of claim 1, wherein the diode has a cut-off frequency exceeding 100 THz.

4. The diode of claim 1, wherein the diode has a cut-off frequency

exceeding 1000 THz.

5. The diode of claim 1, wherein the first metal layer and the second metal layer comprise a same metal, and an interface of the semiconductor layer is degenerately doped for creation of an ohmic contact.

6. The diode of claim 1, wherein the first metal layer comprises a first metal, the second metal layer comprises a second metal, and the first metal and the second metal are different metals.

7. The diode of claim 6, wherein an interface of the semiconductor layer is degenerately doped for creation of an ohmic contact.

8. ( The diode of claim 1, wherein the semiconductor layer comprises one or more of a crystalline semiconductor and a polycrystalline semiconductor.

9. The diode of claim 8, wherein the semiconductor layer comprises one or more of silicon (Si), germanium (Ge), silicon germanium (SiGe), aluminum antimonide (AlSb), gallium antimonide (GaSb), gallium arsenide (GaAs), indium antimonide (InSb), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), indium phosphide (InP), cadmium selenide (CdSe), cadmium telluride (CdTe), cadmium sulfide (CdS), zinc selenide (ZnSe), zinc telluride (ZnTe), zinc sulfide (ZnS), zinc oxide (ZnO), titanium oxide ($TiO_2$), lead sulfide (PbS), and lead telluride (PbTe).

10. The diode of claim 1, wherein the first metal layer and the second metal layer each comprise at least one metal selected from the group consisting of silver (Ag), aluminum (Al), gold (Au), cobalt (Co), chromium (Cr), copper (Cu), gadolinium (Gd), hafnium (Hf), indium (In), iridium (Ir), magnesium (Mg), manganese (Mn), molybdenum (Mo), nickel (Ni), lead (Pb), palladium (Pd), platinum (Pt), rhodium (Rh), tantalum (Ta), titanium (Ti), tungsten (W), and zinc (Zn).

11. The diode of claim 1, wherein the diode comprises a metal semiconductor-metal heterojunction diode (MSM diode), and wherein the MSM diode further comprises:

a heterojunction between the semiconductor layer and one or more of the first metal layer and the second metal layer.

12. A method for fabricating a diode, comprising:

providing a semiconductor having a first side and a second side opposite the first side, the semiconductor having a thickness between the first side and the second side, the thickness being based on a mean free path of a charge carrier emitted into the semiconductor;

depositing a first metal on the first side of the semiconductor; and

depositing a second metal on the second side of the semiconductor;

wherein the thickness of the semiconductor that is based on the mean free path of the charge carrier increases an amount of ballistic transport of the charge carrier through the semiconductor, relative to an amount of ballistic transport of the charge carrier through another semiconductor with another thickness that is independent of the mean free path of the charge carrier.

13. The method of claim 12, wherein the thickness of the semiconductor is comparable to or less than the mean free path of the charge carrier emitted into the semiconductor.

14. The method of claim 12, wherein obtaining the semiconductor comprises:

obtaining a substrate of layered materials that includes a layer comprising the semiconductor and one or more other layers comprising at least one material that is different from the semiconductor;

bonding the first side of the semiconductor to a carrier wafer to position the first metal between the semiconductor and the carrier wafer; and

removing the one or more other layers to expose the second side of the semiconductor.

15. The method of claim 14, wherein:

depositing the first metal on the first side of the semiconductor comprises patterning the first side of the semiconductor; and

bonding the first side of the semiconductor to the carrier wafer comprises bonding the first side of the semiconductor to the carrier wafer using an insulating adhesive.

16. The method of claim 14, wherein:

depositing the first metal on the first side of the semiconductor comprises depositing the first metal directly onto the first side of the semiconductor as a uniform metal film; and bonding the first side of the semiconductor to the carrier wafer comprises bonding the first side of the semiconductor to the carrier wafer using an adhesive.

17. The method of claim 12, wherein the first metal and the second metal are of a same metal, and the method further comprises:

degenerate doping of a surface of the semiconductor layer for creation of an ohmic contact.

18. The method of claim 12, wherein the first metal and the second metal are different metals.

19. The method of claim 18, further comprising:

degenerate doping of a surface of the semiconductor layer for creation of an ohmic contact.

20. The method of claim 12, wherein the semiconductor comprises one or more of a crystalline semiconductor and a polycrystalline semiconductor.

21. The method of claim 20, wherein the semiconductor comprises one or more of silicon (Si), germanium (Ge), silicon germanium (SiGe), aluminum antimonide (AlSb), gallium antimonide (GaSb), gallium arsenide (GaAs), indium antimonide (InSb), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), indium phosphide (InP), cadmium selenide (CdSe), cadmium telluride (CdTe), cadmium sulfide (CdS), zinc

selenide (ZnSe), zinc telluride (ZnTe), zinc sulfide (ZnS), zinc oxide (ZnO), titanium oxide ($TiO_2$), lead sulfide (PbS), and lead telluride (PbTe).

22. The method of claim 12, wherein the first metal and the second metal each comprise at least one metal selected from the group consisting of silver (Ag), aluminum (Al), gold (Au), cobalt (Co), chromium (Cr), copper (Cu), gadolinium (Gd), hafnium (Hf), indium (In), iridium (Ir), magnesium (Mg), manganese (Mn), molybdenum (Mo), nickel (Ni), lead (Pb), palladium (Pd), platinum (Pt), rhodium (Rh), tantalum (Ta), titanium (Ti), tungsten (W), and zinc (Zn).

23. A p-type metal-semiconductor-metal heterojunction diode (MSM diode), comprising:

a silicon layer having a first side and a second side opposite the first side, a surface of the first side being doped with boron at a surface concentration of $1x10^{20}$ $cm^{-3}$, the silicon layer having a thickness between the first side and the second side, the thickness of the silicon layer being 30 nm;

a platinum layer deposited on the first side of the silicon layer;

a first heterojunction interface between the silicon layer and the platinum layer;

a cobalt layer deposited on the second side of the silicon layer; and

a second heterojunction interface between the silicon layer and the cobalt layer.

24. A n-type metal-semiconductor-metal heterojunction diode (MSM diode), comprising:

a silicon layer having a first side and a second side opposite the first side, a surface of the first side being doped with phosphorus at a surface concentration of $2\text{x}10^{20}$ $\text{cm}^{-3}$, the silicon layer having a thickness between the first side and the second side, the thickness of the silicon layer being 60 nm;

a first chromium layer deposited on the first side of the silicon layer;

a first heterojunction interface between the first chromium layer and the silicon layer;

a second chromium layer deposited on the second side of the silicon layer; and

a second heterojunction interface between the second chromium layer and the silicon layer.

25. A method comprising:

obtaining a diode with (i) a semiconductor layer with a thickness being based on a mean free path of a charge carrier emitted into the semiconductor, (ii) a first metal on a first side of the semiconductor layer, and (iii) a second metal on a second side of the semiconductor layer;

emitting the charge carrier into the semiconductor layer of the diode; and

increasing an amount of ballistic transport of the charge carrier through the semiconductor layer with the thickness that is based on the mean free path of the charge carrier, relative to an amount of ballistic transport of the charge carrier through another semiconductor layer with another thickness that is independent of the mean free path of the charge carrier.