

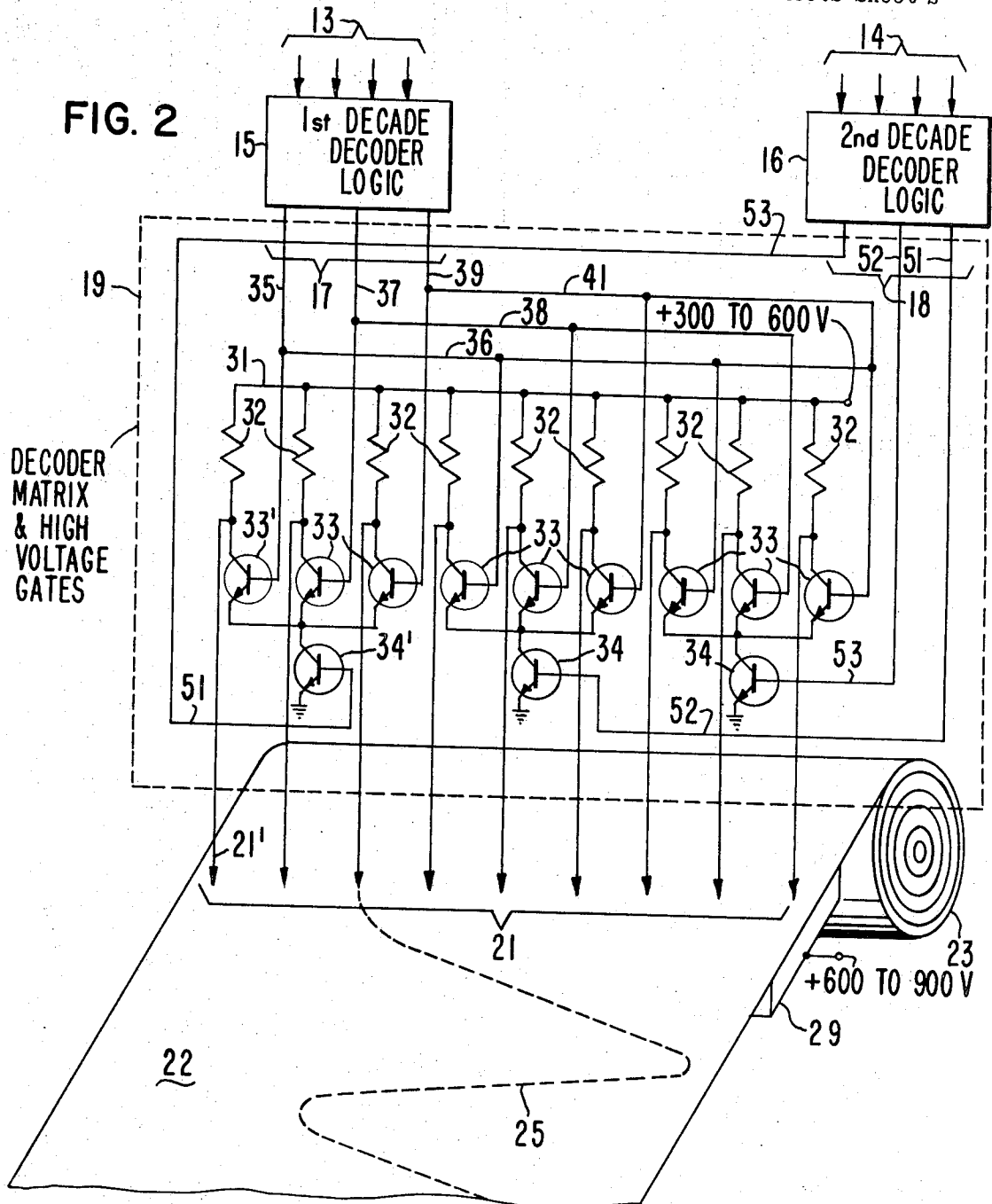
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ELECTROGRAPHIC RECORDER WITH SERIES CONNECTED GATES
IN A DECODING MATRIX DRIVING AN ARRAY
OF ELECTRODES

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ELECTROGRAPHIC RECORDER WITH SERIES CONNECTED GATES IN A DECODING MATRIX DRIVING AN ARRAY OF ELECTRODES
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5 Claims

ABSTRACT OF THE DISCLOSURE

An electrographic recorder is disclosed employing an array of writing electrodes disposed crosswise of an electrographic recording web. The recorder includes an input channel having an analog-to-digital converter means for converting analog input signals into binary coded decimal data outputs. The outputs are fed to first and second digit decoder logic circuits each producing 10 line decimal output signals fed to a one-out-of-100 decoder matrix which decodes the 10 line decimal outputs to produce 100 line output for driving a 100 electrode array to record the input signal on the electrographic web. The one-out-of-a-100 decoder matrix includes a series connection of first and second high voltage gating transistors. There are 100 first gating transistors, there being one transistor for each of the electrodes of the writing array. The control electrodes for the first gating transistors are ganged together in groups of 10 with every tenth transistor ganged together and fed by one of the 10 line decimal outputs of the first digit decoder. There are 10 second gating transistors series connected with the first transistors with one transistor series connected with each group of 10 first transistor gates. The second gating transistors are driven from the output decoder signals derived from the second digit decoder. The series connected first and second gating transistors form a decoding matrix of 100 AND gates for applying the relatively high electrostatic writing potential to the selected writing electrode for reproducing the input signal on the recording medium.

DESCRIPTION OF THE PRIOR ART

Heretofore, electrographic recorders have been proposed employing an array of writing electrodes disposed crosswise of a recording web for recording signals on the recording web. In such a device the input signal is converted into binary decimal coded data by means of an analog-to-digital converter. The binary decimal coded data is fed to a pair of decoder matrices, one matrix for the first decade and the second matrix for the second decade. The writing electrodes are ganged together in groups of 10 with each tenth electrode being ganged together to one of the 10 line outputs of the first decoding matrix. A second writing electrode is disposed under the writing array and this electrode is segmented into 10 segments with the 10 line outputs of the second decade decoder fed to the respective decade segments of the electrode.

One of the problems encountered with this arrangement is that segmenting the electrode plate into the decade segments interferes, to a certain extent, with obtaining uniform writing across the full length of the writing array, as the gaps between adjacent decade plates produce a line type pattern in the recorded image. Therefore, it is desirable to obtain a decoding matrix arrangement which will avoid the difficulties of a segmented writing electrode plate but will have the advantages of incorporating first and second decade decoder logic in combination of pair of decoding matrices.

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SUMMARY OF THE PRESENT INVENTION

The principal object of the present invention is the provision of an improved electrographic recorder.

One feature of the present invention is the provision, in an electrographic recorder of the type which converts an analog input signal into n digits of binary coded decimal representative of the input to be recorded, of a one-out-of- M decoding matrix including a series connection of n gating switch groups for gating the writing potentials to the array of signal tracing electrodes, such n groups forming portions of the decoding matrix, whereby the decoding matrix is simplified.

Another feature of the present invention is the same as the preceding feature wherein $n=2$ and the switches of the first and second gating switch groups are transistors capable of gating a writing potential in excess of 200 volts, whereby the voltage drop across each of the gating transistors is less than the voltage drop across the gate if only one gating transistor were employed.

Another feature of the present invention is the same as any one or more of the preceding features wherein the decoder circuitry includes first and second digit decoders operable upon the binary coded decimal data outputs of the analog-to-digital converter to derive first and second 10 line binary decimal output decoding control signals and wherein the first gates are controlled by the first decoding control signals and the second gates are controlled by the second decoding control signals.

Other features and advantages of the present invention will become apparent upon a perusal of the following specification taken in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram, partly in block diagram form and partly in perspective, of an electrographic recorder incorporating features of the present invention, and FIG. 2 is an enlarged detail view of a portion of the structure of FIG. 1 delineated by line 2—2.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to FIG. 1 there is shown an electrographic recorder 1 incorporating features of the present invention. The recorder 1 includes a pair of input terminals 2 and 3 to which is applied an input signal E_i to be measured. The input signal is fed to a preamplifier 4 wherein it is amplified and fed via resistor 5 to one input of an error detector 6. The series resistor 5 converts the input voltage E_i into an input current I_i to be compared in the error detector 6.

The error detector 6 forms a portion of an analog-to-digital converter 7. The analog-to-digital converter 7 includes a dual decade up-down counter circuit 8. One output of the counter circuit 8 is fed to an array of current generators 9 for generating a current I_r corresponding in amplitude to the count in the counter circuit 8. The output current I_r of the counter forms a reference feedback current fed to the other input of the error detector 6 for comparison with the input signal I_i to be measured.

The output of the error detector 6 is an error voltage E_e which is fed to one input of a dual comparator 11 which compares the error voltage E_e against a pair of reference levels corresponding to the upper and lower level of a dead zone having a width preferably equal to the voltage difference represented by adjacent numerical counts of the counter circuit 8. The output of the dual comparator 11 is a binary coded signal indicative of null balance of the analog-to-digital converter and can take any one of three possible forms. One output is a "DON'T COUNT" command corresponding to an error voltage E_e .

falling within the dead zone of the comparator 11. A second output of the dual comparator 11 is an UP COUNT command produced when the error voltage E_e is above the upper level of the dead zone. A third output of the dual comparator is a DOWN COUNT command obtained when the error voltage E_e is below the lower level of the dead zone. The output of the dual comparator 11 is fed to a decoder controller 12 which decodes the binary count commands and feeds a control signal to the counter circuit 8 causing the counter 8 to track the input signal E_i .

Another output of the counter circuit 8 is a binary coded decimal data output, one of such outputs being provided for each digit of the dual decade counter 8. Counter circuit 8 may handle "n" digits; FIG. 2 merely illustrates an example where $n=2$.

The first digit of binary coded decimal from digit input channel 13 is fed to a first digit decoder logic circuit 15 and the second digit of binary coded decimal from digit input channel 14 of the second decade of the counter 8 is fed to a second digit decoder logic circuit 16. Each of the decoder logic circuits 15 and 16 converts its input into a base N_1 and N_2 output respectively which in FIG. 1 is shown as a 10 line decimal output 17 and 18, respectively. The two 10 line decimal outputs 17 and 18 are fed to a combined one-out-of-M decoder matrix and high voltage gate circuit 19 (M equals $N_1 \times N_2$ equals $10 \times 10 = 100$) which converts the 10 line decimal inputs into a 100 line binary data output 20 fed to an array of 100 signal tracing electrodes 21 disposed crosswise of a strip of electrographic recorder paper 22 pulled from a supply roll 23 past the writing array 21 by means of a motor driven friction drive wheel 24.

The 100 line binary data output applied to the writing array 21 selectively energizes the proper one of the electrodes to lay down a charge image 25 on the charge retentive surface of the electrographic recording paper 22. An inking channel 26 is disposed across the recording paper 22 and includes an inking slot 27 cut through one side wall of the channel 26 to permit liquid ink flowing through the channel 26 to come into fluid contact with the charge image to be developed on the electrographic recording paper 22. The ink includes colloiddally suspended positively charged toner particles which are attracted to the negative charge image 25 for developing same at 25'.

The one-out-of-M decoder matrix 19 includes n gating switch groups forming M and gates through series connected high voltage transistor switches, more fully described below with regard to FIG. 2, for selectively gating a relatively high writing potential to the electrodes of the array 21. More specifically, the writing electrode structure includes a writing electrode plate or conductive means 29 disposed on the opposite side of the electrographic paper 22 from the writing array 21 and operated at a relatively high potential as of plus 600 to 900 volts. It typically takes approximately minus 500 volts on the writing electrodes 21 with respect to the electrode plate 29 to deposit a charge image on the charge retentive surface of the recording paper 22. A relatively high positive standby potential as of plus 300 to 600 volts (insufficient to cause writing) is applied to all of the electrodes of the array 21 with the exception of the electrode which is to perform the writing. The decoder matrix selects the proper writing electrode and the series connected gates drop the potential on the selected electrode from plus 300 volts to ground potential by opening a gate circuit between the electrode and ground. When the selected electrode 21 is gated to ground potential, an additional potential sufficient to write of minus 600 to 900 volts appears on that electrode relative to the plate electrode 29 such that a charge image is deposited on the recording web 22.

Referring now to FIG. 2 the decoder matrix 19 is shown in greater detail. For the sake of simplicity of explanation, the decoder matrix 19 of FIG. 2 will be described as employed with a three line output 17 from the first digit decoder 15 and a three line output from the second de-

coder 16 for application to a writing array 21 containing 9 writing electrodes. In other words, the output of the decoder matrix 19 is described and shown as a 9 line output instead of the actual 100 line output.

The plus 300 to 600 volts standby potential 0, to be applied to the writing array 21 is applied to the array via a bus 31 and an array of resistors 32 series connected between the separate electrodes 21 and the bus 31. Since essentially no current passes from the electrode array 21 to the paper 22 or to the writing electrode plate 29, the potential applied via bus 31 will appear on the electrodes 21.

A first group of gating transistors 33 have their collector electrodes connected to the resistors 32 and their emitters ganged together in groups of 3, which in the case of a decade decoder would be in groups of 10. A second group of transistors 34 are series connected with the first group of transistors 33 such that each ganged group of first transistors 38 includes one second gating transistor 34 connected in series therewith to ground. The collector electrodes of the second gating transistors 34 are connected to the emitters of the first transistors 33 and the emitters of the second transistors 34 are connected to ground.

The base electrodes of the first group of gating transistors 33 are connected to the three line output 17 (10 line in the actual circuit) of the first decade decoder logic circuit 15, whereas the base electrodes of the second transistors 34 are connected to the three line output 18 (10 line in the actual circuit) of the second decade decoder logic circuit 16. The first one 35 of the three line output 17 of the first decade decoder 15 is ganged to the base electrode of every third first gating transistor 33 by means of a ganging bus 36. Similarly, the second output 37 of the first decade decoder 15 is connected to the base electrode of every third first gating transistor 33, starting with the second transistor in the array, via a second ganging bus 38 and the third one 39 of the three line outputs of the first decade decoder 15 is fed to the base of every third gating transistor 33, starting from the third transistor, by means of a ganging bus 41.

When the first electrode 21' of the array 21 is to be energized, the first one 35 of the three line outputs of the first decade decoder 15 is energized which energizes the base electrode of every third one of the gating transistors 33, starting with the first transistor 33' of the array. The output 18 of the second decade decoder logic circuit 16 includes first, second and third line outputs 51, 52 and 53, respectively. To cause the first electrode 21' to write, the first decade output line 51 is energized, whereas 52 and 53 are not, causing the first one of the second gating transistors 34' to be energized, thus, dropping the potential through open gates 33' and 34' connected to the first electrode 21' to ground potential to produce depositing of a charge image on the recording web 22.

The advantage of the arrangement of combined decoder matrix and high voltage series connected gating transistors 33 and 34 is that it permits the gating transistors 33 and 34 to form a portion of the decoder matrix, thereby simplifying and reducing the number of decoding elements required. In addition, it avoids the problems associated with employing a segmented writing electrode 29 as a part of the decoder matrix. A further advantage is that a series connection of the two high voltage transistors 33 and 34 serves to reduce the voltage drop across each one of the transistors, thereby improving the reliability and life.

Since many changes could be made in the above construction and many apparently widely different embodiments of this invention could be made without departing from the scope thereof, it is intended that all matter contained in the above description or shown in the accompanying drawings shall be interpreted as illustrative and not in a limiting sense.

What is claimed is:

1. In an electrographic recorder for providing an image on a recording medium in response to input signals in n digit input channels, the combination comprising:
 - n digit decoder means of the 1-out-of- $N_1, N_2 \dots N_n$ type respectively and having $N_1, N_2 \dots N_n$ outputs respectively, each decoder means being responsive to the input signals in one of the n digit input channels for providing n output signals (one output signal from each of the n digit decoder means) corresponding to the respective n digits of input signal;
 - a one-out-of- M decoding matrix having M output terminals where M is the product of $N_1, N_2 \dots N_n$, the decoding matrix being responsive to the outputs of the n digit decoder means for providing a single output at a single one of the M output terminals;
 - M writing electrodes proximate the recording medium, each electrode being responsive to one of the M output terminals of the decoding matrix;
 - a conductive means proximate the writing electrodes and the recording medium;
 - means for establishing a standby potential insufficient to write between the M writing electrodes and the conductive means;
 - means for establishing an additional potential across the decoding matrix and the writing electrodes which when combined with the standby potential is sufficient to cause writing; and
 - n gating switch groups within the decoding matrix, each gating switch group being responsive to the output of one of the n digit decoder means, one particular gating switch group having M gating switches one connected to each of the M output terminals of the decoding matrix and to the associated writing electrode, the gating switches of each group connected in series electrically with the appropriate gating switches of the other groups to form M AND circuits which permit the outputs of the n digit decoder

- means in concert to activate a single writing electrode by controlling the application of the additional potential to the electrodes, the series electrical connection of the n gating switches forming each AND circuit causing the additional potential applied across the M AND circuits to be divided among n gating switches forming each AND circuit.
2. The electrographic recorder of claim 1, wherein $N_1=N_2=\dots=N_n=10$.
 3. The electrographic recorder of claim 2 where $n=2$ and $M=100$.
 4. The electrographic recorder of claim 1 wherein the additional potential is greater than 200 volts and the gating switches are transistors.
 5. The electrographic recorder of claim 1, wherein a converter means is provided between the n digit decoder means and digit channels of input signals, the converter means having n output digit channels for accommodating n digits of the numbering system to the base $N_1, N_2 \dots N_n$ respectively binary coded (one binary coded digit in each output channel) and responsive to the input signals for providing the n digits of output representative of the input signals.

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