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(71) Applicant (for all designated States except US): **PICO-DRILL SA** [CH/CH]; Avenue des Boveresses 46B, CH-1010 Lausanne (CH).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **SCHMIDT, Christian** [DE/CH]; Chemin des Batailleres, CH-1897 Le Bouveret (CH). **DITTMANN, Leander** [DE/CH]; Place du Vallon 18, CH-1005 Lausanne (CH). **STURA, Enrico** [IT/CH]; Route de la Petite Corniche 12, CH-1091 Grandvaux (CH).

(74) Agents: **ENGELHARD, Markus** et al.; Boehmert & Boehmert, Hollerallee 32, 28209 Bremen (DE).

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(54) Title: A METHOD OF INTRODUCING A STRUCTURE IN A SUBSTRATE

(57) Abstract: This invention relates to methods for the production of micro-structured substrates and their application in natural sciences and technology, in particular in semiconductor, microfluidic and analysis devices. It concerns a method of introducing a structure, such as a hole or cavity or channel or well or recess or a structural change by providing a controlled electrical discharge.

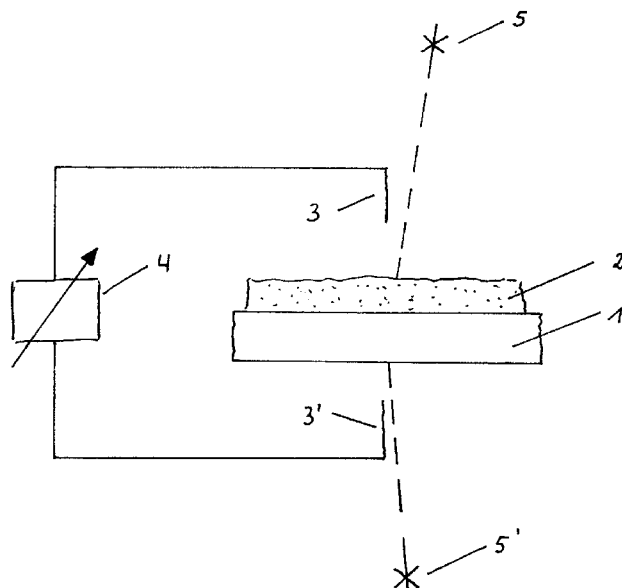


Figure 1



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A method of introducing a structure in a substrate

Field of the Invention

This invention relates to methods for the production of micro-structured substrates and their application in natural sciences and technology, in particular in semiconductor, microfluidic and analysis devices.

Background of the Invention

Many microtechnological applications and devices require high aspect ratio structures such as holes. One eminent example is Through-hole silicon *via* (TSV) used as interconnect in and between silicon chips. The making of high aspect ratio holes (harh) is in many cases difficult, expensive or even impossible. Limits of current hole making technologies such as laser ablation or etching are the minimum hole size, the aspect ratio and the roughness of the inner hole linings/walls. These limits currently pose a serious bottleneck to the large scale application of stacked silicon chips. The devices and methods described here provide a simple, inexpensive and precise approach to circumvent these limitations.

A further problem of current micromachining technologies is the specificity to selected materials. For instance, anisotropic etching of Si using KOH solutions is a simple way to produce grooves and holes in silicon but does not work with many other semiconductors or amorphous materials. Even with Si it functions only for specific crystal lattice orientations. It was therefore a goal of the here disclosed invention to provide a method that allows the machining of many different materials, most of them relevant to current microtechnology such as Si, Ge, GaAs, InP, Sapphire, glass, zirconia. Modifications to the method to machine different materials or even material classes were sought to be minor and easily implantable.

A further goal of the disclosed invention was the applicability of the method to the fabrication of arrays of holes. WO2005/097439 and PCT/EP2008/009419 disclose methods of generating structures in substrates using the application of voltages to a substrate. The methods disclosed therein do not allow a close spacing of holes due to the high voltages applied and the occurrence of voltage-flash-overs through already existing holes. Accordingly there is a need for methods and devices to prevent these detrimental effects for array formation.

Also, many miniaturized fluidic and chemical/biological analysis devices require small reservoirs and connection channels. The dimensions of these channels and containers are often in the micrometer range. Common micromachining techniques, developed mostly for planar structures, fall short of making wells and channels which enter deep into the chip/substrate. That is, the achievable aspect ratio – the ratio between the length and the diameter of a hole, is limited to typically 1:10. This is in particular true for the machining of glass and glass like materials such as fused silica. Significant drawbacks for large scale application derive also from the high production cost.

On the other hand, channels with very high aspect ratio allow for efficient electro-osmotic pumping of fluids through these channels, requiring e.g. for channels of 150 μm length and 2 μm diameter only small voltages and currents (e.g. 5 V) for significant fluid velocities within the channel. Very high aspect ratios will also allow to connect both sides of a typical glass chip of e.g. 0.5 mm thickness by trans-chip channels, thereby enabling simple three-dimensional fluid designs.

Channels with picoliter capacities will also provide a basis for picoliter fluidics, utilizing fluid transport and mixing effects irrelevant in larger volumes.

Accordingly it was an object of the present invention to provide for a method allowing the production of high quality perforated substrates. It was also an object of the present invention to provide for a method of production of such high quality membrane carriers which method is easy to perform and reproducible. It was furthermore an object to provide for a method allowing the controlled production of holes, cavities or channels in substrates, wherein the geometrical features of the holes, cavities and channels can be easily controlled and influenced. It was also an object of the present invention to provide for a method allowing the mass production of perforated substrates. It was furthermore an object of the present invention to provide a method of hole production that can be applied to substrates that were hitherto difficult to process, such as glass, sapphire or elemental silicon.

Summary of the invention

The objects of the present invention are solved by a method of introducing a structure, such as a hole or cavity or channel or well or recess, or a structural change, such as a transition from a crystalline structure to an amorphous structure, in a substrate or a region thereof, said method comprising the steps:

- a) providing a substrate which is electrically insulating or semiconducting at room temperature, and placing it between at least two electrodes connected to a user-controlled voltage supply,
- b) applying, by means of said user-controlled voltage supply, a voltage of user-defined magnitude across a region of said substrate, said voltage being sufficient to give rise to an increase in electrical current through said substrate or said region, thereby applying a defined amount of electrical energy to said substrate,
- c) optionally, applying additional energy, preferably heat, to said substrate or said region so as to increase the temperature and the electrical conductivity of said substrate or said region so as to initiate the current flow in step b), said additional energy, preferably heat, originating either from an additional energy or heat source or from components of said voltage applied in step b),
- d) dissipating said electrical energy applied in step b) in said substrate,

wherein step d) is controlled solely by (i) the user-defined magnitude of the applied voltage of step b), (ii) a user-defined period of time of step b), (iii) an impedance of said voltage supply, or (iv) any combination of (i) – (iii).

In one embodiment, said control of step d) by controlling (i), (ii), (iii) or (iv) is achieved using a programmed or feedback circuit analysing the trans-substrate current or trans-substrate voltage over time.

In one embodiment, said control of step d) by controlling (i), (ii), (iii) or (iv) is achieved by solely user-defining (i), (ii), (iii) or (iv) and without using a programmed or feedback circuit analysing the trans-substrate current or trans-substrate voltage over time.

In one embodiment, said user-defined magnitude of voltage is in the range of 10 V to 10^6 V,

preferably from 10^2 V to 3×10^5 V, more preferably from 10^3 V to 30×10^3 V, and most preferably from 2×10^3 V to 15×10^3 V.

In one embodiment, said user defined period of time is in the range of from 1 ms to 5000 ms, preferably from 10 ms to 2000 ms, more preferably from 10 ms to 1000 ms, and even more preferably from 10 ms to 500 ms.

In one embodiment, said impedance of said voltage supply is an impedance > 1 Ohm, preferably > 10 kOhm, more preferably > 100 k Ohm, and, even more preferably > 1 MOhm.

In one embodiment, said impedance is in the range from 1 Ohm to 1 GOhm, wherein, preferably, said impedance is variable within said range during performance of said method.

In one embodiment, said electrically insulating or semiconducting substrate is made of a material selected from a group comprising carbon-based polymers, such as polypropylene, fluoropolymers, such as Teflon, silicon-based substrates, such as glass, quartz, silicon nitride, silicon oxide, silicon based polymers such as Sylgard, semiconducting materials such as elemental silicon, including doped silicon and crystalline silicon, germanium, compound semiconductors, such as gallium arsenide, indium phosphide, as well as aluminium based crystalline materials such as alumina, spinel, sapphire, as well as ceramics such as zirconia.

In one embodiment, step d) is initiated by either (i) applying a voltage of user-defined magnitude across a region of said substrate in step b), said user defined magnitude of voltage being sufficient to give rise to an increase in electrical current through said substrate or said region and a subsequent dissipation of said electrical energy in said substrate, (ii) applying a voltage of user-defined magnitude across a region of said substrate in step b), said user defined magnitude of voltage not being sufficient to give rise to an increase in electrical current through said substrate or said region and to a subsequent dissipation of said electrical energy in said substrate, and reducing the distance between each of the electrodes and the substrate and, optionally, contacting said substrate with said electrodes, (iii) performing step c), or (iv) a combination of (i) – (iii).

In one embodiment, step c) is omitted, wherein, preferably, said substrate is a substrate having an electrical resistivity $\leq 10^9 \Omega$ cm at room temperature.

In one embodiment, said substrate is electrically semiconducting at room temperature and is preferably made of a semiconducting material selected from elemental silicon, including doped silicon and crystalline silicon, germanium, compound semiconductors such as gallium arsenide, and indium phosphide.

In another embodiment, step c) is performed, wherein, preferably, step c) is performed using an additional energy source which is selected from a heated electrode, a heating element, a laser, a focussed light source, a UV light source, a gas flame, and a high frequency electromagnetic field device. Such a high frequency electromagnetic field device is, for example, a Tesla transformer.

In one embodiment, said additional energy source is a laser which preferably has a wavelength in a wavelength range that is at least partially absorbed by said substrate.

In one embodiment, the site of application of additional energy in step c) determines the region of said substrate in which said structure or said structural change is introduced.

In one embodiment, said substrate which is electrically insulating at room temperature or electrically semiconducting at room temperature is provided in step a) having at least one electrically insulating layer attached, wherein, preferably, said electrically insulating layer is solid, liquid or gaseous at room temperature.

Such insulating layer preferably has a thickness in the range of from 1 μm to 1 cm, more preferably from 10 μm to 1 mm.

In one embodiment, said electrically insulating layer is gaseous at room temperature and is not air.

In one embodiment, said electrically insulating layer has an insulating region which is adjacent to and in contact with said substrate region in which substrate region a structure or structural change is to be introduced, and is preferably effectively reducing the voltage across the substrate (shielding effect) without lowering the voltage between the electrodes, and wherein step c) is performed such that in said electrically insulating layer the electrical

conductivity is raised in said insulating region so as to reduce its voltage shielding effect and augmenting the trans-substrate voltage in said substrate region.

In one embodiment, said electrically insulating layer has an insulating region which is adjacent to and in contact with said substrate region in which substrate region a structure or structural change is to be introduced, wherein step c) is performed such that said electrically insulating layer, if provided as a solid in step a), is liquefied in said insulating region, or is performed such that said electrically insulating layer, if provided as a liquid in step a), is partially evaporated in said insulating region, and wherein during step d), said electrically insulating layer is partially displaced in said insulating region, through the dissipation of said electrical energy, and wherein, after step d), said gaseous, liquefied or partially evaporated electrically insulating layer flows into said generated structure and thereby closes and at least partially fills said structure.

In one embodiment, said electrically insulating layer is attached to said substrate in such a manner that it covers said substrate in step a) or is covered by said substrate in step a), and said substrate region lies opposite said insulating region.

In one embodiment, the insulating layer reduces the voltage across the substrate by formation of an internal counter electric field due to electrical polarization of the insulating layer material.

In one embodiment, the insulating layer is also used to improve the flatness/surface quality of the region surrounding the structure being introduced by absorbing material ejected during the process into the insulating layer and thus avoiding its direct redeposition onto the substrate surface. In one embodiment, the absorbed material is removed together with the insulation layer after the structure has been introduced.

In one embodiment, the insulating layer is used to create a mask on said substrate which mask exposes only the region(s) where the structure(s) will be introduced, protecting the rest of the substrate from unwanted dissipation of electric energy.

In one embodiment, the insulating layer is removed after a structure or an array of structures or a structural change or several structural changes have been introduced into the substrate.

In one embodiment, step c) is performed by directly heating the insulating layer such as through absorption of laser radiation of a wavelength absorbed by the insulating layer.

In one embodiment, step c) is performed by indirectly heating the insulating layer by heating the attached substrate and utilizing heat transfer from the heated substrate to the attached insulating layer.

In one embodiment, said electrically insulating layer is made of a material which is solid and electrically insulating at room temperature and preferably selected from wax, in particular paraffin wax, rubber, hot melt adhesive, poly(styrene-butadiene-styrene), and polyurethane.

In one embodiment, said electrically insulating layer is made of a material which is liquid at room temperature, and which is electrically insulating at room temperature or polar or both and is preferably selected from dodecane, paraffin, water, or high viscosity water based liquids such as Ficoll™ solution or honey like liquids.

In one embodiment, said electrically insulating layer is made of a material which is gaseous at room temperature and is preferably selected from SF₆, Ar, N₂, CO₂.

In one embodiment, said substrate is electrically insulating at room temperature and is preferably made of a substrate material selected from glass, quartz, diamond, alumina, sapphire, aluminium nitride, zirconia, and spinel, more preferably quartz and glass, wherein, preferably, said substrate has an electrical resistivity $> 10^9$ Ohm cm at room temperature.

In one embodiment, said electrically insulating layer, if present, is made of a material which is solid and electrically insulating at room temperature and is preferably selected from paraffin wax, rubber and hot-melt adhesive.

In one embodiment, step c) is performed using a laser, preferably having a wavelength in a wavelength range which is at least partially absorbed by said substrate material and/or said insulating layer, if present.

In one embodiment, said substrate is electrically semiconducting at room temperature and is preferably made of a substrate material selected from elemental silicon, including doped

silicon and crystalline silicon, germanium, compound semiconductors such as gallium arsenide and indium phosphide.

Preferably, said substrate has an electrical resistivity $\leq 10^9$ Ohm cm at room temperature.

In one embodiment, said electrically insulating layer, if present, is made of a material which is liquid and electrically insulating at room temperature, or polar or both and which is preferably selected from dodecane, paraffin, water, honey, or is made of a material which is solid and electrically insulating at room temperature and which is preferably selected from paraffin wax and hot-melt adhesive.

In one embodiment, step c) is performed using a laser, preferably having a wavelength in a wavelength range which is at least partially absorbed by said substrate material and/or said insulating layer, if present.

In one embodiment, step c) is performed such that heating of the insulating layer necessary for a electric field reduction across this layer necessary to initiate step b) and d) is leading to a significant increase in temperature of the substrate leading to a significant change of its temperature dependent mechanical parameters such as hardness and brittleness.

In one embodiment, steps a) – d) are performed once, such that a first structure is generated in the first substrate region, thereafter the substrate is moved by a defined distance, and steps b) – d) are performed a second time such that a second structure is generated in a second substrate region, wherein, preferably, steps b) – d) are performed n times, such that an array of n structures is generated in said substrate, n being an integer > 1 .

In one embodiment, said electrical energy applied in step b) is sufficient to generate a through hole or through channel in said substrate in performing step d).

In another embodiment, said electrical energy applied in step b) is not sufficient to generate a through hole or through channel in said substrate in performing step d) and is sufficient to change the structure in said substrate region, wherein, preferably, step d) changes the structure in said substrate region by heating and/or melting the material present in said substrate region, and wherein such change in structure makes said substrate region more amenable to treatment

by an ablating step e) in which said substrate including said substrate region is exposed to an ablating environment such as an etching agent.

In one embodiment, said electrical energy is not sufficient to cause an ejection of material from said substrate region.

In one embodiment, the method according to the present invention further comprises step

e) exposing said substrate including said substrate region to an ablating environment, such as an etching agent.

If, in the embodiment where step d) changes the structure in said substrate region by heating and/or melting the material present in said substrate region, an insulating layer is present on said substrate, such insulating layer is preferably removed after the structure in said substrate has been changed.

In one embodiment, said substrate is electrically semiconducting at room temperature and is preferably made of a semiconducting material selected from elemental silicon, including doped silicon and crystalline silicon, germanium, compound semiconductors such as gallium arsenide, and indium phosphide.

In one embodiment, said ablating environment is an etching agent and preferably is an etching agent selective for semiconducting materials, and is more preferably selected from KOH, SF₆, tetramethylammonium hydroxide (TMAH), ethylenediamine pyrocatechol (EDP), hydrazine, and HF.

In one embodiment, said ablating environment is created by a reactive ion etching process.

In one embodiment, said ablating environment is SF₆ used for etching.

In one embodiment, steps b) and d) are performed a number of times n, n being an integer > 1, thereby applying electrical energy to a first, second, third, ... n-th region of said substrate, and thereby changing the structure in said first, second, third, ... n-th region of said substrate.

In one embodiment, the method according to the present invention further comprises step e),

wherein step e) is performed once after steps b) and d) have been performed a number of times n, thereby generating an array of n structures in said substrate.

In one embodiment, said substrate is elemental silicon and said etching agent is selected from KOH, TMAH, SF₆.

In one embodiment, a crystalline substrate is chosen having crystal orientation reducing the etch rate parallel to the substrate surface compared to differently oriented substrates.

In one embodiment, a crystalline substrate is chosen having crystal orientation reducing the etch rate perpendicular to the substrate surface compared to differently oriented substrates, such as a <111> silicon wafer in KOH.

In one embodiment, the substrate is coated with a protective layer not or less etched by an etching agent than the substrate itself and which during performing step a)-d) is fully or partially removed or structurally altered so as to allow etching only at the region(s) where step d) has been performed.

In one embodiment, the method according to the present invention uses the insulating layer, as defined above, as protective layer.

The objects of the present invention are also solved by a structure or an array of structures, preferably holes or cavities or channel or wells or recesses, in a substrate, produced by the method according to the present invention.

In a first aspect the present invention relates to a method of introducing a structure or structural change, preferably a hole or cavity or channel or well or recess physically or only defined by structural change such as a transition from a crystalline to an amorphous microstructure, in a substrate located between (at least) two electrodes which are connected to a controlled voltage supply. Energy provided by the voltage source which is fully or in part locally dissipated within the substrate controlled through the voltage magnitude and/or source impedance and the time over which the voltage is applied. In general the voltage can be a function of application time V(t), which changes due to changes of the electric circuit during application and/or a programmed and/or feedback circuit analysing the substrate current

and/or voltage. During voltage application the energy dissipation inside the substrate is controlled so as to achieve local changes in the physico-chemical properties of the substrate such as the transformation of crystalline regions into amorphous regions by raising T in the dissipation region up to the respective melting or transition T. The process may be explicitly stopped before any topological changes such as the formation of holes take place. To initiate the dissipation process in the first place it may be necessary to supply auxiliary heat to the modification region so as to locally increase the temperature and therefore conductivity of the region as already disclosed and outlined in WO2005/097439 and PCT/EP2008/009419. However, the placement of the auxiliary heat allows to define the region which will be modified.

For the application of voltages to substrates in general, the nature and dimensions of substrates and structures, reference is made to WO2005/097439 and PCT/EP2008/009419, which are hereby incorporated in their entirety by reference thereto.

For certain substrates, e.g. such having a high conductivity or such having already holes which cause the applied voltage to short-cut, the substrate (1) is attached to one or two insulating layers (2) (Figure 1). These layers effectively shield the applied voltage (electrodes 3, 3', voltage supply 4, laser 5 or 5', in figure 1) from the substrate, e.g. by having a very high resistivity or by the induction of a counter field within them (as is the case when using polar substances such as water). In other words, part or in some cases most of the voltage applied via the electrodes creates an electric field across the insulating layer thereby reducing the electric field inside the substrate, which can effectively lead to a dramatic reduction of field inside the substrate for a constant voltage across the electrodes, thereby preventing discharges at voltages which would otherwise initiate an electric break-down within the substrate. To initiate the energy dissipation within the substrate the insulating layer has to be raised in conductivity or removed at the site where the attached substrate is to be modified. This can be done upon irradiation (e.g. UV) or heating of this site using e.g. a laser, or by means of a high frequency electromagnetic field causing dissipation in the substrate. After modification of the substrate (see also figure 2), which may involve the formation of holes as e.g. described in WO 2005/097439 or PCT/EP2008/009419, or the local change (6) of the physico-chemical properties as described before, the insulating layer, which has been opened and melted and/or evaporated in parts (7), may be closed again (7) to proceed with the modification of additional regions within the substrate (Figure 2). Using e.g. fluid or gel like insulating layers such as pure water or hydrocarbons (wax, dodecane, paraffin,...) the insulating layer may close by

itself (7) e.g. due to surface tension or substrate adhesion. Solid layers may be closed using heat induced reflux which may be initiated with application of the auxiliary heat, the energy dissipation process itself or by a subsequent heating step after modification. Such layers, with a thickness in the range of 1 μm to 1 cm, preferably from 10 μm to 1mm, may be used to avoid the deposition of the material extracted from the substrate over the surface surrounding the structure, absorbing the expelled material and preventing its adhesion to the substrate (see Figure 10). The combination and repetition of the described steps allows for multiple such substrate structure changes in close spatial proximity to each other e.g. organized in form of an array. To increase the precision in the spatial displacement of such structures, the insulating layer may be used to create a mask, e. g. by mechanical ablation or by laser evaporation/decomposition of portions of insulating material. This will expose only selected regions of the substrate where the structure will be introduced, defining with increased precision the position of such structures on the substrate (Figure 11). Using e.g. a solid wax layer such a mask may be created by piercing or punching the layer at positions where structures are to be introduced, e.g. by means of a needle, which may be the electrode itself, discovering a region of the substrate of diameter in the range of 10 nm to 1mm, more preferably 1 μm to 100 μm . At these positions the wax is partially or totally removed defining the position for the dissipation of electrical energy during step d).

In a further device and method according to the present invention the forgoing methods and devices are used to introduce structural changes within the substrate that modify the physico-chemical properties at the dissipation site(s) in such a way that exposure of the substrate to ablative environments such as an etching solution or reactive ion plasma (RIE) leads to a differential material ablation in the modified and unmodified regions. If the modified region is attacked more strongly hole and well like structures will result, in the opposite case columns of modified regions will stick out of the ablated substrate. The etching step may also be performed to modify structures produced according to WO 2005/097439 and PCT/EP2008/009419 as the heated and expelled material has for certain materials new physico-chemical properties that allow e.g. the ablation of redeposited material or the increase of the produced hole(diameter). An example are holes produced in Si wafers as described and subsequently exposed to a warm solution of 50% KOH (e.g. at 80°C). It should be noted that the term "elemental silicon" or "silicon" includes crystalline (monocrystalline or polycrystalline) silicon such as is used in silicon wafers. The term also includes doped silicon.

To protect the non-modified substrate better during the etching step, effectively allowing to immerse the entire wafer or one side of the wafer to the etching agent, the substrate may be covered with a protective layer. This usually thin layer (typically $<10\text{ }\mu\text{m}$) is removed or altered at the modification region(s) providing only there access of the etching agent to the substrate. An example is a Si_3N_4 layer of typically $<1\text{ }\mu\text{m}$ thickness on an Si wafer. Using subsequently KOH based etching media the Si wafer is not etched due to the nitride layer – except where energy was dissipated.

In order to achieve optimal etching results, such as a reduced etch rate perpendicular the axis of the formed structure or a reduced/increased etch rate perpendicular to the substrate surface the crystal lattice orientation of the substrate may be selected accordingly (where applicable). An example is the usage of $\langle 111 \rangle$ Si wafer treated with KOH solution to reduce the etch rate perpendicular to the wafer surface thereby further increasing the etch rate differences between modified and unmodified regions.

The combination of ablation and micro-structural substrate changes in the formation of holes has, because internal pressure during such step is smaller compared to a step where material is actively expelled from the forming structure, the advantage that breakages or deformation of crevices are less likely to occur. Moreover, subsequent polishing steps which might otherwise have been necessary can be avoided because the conditions applied to the substrate are generally gentle enough and no depositions of substrate material on the substrate surface occur.

According to the present invention, the inventors have established devices and methods to apply electrical energy to a substrate which electrical energy is not sufficient to cause the formation of a through hole or through channel in the substrate but which makes the structure of the region in which the electrical energy is applied, more amenable to a subsequent etching step. In accordance with embodiments of the present invention, the substrate is placed between two electrodes connected to a voltage supply capable of causing an electrical discharge through the substrate upon (1) increase of the field strength between the electrodes by e.g. increase in voltage (typically $1000 - 300\,000\text{ V}$), (2) closing of the electrode distance or (3) local heating of the substrate or (4) local heating of an insulating layer attached to the substrate. The discharge and therefore the voltage supply is controlled so as to provide an electrical power $P(t)$ over a time interval Dt . The interplay between power and time thereby

determines the T-profile building up inside the substrate. Without wishing to be bound by any theory the present inventors believe that this method, in significantly heating the substrate in a defined substrate region, changes the structure of said region. Again, without wishing to be bound by any theory, the present inventors believe that a less ordered structure is generated by such heating procedure. For example, in substrates which are crystalline such as wafers used for chip manufacturing, the method is believed to lead to an amorphous structure upon raising the temperature locally to or close to the melting point. The region in which said electrical energy has been applied, therefore becomes more amenable to etching, and subsequently gets etched selectively upon application of an etching agent. An example is the process applied to silicon in <100> orientation with >10 Ohm cm conductivity and 0.25 mm thickness, electrode spacing between substrate and electrode 0.5 mm each, $V = 2000V$, C ca 1 nF and $Dt < 100$ msec produces holes of ca 30 – 100 μm in diameter upon etching with 50% KOH solution at 80°C. In preferred embodiments of this aspect according to the present invention, the step b) and d) in which electrical voltage is applied to a region of a substrate and consequently electrical energy locally dissipated, is repeated n -times, n being an integer > 1 , and thereafter the etching step is performed, thus leading to the generation of n structures in the substrate. This aspect according to the present invention is particularly suitable for the formation of arrays of structures in electrically semiconducting substrates and application for TSV (Through-hole silicon *via*).

In embodiments according to the present invention, the inventors have also introduced an insulating layer in methods of generating structures in substrates using electrical energy. The step is important for rather conducting substrate materials such as semiconductors as well as arrays of holes in all substrates where in the first case the entire wafer and in the second the pre-existing holes have to be shielded from the applied voltage thus that only the part of the substrate to be modified is exposed to the electrical field so as to define accordingly this region as the discharge place (Figure 3). The insulating layer may consist of gaseous, such as SF₆, liquid such as paraffin and water as well as solid materials such as wax. The layer must shield sufficiently from the applied voltage so as to avoid discharges without further invention. This may occur purely through insulating, that is properties of high resistivity of the insulating layer as well as shielding properties where the applied voltage induces a counterfield within the insulating layer, which is usually the case in polar materials such as water. The actual discharge process, that is the dissipation of energy within the substrate is

initiated upon local raise in conductivity of the insulating layer, e.g. by heating a defined region which lies opposite and adjacent to the region of the substrate, in which the structure is to be generated. Such defined region in the insulating layer, herein also sometimes referred to as an “insulating region”, allows after the change in resistivity or change in the dielectric properties such as the dielectric constant, that a current starts flowing through it and consequently through the adjacent region of the substrate, thereby effectively determining the region of the substrate where energy is dissipated. In preferred embodiments, such insulating region becomes liquid or melts and can be subsequently fully or in part evaporated when the generation of the structure through application and subsequent dissipation of electrical energy to the substrate occurs. However, since the insulating layer typically is still liquid or molten around said region, it may reflow into the generated structure and thereby closes and/or at least partially fills it. In one embodiment after performing step d), there may be a further step f) in which additional energy, preferably heat, is applied to said insulating region, so as to melt or liquefy said insulating layer again or to keep the insulating layer liquid or molten. Preferred means of applying additional energy, either in step c) or step f) are selected from a heated electrode, a heating element, a laser, a focussed light source a gas torch or a high frequency electromagnetic field source, dissipating energy in the material. An example of a high frequency electromagnetic source is a Tesla transformer which can be used in accordance with the present invention. In preferred embodiments, the means for heating is a laser. The laser can heat the insulating layer directly (beam is directly absorbed) or indirectly (the beam is absorbed by substrate and heat is transferred to the insulating layer by heat conduction), or a combination wherein both layers absorb partially. The selection of a specific laser depends on the substrate and insulation material. Examples are CO₂-laser having a wavelength of 10.6 μm . Other preferred lasers are lasers having a wavelength in the range of from 800 nm to 1300 nm. It should be noted that the laser wavelength is also chosen such that it is absorbed by the insulating layer and heats it, and/or it is absorbed by the substrate which heats the insulating layer. This allows a heating of the insulating layer. Absorption may be 100 % or less, i.e. substantially all or fractions of the incident radiation is absorbed by the substrate or the insulating layer or both. As used herein, the term “is at least partially absorbed” is meant to refer to any scenario wherein the substrate and/or the insulating layer absorbs 0.1 % to 100 % of the incident radiation. As used herein, the term “insulating layer” refers to a layer that is attached to the substrate, preferably in a side-by-side-manner, such that the insulating layer and the substrate are adjacent and opposite to each other. In this arrangement the region, in which a structure is to be generated in the substrate is also

sometimes referred to as a “substrate region”, and the corresponding region in the insulating layer lying opposite such substrate region, is also referred to as “insulating region”. Effectively, such insulating region lies on top of or underneath said substrate region. In one embodiment, the insulating region and the substrate region are of the same size. In another embodiment, the insulating region is 5% or more, such as 10%, 15%, 20%, 25%, 30%, ..., 100%, 200%, 300%, 400%, ... 1.000%, 2.000%, 3.000%, ..., 10.000% or more larger in area than the substrate region.

The use of an insulating layer in the aforementioned sense in a method of generating a structure has several advantages: It avoids short circuits occurring if several structures are generated in the substrate, because once a structure, such as a hole, is formed, it is subsequently closed and therefore unavailable as a potential by-path for electrical energy to be dissipated when subsequent structures are to be generated. Moreover, the insulating layer also provides structural support to the substrate and stabilizes it. In some embodiments there may be more than one insulating layer, for example one insulating layer on either side of the substrate. Furthermore, the use of an insulating layer allows the production of several structures in a substrate next to each other, such that an array of structures in a substrate is formed. The method according to the present invention is therefore amenable to mass-production and also allows the formation of structures which are close to each other. For example, in a substrate made of an electrically semiconducting material, such as silicon wafers of >100 Ohm cm and < 0.5 mm thickness, the structures of e.g. 30 μm diameter formed therein using a insulating layer in accordance with the present invention, may be as close to each other as 60 μm .

For certain substrate materials, in particular low conducting materials such as glass, the insulating layers and the substrate may have to be heated to initiate the energy dissipation process. Therefore, the method/device described for microstructural changes as well as the method/devices disclosed in WO2005/097439 and PCT/EP2008/009419 may be combined with it so as to not only heat the insulating layer but effectively raising the temperature of the underlying substrate region to initiate the energy dissipation step. This becomes of importance when producing arrays in insulating materials where the insulating layer shields pre-existing holes and the heating is necessary to not only make the insulating layer more conductive but also the substrate in order to initiate the discharge process. However, pre-heating of the substrate prior to the actual energy dissipation process in step d) taking place may also be

employed to change mechanical substrate parameters such hardness and brittleness and thus to reduce or avoid the formation of cracks within the substrate. Finding an optimum for this pre-heating requires a certain ratio between heat absorption of the substrate and the insulating layer. Typically, this ratio is controlled and can be determined by choosing the wavelength of the initiation laser in step d) and the substrate side from which heat is applied.

In accordance with the control of the energy dissipation aspect of the present invention, the inventors have surprisingly found that it is possible to generate structures, preferably holes or cavities or channels or recesses in a substrate using electrical energy which is applied to the substrate, wherein the amount of energy is solely defined by the voltage applied across the electrodes and the time over which such voltage is applied. Other parameters to control and features to control them are no longer necessary. In previous patent applications, the overall amount of energy that is applied to the substrate had been limited by an appropriate capacitor, or the rate of dissipation of the energy stored across the substrate had been controlled by an ohmic resistor. In the present aspect of the method according to the present invention, these features are no longer necessary, and the amount of electrical energy applied can be defined only by the defined duration of step b) and the defined voltage applied in step b). This makes the process very versatile and very easy to perform. It is particularly suitable for semiconducting substrates such as standard silicon wafers, wherein preferred voltage ranges are from 100 V to 10^5 V, more preferably 1.000 V to 15.000 V, and preferred durations of step b) are 10 ms to 2 s, preferably 50 ms to 500 ms. Furthermore, especially with semiconducting substrates, it is no longer necessary to use additional energy, such as heat to be applied, in order to generate the structure (Figure 4). According to this aspect, the method according to the present invention can be performed without a source of additional energy, such as heat, for example a laser, and the amount of electrical energy is solely determined by the applied voltage and the duration of step b), which parameters come to lie in the ranges of 100 V – 100.000 V, preferably 1.000 V to 15.000 V, and 10 ms to 2 s, preferably 50 ms to 500 ms. The size of the structure generated is only dependent on these two parameters. Accordingly, the use of an additional energy source, such as a laser in these embodiments is no longer necessary.

In yet a further aspect according to the present invention, the present invention relates to individual structures in substrates, such as holes, cavities, channels etc. in substrates, as well

as arrays of such structures in substrates, produced by any of the aforementioned methods according to the various aspects.

Using the method according to the present invention, structures and arrays of structures may be formed having dimensions in the μm range or even below.

More specifically, using the method and the device according to the present invention, the controlled formation of holes $0.1 - 10 \mu\text{m}$ in diameter with aspect ratios ≤ 330 and arranged in arrays has been achieved in amorphous dielectrics, such as glass and fused silica, by fast resistive heating. A strongly focussed hyper-exponential temperature increase inside the dielectric led to fast material melting and evaporation. Time intervals between melting and evaporation were estimated $\sim 10^{-11}$ s with power densities reaching $100 \text{ W}/\mu\text{m}^3$. The hole size was a function of the substrate conductivity $\sigma(T)$ and the applied voltage $U(t)$ and characterized by a high reproducibility. The exemplary application of large aspect ratio holes in electroosmotic pumps and low noise ion channel measurements was demonstrated.

In the following reference is made to the examples and figures which show the following:

Examples

Figure 1 depicts an embodiment for the formation of holes using an insulating layer. The insulating layer (2) is attached to the substrate (1) and placed between two electrodes (3, 3') connected to a user and optionally process controlled voltage source (4). Upon application of a voltage between the electrodes sufficient for dielectric break-down within the substrate the insulating layer reduces the actual voltage across the substrate below the break-down threshold. Upon further increase of the voltage or optionally heat induced local breakage of the insulating layer using either laser 5 or 5' the energy dissipation step inside the substrate is triggered. The duration (as well as the voltage source properties) determine the extension of the region where energy was dissipated and therefore the temperature profile within this substrate region.

Figure 2 illustrates the substrate (1) – insulating layer (2) compound undergoing modification. In (A) the combination is shown before modification, in (B) energy has been dissipated and the actual modification process has been terminated. The substrate region has been altered (6)

and the insulating layer is opened (7). (C) shows the combination after the insulating layer has resealed. This last step may occur spontaneously (as with liquid insulators such as water or dodecane or with solid insulators that heat up sufficiently to reflow such as paraffin wax) or after local or global re-heating of the substrate. For the latter process a laser used for process initiation may be used (in absence of voltage) to heat the insulator surrounding the modified region.

Figure 3 illustrates the formation of multiple structures in close proximity on a single substrate. After formation of holes (6) in the substrate (1) and resealing (7) of the insulating layer (2) the substrate attached to a moveable support (8) is moved, voltage applied to the electrodes (3, 3') and the dissipation process restarted using a focused laser beam (5). Closing of the pre-existing holes is – depending on the inter-hole distance and voltage magnitude – required to prevent pre-discharges through the already existing holes where e.g. a gas such as air breaks down much quicker than the actual substrate (e.g. glass).

Figure 4 depicts and embodiment for the introduction of structural changes using voltage induced dielectric break-down rather than laser induction. For that electrodes (3, 3') are placed in close proximity to the substrate (1) determining the break-down and energy release position on the wafer. The close substrate-electrode distance also allows for relatively low voltages to start the dissipation process, in particular in semiconductors for which this setup is most suited. The voltage source (4) is programmed to either produce open holes or microstructural changes such as a transformation of a crystalline region into an amorphous region (6). Voltage magnitude and application time determine the extension and the degree of transformation inside the substrate. High voltages for short durations provide regions narrow in diameter while longer application time, and if necessary lower voltages to avoid evaporation, provide larger diameter regions. The newly formed regions (6) may have a higher electrical resistivity than the untransformed substrate thus avoiding short-circuiting and the usage of insulating layers.

Figure 5 shows an array of holes generated in a 150um thick borosilicate glass substrate using an insulating layer of paraffin wax of a thickness <500um on one side. The DC voltage applied was 9kV and was switched off at a trans-substrate current of 300uA. The discharge process was initiated by laser irradiation at a wavelength of 10.6um (CO₂-laser) and a power

of 5W for 20ms using a focal spot of 100µm in diameter. Other insulating layers (see above) are also possible (results not shown).

Figure 6 shows a through-hole generated in a silicon substrate using the method employing a final etching step after introducing a structural change without creating a through-hole, as outlined above. The silicon wafer was 254µm thick with an electrical resistivity of $>100 \Omega \text{ cm}$ (P-Boron doped). A DC voltage of 2kV was applied for 20ms without using an insulating layer and additional heat. The distance between electrode and substrate was approximately 0.4mm on each side. KOH (50%, 80°C) was used as the etching agent, and the square-like appearance of the hole results from the $\langle 100 \rangle$ orientation of the wafer.

Figure 7 shows an array of holes generated in a silicon substrate using a $<1\text{mm}$ thick insulating layer of hot melt adhesive (Pattex PTK6) on one side. The silicon wafer had a thickness of 275µm, an electrical resistivity of $>300 \Omega \text{ cm}$ (P-Boron doped) and $\langle 100 \rangle$ orientation. The DC voltage applied was 7kV for 600ms. Electrode distance was approximately 0.4mm to the substrate and 1mm to the insulating layer. The discharge process was initiated by laser irradiation at a wavelength of 10.6µm (CO₂-laser) and a power of 3.5W for 600ms using a focal spot of 100µm in diameter. Other insulating layers, such as dodecane, etc. (see above) are also possible (results not shown).

Figure 8 shows an enlarged picture of a hole generated in a 254µm thick silicon wafer with an electrical resistivity of $>100 \Omega \text{ cm}$ (P-Boron doped) and $\langle 100 \rangle$ orientation. The hole was created by applying a DC voltage of 3kV for 400ms, without using an insulating layer and additional heat. The distance between electrode and substrate was approximately 0.5mm on each side. The substrate has been subsequently polished.

Figure 9a) shows a hole generated in a 400µm thick substrate of monocrystalline zirconia (ZrO₂) using a voltage of 10kV for 800ms and an irradiation of laser light at a wavelength of 10.6µm (CO₂-laser), power of 10W, focal diameter of 100µm for initiation.

Figure 9b) shows a hole generated in a 300µm thick substrate of polycrystalline zirconia (ZrO₂) using a voltage of 8kV for 500ms and an irradiation of laser light at a wavelength of 10.6µm (CO₂-laser), power of 8W, focal diameter 100µm for initiation. After hole formation the surface was mechanically polished.

Figure 9c) shows a hole generated in a 400um thick substrate of sapphire using a voltage of 10kV for 2000ms and an irradiation of laser light at a wavelength of 10.6um (CO2-laser), power of 22W, focal diameter 100um for initiation.

Figure 9d) shows a hole generated in a 500um thick substrate of indium phosphide with an electrical resistivity of 0.0016 Ohm cm and orientation <100> using an insulating layer of Parafilm M. The applied voltage was 11kV for 200ms. The process was initiated by irradiation of laser light at a wavelength of 1064nm (fiber-laser), power of 20W, focal diameter of approximately 20um.

Figure 9e) shows a hole generated in a 400um thick substrate of gallium arsenide with an electrical resistivity of 0.158 Ohm cm and orientation <111> using an insulating layer of Parafilm M. The applied voltage was 10kV for 200ms. The process was initiated by irradiation of laser light at a wavelength of 1064nm (fiber-laser), power of 20W, focal diameter of approximately 20um.

Figure 10) shows a hole generated in a 250um thick substrate of monocrystalline silicon using a voltage of 3KV for 200ms, using a solid paraffin layer 200 um thick (Paraplast Plus, Fluka) as insulating/protecting layer to avoid the deposition of the extracted material on the substrate.

Figure 11a) shows an array of holes generated in a 250um thick substrate of monocrystalline silicon using 3KV for 200 ms for each hole, using paraffin as insulating/protecting layer.

Figure 11b) shows an array of holes generated using the same parameters of the array in figure 11a) but without any insulating/protecting layer, allowing the extracted material to settle in the area surrounding each hole.

The features of the present invention disclosed in the specification, the claims and/or in the accompanying drawings, may, both separately, and in any combination thereof, be material for realizing the invention in various forms thereof.

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Claims

1. A method of introducing a structure, such as a hole or cavity or channel or well or recess, or a structural change, such as a transition from a crystalline structure to an amorphous structure, in a substrate or a region thereof, said method comprising the steps:

- a) providing a substrate which is electrically insulating or semiconducting at room temperature, and placing it between at least two electrodes connected to a user-controlled voltage supply,
- b) applying, by means of said user-controlled voltage supply, a voltage of user-defined magnitude across a region of said substrate, said voltage being sufficient to give rise to an increase in electrical current through said substrate or said region, thereby applying a defined amount of electrical energy to said substrate,
- c) optionally, applying additional energy, preferably heat, to said substrate or said region so as to increase the temperature and the electrical conductivity of said substrate or said region so as to initiate the current flow in step b), said additional energy, preferably heat, originating either from an additional energy or heat source or from components of said voltage applied in step b),
- d) dissipating said electrical energy applied in step b) in said substrate,

wherein step d) is controlled solely by (i) the user-defined magnitude of the applied voltage of step b), (ii) a user-defined period of time of step b), (iii) an impedance of said voltage supply, or (iv) any combination of (i) – (iii).

2. The method according to claim 1, wherein said control of step d) by controlling (i), (ii), (iii) or (iv) is achieved using a programmed or feedback circuit analysing the trans-substrate current or trans-substrate voltage over time.

3. The method according to claim 1, wherein said control of step d) by controlling (i), (ii), (iii)

or (iv) is achieved by solely user-defining (i), (ii), (iii) or (iv) and without using a programmed or feedback circuit analysing the trans-substrate current or trans-substrate voltage over time.

4. The method according to any of claims 1 – 3, wherein said user-defined magnitude of voltage is in the range of 10 V to 10^6 V, preferably from 10^2 V to 3×10^5 V, more preferably from 10^3 V to 30×10^3 V, and most preferably from 2×10^3 V to 15×10^3 V.

5. The method according to any of claims 1 – 4, wherein said user defined period of time is in the range of from 1 ms to 5000 ms, preferably from 10 ms to 2000 ms, more preferably from 10 ms to 1000 ms, and even more preferably from 10 ms to 500 ms.

6. The method according to any of the foregoing claims, wherein said impedance of said voltage supply is an impedance > 1 Ohm, preferably > 10 kOhm, more preferably > 100 kOhm, and, even more preferably > 1 MOhm.

7. The method according to claim 6, wherein said impedance is in the range from 1 Ohm to 1 GOhm, wherein, preferably, said impedance is variable within said range during performance of said method.

8. The method according to any of the foregoing claims, wherein said electrically insulating or semiconducting substrate is made of a material selected from a group comprising carbon-based polymers, such as polypropylene, fluoropolymers, such as Teflon, silicon-based substrates, such as glass, quartz, silicon nitride, silicon oxide, silicon based polymers such as Sylgard, semiconducting materials such as elemental silicon, including doped silicon and crystalline silicon, germanium, compound semiconductors, such as gallium arsenide, indium phosphide, as well as aluminium based crystalline materials such as alumina, spinel, sapphire, as well as ceramics such as zirconia.

9. The method according to any of the foregoing claims, wherein step d) is initiated by either (i) applying a voltage of user-defined magnitude across a region of said substrate in step b), said user defined magnitude of voltage being sufficient to give rise to an increase in electrical current through said substrate or said region and a subsequent dissipation of said electrical energy in said substrate, (ii) applying a voltage of user-defined magnitude across a region of

said substrate in step b), said user defined magnitude of voltage not being sufficient to give rise to an increase in electrical current through said substrate or said region and to a subsequent dissipation of said electrical energy in said substrate, and reducing the distance between each of the electrodes and the substrate and, optionally, contacting said substrate with said electrodes, (iii) performing step c), or (iv) a combination of (i) – (iii).

10. The method according to any of the foregoing claims, wherein step c) is omitted.

11. The method according to claim 10, wherein said substrate is a substrate having an electrical resistivity $\leq 10^9 \Omega \text{ cm}$ at room temperature.

12. The method according to any of claims 10 - 11, wherein said substrate is electrically semiconducting at room temperature and is preferably made of a semiconducting material selected from elemental silicon, including doped silicon and crystalline silicon, germanium, compound semiconductors such as gallium arsenide, and indium phosphide.

13. The method according to any of claims 1 – 9, wherein step c) is performed.

14. The method according to claim 13, wherein step c) is performed using an additional energy source which is selected from a heated electrode, a heating element, a laser, a focussed light source, a UV light source, a gas flame, and a high frequency electromagnetic field device, such as a Tesla transformer.

15. The method according to any of claims 13 – 14, wherein said additional energy source is a laser which preferably has a wavelength in a wavelength range that is at least partially absorbed by said substrate.

16. The method according to any of claims 13 – 15, wherein the site of application of additional energy in step c) determines the region of said substrate in which said structure or said structural change is introduced.

17. The method according to any of the foregoing claims, wherein said substrate which is electrically insulating at room temperature or electrically semiconducting at room temperature is provided in step a) having at least one electrically insulating layer attached.

18. The method according to claim 17, wherein said electrically insulating layer is solid, liquid or gaseous at room temperature.

19. The method according to claim 18, wherein said electrically insulating layer is gaseous at room temperature and is not air.

20. The method according to any of claims 17 – 19, wherein said electrically insulating layer has an insulating region which is adjacent to and in contact with said substrate region in which substrate region a structure or structural change is to be introduced, and is preferably effectively reducing the voltage across the substrate (shielding effect) without lowering the voltage between the electrodes, and wherein step c) is performed such that in said electrically insulating layer the electrical conductivity is raised in said insulating region so as to reduce its voltage shielding effect and augmenting the trans-substrate voltage in said substrate region.

21. The method according to any of claims 17-19, 20, wherein said electrically insulating layer has an insulating region which is adjacent to and in contact with said substrate region in which substrate region a structure or structural change is to be introduced, wherein step c) is performed such that said electrically insulating layer, if provided as a solid in step a), is liquefied in said insulating region, or is performed such that said electrically insulating layer, if provided as a liquid in step a), is partially evaporated in said insulating region, and wherein during step d), said electrically insulating layer is partially displaced in said insulating region, through the dissipation of said electrical energy, and wherein, after step d), said gaseous, liquefied or partially evaporated electrically insulating layer flows into said generated structure and thereby closes and at least partially fills said structure.

22. The method according to any of claims 20-21, wherein said electrically insulating layer is attached to said substrate in such a manner that it covers said substrate in step a) or is covered by said substrate in step a), and said substrate region lies opposite said insulating region.

23. The method according to any of claims 17-22, wherein the insulating layer reduces the voltage across the substrate by formation of an internal counter electric field due to electrical polarization of the insulating layer material.

24. The method according to any of claims 17-23, wherein the insulating layer is used to create a mask on said substrate, which mask exposes only the region(s) of the substrate where a structure or several structures or a structural change or several structural changes will be introduced.

25. The method according to any of claims 17-24, wherein the insulating layer is used to improve the flatness/surface quality of the region surrounding the structure introduced by absorbing material ejected during step d) into the insulating layer and thus avoiding redeposition of said ejected material directly onto the substrate surface, wherein, preferably, said absorbed material is subsequently removed together with the insulating layer, after introduction of the structure(s)/structural change(s) into the substrate.

26. The method according to any of claims 17-25, wherein step c) is performed by directly heating the insulating layer such as through absorption of laser radiation of a wavelength absorbed by the insulating layer.

27. The method according to any of claims 17-25, wherein step c) is performed by indirectly heating the insulating layer by heating the attached substrate and utilizing heat transfer from the heated substrate to the attached insulating layer.

28. The method according to any of claims 17-27, wherein said electrically insulating layer is made of a material which is solid and electrically insulating at room temperature and preferably selected from wax, in particular paraffin wax, rubber, hot melt adhesive, poly(styrene-butadiene-styrene), and polyurethane.

29. The method according to any of claims 17 - 28, wherein said electrically insulating layer is made of a material which is liquid at room temperature, and which is electrically insulating at room temperature or polar or both and is preferably selected from dodecane, paraffin, water, or high viscosity water based liquids such as Ficoll™ solution or honey like liquids.

30. The method according to any of claims 17 - 28, wherein said electrically insulating layer is made of a material which is gaseous at room temperature and is preferably selected from SF₆, Ar, N₂, CO₂.

31. The method according to any of the foregoing claims, wherein said substrate is electrically insulating at room temperature and is preferably made of a substrate material selected from glass, quartz, diamond, alumina, sapphire, aluminium nitride, zirconia, and spinel, more preferably quartz and glass.

32. The method according to claim 31, wherein said substrate has an electrical resistivity $> 10^9$ Ohm cm at room temperature.

33. The method according to any of claims 31 - 32, wherein said electrically insulating layer, if present, is made of a material which is solid and electrically insulating at room temperature and is preferably selected from paraffin wax, rubber and hot-melt adhesive.

34. The method according to any of claims 31 - 33, wherein step c) is performed using a laser, preferably having a wavelength in a wavelength range which is at least partially absorbed by said substrate material and/or said insulating layer, if present.

35. The method according to any of claims 1-30, wherein said substrate is electrically semiconducting at room temperature and is preferably made of a substrate material selected from elemental silicon, including doped silicon and crystalline silicon, germanium, compound semiconductors such as gallium arsenide and indium phosphide.

36. The method according to claim 35, wherein said substrate has an electrical resistivity $\leq 10^9$ Ohm cm at room temperature.

37. The method according to any of claims 35 - 36, wherein said electrically insulating layer, if present, is made of a material which is liquid and electrically insulating at room temperature, or polar or both and which is preferably selected from dodecane, paraffin, water, honey, or is made of a material which is solid and electrically insulating at room temperature and which is preferably selected from paraffin wax and hot-melt adhesive.

38. The method according to any of claims 35-37, wherein step c) is performed using a laser, preferably having a wavelength in a wavelength range which is at least partially absorbed by said substrate material and/or said insulating layer, if present.

39. The method according to any of claims 17-38, wherein step c) is performed such that heating of the insulating layer necessary for a electric field reduction across this layer necessary to initiate step b) and d) is leading to a significant increase in temperature of the substrate leading to a significant change of its temperature dependent mechanical parameters such as hardness and brittleness.

40. The method according to any of the foregoing claims, wherein steps a) – d) are performed once, such that a first structure is generated in the first substrate region, thereafter the substrate is moved by a defined distance, and steps b) – d) are performed a second time such that a second structure is generated in a second substrate region.

41. The method according to claim 40, wherein steps b) – d) are performed n times, such that an array of n structures is generated in said substrate, n being an integer > 1 .

42. The method according to any of the foregoing claims, wherein said electrical energy applied in step b) is sufficient to generate a through hole or through channel in said substrate in performing step d).

43. The method according to any of claims 1-41, wherein said electrical energy applied in step b) is not sufficient to generate a through hole or through channel in said substrate in performing step d) and is sufficient to change the structure in said substrate region.

44. The method according to claim 43, wherein step d) changes the structure in said substrate region by heating and/or melting the material present in said substrate region, and wherein such change in structure makes said substrate region more amenable to treatment by an ablating step e) in which said substrate including said substrate region is exposed to an ablating environment such as an etching agent.

45. The method according to any of claims 43-44, wherein said electrical energy is not sufficient to cause an ejection of material from said substrate region.

46. The method according to any of claims 43-45, further comprising step

e) exposing said substrate including said substrate region to an ablating environment,

such as an etching agent.

47. The method according to any of claims 43-46, wherein said substrate is electrically semiconducting at room temperature and is preferably made of a semiconducting material selected from elemental silicon, including doped silicon and crystalline silicon, germanium, compound semiconductors such as gallium arsenide, and indium phosphide.

48. The method according to claim 47, wherein said ablating environment is an etching agent and preferably is an etching agent selective for semiconducting materials, and is more preferably selected from KOH, SF₆, tetramethylammonium hydroxide (TMAH), ethylenediamine pyrocatechol (EDP), hydrazine, and HF.

49. The method according to any of claims 47-48, wherein said ablating environment is created by a reactive ion etching process.

50. The method according to any of claims 47-49, wherein said ablating environment is SF₆ used for etching.

51. The method according to any of claims 43-50, wherein steps b) and d) are performed a number of times n, n being an integer > 1, thereby applying electrical energy to a first, second, third, ... n-th region of said substrate, and thereby changing the structure in said first, second, third, ... n-th region of said substrate.

52. The method according to claims 46 and 51, further comprising step e) as defined in claim 46, wherein step e) is performed once after steps b) and d) have been performed a number of times n, thereby generating an array of n structures in said substrate.

53. The method according to any of claims 44-52, wherein said substrate is elemental silicon and said etching agent is selected from KOH, TMAH, SF₆.

54. The method according to any of claims 46-53, wherein a crystalline substrate is chosen having crystal orientation reducing the etch rate parallel to the substrate surface compared to differently oriented substrates.

55. The method according to any of claims 46-53, wherein a crystalline substrate is chosen having crystal orientation reducing the etch rate perpendicular to the substrate surface compared to differently oriented substrates, such as a $\langle 111 \rangle$ silicon wafer in KOH.

56. The method according to any of claims 46-55, wherein the substrate is coated with a protective layer not or less etched by an etching agent than the substrate itself and which during performing step a)-d) is fully or partially removed or structurally altered so as to allow etching only at the region(s) where step d) has been performed.

57. The method according to claim 56, using the insulating layer, as defined in any of claims 17-39, as protective layer.

58. A structure or an array of structures, preferably holes or cavities or channel or wells or recesses, in a substrate, produced by the method according to any of the foregoing claims, in particular according to any of claims 1 – 16, 17 – 42, or 43 – 57.

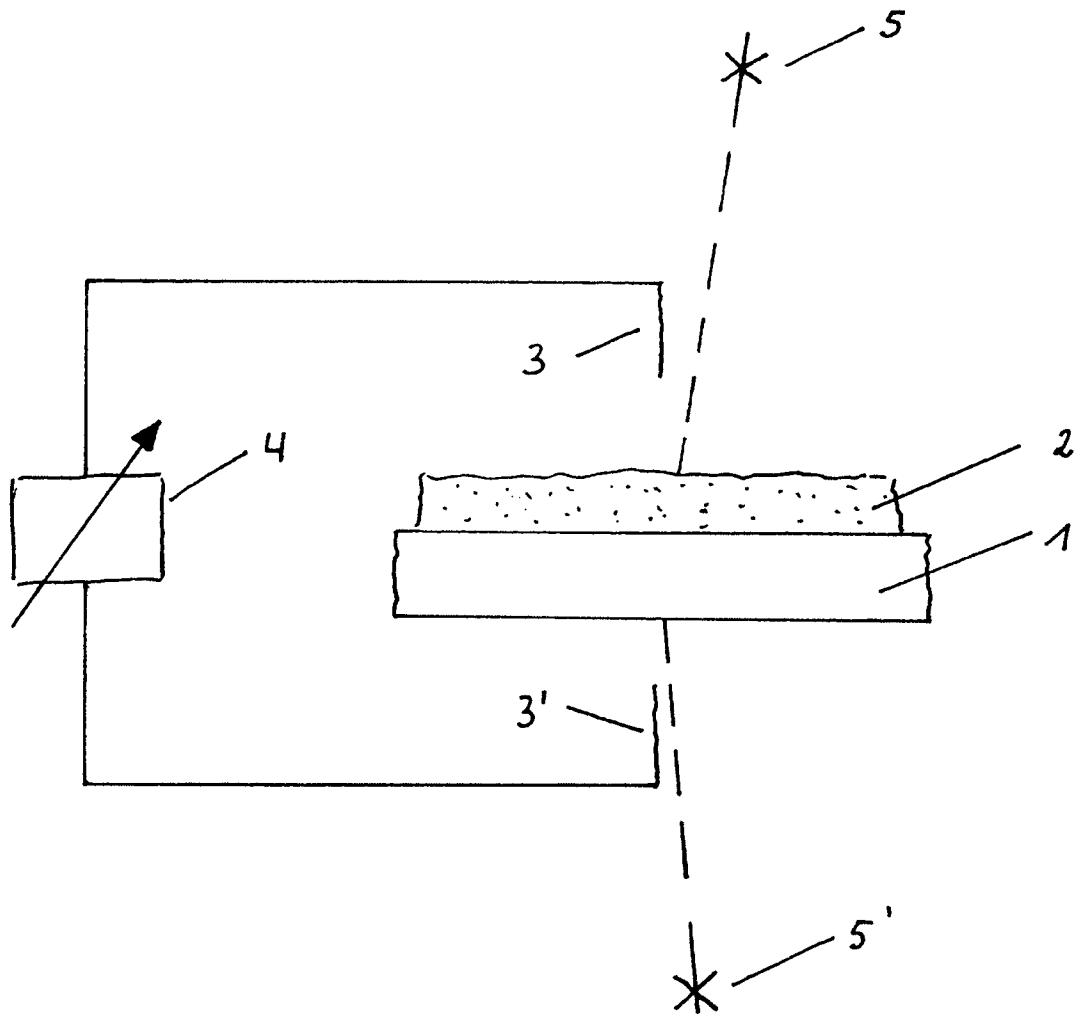


Figure 1

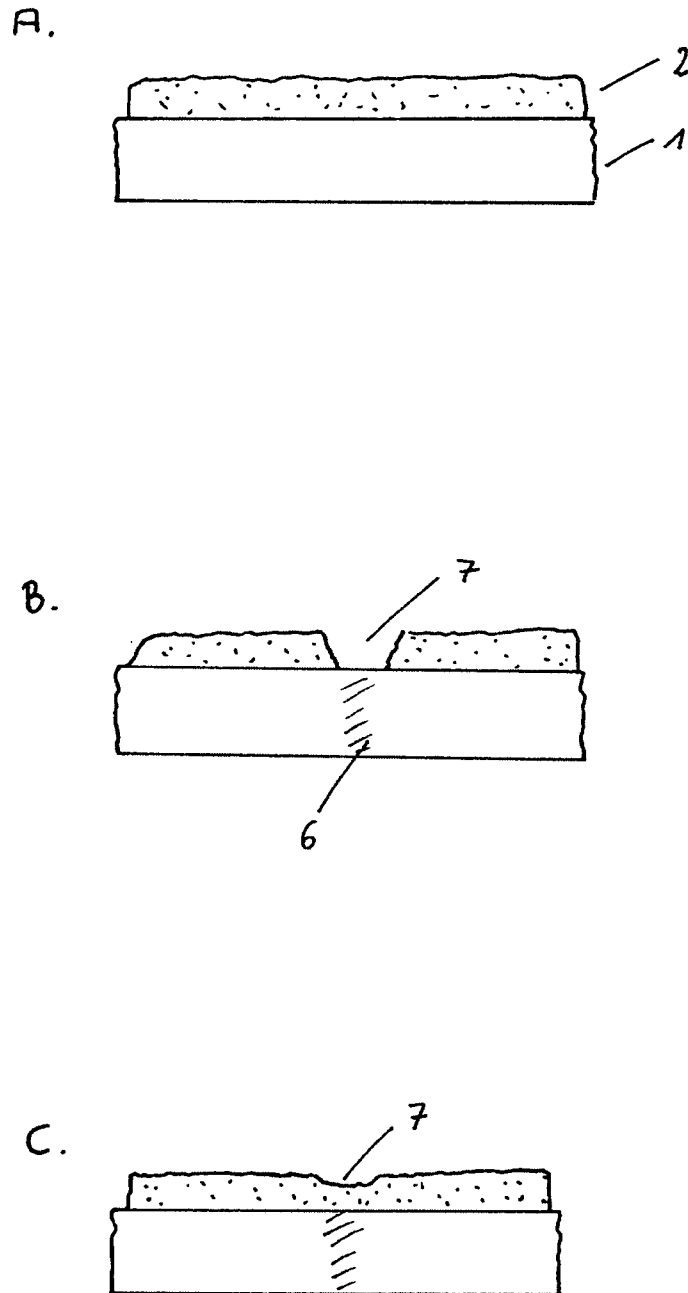
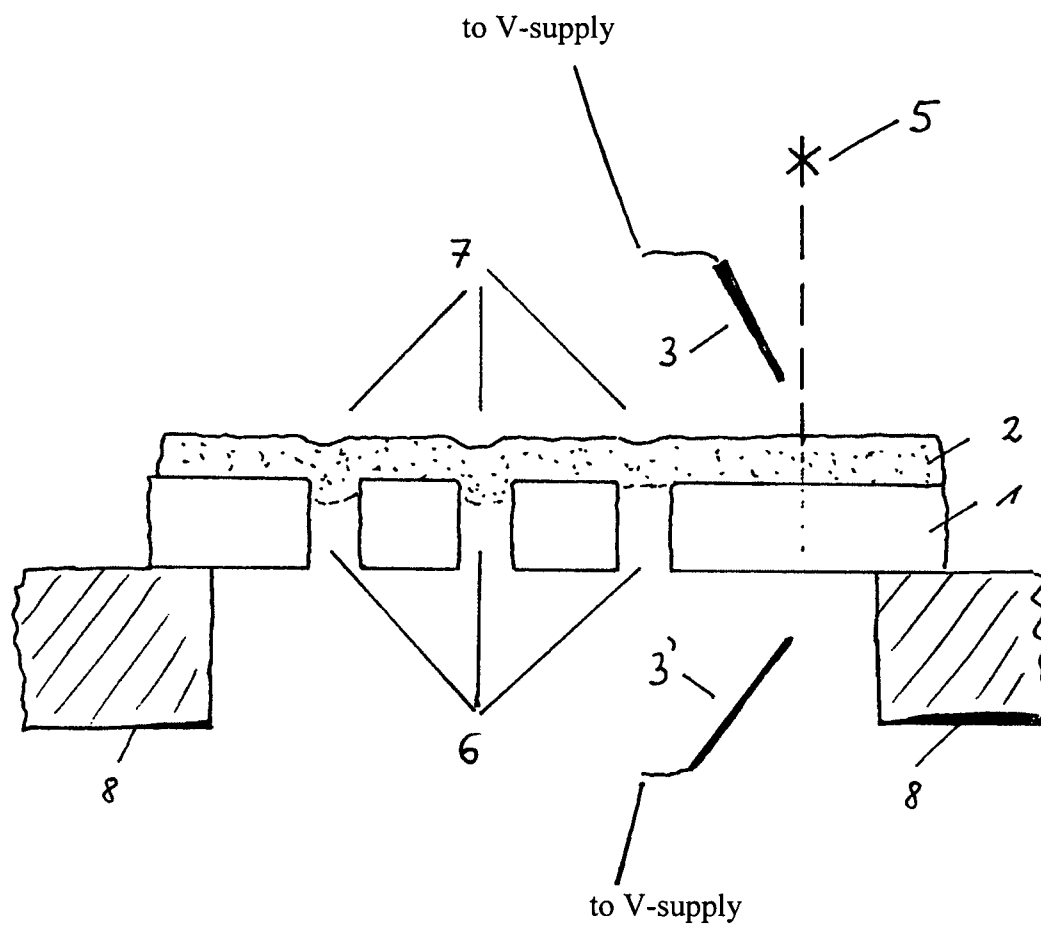


Figure 2

**Figure 3**

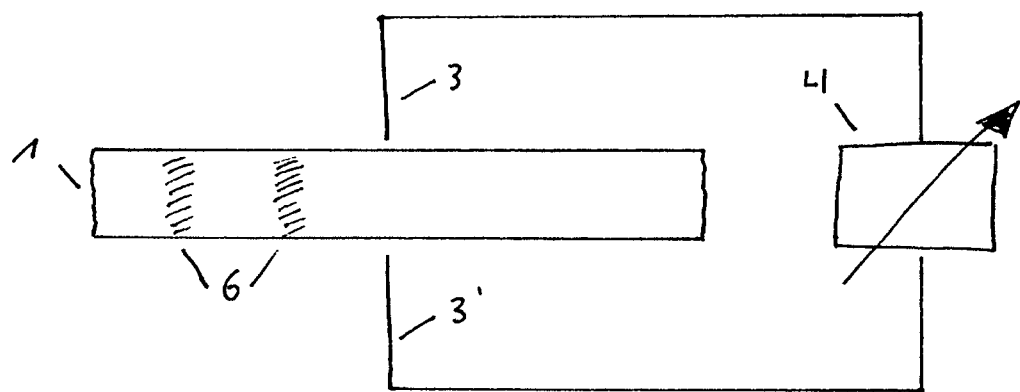


Figure 4

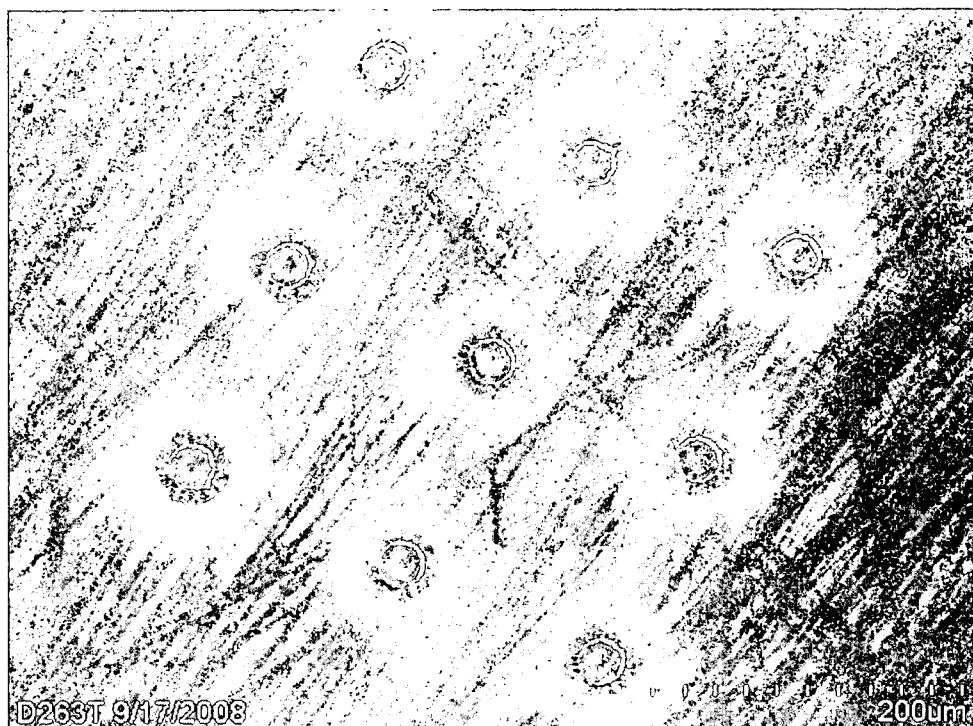


Figure 5

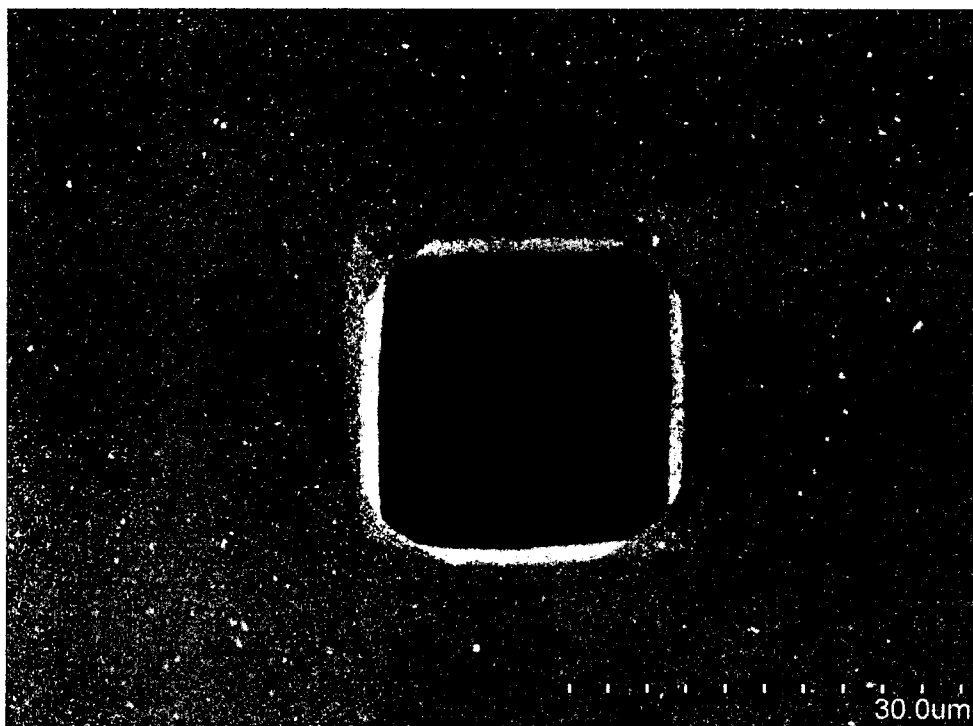


Figure 6

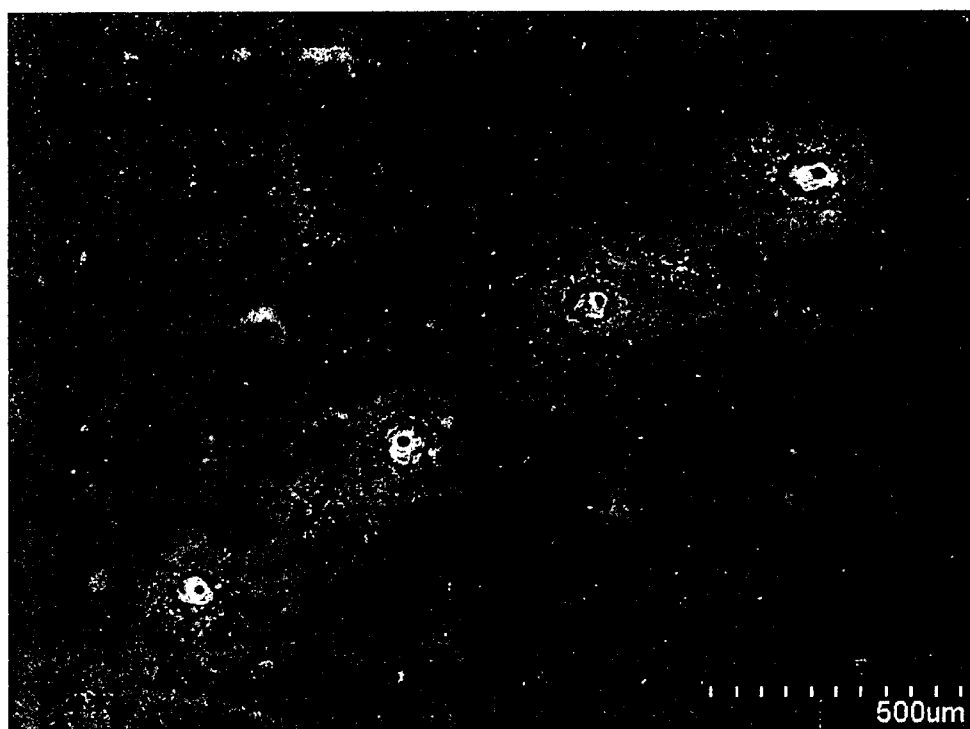
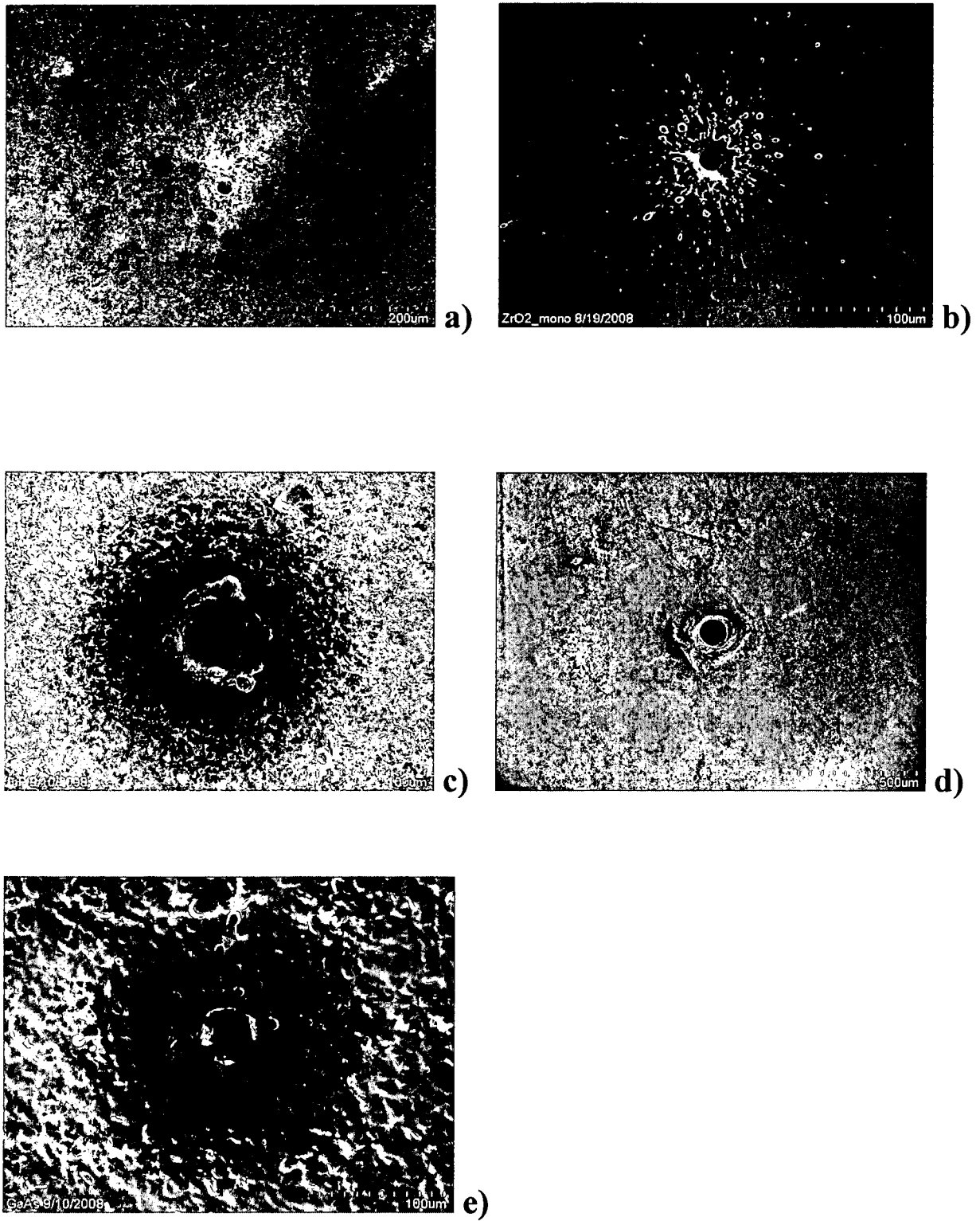


Figure 7



Figure 8

**Figure 9**

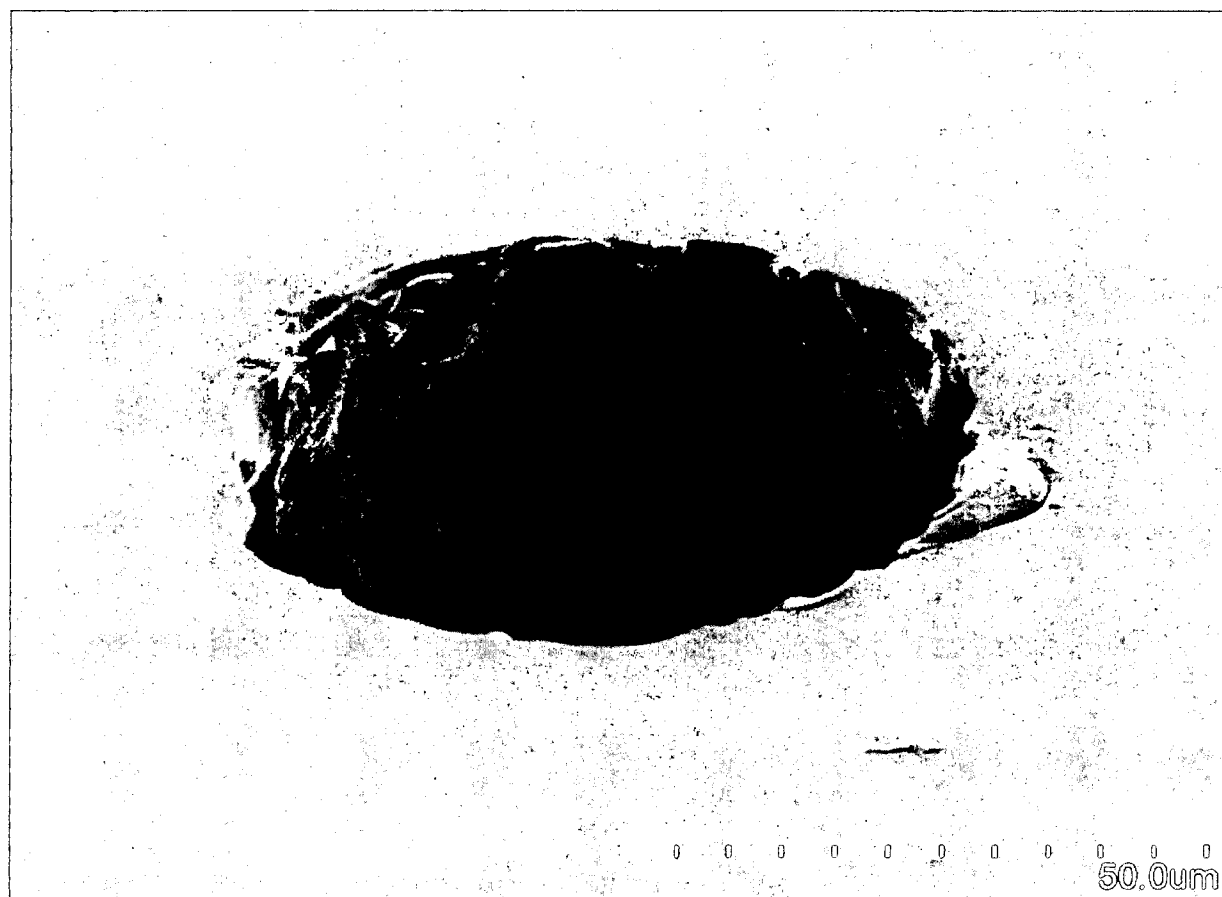


Figure 10

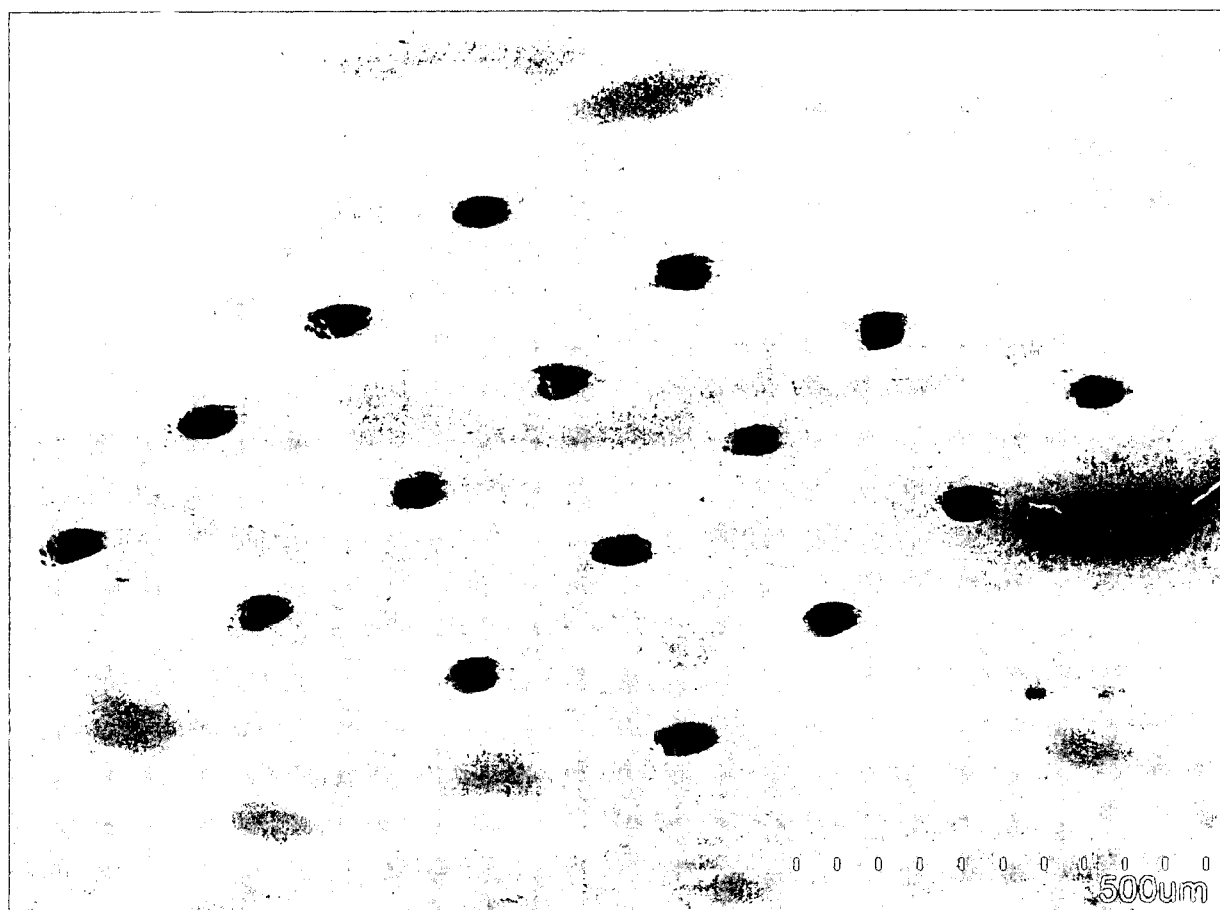


Figure 11a

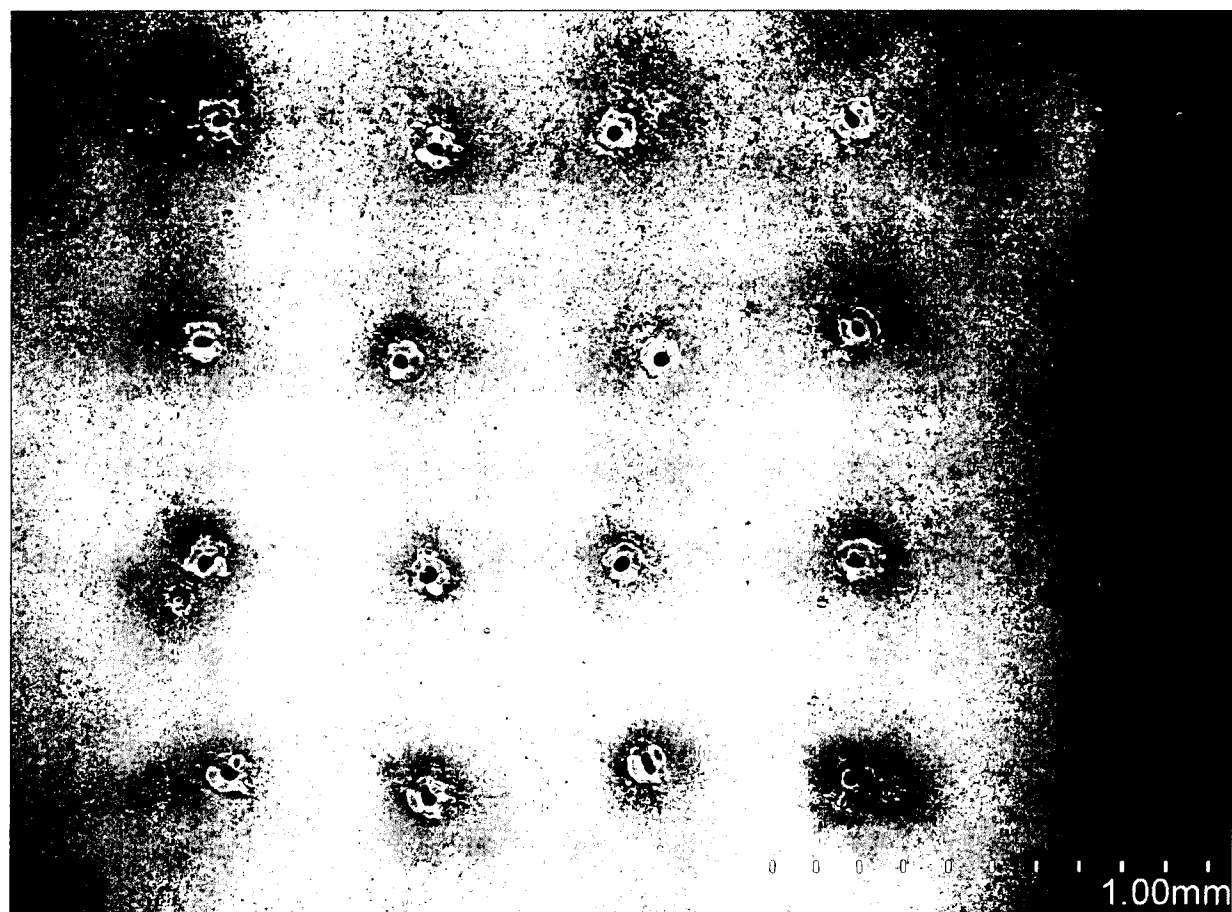


Figure 11b

INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2009/008598

A. CLASSIFICATION OF SUBJECT MATTER

INV. B26F1/28

ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

B26F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2005/097439 A2 (SCHMIDT CHRISTIAN [CH]) 20 October 2005 (2005-10-20) the whole document	1-58
X,P	WO 2009/074338 A1 (PICODRILL SA [CH]; SCHMIDT CHRISTIAN [CH]; DITTMANN LEANDER [CH]) 18 June 2009 (2009-06-18) the whole document	1,58
X,P	WO 2009/059786 A1 (PICODRILL SA [CH]; SCHMIDT CHRISTIAN [CH]) 14 May 2009 (2009-05-14) the whole document	1,58



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

20 April 2010

Date of mailing of the international search report

03/05/2010

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Canelas, Rui

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2009/008598

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2005097439 A2	20-10-2005	EP 1744860 A2 US 2008047935 A1	24-01-2007 28-02-2008
WO 2009074338 A1	18-06-2009	NONE	
WO 2009059786 A1	14-05-2009	NONE	