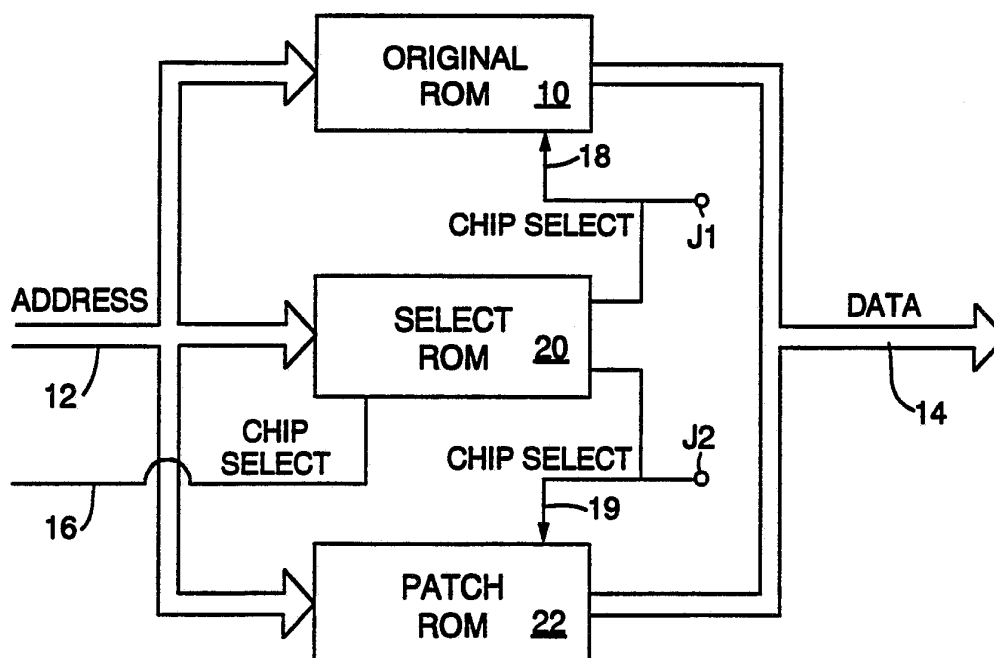




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(54) Title: ROM PATCH DEVICE**(57) Abstract**

A device for enhancing the program code of a first ROM includes an original ROM (10) connected to address and data busses (12 and 14, respectively) in parallel with a patch ROM (22). The original ROM (10) contains a given set of code or data, while the patch ROM (22) contains replacement code or data, such as enhancements to the code. A select ROM (20) has inputs connected to the address bus (12) and outputs (18 and 19) connected to the chip select input pins of the original and patch ROMs (10 and 22, respectively). When the ROMs are addressed, the select ROM selects either the original ROM (10) or the patch ROM (22), depending upon the address. The select ROM (20) controls the data bus by enabling the appropriate chip select pins of the original and patch ROMs (10 and 22, respectively).

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⁺ Any designation of "SU" has effect in the Russian Federation. It is not yet known whether any such designation has effect in other States of the former Soviet Union.

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ROM PATCH DEVICE

BACKGROUNDField of the Invention

5 The present invention relates to an apparatus
for use in conjunction with an existing ROM which
contains original information stored as binary bits.
The information provided by the apparatus is
different from the original information even though
the original information stored in the ROM is not
10 altered.

Discussion of the Prior Art

 The information stored as binary bits in a read-
only-memory (ROM) cannot be selectively changed. In
order to change ROM code, a new program mask must be
15 made. Similarly, with programmable-read-only-
memories (PROM) and electrically-programmable-read-
only-memories (EPROM) a device must be entirely
reprogrammed. The same is true of EAROMs and certain
classes of EEPROMs. In other words, if one wanted to
20 duplicate the information stored in a ROM except for
changing a few locations, the entire code must copied
into the data space of a blank device. (With certain
classes of EEPROMs, the device can be byte erased and
reprogrammed.) Because PROMs and EPROMs are merely
25 subclasses of ROMs, insofar as this invention are
concerned, we will only refer to ROMs. It will be
understood that a reference to a ROM also refers to
PROMs, EPROMs, EAROMs and EEPROMs.

 More importantly, ROMs or systems containing
30 ROMs are sold where the ROM (or PROM or EPROM)
contains the vendor's copyrighted software or data.
A common example of such a system is a personal
computer (PC) containing a basic input/output system
(BIOS) ROM which contains program code that handles
35 microprocessor-to-peripheral communications for the
PC. A user or a value added reseller (VAR) could

develop a BIOS program which merely enhanced the performance of one or several of the BIOS routines by programming a new ROM, PROM or EPROM to contain most of the original copyrighted program code with the enhancements developed by the user. However, this is copyright infringement.

Thus, the end user is limited to the BIOS code provided by the PC vendor or to developing an entirely new code in a so called clean room. A device is needed to allow a user to develop and implement enhancements to software or data stored in a ROM, PROM or EPROM without infringing a copyright in the original data or software.

SUMMARY OF THE INVENTION

A device for enhancing the program code of a first ROM is presented. An original ROM is connected to address and data busses in parallel with a patch ROM. The original ROM contains a given set of code or data, while the patch ROM contains replacement code or data, such as enhancements to the code. A select ROM has inputs connected to the address bus and outputs connected to the chip select input pins of the original and patch ROMs. When the ROMs are addressed, the select ROM selects either the original ROM or the patch ROM, depending upon the address. The select ROM controls the data bus by enabling the appropriate chip select pins of the original and patch ROMs.

In the preferred embodiment, the patch and select ROM's are contained in a single module, which plugs into the socket provided for the original ROM. The original ROM is then plugged into the module to complete the interconnections among the ROMs.

A better understanding of the features and advantages of the present invention will be obtained by reference to the following detailed description of

the invention and accompanying drawings which set forth an illustrative embodiment in which the principles of the invention are utilized.

BRIEF DESCRIPTION OF THE DRAWINGS

5 Figure 1 is a block diagram of a ROM and socket module according to the prior art.

 Figure 2 is a block diagram of a Rom patch device according to the present invention.

10 Figure 3 is a side elevation view of the prior art.

 Figure 4 is a side elevation view of a ROM patch module according to the present invention.

 Figure 5 is a bottom view of the ROM patch module of Figure 4.

DETAILED DESCRIPTION OF THE INVENTION

15 Referring now to Figure 1, a ROM 10, as is well known, contains program code stored to be retrievable by a series of binary address locations. A typical ROM 10, such as an Intel 2764 EPROM, has an address
20 bus 12 for selecting an appropriate memory location, a data bus for providing the information stored in the selected memory location and a chip select pin 16 to activate the ROM so that the information stored in the selected memory location becomes available
25 external to the ROM. In the absence of the appropriate logic signal on the chip select line 16, the lines of the data bus remain floating.

 A typical function of a ROM 10 in a PC is to control the Basic Input/Output System (BIOS), so that
30 the ROM 10 contains instructions to enable the microprocessor to communicate with peripheral equipment such as printers, displays, memory controllers and the like. When the ROM 10 is enabled, program instructions beginning at the

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address on the address bus 12 are presented on the data bus 14.

5 In Figure 2, the ROM patch device of the present invention enables the user to enhance or alter the instructions provided by an original ROM without altering the instructions which are stored in the original ROM 10, and thus, without infringing the copyright on the BIOS code. As in Figure 1, the address bus 12 is tied to the input and the data bus 10 14 is tied to the output of the ROM 10. The select ROM 20 and the patch ROM 22 are connected in parallel to the ROM 10 with respect to the address bus 12; i.e., the address bus 12 is coupled to the input of both the select ROM 20 and the patch ROM 22. 15 However, only the output of the patch ROM 22 is coupled in parallel to the original ROM 10 with respect to the data bus 14.

ROM 20 and ROM 22 may be user programmable EPROMs. In this case, the contents of the ROM 20 and 20 the ROM 22 contained in device 54 may be initially blank. A user may plug device 54 into a commercially available PROM programming equipment, and program each of ROM 20 and ROM 22 sequentially. In this useful application, the chip selects 18 and 19 are 25 brought to the external pins J1 and J2, as shown in Figure 2. The external pins J1 and J2 may be connected by an external cable to the PROM programming equipment. By controlling the signals applied to the external pins J1 and J2, the address 30 bus 12 and the data bus 14 available at the socket pins 60, the contents of the ROMs 20 and 22 can be programmed to suit a particular user application.

Commercially available ROMs have eight lines in the data bus to provide a byte of binary data for 35 each location addressed. Only two of the output lines of the of the select ROM 20 are used for the present invention: a first output line is coupled as

the chip select 18 of the original ROM 10 and a second output line is coupled as the chip select 19 of the patch ROM 22. Further, the chip select 16 for selecting the original ROM 10 before the ROM patch device is used, is now coupled to enable the select ROM 20. Thus, whenever a host system would have accessed data or code from the original ROM 10, it will now access data or code from either the original ROM 10 or the patch ROM 22 under control of the select ROM 20.

Preferably, every address location having a corresponding valid address in the original ROM 10 has information stored in the select ROM 20. In each case, the data site that supplies a binary bit as the chip select 18 to the original ROM 10 will contain the opposite binary condition as the data site that supplies a binary bit as the chip select 19 to the patch ROM 22 so that only one or the other of the original ROM 10 or the patch ROM 22 can drive the data bus 14. In other words, the select ROM is coded so that either the original ROM or the patch ROM are enabled but not both.

The ROM 22 contains alternative or substitute instructions that are programmed by the user. For example, Table I contains a series of sample instructions for the original ROM 10, the select ROM 20 and the patch ROM 22.

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TABLE I

	Address	Original ROM	Select ROM	Patch ROM
	1	instruction A	10xxxxxx	empty
	2	instruction B	10xxxxxx	empty
5	3	instruction C	10xxxxxx	empty
	4	instruction D	10xxxxxx	empty
	5	instruction E	10xxxxxx	empty
	6	instruction F	01xxxxxx	alternate F
	7	instruction G	10xxxxxx	empty
10	8	instruction H	10xxxxxx	empty
	9	instruction I	10xxxxxx	empty
	10	instruction J	01xxxxxx	alternate J
	11	instruction K	10xxxxxx	empty
	12	instruction L	10xxxxxx	empty
15	13	instruction M	10xxxxxx	empty
	14	instruction N	10xxxxxx	empty
	15	instruction O	10xxxxxx	empty

The original ROM 10 contains fifteen original
 instructions A - O. The user wants to modify the
 software by substituting the alternate instruction F
 and alternate instruction J for the original
 instructions F and J stored in address 6 and 10,
 respectively. The select ROM has eight outputs
 because that is the type of device commercially
 available. The first output is used to drive the
 original ROM's chip select and the second output is
 used to drive the patch ROM's chip select. In each
 address, the condition of the first and second
 outputs for the select ROM are opposite. In each
 case, except for addresses 6 and 10, the first output
 is a binary "1" and the second output is a binary "0"
 to select the original ROM. For addresses 6 and 10,
 the binary conditions are reversed to select the
 patch ROM. The remaining six outputs do not matter
 to this invention and are indicated by an "x" for a
 "don't care" condition.

Ordinarily, when the original ROM 10 contains a
 BIOS program it is packaged in a dual-in-line (DIP)
 package and mounted in a socket 50 on a PC mother
 board 52 as shown in Figure 3 rather than being

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soldered. In the preferred embodiment of the present invention shown in Figure 4, the original ROM 10 is removed from the socket 50 and is inserted into a socket 58 on a ROM patch device 54. The ROM patch device 54 includes a printed circuit board 56 on which the select ROM 20 and the patch ROM 22 are mounted. Preferably, the select ROM 20 and the patch ROM 22 are packaged in leadless chip carrier (LCC) packages. Thus, they are sufficiently small to fit within the boundaries of the pins 60 on the printed circuit board 56 as shown in Figure 5.

The printed circuit board 56 includes the appropriate interconnection traces to electrically couple the socket 58 for the original ROM 10, the select ROM 20 and the patch ROM 22 to one another and to the appropriate pins 60. The ROM patch device 54 is inserted into the socket 50 on the PC mother board 52 by the pins 62. Thus, the ROM patch device 54 does not require any additional space on the mother board 52. In such a design, ROM patch device 54 has length and width substantially identical to ROM 10, but the height is slightly increased. Ordinarily, this will not be a problem.

It should be understood that the invention is not intended to be limited by the specifics of the above-described embodiment, but rather defined by the accompanying claims. For example, in the event that LCC packaged ROMs are not available, the physical configuration of the module would necessarily be changed. Further, three or more outputs of the select ROM could be used to select from among information stored in three or more ROMs.

C L A I M S

What is claimed is:

- 1 1. A memory device comprising:
 - 2 first and second memory chips coupled in parallel
 - 3 to an address bus and a data bus and each having a
 - 4 chip select input pin, wherein the second memory chip
 - 5 contains data at one or more specified locations for
 - 6 replacing the data stored at corresponding locations
 - 7 of the first memory chip; and
 - 8 a selector chip having address input pins coupled
 - 9 to the address bus and having data output pins
 - 10 coupled to the chip select input pins of the first
 - 11 and second memory chips, wherein the selector chip
 - 12 contains data that when output selects the second
 - 13 memory chip when one of the specified locations is
 - 14 addressed and selects the first memory chip when any
 - 15 other location is addressed.
- 1 2. A device for patching data contained in a first
 - 2 memory chip containing first address pins, first data
 - 3 pins, and a first chip select pin, said device
 - 4 comprising:
 - 5 a plurality of signal pins coupled to receive an
 - 6 address and a chip select from an external device and
 - 7 to transmit data to the external device;
 - 8 a plurality of first sockets for receiving and
 - 9 contacting the pins of the first memory chip,
 - 10 including address, data and chip select sockets
 - 11 corresponding to the first address, first data, and
 - 12 first chip select pins, respectively, of the first
 - 13 memory chip so that the address and data first
 - 14 sockets are coupled to the address and data signal
 - 15 pins, respectively;
 - 16 a plurality of second sockets for receiving and
 - 17 contacting pins of a patch memory chip having second

18 address pins, second data pins and a second chip
19 select pin, the plurality of second sockets including
20 address, data and chip select sockets corresponding
21 to the second address, second data, and second chip
22 select pins, respectively, of the patch memory chip
23 so that the address and data second sockets are
24 coupled to the address and data signal pins,
25 respectively; and
26 a plurality of third sockets for receiving and
27 contacting pins of a select memory chip having third
28 address pins, third data pins and a third chip select
29 pin, the plurality of third sockets including
30 address, data and chip select sockets corresponding
31 to the third address, third data, and third chip
32 select pins, respectively, of the select memory chip
33 so that the address and chip select third sockets are
34 coupled to the address and chip select signal pins,
35 respectively and one of the data third sockets is
36 coupled to each of the second and third chip select
37 sockets.

1 3. The device of Claim 2, wherein the plurality of
2 first, second and third sockets are combined on a
3 single modular package.

1 4. A device for enhancing a program code stored in
2 a first ROM, wherein the first ROM has a first input
3 coupled to an address bus, a first output coupled to
4 a data bus, and a first select pin for enabling the
5 first ROM, whereby presentation of a valid address on
6 the address bus to the first input combined with
7 enabling of the first ROM by activating the first
8 select pin causes data stored at the valid address in
9 the ROM to be presented on the data bus, the device
10 comprising:

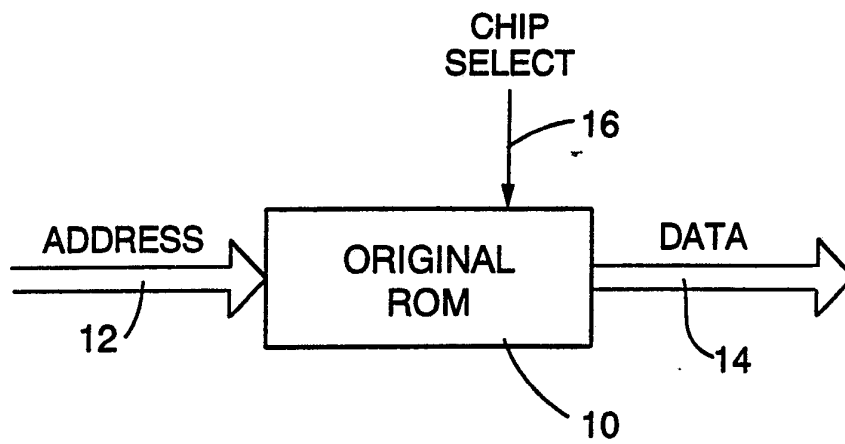
11 a) a second ROM having a second input coupled to
12 the address bus, a second output coupled to the

-10-

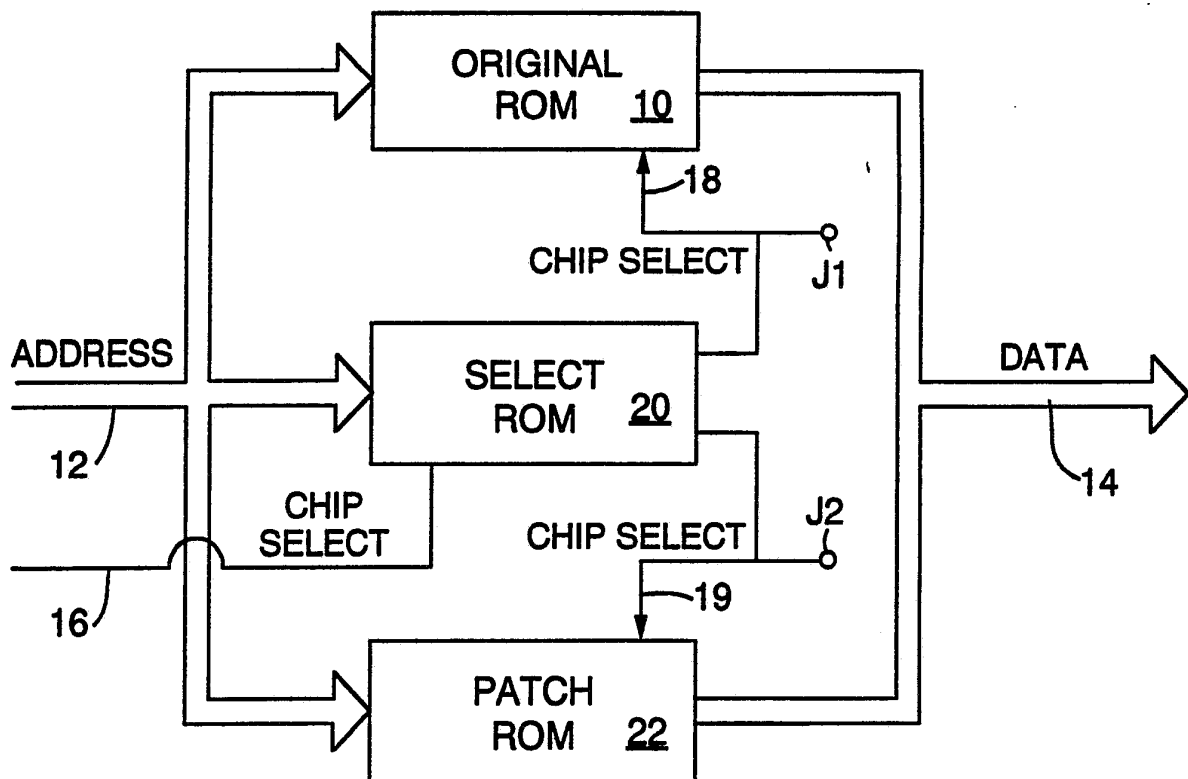
13 data bus, and a second select pin for enabling
14 the second ROM, whereby presentation of a valid
15 address on the address bus to the second input
16 combined with enabling of the second ROM by
17 activating the second select pin causes data
18 stored at the valid address in the second ROM to
19 be presented on the data bus; and
20 b) a third ROM having a third input coupled to
21 the address bus, and a first and a second output
22 pin, wherein the first output pin is coupled to
23 the first select pin, and the second output pin
24 is coupled to the second select pin, and whereby
25 the third ROM is programmed to activate only one
26 of the first ROM or the second ROM.

1 5. The device of Claim 4, wherein the modular
2 package is inserted into a socket on a printed
3 circuit board, and wherein the first ROM is coupled
4 to the modular package.

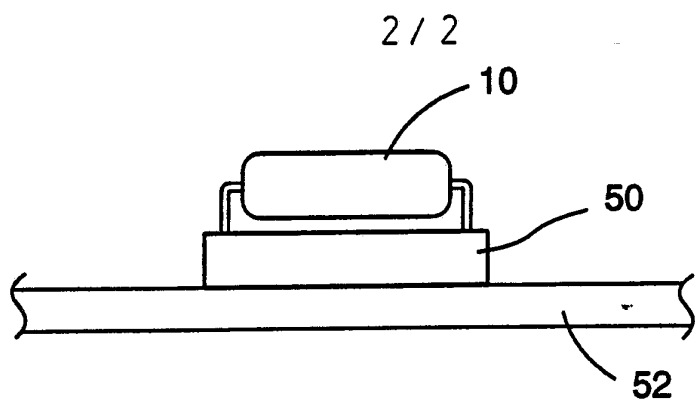
1 / 2



(PRIOR ART)

FIG. 1**FIG. 2**

SUBSTITUTE SHEET



(PRIOR ART)
FIG. 3

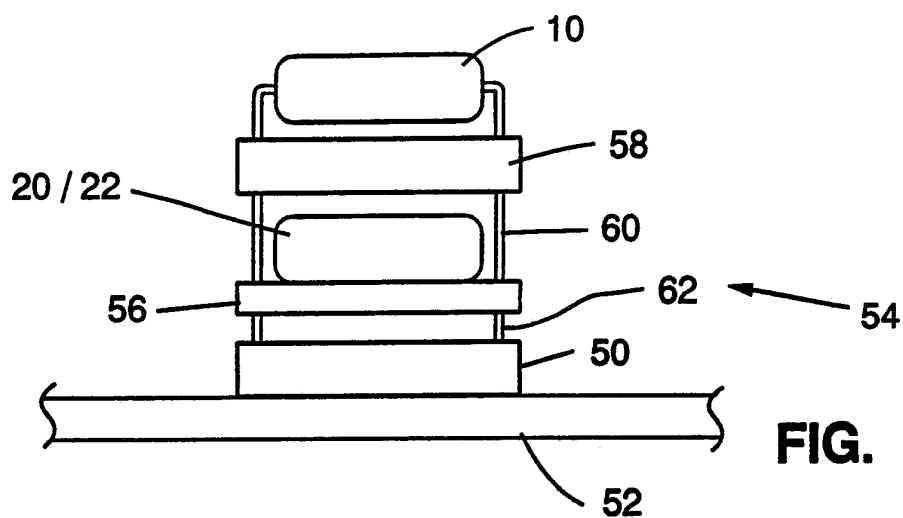


FIG. 4

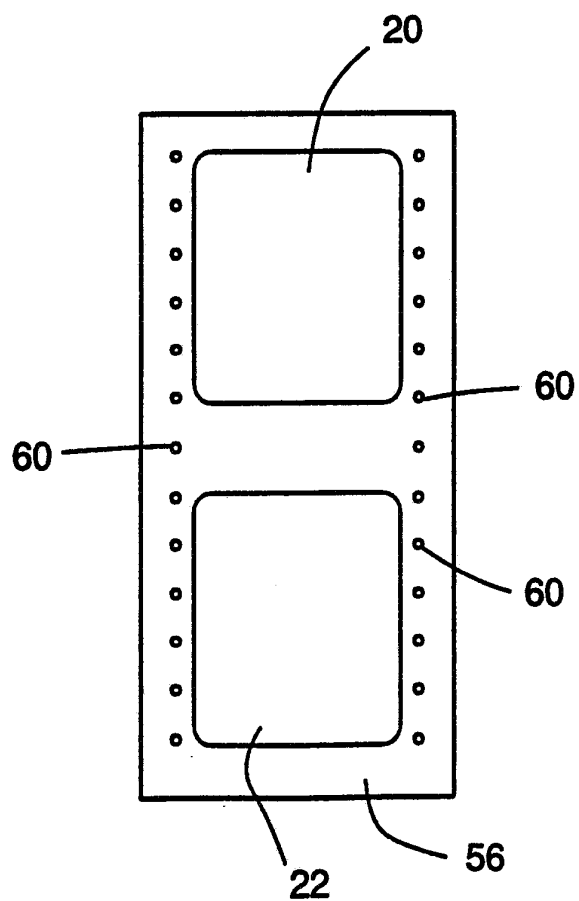


FIG. 5

INTERNATIONAL SEARCH REPORT

International Application No. PCT/US91/08098

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) ⁶		
According to International Patent Classification (IPC) or to both National Classification and IPC		
IPC (5): G11C 17/14		
U.S.Cl.: 365/52,63,72,94,96,103,104,200,230.03		
II. FIELDS SEARCHED		
Minimum Documentation Searched ⁷		
Classification System	Classification Symbols	
U.S.Cl.	365/52,63,72,94,103,104,200,230.03	
Documentation Searched other than Minimum Documentation to the extent that such Documents are Included in the Fields Searched ⁸		
NONE		
III. DOCUMENTS CONSIDERED TO BE RELEVANT ⁹		
Category [*]	Citation of Document, ¹¹ with indication, where appropriate, of the relevant passages ¹²	Relevant to Claim No. ¹³
<u>X</u>	US, A, 4,319,343 (POWELL) 09 March 1982	1,2,4
Y	(Note Especially Column 3).	3,5
Y	US, A, 4,884,237 (MUELLER ET AL.) 28 November 1989 (Note Figure 2).	3,5
A	US, A, 4,490,812 (GUTERMAN) 25 December 1984	1,2,4
A	US, A, 4,609,985 (DOZIER) 02 September 1986	1,2,4
A	US, A, 4,610,000 (LEE) 02 September 1986	1,2,4
A	US, A, 4,785,425 (LAVELLE) 15 November 1988	1,2,4
[*] Special categories of cited documents: ¹⁰ "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art. "&" document member of the same patent family		
IV. CERTIFICATION		
Date of the Actual Completion of the International Search		Date of Mailing of this International Search Report
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