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(54) Title: CONDUCTIVITY IMPROVEMENTS FOR III-V SEMICONDUCTOR DEVICES

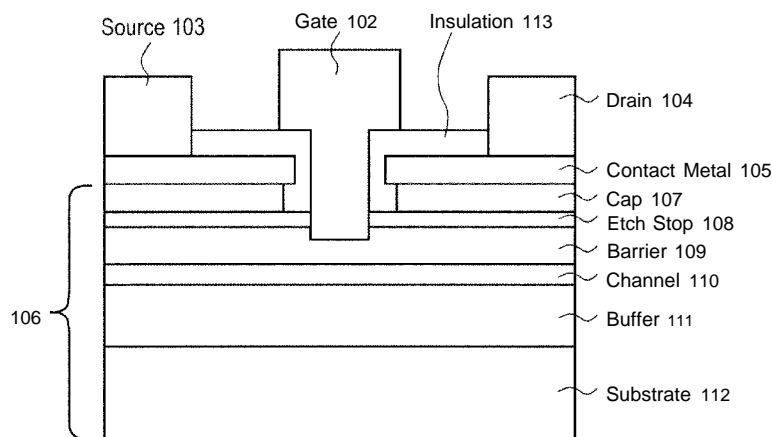


FIG. 1

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(57) Abstract: Conductivity improvements in III-V semiconductor devices are described. A first improvement includes a barrier layer that is not coextensively planar with a channel layer. A second improvement includes an anneal of a metal/Si, Ge or Silicon - Germanium/ni-V stack to form a metal-Silicon, metal-Germanium or metal-SiliconGermanium layer over a Si and/or Germanium doped III-V layer. Then, removing the metal layer and forming a source/drain electrode on the metal-Silicon, metal-Germanium or metal-SiliconGermanium layer. A third improvement includes forming a layer of a Group IV and/or Group VI element over a III-V channel layer, and, annealing to dope the III-V channel layer with Group IV and/or Group VI species. A fourth improvement includes a passivation and/or dipole layer formed over an access region of a III-V device.

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B. FIELDS SEARCHED

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

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Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: "semiconductor" and "conductivity" and "hetero-junction"

c. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6281528 B1 (WADA; SHINICHI) 28 August 2001 See the abstract ; figs . 1-6 ; column 3, line 55 - column 8, line 14.	1-43
A	JP 2009-054807 A (SANKEN ELECTRIC CO LTD) 12 March 2009 See the abstract ; figs . 1-6 ; paragraphs [0012]-[0035] .	1-43
A	US 2002-0175343 A1 (ZEMPEI KAWAZU et al.) 28 November 2002 See the abstract ; figs . 1-15 ; paragraphs [0046] -[0097] .	1-43

 Further documents are listed in the continuation of Box C. See patent family annex.

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