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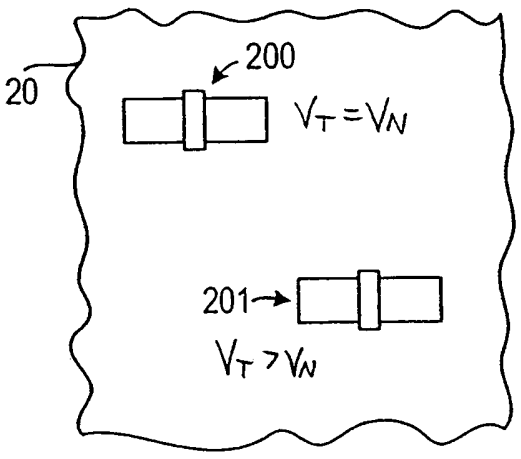
(54) Title: ENHANCED PASSGATE STRUCTURES FOR REDUCING LEAKAGE CURRENT



(57) Abstract: Enhanced passgate structures for use in low-voltage systems are presented in which the operational speed of the passgate structures is maximized, while minimizing leakage current when the structure is turned "OFF." In one arrangement, the VT of the passgate structures is increased relative to the VT of other transistors fabricated according to a particular process dimension. In addition, a passgate activation voltage is applied to the passgate structures such that the passgate activation voltage is higher in voltage than a nominal voltage being supplied to circuitry other than the passgate structures.

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ENHANCED PASSGATE STRUCTURES FOR REDUCING LEAKAGE CURRENT

Background of the Invention

[0001] This invention relates to integrated circuit devices, and more particularly to the passgate structures that may be used in such devices.

[0002] One of the most ubiquitous structures within an integrated circuit device is the single-transistor passgate, which is commonly used to implement (either singly or in combination with other circuits) switches, multiplexers, logic functions (e.g., pass transistor logic), and gating mechanisms for tristatable circuits (e.g., buffers and drivers). In some integrated circuit devices, single-transistor passgate structures may account for a significant portion of the circuitry; for example, in the case of programmable logic devices, single-transistor passgates are used extensively throughout the device as part of the programmable interconnection circuitry.

[0003] The operation of a typical single-transistor passgate may be succinctly illustrated by a description of an NMOS passgate (analogous principles of operation, as understood by one skilled in the art, would apply

for a PMOS passgate). Depending on whether the potential difference between its gate terminal, V_{GATE}, and its source terminal, V_{SOURCE}, exceeds the threshold voltage, V_T, a NMOS passgate acts as an "open" or a "closed" switch. (As is well-known in the art, there is no physical difference between the "source" and "drain" terminals of a MOS device; the source terminal of a NMOS transistor is the terminal having the lower voltage.) When V_{GATE}-V_{SOURCE} is less than V_T, the NMOS passgate is in the "cutoff" state, thereby acting as an "open" switch; when V_{GATE}-V_{SOURCE} is greater than V_T, the NMOS passgate is in the conduction state, thereby acting as a "closed" switch.

[0004] As is well-known in the art, V_T is not a discrete value for an MOS transistor; it may be considered a range of values that is influenced by a variety of second-order effects, such as substrate bias and subthreshold conduction. However, in order to simplify the illustration of the principles of the present invention, V_T will be discussed herein as if it is a discrete value rather than a range of values.

[0005] With the current trend in scaling down device geometries (e.g., 0.18μm process down to 0.13μm, 90nm, and lower) and the consequent use of ever-lower operating voltages (e.g., supply voltages, bias voltages, etc.), which are nearing levels comparable to V_T, the ability of transistor passgate structures to function at relatively high speeds while at the same time minimizing leakage current is a difficult design hurdle to overcome.

[0006] Moreover, this trend of smaller device geometries and consequent use of lower operating voltages is creating a design tradeoff between speed

(e.g., response time for the passgate transistor to turn ON) and leakage current (e.g., the current that passes through the passgate transistor when turned OFF) that was not previously experienced with larger device geometries and the consequent use of higher operating voltages. That is, if conventional design techniques are applied to smaller device geometries, high speed passgate operation is accompanied with high leakage current, whereas low leakage current is accompanied with low speed passgate operation. High leakage current is undesirable because it results in excess heat, power loss, and poorer performance.

[0007] Another problem associated with shrinking geometries is the consequent use of lower operating voltages. This lower operating voltage is typically a nominal voltage supplied to the integrated circuitry, and may be insufficient for certain circuitry, such as configurable memory cells (e.g., SRAM) within the integrated circuitry, to operate properly. For example, as the supply voltage decreases, the soft-error-rate increases because the critical charge needed to flip the cells (from one logic state to another) is reduced.

Summary of the Invention

[0008] The present invention relates to enhanced passgate structures for use in low-voltage systems. In accordance with the principles of the present invention, various techniques are presented for reducing leakage current, while at the same time maintaining high speed operation of the passgate structures. Although the techniques described herein

are illustrated using NMOS passgates, they may be readily adapted to PMOS structures.

[0009] In one arrangement, leakage current is reduced and high speed operation is maintained by raising the V_T of the passgate structure above that of the V_T of other structures (e.g., logic transistors) and by applying a passgate activation voltage that is higher than a nominal voltage (e.g., "low" system voltage) to the gate of the passgate structure. An advantage realized by increasing the V_T of the passgate structures is that it reduces the leakage current when the passgate structures are turned OFF. The passgate activation voltage is sufficient to enable the passgate structure to operate at a desired speed even though the V_T has been increased relative to the V_T of other structures other than the passgate structures.

[0010] Because the passgate activation voltage is higher than the nominal voltage, the power source providing the activation voltage may be used to power configurable memory cells such as SRAM. Powering the configurable memory cells with a voltage higher than the nominal voltage reduces the soft-error-rate because the higher voltage increases the critical charge needed to flip the cell.

[0011] Further features of the invention, its nature and various advantages will be more apparent from the accompanying drawings and the following detailed description of the invention.

Brief Description of the Drawings

[0012] FIG. 1 is a schematic representation of an enhanced passgate structure which may be constructed in

accordance with the principles of the present invention.

[0013] FIG. 2 is a simplified illustration of an aspect of an integrated circuit device which may be fabricated in accordance with the principles of the present invention.

[0014] FIG. 3 is a simplified illustration of an aspect of another integrated circuit device which may be fabricated in accordance with the principles of the present invention.

[0015] FIG. 4 is a schematic representation of another enhanced passgate structure which may be fabricated in accordance with the principles of the present invention.

[0016] FIG. 5 illustrates an aspect of the enhanced passgate structure of FIG. 4 in greater detail.

[0017] FIGS. 6A and 6B are illustrative graphs of different modes of operation of transistors having a nominal V_T and passgate structures having an increased V_T in accordance with the principles of the present invention.

[0018] FIG. 7 is a simplified block diagram of a programmable logic device in accordance with the principles of the present invention.

[0019] FIG. 8 illustrates how an aspect of the programmable logic device of FIG. 7 may be improved in accordance with the principles of the present invention.

[0020] FIG. 9 illustrates another aspect of the programmable logic device of FIG. 7 may be improved in accordance with the principles of the present invention.

[0021] FIG. 10 is a simplified block diagram of configurable memory cells that selectively drive passgate structures in accordance with the principles of the present invention.

[0022] FIG. 11 is a simplified block diagram of an illustrative system that includes an integrated circuit device that has been improved in accordance with the principles of the present invention.

Detailed Description of the Invention

[0023] For the purpose of simplifying the discussion of the principles of the present invention, the techniques and embodiments described herein will focus on NMOS passgates. However, the principles illustrated herein are applicable to similar arrangements involving PMOS passgates.

[0024] As defined herein, a nominal voltage is the voltage that is used predominately throughout an integrated circuit, such as a programmable logic device, and is typically associated with "low" voltages. The nominal voltage is sometimes referred to as a system voltage or a core circuitry voltage.

[0025] As defined herein, a nominal threshold voltage is the threshold voltage of transistors other than the passgate transistors according to the invention that are included in the integrated circuitry (e.g., programmable logic device). A nominal V_T may be the V_T of a transistor (e.g., a logic transistor) fabricated using a particular process (e.g., a 90nm process) without attempting to produce a V_T that would not normally be fabricated according to that particular process.

[0026] FIG. 1 illustrates one arrangement for reducing leakage current, while maintaining high speed operation of the NMOS passgates in accordance with the principles of the present invention. In the arrangement shown in FIG. 1, the V_T of NMOS passgate 100 is fabricated to have a higher than nominal V_T than other transistors fabricated according to a particular process dimension (e.g., a 90nm process). The voltage being applied to the gate, V_{GATE}, of NMOS passgate 100 is higher than the nominal voltage. V_{GATE} is sometimes referred to herein as the passgate activation voltage. In some designs, depending on the process being used and the voltage difference between V_{IN} and V_{GATE} or the difference between V_{OUT} and V_{GATE}, NMOS passgate 100 may be a high-voltage tolerant transistor, such as a thick-oxide device, in order to reliably handle voltage being applied to its gate to prevent, for example, gate-oxide breakdown.

[0027] For the purposes of the present invention, V_{GATE} may be a static bias voltage or a dynamic signal. In one embodiment, as illustrated in FIG. 1, the passgate activation voltage may be derived from any of a variety of sources 104, such as a dedicated external pin on which a voltage greater than the nominal voltage is provided, an I/O pin (e.g., control/data signals provided from an external source that provides a voltage higher than a nominal voltage), or a positive I/O supply voltage, $V_{DD-I/O}$ (e.g., when the core circuitry and the I/O circuitry have separate power supplies and $V_{DD-I/O}$ is greater than the nominal voltage).

[0028] In other embodiments, depending on the application, the passgate activation voltage may also be generated by any of a variety of voltage

boosting/conversion circuitry such as charge pumps and voltage converters (e.g., DC/DC, AC/DC, etc.). In yet other embodiments, the passgate activation voltage may be provided by a memory cell such as an SRAM-cell.

[0029] It will be understood that the extent to which the passgate activation voltage exceeds the nominal voltage can vary depending on several factors such as type of transistor and gate-oxide thickness. It will further be understood that the passgate activation voltage exceeds the nominal voltage by a predetermined voltage. For example, the predetermined percentage may range from about one percent to about two hundred percent, depending on various factors.

[0030] The application of this passgate activation voltage to the gates of the passgate structures insures that the desired passgate operation speed is obtained.

[0031] As semiconductor processes continue to decrease in size, V_T continues to decrease. As is known in the art, a reduction in V_T results in a corresponding increase in leakage current during the "OFF" state. In accordance with the principles of the present invention, it is thus preferable to increase the threshold voltages of those specific transistors being used as passgates.

[0032] One arrangement for accomplishing this is shown in FIG. 2, which schematically illustrates a portion of a representative integrated circuit device 20, in which two transistors have been fabricated with different threshold voltages. As shown in FIG. 2, transistor 200 is configured to operate as something other than a passgate structure and may be fabricated with an associated V_T equal to V_N (a nominal V_T). The other transistor 201 is configured to operate

as a passgate, and may be fabricated with an associated V_T that is higher than V_N by a predetermined percentage.

[0033] The above-mentioned predetermined percentage may range from about one percent to about two hundred percent, from about one percent to about one hundred percent, from about one percent to about fifty percent, from about five percent to about forty-five percent, from about ten percent to about forty percent, from about fifteen percent to about thirty-five percent, from about twenty percent to about thirty percent, from about one percent to about thirty percent, from about five percent to about thirty percent, from about ten percent to about thirty percent, from about twenty percent to about forty percent, from about twenty-five percent to about thirty-five percent, or from about thirty percent to about fifty percent.

[0034] It will be understood that any increase in threshold voltage over the nominal threshold voltage assists in minimizing leakage current and is in accordance with the principles of the present invention. Thus it is understood that the present invention is not limited to the percentages enumerated herein.

[0035] Expanding on the arrangement shown in FIG. 2, FIG. 3 shows a portion of an integrated circuit device 30, which is divided into different sections 301/302/303, wherein all the transistors within a given section have been fabricated with a specific threshold voltage that may be different from that of the transistors in the other sections. For example, sections 301 and 302 may each be a routing network with a high concentration of passgates (which may be used to construct, for example, interconnection switches and

multiplexers). Accordingly, the transistors in sections 301 and 302 could be fabricated with a V_T that is higher than that of the transistors in other sections 303.

[0036] As an alternative, or in addition, to selectively fabricating low V_T transistors, FIGS. 4 and 5 illustrate an arrangement wherein a higher than nominal V_T may be achieved by controlling the bias voltage, V_{BIAS}, of the well 405 in which the NMOS passgate 400 is fabricated. For the purposes of the present invention, NMOS passgate 400 is preferably fabricated in a well 405 which is capable of being biased to a voltage that is different from that which is used to bias the substrate 520. In the illustrative embodiment shown in FIG. 5, for example, a triple-well process may be used to allow p-well 405 to be biased separately from the p-substrate 520, thereby allowing the V_T of NMOS passgate 400 to be adjusted as a function of the source-to-bulk potential difference, V_{SB}, which, in the arrangement shown in FIG. 5, is dependent on V_{BIAS}. The relationship between V_T and V_{SB} for an NMOS transistor, which should be familiar to those skilled in the art, may be expressed as follows:

$$V_T = V_{t0} + \gamma[\mathrm{sqrt}(V_{SB} + 2\Phi_F) - \mathrm{sqrt}(2\Phi_F)]$$

(wherein V_{t0} is the threshold voltage when V_{SB} is zero, g is the body-effect constant, and Φ_F is a term associated with the doping of the well). Accordingly, the V_T of NMOS passgate 400 may thus be increased by creating a positive V_{SB} by setting the bias voltage, V_{BIAS}, of well 405 to a level that is lower than the voltage level present on the source terminal of NMOS passgate 400. For the purposes of the present invention, V_{BIAS} should not be too low so as to forward

bias the junction between the source/drain 401/402 and the p-well 405.

[0037] In accordance with the principles of the present invention, V_{BIAS} may be derived from any of a variety of sources and bias generation schemes 500, which may be either internal or external to the integrated circuit device which includes NMOS passgate 400. Such sources 500 may include external pins, charge pumps, voltage references, voltage dividers, level-shifters, control/feedback circuitry, and the like. In some designs, V_{BIAS} may be provided as a static voltage, which may or may not correspond to any of the supply voltages used on the integrated circuit device. In other designs, it may be preferable to use a dynamic voltage for V_{BIAS}, which may be provided by a control circuit that generates a variable V_{BIAS} that may be a function of any of a variety of parameters, such as process variations, temperature, voltage, current, or a combination thereof. As a result, the V_T of NMOS passgate 400 may be tuned in a feedback loop to achieve a high V_T that, when coupled with higher than nominal gate voltages, optimizes, for example, the tradeoff between high speed passgate operation and reducing leakage current.

[0038] FIGS. 6A and 6B show graphs comparing performance characteristics of passgate structures constructed according to the invention and to other transistors not being used as passgates, both of which are fabricated according to a given process dimension. Both FIGS. 6A and 6B show an illustrative trend in supply voltages (line 610) for a given process dimension. FIGS. 6A and 6B show an illustrative trend of nominal threshold voltages, V_{TN}, of transistors other

than the passgate structures according to the invention. FIGS. 6A and 6B also illustratively show a higher than nominal threshold voltages, V_{TN+}, of the passgate structures according to the invention. Note that the supply voltage decreases as the process dimension decreases. Further note that V_{TN} decreases as the process dimension decreases, whereas V_{TN+} is higher than V_{TN} by a predetermined percentage for various process dimensions (e.g., process dimensions smaller than 0.13μm). Yet further note that a portion of the trends shown in FIGS. 6A and 6B have dashed lines. These dashed lines generally represent anticipated values of voltage, leakage current, and frequency that may be obtained in future process dimensions.

[0039] Referring now specifically to FIG. 6A, the leakage current (line 612) for a transistor having V_{TN} is compared to the leakage current (line 614) for a passgate transistor having V_{TN+} for a given process. Note that for "larger" processes (e.g., greater than 0.13μm processes), the threshold voltage of the passgate structures need not be higher than the nominal threshold voltage. Thus, this is why FIGS. 6A and 6B do not show the V_{TN+} "circles" extending to the far left in the figure. As shown, the leakage current is low for transistors fabricated according to "larger" process dimensions and that have a threshold voltage of V_{TN}. However, as the process dimension decreases, the leakage current for transistors having V_{TN} rises dramatically, whereas the leakage current for transistors having V_{TN+} remains relatively low (i.e., the leakage current is reduced compared to the leakage current experienced by transistors having a nominal threshold voltage).

[0040] Referring now to FIG. 6B, the frequency of transistors having V_{TN} or V_{TN+} and being driven by a nominal voltage or passgate activation voltage are compared. Line 620 represents an "ideal" operational speed attained with transistors having V_{TN} and being driven by a nominal voltage. However, this speed is achieved at the cost of high leakage current, as indicated by line 612 in FIG. 6A. Line 630 represents a speed profile of transistors having V_{TN+}, but is driven with a nominal gate voltage. As shown in FIG. 6B, the speed of line 630 is substantially less than ideal at the smaller process dimensions. However, line 640, which represents the speed of passgate transistors according to the invention have V_{TN+} and are driven by a passgate activation voltage (e.g., a voltage higher than the nominal voltage), substantially matches the ideal speed of line 620, while at the same time benefits from having a relative low leakage current.

[0041] The above-described passgate structures 10/201/40 that may be constructed in accordance with the principles of the present invention are especially useful in integrated circuit devices, such as programmable logic devices, in which such passgate structures are used as interconnection switches to allow programmable routing and switching. FIG. 7 is a simplified block diagram of an illustrative programmable logic device 70 in which interconnection switches using passgate structures that have been constructed in accordance with the principles of the present invention may be readily used. Programmable logic device 70 includes a plurality of regions of programmable logic 710 operatively disposed in a two-

dimensional array of rows and columns, and a programmable network of horizontal 730 and vertical 735 interconnection conductors for conveying signals amongst the logic regions 710 and various I/O structures 780. In the network of interconnection conductors 730/735, signals may be programmably routed via interconnection switches 700, which, in some designs, may also be grouped to form multiplexers. In some embodiments, programmable logic device 70 may also include any of a variety of functional blocks 750, such as memory structures, multiplier/accumulator blocks, arithmetic logic units, microprocessors, etc. Functional blocks 750 may be dedicated structures that are configured to implement a specific function, or, alternatively, they may be user-programmable/ reconfigurable structures.

[0042] FIG. 8 illustrates in greater detail how interconnection switches 700 may be used in the network of interconnection conductors 730/735 to route signals within programmable logic device 70. For the purpose of illustrating the principles of the present invention, a signal source/destination within programmable logic device 70 may be any of the logic regions 710, functional blocks 750, I/O structures 780, or other circuitry within programmable logic device 70. As schematically illustrated in FIG. 8, a signal may be routed from any given source to any given destination by using interconnection switches 700 to multiplex or switch signals provided on the output leads 725 of signal source 710/750/780/etc. onto the network of interconnection conductors 730/735 (within which interconnection switches 700 may also be used to programmably connect one interconnection conductor to

another), from which the signal may be eventually multiplexed or switched onto the input lead 720 of signal destination 710/750/780/etc. As shown in FIG. 8, the electrical characteristics of the network of interconnection conductors 730/735 may be represented as a chain of resistors 820 and capacitors 821a/b in a "black-box" abstraction.

[0043] Also shown in FIG. 8 is one embodiment of an interconnection switch 700 that may be constructed using the above-described enhanced passgate structures in accordance with the principles of the present invention. As illustrated in FIG. 8, interconnection switch 700 may include any of the passgates 10/201/40 as the switching mechanism. In some embodiments, a pair of inverters 801a and 801b, along with a "half-latch" PMOS transistor 802, may also be included to provide buffering of the input and output signals. Half-latch PMOS transistor 802 may be used to recover from the voltage drop across the passgate 10/201/40.

[0044] FIG. 9 shows another embodiment of an interconnection switch 900 that may be constructed using the above-described enhanced passgate structures in accordance with the principles of the present invention. As illustrated in FIG. 9, interconnection switch 900 may include two of passgates 10/201/40 for use as a dual-passgate switching mechanism. If desired, switch 900 may include inverters 901a and 901b to buffer the input and output signals. Half-latch PMOS transistor 910 may be included to compensate for the voltage drop across the dual-passgate switching mechanism. It is understood that interconnection switch 900 can be used in place or intermixed with interconnection switch 700 in FIG. 7.

[0045] FIG. 10 shows a portion of an integrated circuit 1000 employing the use of memory cells 1010 to drive passgate transistors 700/900 according to the principles of the present invention. Memory cells 1010 may be configurable ram cells such as SRAM cells. Passgate transistors 700/900 may be any of the enhanced passgate structures that have been described in the foregoing.

[0046] Also shown in FIG. 10 is a higher than nominal voltage source, V_{ccx}, which is coupled to memory cells 1010. As discussed above, the higher than nominal voltage may be supplied by a separate I/O pin that provides a supply voltage higher than the nominal supply voltage, generated from a charge pump, a voltage leveler, or the like.

[0047] An advantage realized by powering memory cells 1010 with a higher than nominal voltage is that it reduces the potential for soft-error. Soft-error occurs when the logic state being stored in the memory cell inadvertently changes. Soft-error can be caused by, for example, sub-atomic particles (sometimes referred to as alpha particles or neutron beams) that disrupt the operation of silicon by changing the charge of the memory cell. Soft-error can also be caused by cross-coupling of memory cells. As supply voltages (e.g., nominal voltages) continue to decrease, the soft-error-rate increases because the critical charge needed to flip the cell decreases as the supply voltage decreases. Therefore, application of V_{ccx}, as opposed to a nominal voltage, provides a supply voltage that enables memory cells 1010 to operate with a relatively low soft-error-rate.

[0048] Thus, a synergy is created among memory cells 1010 and the passgate transistors 700/900 because V_{CCX} provides voltage sufficient to minimize soft-error and is also sufficient to drive passgate transistors at a predetermined operational speed (i.e., V_{CCX} is at least equal to the passgate activation voltage). That is, memory cells 1010 selectively drive passgate transistors 700/900 by applying the voltage provided by V_{CCX} (e.g., a passgate activation voltage) to the gates of the passgate transistors 700/900. Thus, the advantage of powering memory cells 1010 with higher than nominal voltage prevents inadvertent flipping, while at the same time enables memory cells 1010 to drive passgates 700/900 with the requisite voltage.

[0049] FIG. 11 shows how an integrated circuit device 1190 (e.g., a programmable logic device) employing any of the enhanced passgate structures that have been described in the foregoing may be used in a system 1100. System 1100 may include one or more of the following components: various peripheral devices 1102, I/O circuitry 1103, a processor 1104, and a memory 1105. These components may be coupled together by a system bus 1101 and may be populated on a circuit board 1106 which is contained in an end-user system 1107.

[0050] System 1100 can be used in a wide variety of applications, such as computer networking, data networking, instrumentation, video processing, digital signal processing, or any other application where the advantage of using programmable or reprogrammable logic is desirable. Integrated circuit device 90, employing passgate structures that have been constructed in accordance with the principles of the present

invention, may be used to perform a variety of different logic functions. For example, integrated circuit device 1190 can be configured as a processor or controller that works in cooperation with processor 1104. Integrated circuit device 1190 may also be used as an arbiter for arbitrating access to a shared resource in system 1100. In yet another example, integrated circuit device 1190 may be configured as an interface between processor 1104 and one of the other components in system

[0051] Various technologies may be used to implement the integrated circuit device 1190 employing passgate structures that have been constructed in accordance with the principles of the present invention. Moreover, this invention is applicable to both one-time-only programmable and reprogrammable devices.

[0052] Thus, it is seen that enhanced passgate structures for an integrated circuit device have been presented. One skilled in the art will appreciate that the present invention may be practiced by other than the described embodiments, which are presented for purposes of illustration and not of limitation, and the present invention is limited only by the claims which follow.

What is Claimed is:

1. A programmable logic device, comprising:

an array of logic blocks;

a plurality of interconnect lines;

a plurality of switches for programmably routing logic signals between the logic blocks over the interconnect lines, wherein the switches include passgate transistors having threshold voltages that are higher than the threshold voltages of other transistors in the programmable logic device, and wherein the passgate transistors are selectively activated with a passgate activation voltage that is higher than the voltages being applied to the other transistors in the programmable logic device.

2. The programmable logic device defined in claim 1 further comprising a plurality of memory cells that are powered with a memory cell supply voltage that is equal to or greater than the passgate activation voltage.

3. The programmable logic device defined in claim 2, wherein the memory cells selectively provide the passgate activation voltage to the passgate transistors.

4. The programmable logic device defined in claim 2, wherein the memory cells are SRAM cells.

5. The programmable logic device defined in claim 2, wherein the memory cell supply voltage is provided by a level-shifter, a charge pump, a reference voltage generator, a voltage divider circuit, or an input/output pin on the programmable logic device.

6. The programmable logic device defined in claim 1, wherein at least one of the passgate transistors is fabricated to have said threshold voltage that is higher than the threshold voltage of the other transistors.

7. The programmable logic device defined in claim 1, wherein at least one of the passgate transistors is a semiconductor transistor comprising a gate well region and a connection for biasing the gate well region with respect to other regions of the semiconductor transistor, thereby setting a threshold voltage to a voltage level higher than the threshold voltage non-pass-gate transistors.

8. The programmable logic device defined in claim 1, wherein the passgate transistors are NMOS transistors.

9. A digital processing system comprising:

processing circuitry;

a system memory coupled to the processing circuitry; and

the programmable logic device defined in claim 1 coupled to the processing circuitry and the system memory.

10. A printed circuit board on which is mounted the programmable logic device defined in claim 1.

11. An integrated circuit, comprising:

a first set of transistors having a nominal threshold voltage, each transistor of said

first set being selectively activated with a nominal voltage; and

a set of passgate transistors having a passgate threshold voltage that is higher than the nominal threshold voltage by a predetermined percentage, each passgate transistor being selectively activated with a passgate activation voltage that exceeds the nominal voltage.

12. The integrated circuit defi ned in claim 11, wherein said predetermined percentage ranges from about one percent to about two hundred percent.

13. The integrated circuit defined in claim 11, wherein said predetermined percentage ranges from about five percent to about forty percent.

14. Th e integrated circuit defined in claim 11, wherein said predetermined percentage ranges from about ten percent to about thirty-five percent.

15. The integrated circuit defined in claim 11, wherein said predetermined percentage ranges from about fifteen percent to about thirty percent.

16. The integrated circuit defined in claim 11, wherein said nominal voltage is a supply voltage provided to the integrated circuit.

17. The integrated circuit defined in claim 11 further comprising a passgate activation voltage source that provides the passgate activation voltage.

18. The integrated circuit defined in claim 17, wherein the passgate activation voltage

source is provided by a level-shifter, a charge pump, a reference voltage generator, a voltage divider circuit, or an input/output pin on the integrated circuit.

19. The integrated circuit defined in claim 11 further comprising:

at least one memory cell that is being powered with a memory cell supply voltage that is equal to or greater than the passgate activation voltage, said at least one memory cell is coupled to at least one of the passgate transistors and is operative to selectively provide the passgate activation voltage to at least one passgate transistor.

20. The integrated circu it defined in claim 19, wherein the memory cell is an SRAM cell.

21. The integrated circuitry defined in claim 11, wherein said passgate transistors are NMOS transistors.

22. The integrated circuitry defined in claim 11 further comprising:

an array of logic blocks;

a plurality of interconnect lines; and

a plurality of switches for programmably routing logic signals between the logic blocks over the interconnect lines, wherein each switch includes at least one of the passgate transistors.

23. A digital processing system comprising:

processing circuitry;

a system memory coupled to the processing circuitry; and

the integrated circuit defined in claim 11 coupled to the processing circuitry and the system memory.

24. A printed circ uit board on which is mounted the integrated circuit defined in claim 11.

25. The printed circuit board defined in claim 24 further comprising:

a board memory mounted on the printed circuit board and coupled to the integrated circuit device.

26. The printed cir cuit board defined in claim 25 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the integrated circuit device.

27. A programmable logic device, comprising:

a high voltage power source that provides a voltage higher than a low voltage being supplied to the programmable logic device;

a configurable memory cell that is coupled to the high voltage power source;

a passgate transistor having a gate, input, and output terminals, the gate terminal is coupled to the configurable memory cell, the passgate transistor has a threshold voltage that is higher than the threshold voltage of other transistors in the programmable logic device, and the passgate transistor is selectively activated with the application of the high voltage to the gate terminal.

28. The programmable logic device of claim 28, wherein the configurable memory cell is an SRAM cell.

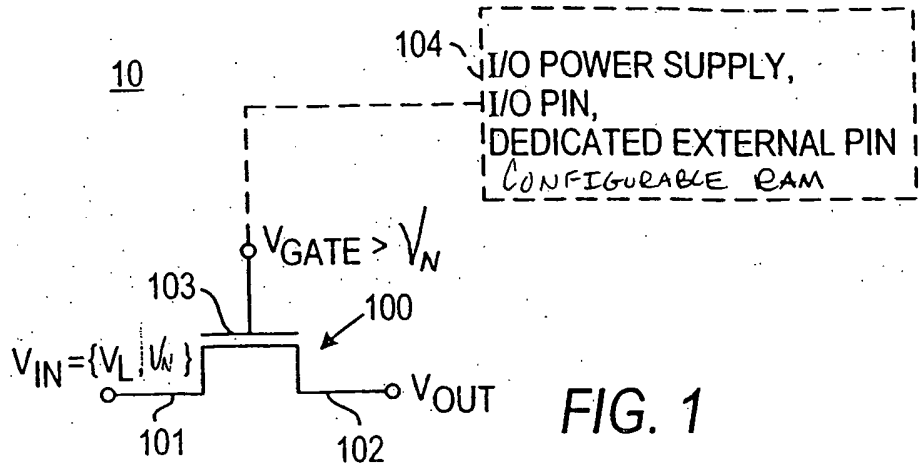

FIG. 1

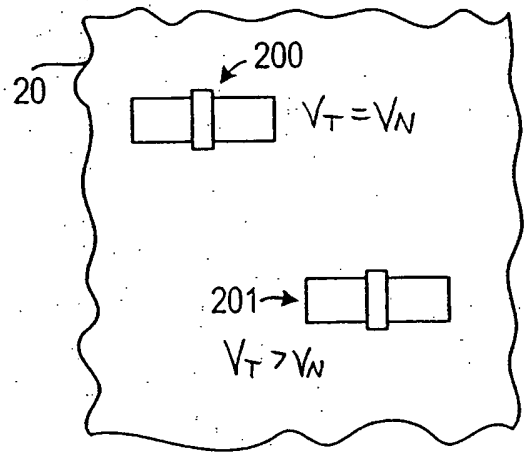

FIG. 2

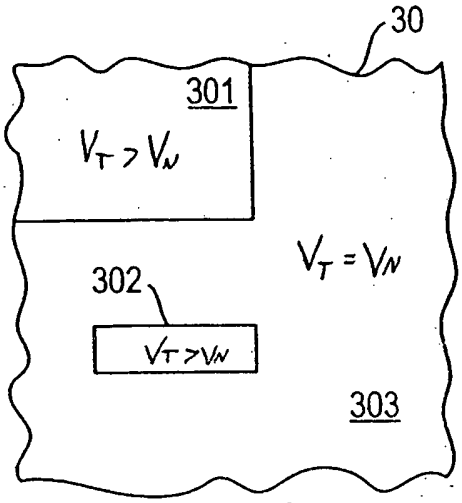

FIG. 3

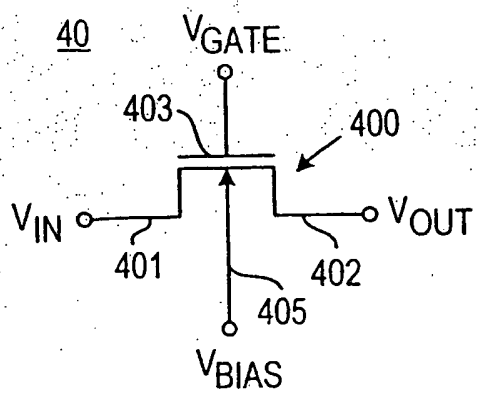

FIG. 4

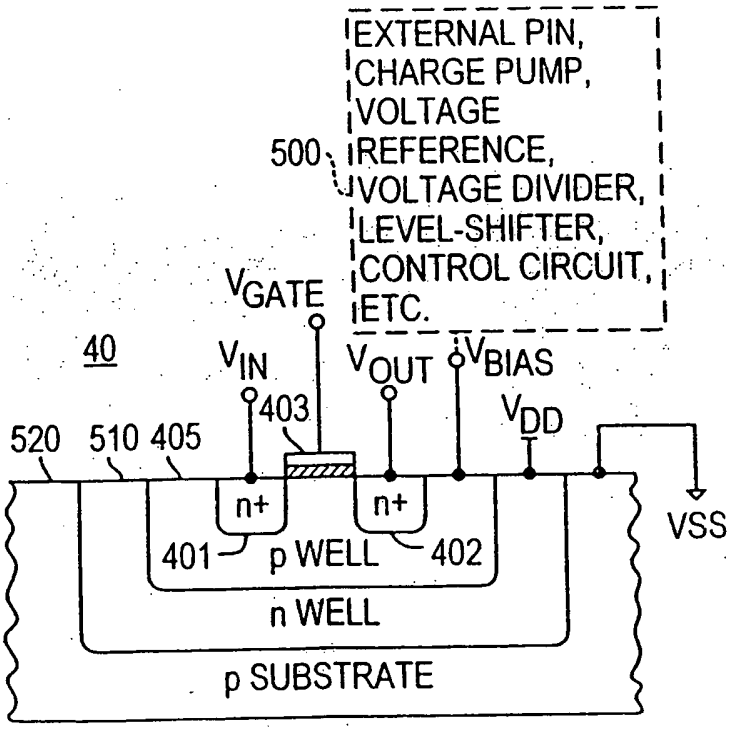

FIG. 5

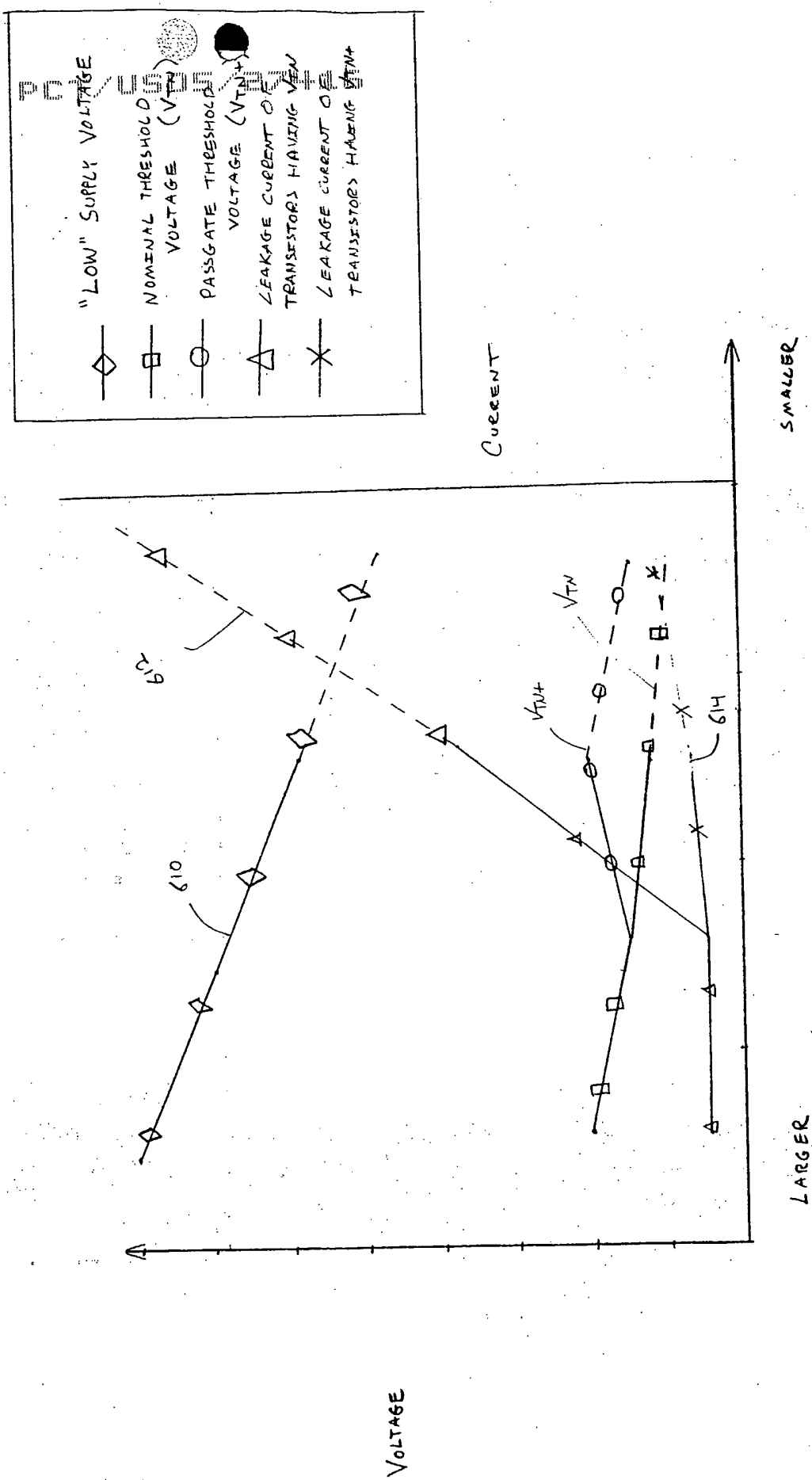
"LOW" SUPPLY VOLTAGE
NOMINAL THRESHOLD VOLTAGE (V_{TN})
PASSGATE THRESHOLD VOLTAGE (V_{TN+})
LEAKAGE CURRENT OF TRANSISTORS HAVING V_{TN}
LEAKAGE CURRENT OF TRANSISTORS HAVING V_{TN+}
CURRENT
SMALLER
LARGER
PROCESS DIMENSION
VOLTAGE
612
610
V_{TN}
V_{TN+}
614

FIG. 6A

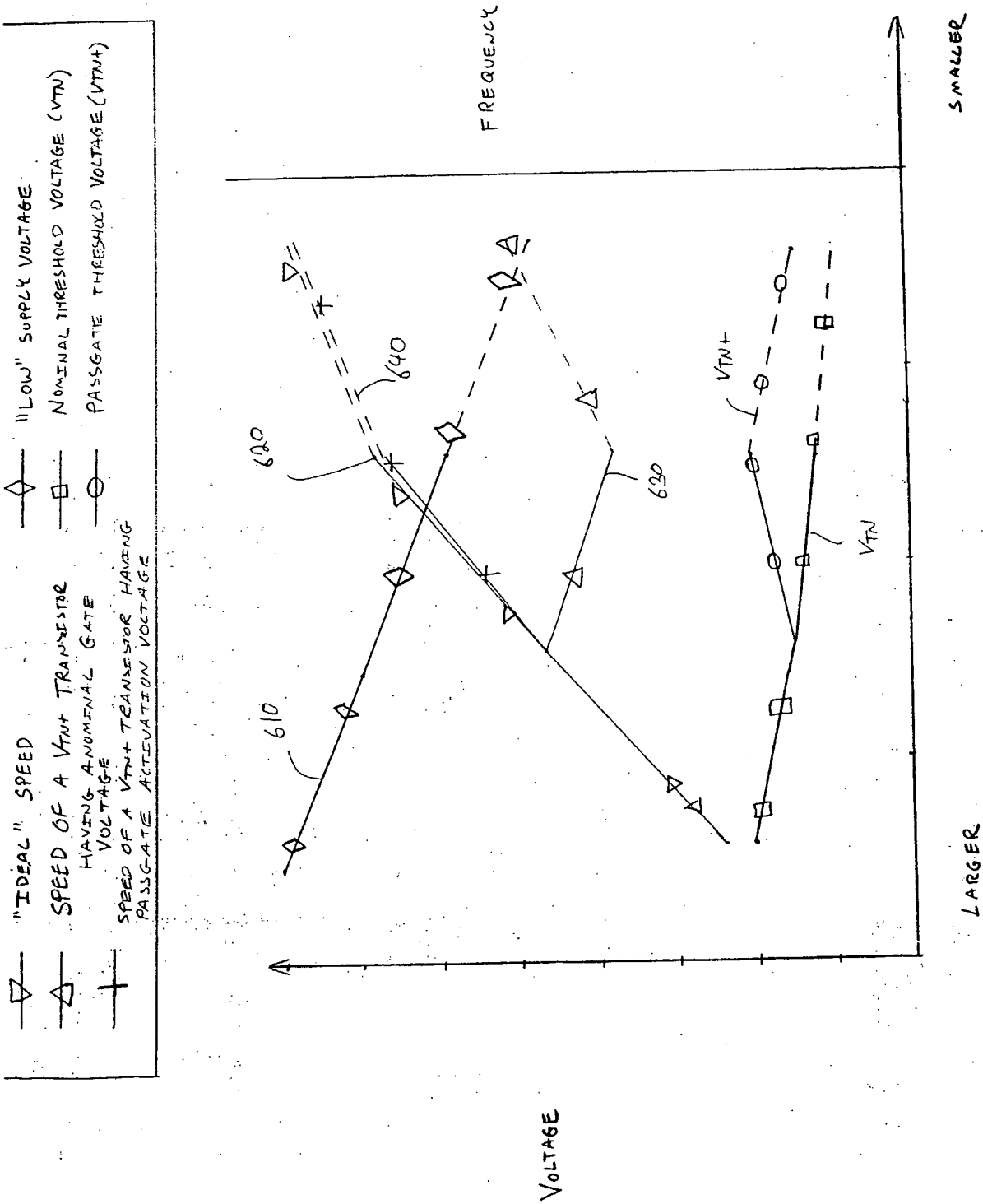
"IDEAL" SPEED
SPEED OF A VTNT TRANSISTOR HAVING ANOMENAL GATE VOLTAGE
SPEED OF A VTNT TRANSISTOR HAVING PASSGATE ACTIVATION VOLTAGE
"LOW" SUPPLY VOLTAGE
NOMINAL THRESHOLD VOLTAGE (VTN)
PASSGATE THRESHOLD VOLTAGE (VTNT)
610
620
630
640
VTNT
VTN
FREQUENCY
VOLTAGE
LARGER
SMALLER
PROCESS DIMENSION

FIG. 6B

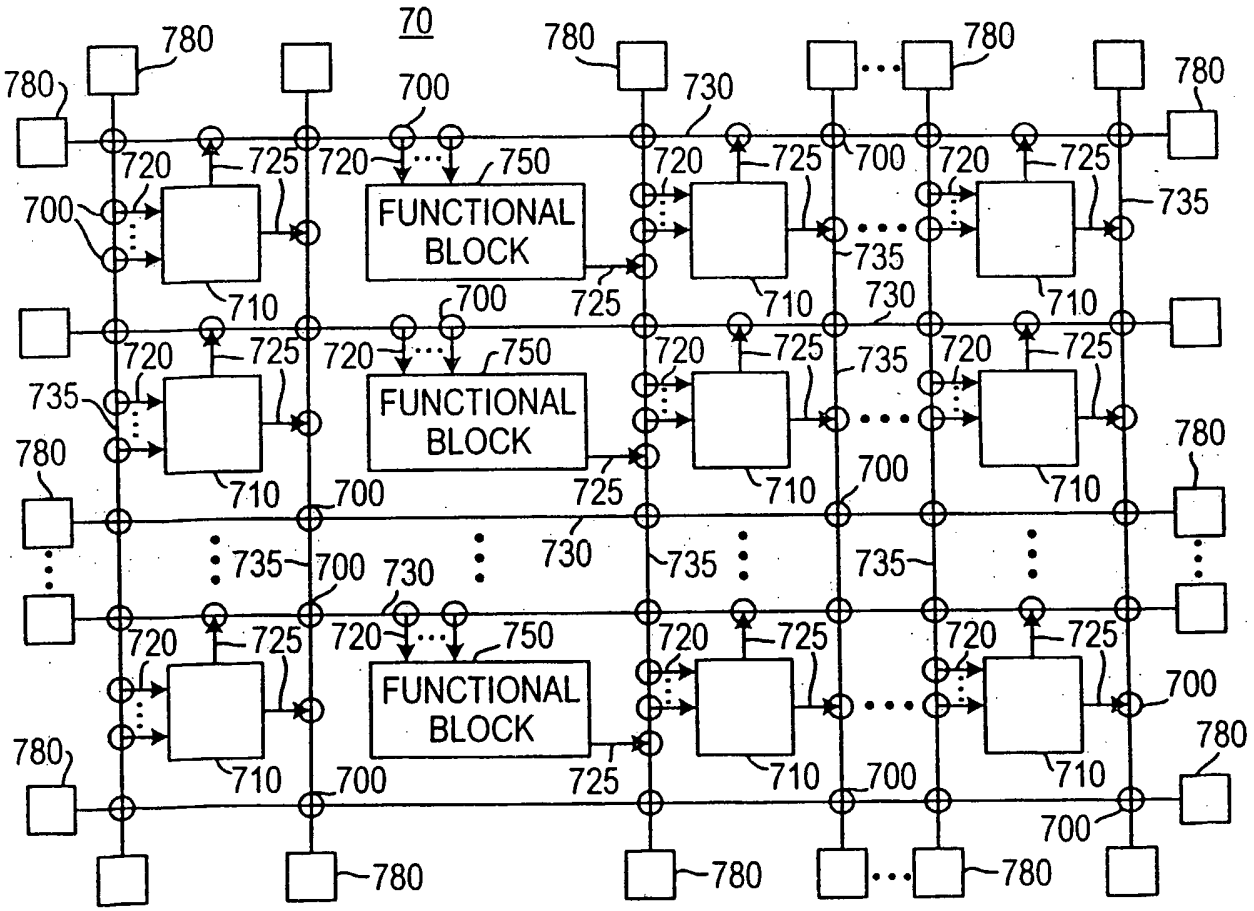

FIG. 7

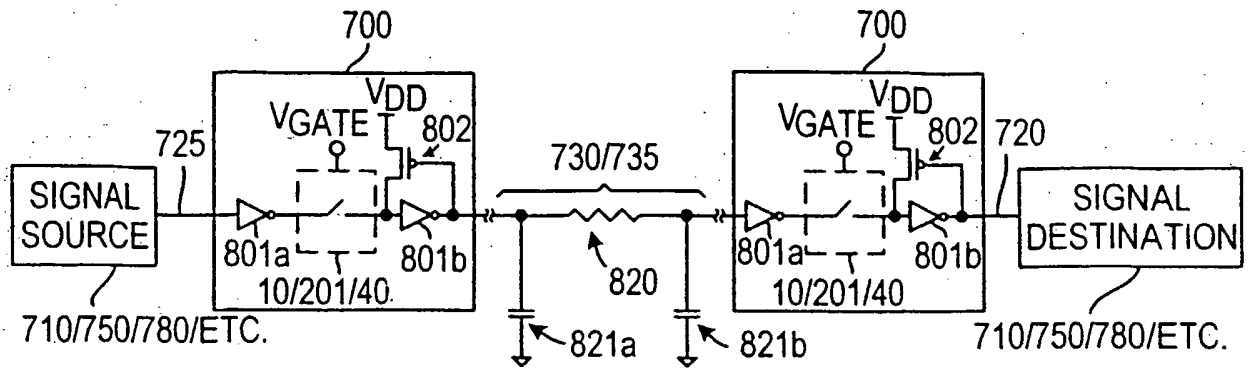
700
700
VDD
VGATE
802
VDD
VGATE
802
725
730/735
720
SIGNAL SOURCE
801a
801b
10/201/40
820
801a
801b
10/201/40
SIGNAL DESTINATION
710/750/780/ETC.
821a
821b
710/750/780/ETC.

FIG. 8

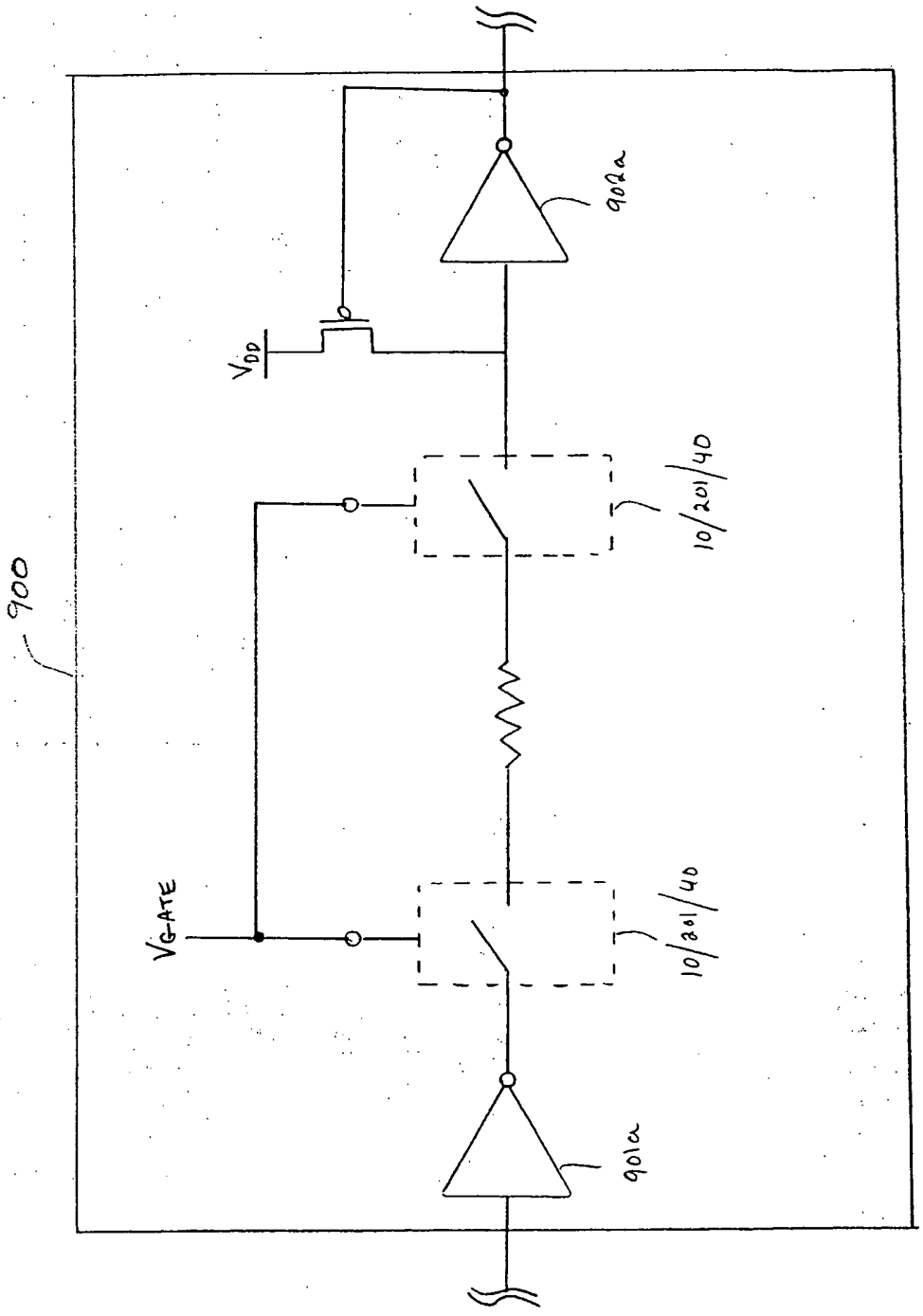

FIG. 9

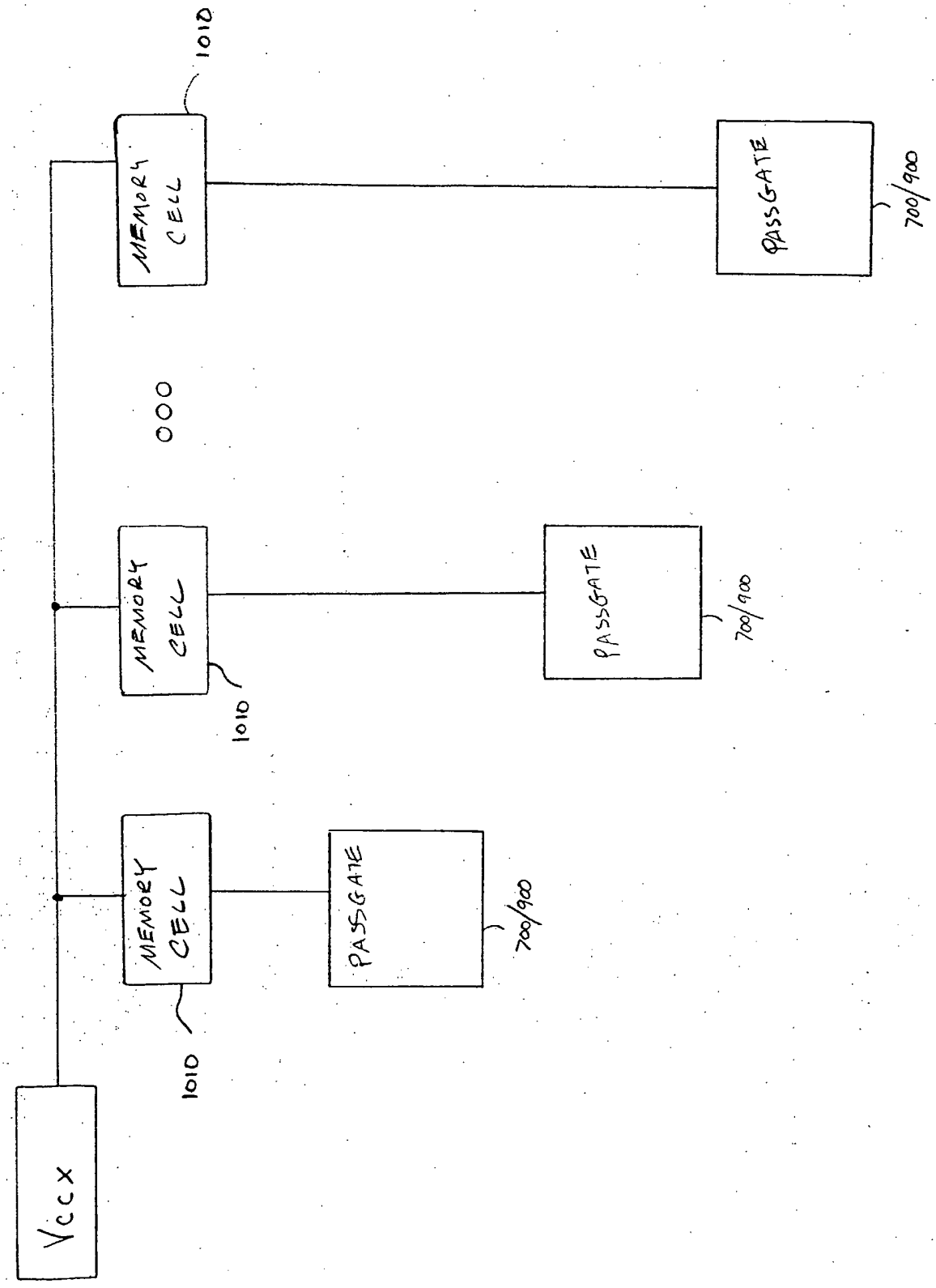

FIG. 10

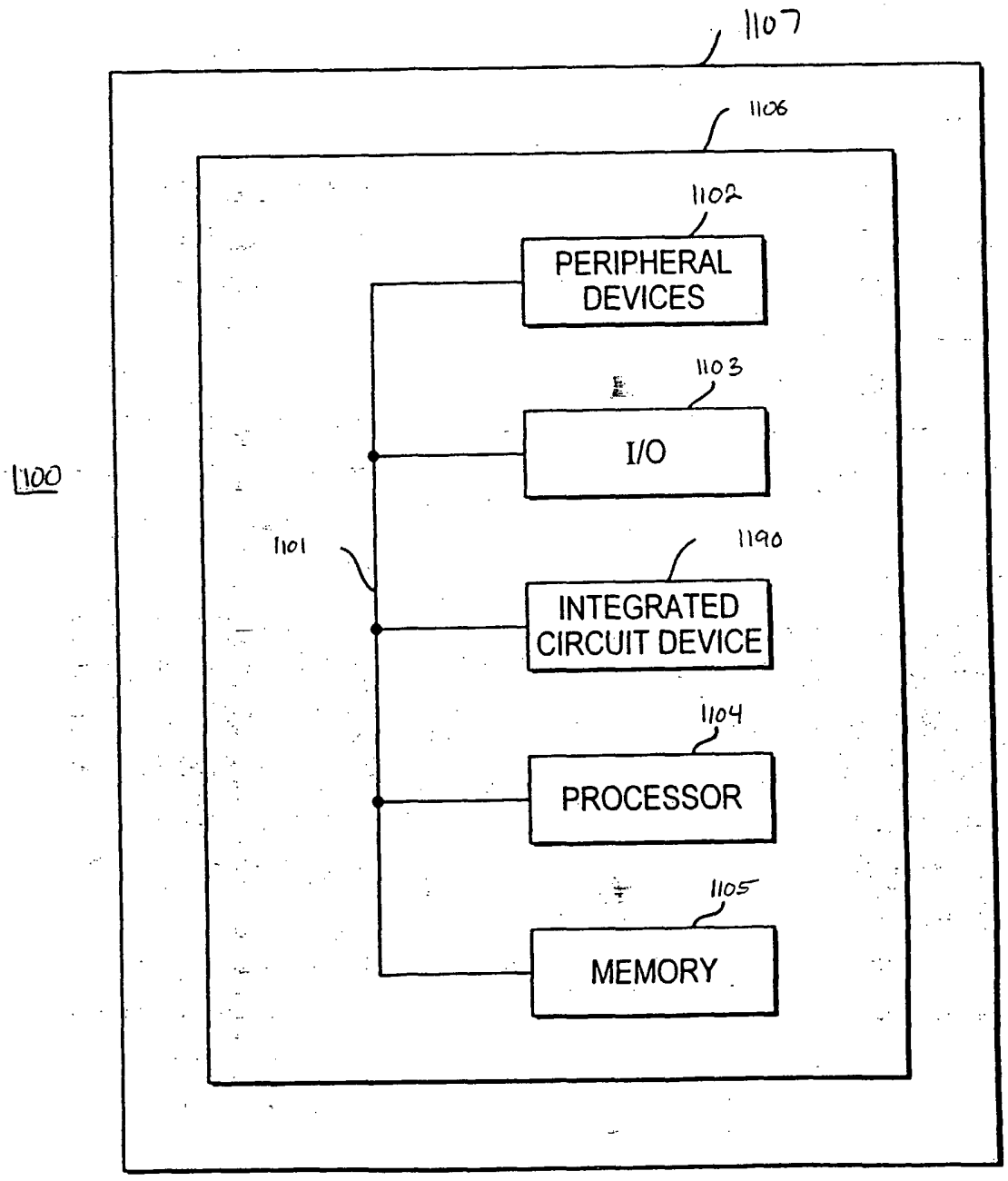
1107
1106
1102
PERIPHERAL DEVICES
1103
I/O
1100
1101
1190
INTEGRATED CIRCUIT DEVICE
1104
PROCESSOR
1105
MEMORY

FIG. 11

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2005/027416

A. CLASSIFICATION OF SUBJECT MATTER
H03K19/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No
X Y	US 2003/053335 A1 (HART MICHAEL J ET AL) 20 March 2003 (2003-03-20) abstract; figures 1a,1b,2a,2g,3,8 paragraphs '0002!, '0013!, '0015!, '0019!, '0025!, '0040!, '0044!, '0072!, '0073!	1-10 11-18, 20-24, 26-28
X X A	US 2003/071681 A1 (FUJIMORI YOSHIKAZU) 17 April 2003 (2003-04-17) abstract; figures 1,3 paragraphs '0001!, '0003!, '0005!, '0007!, '0008!, '0047!	1,6-8 11-15, 17,21,22 27

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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'A' document defining the general state of the art which is not considered to be of particular relevance

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'O' document referring to an oral disclosure, use, exhibition or other means

'P' document published prior to the international filing date but later than the priority date claimed

'T' later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

'X' document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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'&' document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 January 2006	25/01/2006

Name and mailing address of the ISA	Authorized officer
European Patent Office, P B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Mesic, M

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No
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A	BETZ ET AL: "FPGA ROUTING ARCHITECTURE: SEGMENTATION AND BUFFERING TO OPTIMIZE SPEED AND DENSITY" 21 February 1999 (1999-02-21), ACM/SIGDA INTERNATIONAL SYMPOSIUM ON FIELD PROGRAMMABLE GATE ARRAYS. FPGA '99. MONTEREY, CA, FEBRUARY 21 - 23, 1999, NEW YORK, NY : ACM, US, PAGE(S) 59-68 , XP000868479 ISBN: 1-58113-088-0 abstract; figures 1,2,5,9a,9b page 60, right-hand column, line 41 - line 50 page 66, left-hand column, line 22 - line 29 page 67, right-hand column, line 22 - line 23	1-5,27, 28
A	DOBBELAERE I ET AL: "REGENERATIVE FEEDBACK REPEATERS FOR PROGRAMMABLE INTERCONNECTIONS" November 1995 (1995-11), IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE SERVICE CENTER, PISCATAWAY, NJ, US, PAGE(S) 1246-1253 , XP000553062 ISSN: 0018-9200 page 1246, left-hand column, line 5 - line 17; figures 1,9 page 1248, left-hand column, paragraph 3A - lines 12-14 page 1249, left-hand column, paragraph 3B - lines 1-10 page 1249, right-hand column, paragraph 3D - lines 7-12	1,4,6,8, 11-16, 20-22, 27,28
A	US 5 880 620 A (GITLIN ET AL) 9 March 1999 (1999-03-09) abstract; figures 1a,1b,2 column 1 column 6, line 39 - line 41	1,7, 11-15,27

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2005/027416

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,X P,A	WO 2005/013490 A (KONINKLIJKE PHILIPS ELECTRONICS N.V; KRISHNAN, ROHINI; PINEDA DE GYVEZ) 10 February 2005 (2005-02-10) abstract; figures 1,4,5a,5b,6 claims 1-7	1,6-8, 11-17, 21,22 27
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US2005/027416

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		WO 03025804 A2	27-03-2003
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		US 2004174187 A1	09-09-2004
		US 2005040851 A1	24-02-2005
		WO 2004079909 A2	16-09-2004