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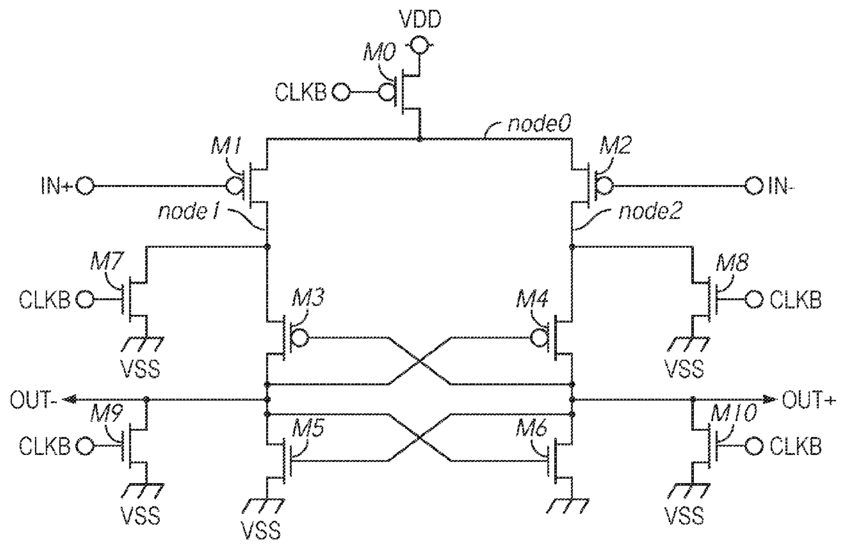

FIG. 1
(Prior Art)

(57) Abstract: Apparatuses for receiving an input signal in a semiconductor device are described. An example apparatus includes: a first amplifier that provides first and second intermediate voltages responsive to first and second input voltages; first and second voltage terminals; a circuit node; a first transistor coupled between the first voltage terminal and the circuit node and is turned on responsive to at least one of the first and second intermediate voltages; a second amplifier including first and second inverters, at least one of the first and second inverters being coupled between the circuit node and the second voltage terminal; and first and second output nodes, the first output node being coupled to an input node of the first inverter and an output node of the second inverter, and the second output node being coupled to an output node of the first inverter and an input node of the second inverter.

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INPUT BUFFER CIRCUIT

BACKGROUND

[001] High data reliability, high speed of memory access, and reduced chip size are features that are demanded from semiconductor memory.

[002] In recent years, there has been an effort to increase access speed while reducing power consumption for semiconductor devices. As part of that effort to increase access speed, it may be desirable to include input receiver circuits having faster operation in input buffers for receiving address signals, command signals and clock signals. Simultaneously, it may be desirable to accommodate a wide range of input signals at the input receiver circuits to meet recent semiconductor devices (e.g., low-power double data rate synchronous DRAM). For example, Low Power Double Data Rate 4 (LPDDR4) specification (JESD209-4) specifies that an data input reference voltage (V_{REF}) operating point range from 10% to 42% of a power supply voltage for data input (V_{DD}). Along these lines, an input receiver circuit including differential amplifiers have been developed. For example, a data latch type input buffer has been used as an input buffer for memory devices (e.g., LPDDR4). A data latch type input (DQ) buffer in a memory device amplifies a data signal and latches the data signal by amplifying a voltage difference between the data input signal and the V_{REF} when a clock signal CLK is at a logic high level, and initializes each node in the DQ buffer by precharging each node when the clock signal CLK is at a logic low level. The DQ input buffer performs a sequence of amplification and latch operation responsive to a signal input and a precharge operation in turn during each clock cycle. Source nodes of input transistors may receive a power supply voltage V_{DD} and gate nodes of the input transistors coupled to input nodes (IN+ node and IN- node) may receive a data input signal DQ and the reference voltage V_{REF}, respectively while performing the sequence of amplification and latch operation. However, the input transistors may not be driven fast enough due to a smaller V_{GS} of the input transistors M1 and M2, if a voltage of the data input signal DQ and the reference voltage V_{REF} become higher (e.g., V_{REF}=42% * V_{DD}).

[003] Fig. 1 is a circuit diagram of a conventional data input buffer circuit. The conventional data input buffer circuit includes a first amplifier including transistors M1, M2, M3, M4, M5 and M6. A transistor M0 is a switch of the first amplifier. A

data input signal DQ is provided to an IN+ node coupled to a gate of the transistor M1. The reference voltage V_{REF} is provided to an IN- node coupled to a gate of the transistor M2. A sequence of amplification and latch operation are executed, when an inverted clock signal CLKB is at a logic low level that activates the transistor M0 and deactivates transistors M7–M10. The power supply voltage V_{DD} is provided to nodes, (node1 and node 2) through transistors M1 and M2, and voltages of the nodes (node1 and node2) are increased from a precharge level V_{SS} responsive to the inverted clock signal CLKB is at the logic low level, depending on the data input signal DQ. Thus, a voltage difference Vdiff between the nodes (node1 and node2) may be caused based on a difference between a voltage of the input data input signal DQ and the reference voltage V_{REF}. Because the power supply voltage V_{DD} is provided to nodes, (node1 and node 2), voltages at an OUT- node and an OUT+ node may be increased from the precharge level V_{SS} through transistors M3 and M4 respectively, when the voltage difference Vdiff exceeds a threshold voltage VTh of the transistor M3 or a threshold voltage VTh of the transistor M4. Due to voltages of the node1 and the node2 that are increased up to approximately the power supply voltage V_{DD}, the first amplifier latches a voltage difference between the OUT- node and the OUT+ node of the first amplifier, and a logic high level signal (V_{DD}) is provided to one of the OUT- node and the OUT+ node and a logic low level signal (V_{SS}) is provided to the other of the OUT- node and the OUT+ node. In a precharge operation, when the inverted clock signal CLKB is at a logic high level, the nodes node1, node2, OUT- and OUT+ are precharged by precharge transistors M7, M8, M9 and M10 to the a logic low level signal (V_{SS}). An increase of the voltage of the node1 above the threshold VTh of the transistor M3 drives capacitors (not shown) related to the transistor M1 and capacitors coupled to the OUT- node, (e.g., capacitors at gates of the transistors M4 and M6, a channel capacitor of the transistor M3 and a drain capacitor of the transistor M5), and a total capacitance of these capacitors is remarkably large. Similarly, a total capacitance of capacitors related to the transistor M2 is large. Accordingly, a time to increase voltages of the nodes (node1 and node2) around the power supply voltage VDD and to complete the sequence of amplification and latch operation to increase voltages at an OUT- node and an OUT+ node is longer when the data input signal DQ and the reference voltage V_{REF}

are higher, and the sequence of amplification and latch operation may not be completed by a precharge operation in the data input buffer circuit.

[004] Fig. 2 is a circuit diagram of a conventional data input buffer circuit. The conventional data input buffer circuit includes a first amplifier and a second amplifier. The first amplifier includes transistors M1 and M2. The second amplifier includes transistors M12, M13, M14, M15, M16 and M17. A transistor M0 is a switch of the first amplifier and a transistor M11 is a switch of the second amplifier. A sequence of amplification and latch operation are executed, when a clock signal CLK is at a logic high level and an inverted clock signal CLKB is at a logic low level. Responsive to a difference in voltage increase speeds between nodes (node1 and node2) at gates of transistors M12 and M13, the second amplifier latches a data signal and a signal at a logic low level (V_{SS}) is provided to one of an OUT- node and an OUT+ node, and a precharge level (V_{DD}) is provided to the other outputted at the other of OUT- and OUT+. In the precharge operation, node1 and node2 are set to a logic low level (V_{SS}), and the OUT- node and the OUT+ node are precharged to the power supply voltage V_{DD} responsive to the transistors M12 and M13 receiving the logic low level signal of the node1 and node2 at gates and coupling the power supply voltage V_{DD} to the OUT- node and the OUT+ node. Since each of the transistors M1 and M2 includes a MOS capacitor having a capacitance smaller than a MOS capacitor in each of the transistors M1 and M2 of Fig. 1, voltages of node1 and node2 are increased faster than the voltages of node1 and node2 of Fig. 1. However, the second amplifier may complete a latch operation before a voltage difference between node1 and node2 is to be generated, if a voltage of the data input signal DQ and the reference voltage V_{REF} become higher (e.g., V_{REF}=42% * V_{DD}). Thus, an activation of the second amplifier needs to be delayed. On the other hand, if the voltage of the data input signal DQ and the reference voltage V_{REF} become lower, the voltages of node1 and node2 are increased too fast due to larger V_{GS} of the transistors M1 and M2, and the voltages of node1 and node2 reach to approximately the power supply voltage V_{DD} and the voltage difference disappears before the second amplifier completes the amplification, which causes a data latching failure.

BRIEF DESCRIPTION OF THE DRAWINGS

[005] Fig. 1 is a circuit diagram of a conventional data input buffer circuit.

[006] Fig. 2 is a circuit diagram of a conventional data input buffer circuit.

[007] Fig. 3 is a block diagram of a semiconductor device in accordance with the present disclosure.

[008] Fig. 4 is a schematic diagram of an input/output circuit including data input circuits in accordance with an embodiment of the present disclosure.

[009] Fig. 5 is a circuit diagram of an input buffer circuit according to an embodiment of the present disclosure.

[010] Fig. 6 is a circuit diagram of an input buffer circuit according to an embodiment of the present disclosure.

[011] Fig. 7 is a circuit diagram of an input buffer circuit according to an embodiment of the present disclosure.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[012] Various embodiments of the present disclosure will be explained below in detail with reference to the accompanying drawings. The following detailed description refers to the accompanying drawings that show, by way of illustration, specific aspects and embodiments in which the present invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the present invention. Other embodiments may be utilized, and structure, logical and electrical changes may be made without departing from the scope of the present invention. The various embodiments disclosed herein are not necessary mutually exclusive, as some disclosed embodiments can be combined with one or more other disclosed embodiments to form new embodiments.

[013] Fig. 3 is a block diagram of a semiconductor device in accordance with an embodiment of the present disclosure. The semiconductor device 10 may be an LPDDR4 SDRAM integrated into a single semiconductor chip, for example. The semiconductor device 10 may be mounted on an external substrate 2 that is a memory module substrate, a mother board or the like. As shown in Fig. 3, the semiconductor device 10 includes a memory cell array 11. The memory cell array 11 includes a

plurality of banks, each bank including a plurality of word lines WL, a plurality of bit lines BL, and a plurality of memory cells MC arranged at intersections of the plurality of word lines WL and the plurality of bit lines BL. The selection of the word line WL is performed by a row decoder 12 and the selection of the bit line BL is performed by a column decoder 13. Sense amplifiers 18 are coupled to corresponding bit lines BL and connected to local I/O line pairs LIOT/B. Local IO line pairs LIOT/B are connected to main IO line pairs MIOT/B via transfer gates TG 19 which function as switches.

[014] Turning to the explanation of a plurality of external terminals included in the semiconductor device 10, the plurality of external terminals includes address terminals 21, command terminals 22, clock terminals 23, data terminals 24 and power supply terminals 25 and 26. The data terminals 24 may be coupled to output buffers for read operations of memories. Alternatively, the data terminals 24 may be coupled to input buffers for read/write access of the memories that will be later described. Fig. 3 shows an example of dynamic random access memory (DRAM), however, any device having external terminals for signal input/output may be included as the external terminals of embodiments of the present disclosure.

[015] The address terminals 21 are supplied with an address signal ADD and a bank address signal BADD. The address signal ADD and the bank address signal BADD supplied to the address terminals 21 are transferred via an address input circuit 31 to an address decoder 32. The address decoder 32 receives the address signal ADD and supplies a decoded row address signal XADD to the row decoder 12, and a decoded column address signal YADD to the column decoder 13. The address decoder 32 also receives the bank address signal BADD and supplies the bank address signal BADD to the row decoder 12 and the column decoder 13.

[016] The command terminals 22 are supplied with a command signal COM. The command signal COM may include one or more separate signals. The command signal COM input to the command terminals 21 is input to a command decoder 34 via the command input circuit 33. The command decoder 34 decodes the command signal COM to generate various internal command signals. For example, the internal commands may include a row command signal to select a word line and a column command signal, such as a read command or a write command, to select a bit line.

[017] Accordingly, when a read command is issued and a row address and a column address are timely supplied with the read command, read data is read from a memory cell MC in the memory cell array 11 designated by these row address and column address. The read data DQ is output externally from the data terminals 24 via a read/write amplifier 15 and an input/output (IO) circuit 17. Similarly, when the write command is issued and a row address and a column address are timely supplied with the write command, and then write data DQ is supplied to the data terminals 24, the write data DQ is supplied via the input/output circuit 17 and the read/write amplifier 15 to the memory cell array 11 and written in the memory cell MC designated by the row address and the column address. The input/output circuit 17 may include input buffers, according to one embodiment. The clock terminals 23 are supplied with external clock signals CLK and CLKB, respectively. These external clock signals CLK and CLKB are complementary to each other and are supplied to the input/output circuit 17. The input/output circuit 17 receives the external clock signals CLK and CLKB that are used as a timing signal for determining input timing of write data DQ and output timing of read data DQ.

[018] The power supply terminals 25 are supplied with power supply potentials VDD and VSS. These power supply potentials VDD and VSS are supplied to a voltage generator 39. The voltage generator 39 may generate various internal potentials VPP, VOD, VARY, VPERI, and the like based on the power supply potentials VDD and VSS. The internal potential VPP may be mainly used in the row decoder 12, the internal potentials VOD and VARY may be mainly used in the sense amplifiers 18 included in the memory cell array 11, and the internal potential VPERI may be used in many other circuit blocks.

[019] Power supply potentials VDDQ and VSSQ are supplied to the input/output circuit 17. The power supply potentials VDDQ and VSSQ may be the same potentials as the power supply potentials VDD and VSS that are supplied to the power supply terminals 25, respectively. However, the dedicated power supply potentials VDDQ and VSSQ may be used for the input/output circuit 17 so that power supply noise generated by the input/output circuit 17 does not propagate to the other circuit blocks.

[020] Fig. 4 is a schematic diagram of an input/output circuit 17 including data input circuits according to an embodiment of the present disclosure. The input/output circuit

17 includes data terminals 424 including a data strobe terminal DQS, a complementary data strobe terminal DQSB and a plurality of data terminals DQ0 – DQn where "n+1" is the number of the plurality of data terminals. A data strobe signal is used for capturing data at high data rates. The input/output circuit 17 also includes a data strobe (DQS) input circuit 170, a plurality of data input circuits 417 and a plurality of latch circuits 416 respective to the plurality of data terminals. The plurality of data input circuits 417 may be any data input circuit included in an input/output circuit 17 as will be described in Figs. 5–7. The plurality of data input circuits 417 receive a reference voltage (VREF) and respective data the respective data terminals 424, and provide output signals. Each latch circuit 416 receives a data strobe signal from the DQS input circuit 170 and the respective output signal from the respective data input circuit for capturing the data.

[021] Fig. 5 is a circuit diagram of an apparatus including an input buffer circuit 5 according to an embodiment of the present disclosure. The input buffer circuit 5 may be included in the input/output circuit 17 of Figs. 3 and 4 in some embodiments. The input buffer circuit 5 may include an input node IN+ that may receive a data input signal DQ, such as one of the write data that is supplied to the data terminals 24 in Fig. 3, and a reference node IN- supplied with a reference voltage (VREF). The input buffer circuit 5 may include amplifiers 511 and 512. The amplifier 511 may include transistors 51 and 52. The transistor 51 may be coupled between a node 530 and a node 531. The transistor 51 includes a gate coupled to the input node IN+. The transistor 52 may be coupled between the node 530 and a node 532. The transistor 52 includes a gate coupled to the reference node IN-. The node 530 may be a power supply node that is supplied with a power supply potential VDD from one of the power supply terminals 25 in Fig. 3 to the transistors 51 and 52, responsive to an inverted clock signal CLKB received at a gate of a transistor 50 that may function as a voltage switch for the amplifier 511. The amplifier 511 may provide intermediate voltages on the nodes 531 and 532 responsive to a voltage of the data input signal DQ and the reference voltage VREF via the transistors 51 and 52, respectively.

[022] The input buffer circuit 5 may include a transistor 518 between a power supply node that is supplied with the power supply potential VDD from the one of the power supply terminals 25 in Fig. 3 and a node 535 (e.g., a circuit node). The input buffer

circuit 5 may include a control circuit 515 that may include transistors 522 and 523 between the amplifiers 511 and 512. The transistors 522 and 523 includes gates that receive intermediate voltages on the nodes 531 and 532, respectively. For each of the transistors 522 and 523, one of a source or a drain may be coupled to a node 534 that is coupled to a gate of the transistor 518. Thus, the gate of the transistor 518 may be turned on by a voltage at the node 534 that may be responsive to at least the one of intermediate voltages on the nodes 531 and 532 via the transistors 522 and 523. The input buffer circuit 5 may include a transistor 53 that may include one of source and drain supplied with one of the intermediate voltages on the node 531 and the other of source and drain coupled to an output node OUT-. A gate of the transistor 53 may be coupled to an output node OUT+. The input buffer circuit 5 may include a transistor 54 that may include one of source and drain supplied with the other of the intermediate voltages on the node 532 and the other of source and drain coupled to the output node OUT+. A gate of the transistor 54 may be coupled to the output node OUT-.

[023] The amplifier 512 may include inverters 513 and 514. The transistor 518 may function as a voltage switch for the amplifier 512. For example, the inverter 513 may be coupled between the node 535 and a power supply potential VSS from the other of the power supply terminals 25 in Fig. 3, and may include different types of transistors 55 and 519. The inverter 514 may be coupled between the node 535 and a power supply potential VSS from the other of the power supply terminals 25 in Fig. 3, and may include different types of transistors 56 and 520. For example, types of the transistors 55 and 56 may be the same and types of the transistors 519 and 520 may be the same. For example, the transistor 519 may be coupled between the node 535 and the output node OUT-. The transistor 519 may include a gate coupled to the output node OUT+. The transistor 520 may be coupled between the node 535 and the output node OUT+. The transistor 520 may include a gate coupled to the output node OUT-. The node 535 may be a power supply node that is supplied with the power supply potential VDD from the one of the power supply terminals 25 in Fig. 3 to the transistors 519 and 520, via the transistor 518 responsive to the voltage of the node 534 as earlier described. In other words, the output node OUT- may be coupled to an input node of the inverter 514 corresponding to the gates of the transistors 520 and 56, and an output node of the inverter 513 corresponding to either sources or drains of the transistors 519

and 55. Similarly, the output node OUT+ may be coupled to an input node of the inverter 513 corresponding to the gates of the transistors 519 and 55 and an output node of the inverter 514 corresponding to either sources or drains of the transistors 520 and 56.

[024] A sequence of amplification and latch operation may be executed, when an inverted clock signal CLKB is at a logic low level that activates the transistor 50 and deactivates transistors 57, 58, 59 and 510. The power supply voltage VDD is provided to nodes, 531 and 532 through the transistors 51 and 52, and voltages of the nodes 531 and 532 are increased from a precharge level VSS responsive to the inverted clock signal CLKB is at the logic low level, depending on the data input signal DQ. Thus, a voltage difference Vdiff between the nodes 531 and 532 may be caused based on a difference between a voltage of the input data input signal DQ and the reference voltage VREF. Because the power supply voltage VDD may be provided to the nodes 531 and 532, voltages of the output nodes OUT- and OUT+ may be increased from the precharge level VSS through transistors 53 and 54 respectively, when the voltages of the nodes 531 and 532 exceed the threshold voltage VTh of the transistor 53 and a threshold voltage VTh of the transistor 54 respectively. Either the transistor 522 or the transistor 523 may be turned on to change a voltage of the node 534 from VDD to VSS and may activate the amplifier 512 by turning on the transistor 518 upon detecting either the voltage of the node 531 or the voltage of the node 532 exceeding the threshold voltage VTh of the transistors 53 or 54. Because the transistors 519 and 520 may receive the power supply voltage VDD via the transistor 518, driving currents of the transistors 519 and 520 of the amplifier 512 may be unaffected by the voltages of the data input signal DQ and the reference voltage VREF. Thus, the amplifier 512 may complete the sequence of amplification and latch operation and may provide the voltages of the output nodes OUT- and OUT+ by configuring the driving currents to be large, without waiting for the voltages of the nodes 531 and 532 to reach to approximately the power supply voltage VDD. In a precharge operation, the node 534 may be precharged to the power supply voltage VDD by a transistor 521.

[025] Fig. 6 is a circuit diagram of an input buffer circuit 6 according to an embodiment of the present disclosure. The input buffer circuit 6 may be included in the input/output circuit 17 of Figs. 3 and 4 in some embodiments. The input buffer circuit 6 may include an input node IN+ that may receive a data input signal DQ, such as one of the write data that is supplied to the data terminals 24 in Fig. 3, and a reference node IN- supplied with a reference voltage (VREF). The input buffer circuit 6 may include amplifiers 611 and 612. The amplifier 611 may include transistors 61 and 62. The transistor 61 may be coupled between a node 630 and a node 631. The transistor 61 includes a gate coupled to the input node IN+. The transistor 62 may be coupled between the node 630 and a node 632. The transistor 62 includes a gate coupled to the reference node IN-. The node 630 may be a power supply node that is supplied with a power supply potential VDD from one of the power supply terminals 25 in Fig. 3 to the transistors 61 and 62, responsive to an inverted clock signal CLKB received at a gate of a transistor 60 that may function as a voltage switch for the amplifier 611. The amplifier 611 may provide intermediate voltages on the nodes 631 and 632 responsive to a voltage of the data input signal DQ and the reference voltage VREF via the transistors 61 and 62, respectively.

[026] The input buffer circuit 6 may include a transistor 618 between a power supply node that is supplied with the power supply potential VDD from the one of the power supply terminals 25 in Fig. 3 and a node 635 (e.g., a circuit node). The input buffer circuit 6 may include a control circuit 615 that may include transistors 622 and 623 between the amplifiers 611 and 612. The transistors 622 and 623 includes gates that receive intermediate voltages on the nodes 631 and 632, respectively. For each of the transistors 622 and 623, one of a source or a drain may be coupled to a node 634 that is coupled to a gate of the transistor 618. Thus, the gate of the transistor 618 may be activated by a voltage of the node 634 that may be responsive to at least the one of intermediate voltages on the nodes 631 and 632 via the transistors 622 and 623.

[027] The amplifier 612 may include inverters 613 and 614. The transistor 618 may function as a voltage switch for the amplifier 612. For example, the inverter 613 may be coupled between the node 635 and a power supply potential VSS from the other of the power supply terminals 25 in Fig. 3, and may include different types of transistors 616 and 619. The inverter 614 may be coupled between the node 635 and a power supply potential VSS from the other of the power supply terminals 25 in Fig. 3, and may include different types of transistors 617 and 620. For example, types of the transistors 616 and 617 may be the same and types of the transistors 619 and 620 may

be the same. For example, the transistor 619 may be coupled between the node 635 and an output node OUT-. The transistor 619 may include a gate coupled to an output node OUT+. The transistor 620 may be coupled between the node 635 and the output node OUT+. The transistor 620 may include a gate coupled to the output node OUT-. The node 635 may be a power supply node that is supplied with the power supply potential VDD from the one of the power supply terminals 25 in Fig. 3 to the transistors 619 and 620, via the transistor 618 responsive to the voltage of the node 634 as earlier described. In other words, the output node OUT- may be coupled to an input node of the inverter 614 corresponding to the gates of the transistors 620 and 617, and an output node of the inverter 613 corresponding to either sources or drains of the transistors 619 and 616. Similarly, the output node OUT+ may be coupled to an output node of the inverter 614 corresponding to the gates of the transistors 619 and 616 and an input node of the inverter 613 corresponding to either sources or drains of the transistors 620 and 617.

[028] The input buffer circuit 6 may include a switch 626 between the amplifiers 611 and 612. For example, the switch may include transistors 624 and 625. The transistor 624 may be coupled between the node 631 and the output node OUT-. The transistor 625 may be coupled between the node 632 and the output node OUT+. Gates of the transistors 624 and 625 of the switch 626 may be coupled to one of a source or a drain of each of the transistors 622 and 623 in the control circuit 615, respectively. Thus, the switch 626 may couple the node 631 to the output node OUT- and may couple the node 632 to the output node OUT+, responsive to the voltage on the node 634.

[029] A sequence of amplification and latch operation may be executed, when an inverted clock signal CLKB is at a logic low level that activates the transistor 60 and deactivates transistors 67, 68, 69 and 610. The power supply voltage VDD is provided to nodes, 631 and 632 through the transistors 61 and 62, and voltages of the nodes 631 and 632 are increased from a precharge level VSS responsive to the inverted clock signal CLKB is at the logic low level, depending on the data input signal DQ. Thus, a voltage difference Vdiff between the nodes 631 and 632 may be caused based on a difference between a voltage of the input data input signal DQ and the reference voltage VREF, when the voltages of the node 631 or the node 632 coupled to gates of the transistor 622 or the transistor 623 exceeds the threshold voltage VTh of the

transistor 622 or the threshold voltage VTh of the transistor 623, respectively. Thus, the transistors 622 and 623 in the control circuit 615 may be activated, respectively. A voltage of the node 634 may decrease from the power supply voltage VDD to the power supply voltage VSS, responsive to either the activate transistor 622 or the activated transistor 623. As a result, the decrease of the voltage of the node 634 may activate the transistor 618 and may deactivate the transistors 624 and 625. For example, the transistors 624 and 625 may be deactivated when a higher one of the voltages of the output nodes OUT- and OUT+ becomes a threshold voltage Vt, and the voltage difference Vdiff between the nodes 631 and 632 may be suitable for the amplifying operation. The output nodes OUT- and OUT+ may hold the voltages of the nodes 631 and 632 until the transistors 624 and 625 are deactivated. The voltage difference Vdiff between the nodes 631 and 632 may be maintained until the deactivation of the transistors 624 and 625 and may be amplified and latched by the amplifier 612 responsive to the deactivation of the transistors 624 and 625 due to the decrease of the voltage of the node 634. Thus, the amplifier 612 may start the sequence of amplification and latch operation regardless of the voltage of data input signal DQ and the reference voltage VREF.

[030] Fig. 7 is a circuit diagram of an input buffer circuit 7 according to an embodiment of the present disclosure. The input buffer circuit 7 may be included in the input/output circuit 17 of Figs. 3 and 4 in some embodiments. The input buffer circuit 7 may include an input node IN+ that may receive a data input signal DQ, such as one of the write data that is supplied to the data terminals 24 in Fig. 3, and a reference node IN- supplied with a reference voltage (VREF). The input buffer circuit 7 may include amplifiers 711 and 712. The amplifier 711 may include transistors 71 and 72. The transistor 71 may be coupled between a node 730 and a node 731. The transistor 71 includes a gate coupled to the input node IN+. The transistor 72 may be coupled between the node 730 and a node 732. The nodes 731 and 732 may be isolated from each other, via transistors 716 and 717. The transistor 72 includes a gate coupled to the reference node IN-. The node 730 may be a power supply node that is supplied with a power supply potential VDD from one of the power supply terminals 25 in Fig. 3 to the transistors 71 and 72, responsive to an inverted clock signal CLKB received at a gate of a transistor 70 that may function as a voltage switch for the amplifier 711.

The amplifier 711 may provide intermediate voltages on the nodes 731 and 732 responsive to a first input voltage of the data input signal DQ and a second input voltage (e.g., the reference voltage VREF) via the transistors 71 and 72, respectively.

[031] The amplifier 712 may include inverters 718 and 719. The inverter 718 may include a transistor 714 and the transistor 716. The inverter 719 may include a transistor 715 and the transistor 717. For example, the inverter 718 may be coupled between a node 733 (e.g., a circuit node) and the power supply potential VDD from the one of the power supply terminals 25 in Fig. 3, and may include different types of transistors 714 and 716. The inverter 719 may be coupled between a node 734 (e.g., a circuit node) and the power supply potential VDD from the one of the power supply terminals 25 in Fig. 3, and may include different types of transistors 715 and 717. For example, types of the transistors 714 and 715 may be the same and types of the transistors 716 and 717 may be the same. For example, the transistor 716 may be coupled between the node 733 and an output node OUT+. The transistor 716 may include a gate coupled to an output node OUT-. For example, the transistor 717 may be coupled between the node 734 and the output node OUT-. The transistor 717 may include a gate coupled to the output node OUT+.

[032] A voltage switch 720 may include transistors 726 and 727. The transistors 726 and 727 have gates that may receive the intermediate voltages on the node 731 and 732, respectively. Thus, the transistors 726 and 727 may be activated (e.g., turned on) responsive to the intermediate voltages on the node 731 and 732, respectively. The nodes 733 and 734 may be power supply nodes that are supplied with a power supply potential VSS from the other of the power supply terminals 25 in Fig. 3 to the transistors 716 and 717, via the transistors 726 and 727 responsive to the intermediate voltages of the nodes 731 and 732 as earlier described. In other words, the output node OUT- may be coupled to an input node of the inverter 718 corresponding to the gates of the transistors 714 and 716, and an output node of the inverter 719 corresponding to either sources or drains of the transistors 715 and 717. Similarly, the output node OUT+ may be coupled to an input node of the inverter 719 corresponding to the gates of the transistors 715 and 717, and an output node of the inverter 718 corresponding to either sources or drains of the transistors 714 and 716.

[033] A sequence of amplification and latch operation may be executed, when an inverted clock signal CLKB is set to a logic low level that activates the transistor 70, transistors 77 and 78 coupled between the power supply voltage VSS and the nodes 731 and 732, respectively. Simultaneously, a clock signal CLKT is set to a logic high level that deactivates transistors 728 and 729, coupled between the power supply voltage VDD and the output nodes OUT+ and OUT-, respectively. The power supply voltage VDD is provided to nodes, 731 and 732 through the transistors 71 and 72, and voltages of the nodes 731 and 732 are increased from a precharge level VSS responsive to the inverted clock signal CLKB is at the logic low level, depending on the data input signal DQ. Thus, a voltage difference Vdiff between the nodes 731 and 732 may be caused based on a difference between a voltage of the input data input signal DQ and the reference voltage VREF, when the voltages of the nodes 731 and 732 exceed the threshold voltage VTh of the transistor 726 or the threshold voltage VTh of the transistor 727. Because the transistors 71 and 72 may activate the transistors 726 and 727 by driving gate capacitors of the transistors 726 and 727 respectively, the intermediate voltages of the nodes 731 and 732 may increase quickly after the inversed clock signal CLKB is set to the logic low level. Thus the amplifier 712 may complete the sequence of amplification and latch operation by the activation of the transistors 726 and 727, when the voltage of the node 731 or the voltage of the node 732 exceeds the threshold voltage VTh of the transistor 726 or the threshold voltage VTh of the transistor 727, respectively. Thus, the amplifier 712 may start the sequence of amplification and latch operation regardless of the voltage of data input signal DQ and the reference voltage VREF. In the precharge operation, the output nodes OUT- and OUT+ may be precharged to the power supply voltage VDD by the transistors 728 and 729.

[034] Logic levels of signals used in the embodiments described the above are merely examples. However, in other embodiments, combinations of the logic levels of signals other than those specifically described in the present disclosure may be used without departing from the scope of the present disclosure.

[035] Although this invention has been disclosed in the context of certain preferred embodiments and examples, it will be understood by those skilled in the art that the inventions extend beyond the specifically disclosed embodiments to other alternative

embodiments and/or uses of the inventions and obvious modifications and equivalents thereof.

[036] It is also contemplated that various combination or sub-combination of the specific features and aspects of the embodiments may be made and still fall within the scope of the inventions. It should be understood that various features and aspects of the disclosed embodiments can be combined with or substituted for one another in order to form varying mode of the disclosed invention.

[037] In an embodiment of the disclosure, an apparatus includes a first amplifier configured to provide first and second intermediate voltages responsive to first and second input voltages, first and second voltage terminals, and a circuit node. A first transistor is coupled between the first voltage terminal and the circuit node and configured to be turned on responsive to at least one of the first and second intermediate voltages. A second amplifier includes first and second inverters, at least one of the first and second inverters being coupled between the circuit node and the second voltage terminal. A first output node is coupled to an input node of the first inverter and an output node of the second inverter. A second output node is coupled to an output node of the first inverter and an input node of the second inverter.

[038] Additionally or alternatively, further included are an additional circuit node and a second transistor coupled between the first voltage terminal and the additional circuit node, wherein the first inverter is coupled between the circuit node and the second voltage terminal, and wherein the first transistor is configured to be turned on responsive to the first intermediate voltage and the second transistor is configured to be turned on responsive to the second intermediate voltage.

[039] Additionally or alternatively, the circuit node and the additional circuit node are isolated from each other.

[040] Additionally or alternatively, the second amplifier is configured to be activated responsive to either the first intermediate voltage exceeding a threshold voltage of the first transistor or the second intermediate voltage exceeding a threshold voltage of the second transistor.

[041] Additionally or alternatively, further included is a control circuit including a second transistor having a gate supplied with one of the first and second intermediate voltages and one of a source and a drain coupled to a gate of the first transistor.

[042] Additionally or alternatively, further included are a control circuit including a second transistor having a gate supplied with the first intermediate voltage and one of a source and a drain coupled to a gate of the first transistor, and a third transistor having a gate supplied with the second intermediate voltage and one of a source and a drain coupled to the gate of the first transistor.

[043] Additionally or alternatively, further included are a fourth transistor having one of a source and a drain supplied with the first intermediate voltage and an other of the source and the drain coupled to the first output node, and a fifth transistor having one of a source and a drain supplied with the second intermediate voltage and an other of the source and the drain coupled to the second output node.

[044] Additionally or alternatively, the fourth transistor has a gate coupled to the second output node and the fifth transistor has a gate coupled to the first output node.

[045] Additionally or alternatively, the fourth transistor has a gate coupled to the one of the source and the drain of the second transistor and the fifth transistor has a gate coupled to the one of the source and the drain of the third transistor.

[046] Additionally or alternatively, the fourth and fifth transistors are configured to be deactivated when a voltage of the first output node or the second output node exceeds a threshold voltage of the fourth transistor and the fifth transistor.

[047] In another aspect of the disclosure, an apparatus includes a first amplifier configured to receive a first input voltage and a second input voltage and further configured to provide a first intermediate voltage on a first node and a second intermediate voltage on a second node. A first voltage switch is configured to provide a first power supply voltage from a first power terminal to the first amplifier responsive to a clock signal. A second voltage switch is configured to provide the first power supply voltage responsive to the first intermediate voltage and the second intermediate voltage. A second amplifier is configured to provide at least one output signal responsive to the first power supply voltage from the second voltage switch.

[048] Additionally or alternatively, the first input voltage is provided as a data input signal and the second input voltage is a reference voltage.

[049] Additionally or alternatively, further included is a first transistor including a gate configured to receive the first intermediate voltage, the first transistor configured to change a voltage of a third node from the first power supply voltage to a second

power supply voltage responsive to the first intermediate voltage, wherein the first voltage switch comprises a transistor including a gate coupled to the third node.

[050] Additionally or alternatively, further included is a second transistor including a source and a drain, wherein one of the source and the drain is coupled to the first node and an other of the source and the drain is coupled to an output node, wherein the first transistor is configured to change the voltage of the third node responsive to the first intermediate voltage exceeding a threshold voltage of the second transistor.

[051] Additionally or alternatively, further included is a second transistor including a gate configured to receive the second intermediate voltage, configured to change the voltage of the third node from the first power supply voltage to the second power supply voltage, responsive to the second intermediate voltage

[052] Additionally or alternatively, further included are a third transistor including a source and a drain, wherein one of the source and the drain is coupled to the first node and an other of the source and the drain is coupled to a first output node, a fourth transistor including a source and a drain, wherein one of the source and the drain is coupled to the second node and an other of the source and the drain is coupled to a second output node, wherein the first transistor is configured to change the voltage of the third node responsive to the first intermediate voltage exceeding a threshold voltage of the third transistor, and wherein the second transistor is configured to change the voltage of the third node responsive to the second intermediate voltage exceeding a threshold voltage of the fourth transistor.

[053] Additionally or alternatively, the third transistor and the fourth transistor have gates coupled to the third node, and wherein the third and fourth transistors are configured to be deactivated when a voltage of the first output node or the second output node exceeds a threshold voltage of the third transistor and the fourth transistor.

[054] In another aspect of the disclosure an apparatus includes a first voltage switch configured to provide a first power supply voltage from a first power terminal to the first amplifier responsive to a clock signal. A first amplifier is configured to receive a first input voltage and a second input voltage and further configured to provide a first intermediate voltage on a first node and a second intermediate voltage on a second node. A second voltage switch is configured to provide a second power supply voltage from a second power terminal responsive to the first intermediate voltage and the

second intermediate voltage. A second amplifier configured to provide at least one output signal responsive to the second power supply voltage from the second voltage switch.

[055] Additionally or alternatively, the first input voltage is provided as a data input signal and the second input voltage is a reference voltage.

[056] Additionally or alternatively, the second voltage switch includes a first transistor and a second transistor, wherein a gate of the first transistor is configured to receive the first intermediate voltage, and wherein a gate of the second transistor is configured to receive the second intermediate voltage.

[057] Additionally or alternatively, the second amplifier further includes a first inverter coupled between the first transistor and the first power terminal, and a second inverter coupled between the second transistor and the first power terminal.

[058] Additionally or alternatively, the second amplifier is configured to be activated responsive to either the first intermediate voltage exceeding a threshold voltage of the first transistor or the second intermediate voltage exceeding a threshold voltage of the second transistor.

[059] Other modifications which are within the scope of this invention will be readily apparent to those of skill in the art based on this disclosure. Thus, it is intended that the scope of at least some of the present invention herein disclosed should not be limited by the particular disclosed embodiments described above.

CLAIMS

What is claimed is:

1. An apparatus comprising:

a first amplifier configured to provide first and second intermediate voltages responsive to first and second input voltages;

first and second voltage terminals;

a circuit node;

a first transistor coupled between the first voltage terminal and the circuit node and configured to be turned on responsive to at least one of the first and second intermediate voltages;

a second amplifier comprising first and second inverters, at least one of the first and second inverters being coupled between the circuit node and the second voltage terminal; and

first and second output nodes, the first output node being coupled to an input node of the first inverter and an output node of the second inverter, and the second output node being coupled to an output node of the first inverter and an input node of the second inverter.

2. The apparatus of claim 1, further comprising:

an additional circuit node; and

a second transistor coupled between the first voltage terminal and the additional circuit node,

wherein the first inverter is coupled between the circuit node and the second voltage terminal, and

wherein the first transistor is configured to be turned on responsive to the first intermediate voltage and the second transistor is configured to be turned on responsive to the second intermediate voltage.

3. The apparatus of claim 2, wherein the circuit node and the additional circuit node are isolated from each other.

4. The apparatus of claim 2, wherein the second amplifier is configured to be activated responsive to either the first intermediate voltage exceeding a threshold voltage of the first transistor or the second intermediate voltage exceeding a threshold voltage of the second transistor.

5. The apparatus of claim 1, further comprising a control circuit including a second transistor having a gate supplied with one of the first and second intermediate voltages and one of a source and a drain coupled to a gate of the first transistor.

6. The apparatus of claim 1, further comprising a control circuit including:

a second transistor having a gate supplied with the first intermediate voltage and one of a source and a drain coupled to a gate of the first transistor; and

a third transistor having a gate supplied with the second intermediate voltage and one of a source and a drain coupled to the gate of the first transistor.

7. The apparatus of claim 6, further comprising:

a fourth transistor having one of a source and a drain supplied with the first intermediate voltage and an other of the source and the drain coupled to the first output node; and

a fifth transistor having one of a source and a drain supplied with the second intermediate voltage and an other of the source and the drain coupled to the second output node.

8. The apparatus of claim 7, wherein the fourth transistor has a gate coupled to the second output node and the fifth transistor has a gate coupled to the first output node.

9. The apparatus of claim 7, wherein the fourth transistor has a gate coupled to the one of the source and the drain of the second transistor and the fifth transistor has a gate coupled to the one of the source and the drain of the third transistor.

10. The apparatus of claim 9, wherein the fourth and fifth transistors are configured to be deactivated when a voltage of the first output node or the second output node exceeds a threshold voltage of the fourth transistor and the fifth transistor.

11. An apparatus comprising:

a first amplifier configured to receive a first input voltage and a second input voltage and further configured to provide a first intermediate voltage on a first node and a second intermediate voltage on a second node;

a first voltage switch configured to provide a first power supply voltage from a first power terminal to the first amplifier responsive to a clock signal;

a second voltage switch configured to provide the first power supply voltage responsive to the first intermediate voltage and the second intermediate voltage; and

a second amplifier configured to provide at least one output signal responsive to the first power supply voltage from the second voltage switch.

12. The apparatus of claim 11, wherein the first input voltage is provided as a data input signal and the second input voltage is a reference voltage.

13. The apparatus of claim 11, further comprising:

a first transistor including a gate configured to receive the first intermediate voltage, the first transistor configured to change a voltage of a third node from the first power supply voltage to a second power supply voltage responsive to the first intermediate voltage,

wherein the first voltage switch comprises a transistor including a gate coupled to the third node.

14. The apparatus of claim 13, further comprising:

a second transistor including a source and a drain, wherein one of the source and the drain is coupled to the first node and an other of the source and the drain is coupled to an output node, wherein the first transistor is configured to change the voltage of the third node responsive to the first intermediate voltage exceeding a threshold voltage of the second transistor.

15. The apparatus of claim 13, further comprising:

a second transistor including a gate configured to receive the second intermediate voltage, configured to change the voltage of the third node from the first power supply voltage to the second power supply voltage, responsive to the second intermediate voltage

16. The apparatus of claim 15, further comprising:

a third transistor including a source and a drain, wherein one of the source and the drain is coupled to the first node and an other of the source and the drain is coupled to a first output node;

a fourth transistor including a source and a drain, wherein one of the source and the drain is coupled to the second node and an other of the source and the drain is coupled to a second output node,

wherein the first transistor is configured to change the voltage of the third node responsive to the first intermediate voltage exceeding a threshold voltage of the third transistor, and

wherein the second transistor is configured to change the voltage of the third node responsive to the second intermediate voltage exceeding a threshold voltage of the fourth transistor.

17. The apparatus of claim 16, wherein the third transistor and the fourth transistor have gates coupled to the third node, and

wherein the third and fourth transistors are configured to be deactivated when a voltage of the first output node or the second output node exceeds a threshold voltage of the third transistor and the fourth transistor.

18. An apparatus comprising:

a first voltage switch configured to provide a first power supply voltage from a first power terminal to the first amplifier responsive to a clock signal;

a first amplifier configured to receive a first input voltage and a second input voltage and further configured to provide a first intermediate voltage on a first node and a second intermediate voltage on a second node;

a second voltage switch configured to provide a second power supply voltage from a second power terminal responsive to the first intermediate voltage and the second intermediate voltage; and

a second amplifier configured to provide at least one output signal responsive to the second power supply voltage from the second voltage switch.

19. The apparatus of claim 18, wherein the first input voltage is provided as a data input signal and the second input voltage is a reference voltage.

20. The apparatus of claim 18, wherein the second voltage switch includes a first transistor and a second transistor,

wherein a gate of the first transistor is configured to receive the first intermediate voltage, and

wherein a gate of the second transistor is configured to receive the second intermediate voltage.

21. The apparatus of claim 20, wherein the second amplifier further includes:

a first inverter coupled between the first transistor and the first power terminal; and

a second inverter coupled between the second transistor and the first power terminal.

22. The apparatus of claim 20, wherein the second amplifier is configured to be activated responsive to either the first intermediate voltage exceeding a threshold voltage of the first transistor or the second intermediate voltage exceeding a threshold voltage of the second transistor.

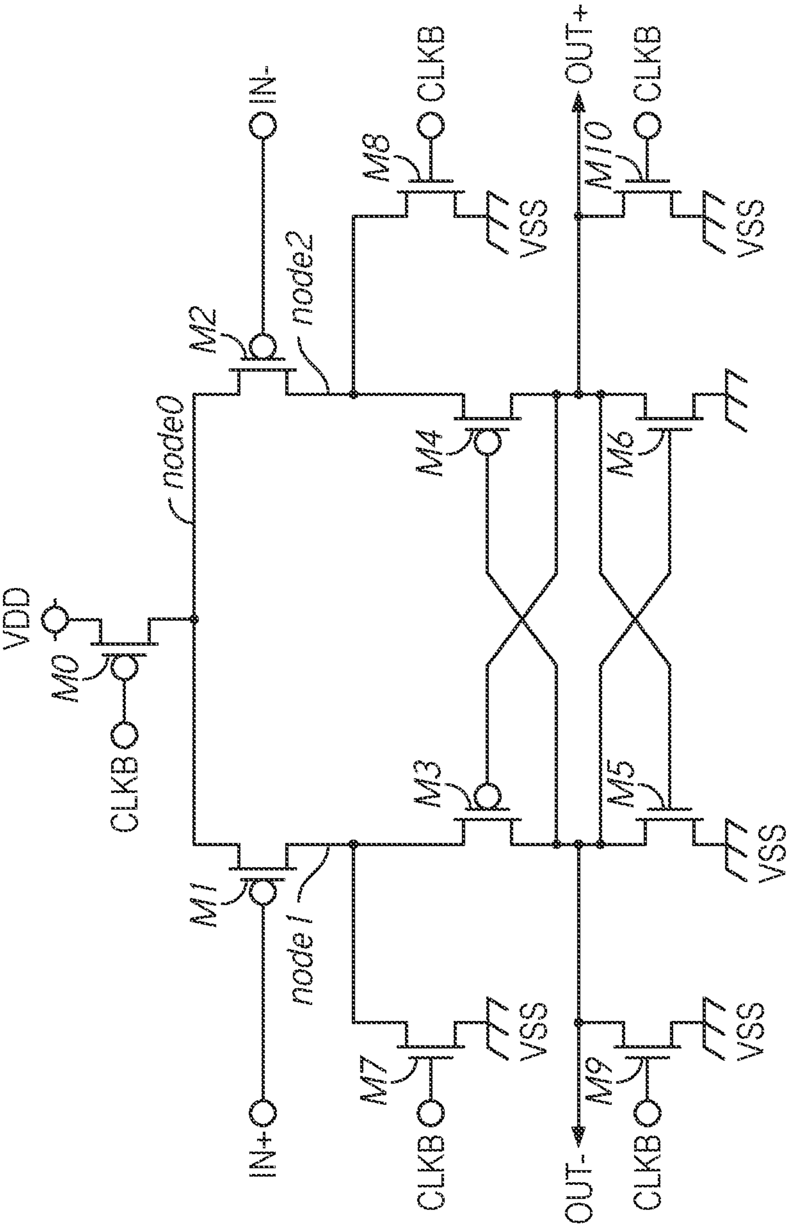


FIG. 1
(Prior Art)

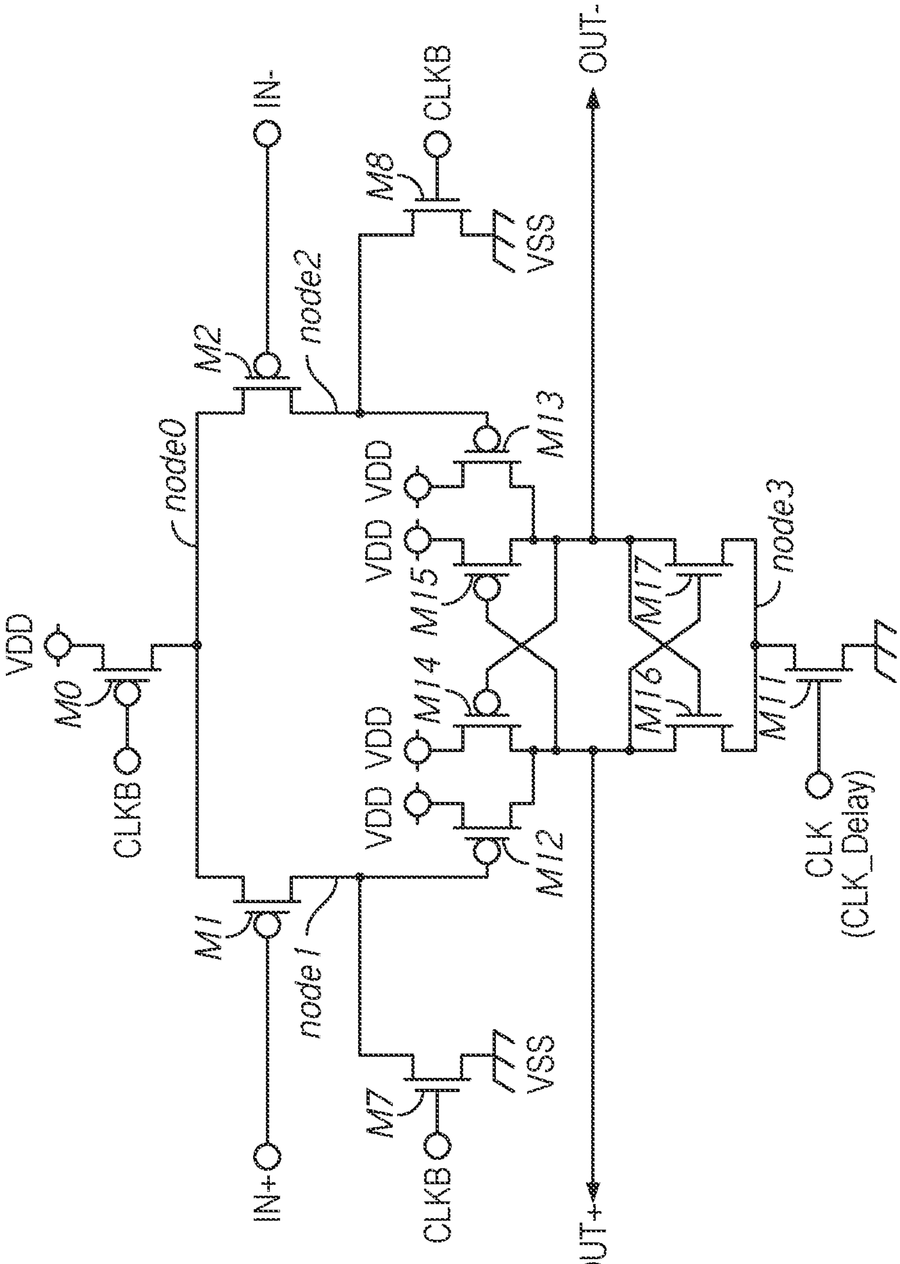
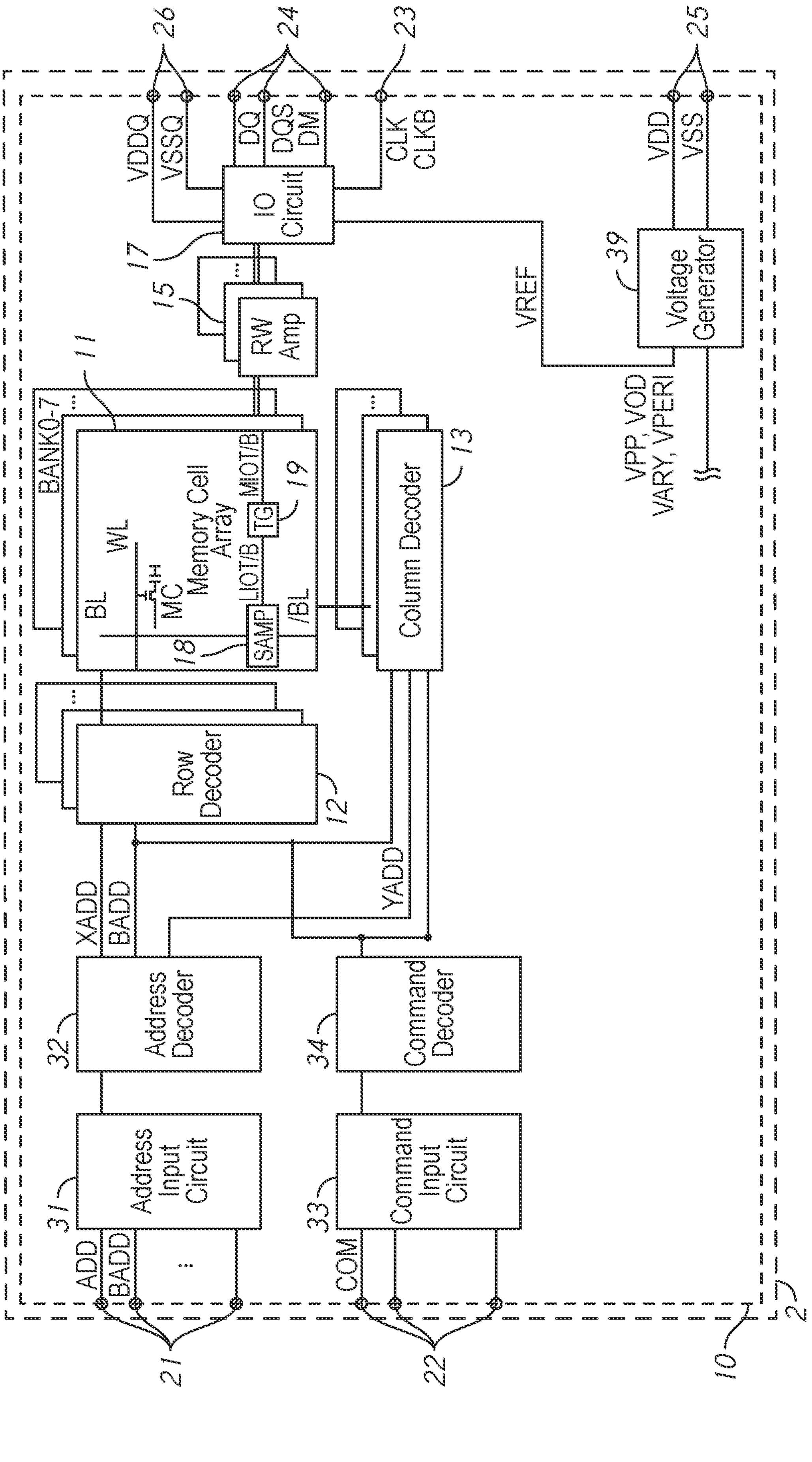


FIG. 2
(Prior Art)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24
23
25
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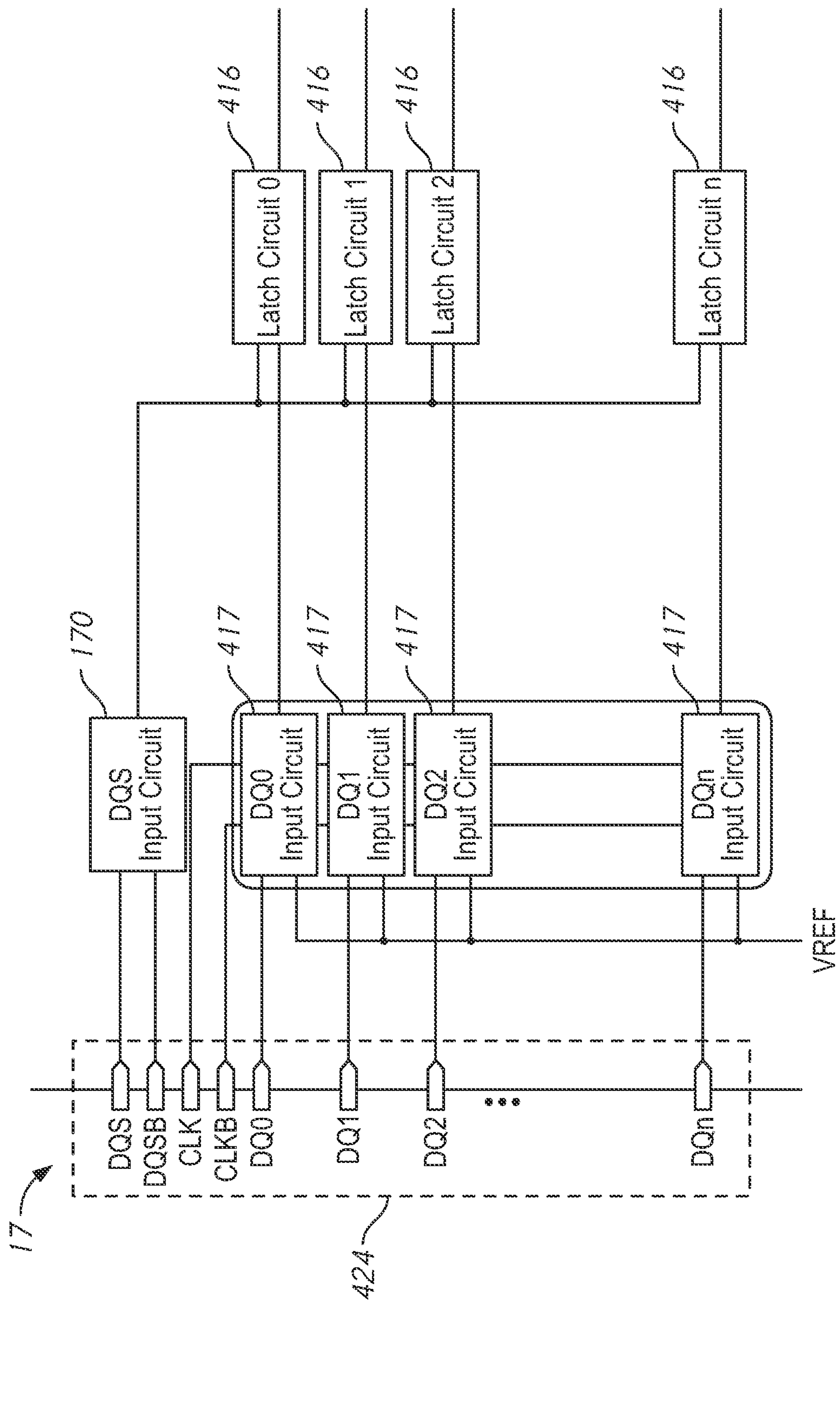
VSSQ
DQ
DQS
DM
CLK
CLKB
VDD
VSS
IO Circuit
17
15
RW Amp
VREF
39
Voltage Generator
11
BANK0-7
Memory Cell Array
BL
WL
MC
LIOT/B
MIOT/B
TG
19
SAMP
18
/BL
Column Decoder
13
VPP, VOD
VARY, VPERI
Row Decoder
12
XADD
BADD
YADD
Address Decoder
32
Command Decoder
34
Address Input Circuit
31
Command Input Circuit
33
ADD
BADD
COM
21
22
10
2

FIG. 3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424
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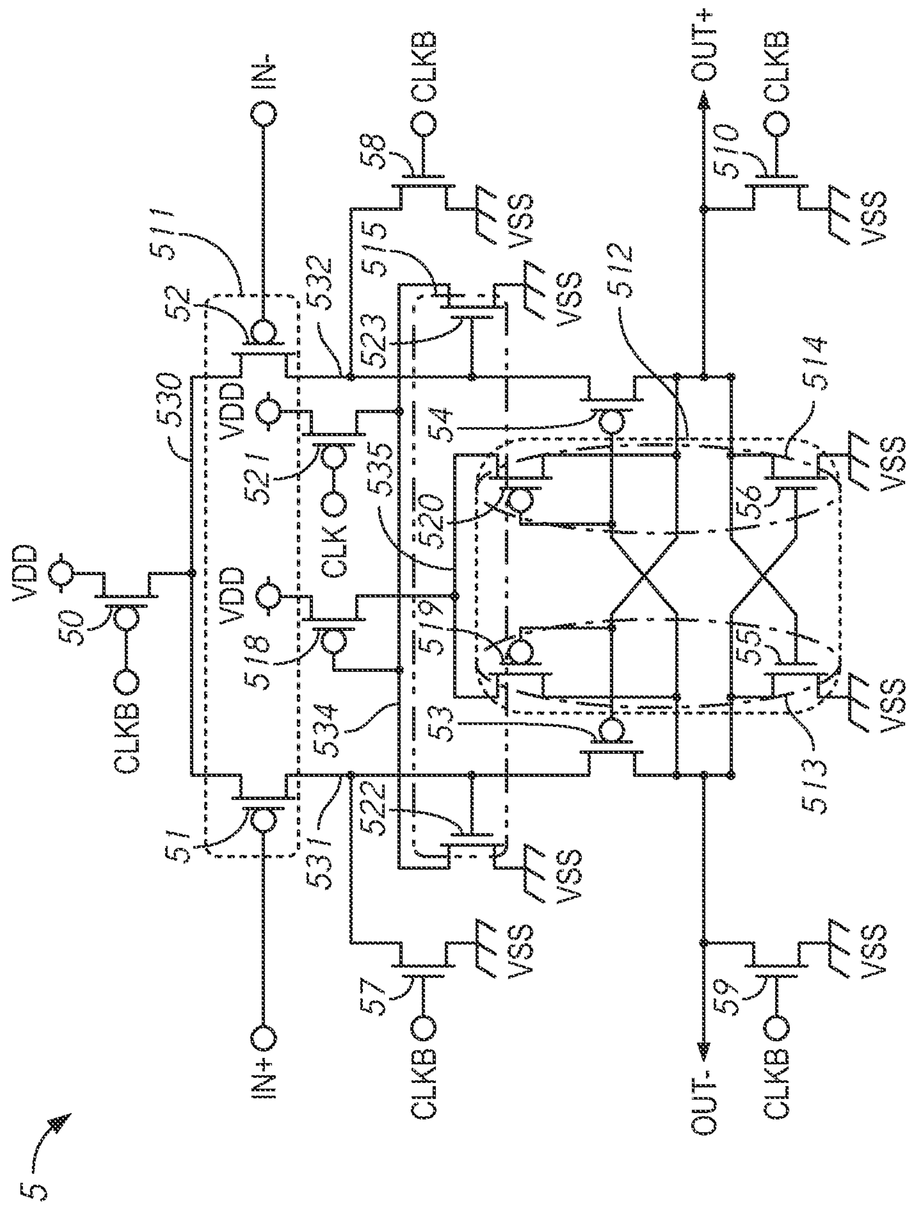
DQSB
CLK
CLKB
DQ0
DQ1
DQ2
DQn
VREF
170
DQS Input Circuit
417
DQ0 Input Circuit
DQ1 Input Circuit
DQ2 Input Circuit
DQn Input Circuit
416
Latch Circuit 0
Latch Circuit 1
Latch Circuit 2
Latch Circuit n

FIG. 4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CLKB
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IN+
IN-
51
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531
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VDD
CLK
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CLKB
CLKB
57
58
VSS
VSS
522
523
515
VSS
VSS
53
54
519
520
512
513
514
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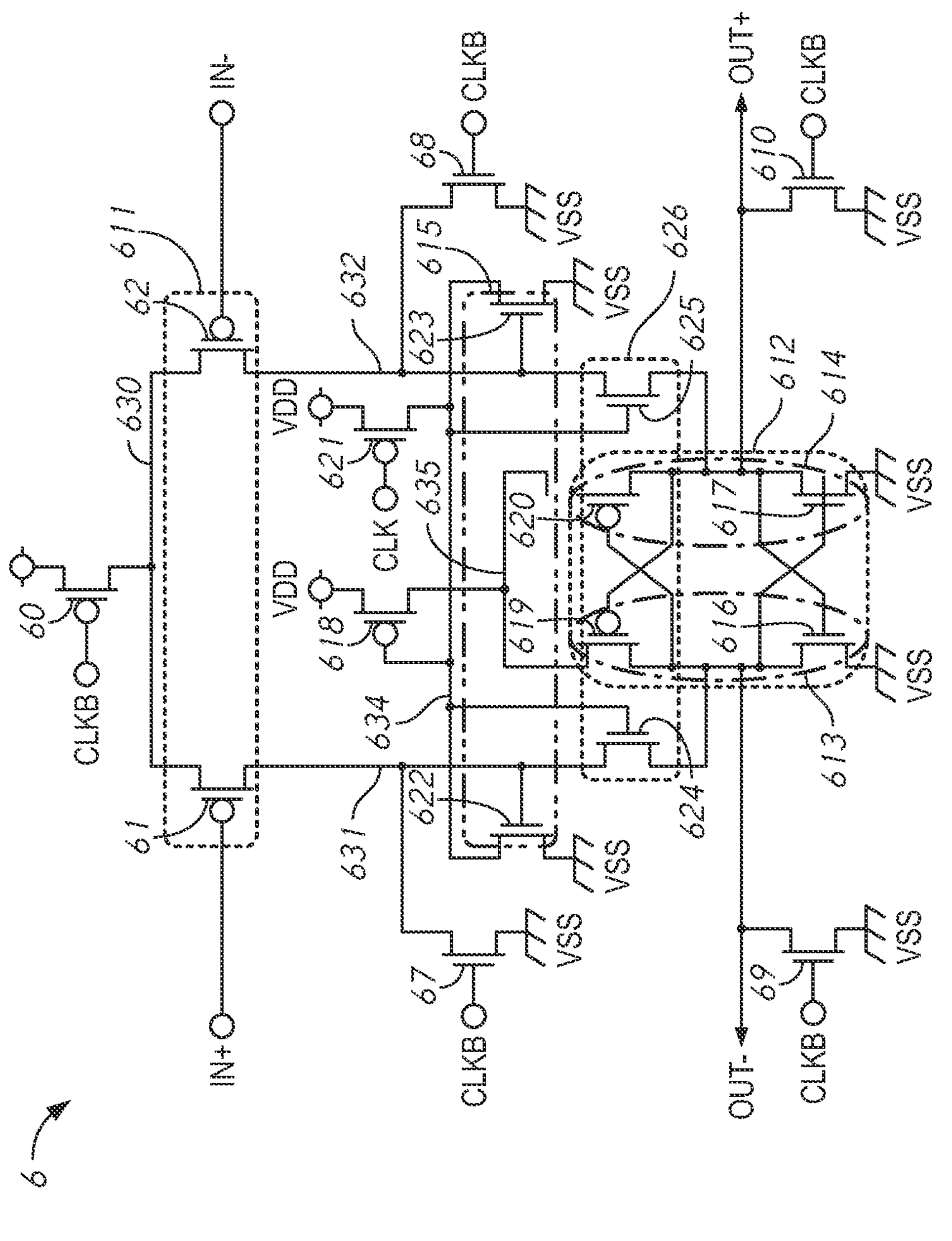
56
VSS
VSS
OUT-
OUT+
CLKB
CLKB
59
510
VSS
VSS

FIG. 5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IN-
CLK
OUT+
OUT-
VSS
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67
68
69
610
611
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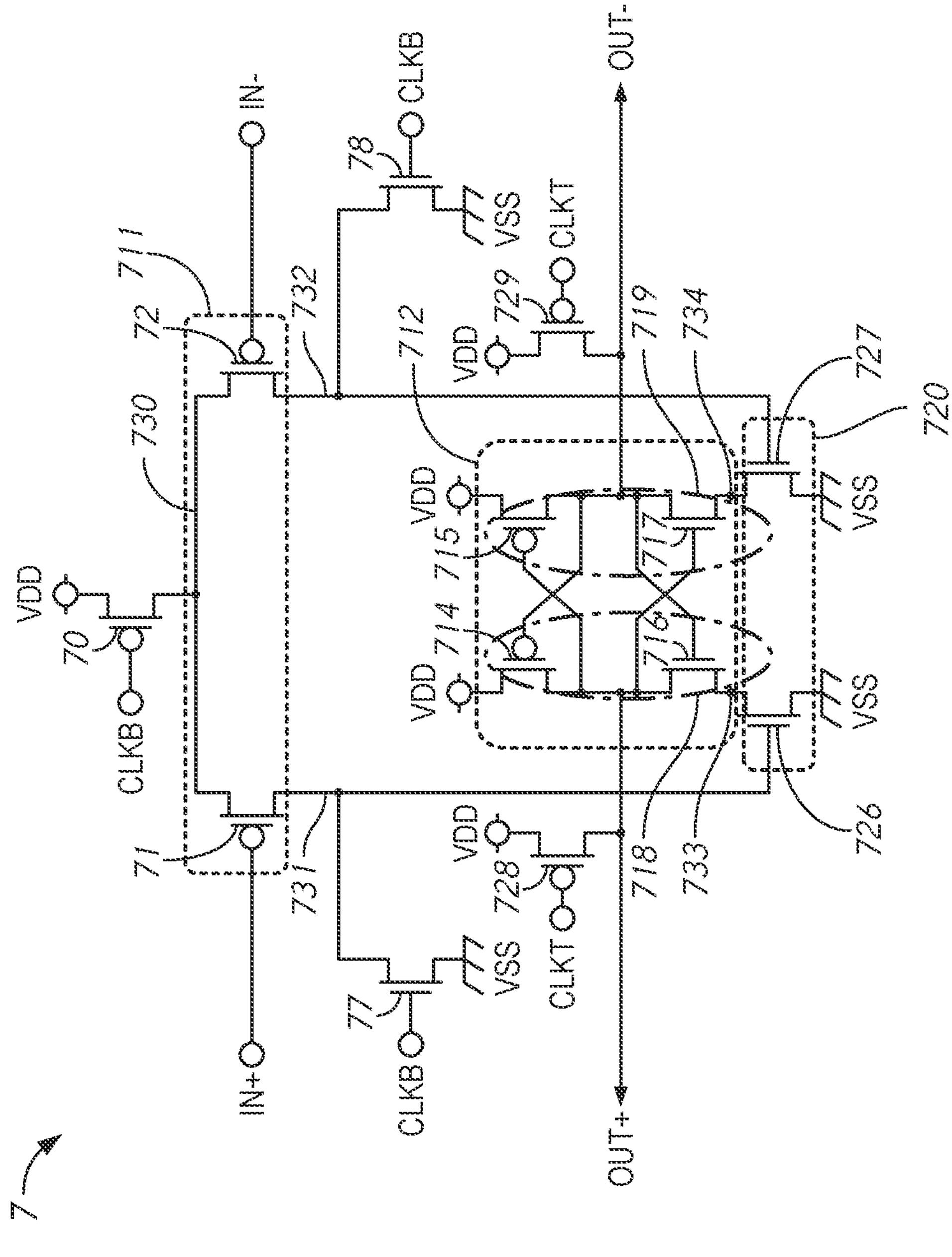
FIG. 6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IN+
IN-
CLKB
VDD
VSS
CLKT
OUT+
OUT-
70
71
72
77
78
711
712
714
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FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2018/017984

A. CLASSIFICATION OF SUBJECT MATTER

G11C 7/10(2006.01)i, H03F 3/45(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C 7/10; G11C 11/419; G11C 11/34; G11C 8/00; G11C 7/00; G11C 7/02; G11C 11/409; G11C 11/4097; G11C 16/06; H03F 3/45

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: amplifier, switch, intermediate voltage, transistor, inverter, circuit, threshold, source, drain, gate, output node

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	JP 2002-093177 A (HITACHI LTD.) 29 March 2002 See paragraphs [0005], [0021], [0024]-[0025], [0028]; and figure 1.	18-22 1-17
Y	US 6950368 B2 (DONALD M. MORGAN) 27 September 2005 See column 3, lines 43-61; column 4, lines 14-30; claim 37; and figure 2.	18-22
A	US 2007-0268750 A1 (TOSHIHIRO SUZUKI et al.) 22 November 2007 See paragraphs [0125]-[0144]; claim 1; and figure 12.	1-22
A	US 8873307 B2 (KAZUHIKO KAJIGAYA) 28 October 2014 See column 10, line 50 - column 11, line 9; claim 1; and figure 4.	1-22
A	US 6714470 B2 (WINGYU LEUNG et al.) 30 March 2004 See column 7, lines 1-31; claim 1; and figure 6.	1-22

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 July 2018 (24.07.2018)	**24 July 2018 (24.07.2018)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

Facsimile No. +82-42-481-8578

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BYUN, Sung Cheal

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2018/017984

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