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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L 21/00, 21/76 — A1

(11) International Publication Number: **WO 00/02235**

(43) International Publication Date: 13 January 2000 (13.01.00)

(21) International Application Number: PCT/US99/15156

(22) International Filing Date: 2 July 1999 (02.07.99)

(30) Priority Data:

60/091,790	6 July 1998 (06.07.98)	US
09/347,611	2 July 1999 (02.07.99)	US

(81) Designated States: DE, GB, JP, KR.

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

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(54) Title: METHOD OF PLANARIZING INTEGRATED CIRCUITS

(57) Abstract

A method is provided for fabricating an integrated circuit. The method includes a variety of steps such as providing a semiconductor substrate having a planar surface. The method includes a first spatially selective partial planarization process and a second material selective planarization process. This provides a substantially planar substrate for shallow trench isolation and interlayer dielectric applications in the manufacture of semiconductor devices or the like.

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METHOD OF PLANARIZING INTEGRATED CIRCUITS

CROSS-REFERENCES TO RELATED APPLICATIONS

This application claims priority to Serial No. 60/091,790 filed on July 6, 1998, which is hereby incorporated by reference for all purposes. The application also claims priority to U.S. Serial No. _____ (Attorney Docket No. 17074-000910US) filed July 2, 1999, which is also hereby incorporated by reference for all purposes.

BACKGROUND OF THE INVENTION

In the fabrication of conventional very large scale integration ("VLSI") and ultra large scale integration ("ULSI") integrated circuits ("ICs"), various planarization techniques have been developed. Generally, planarization techniques are used to improve the surface topology of a substrate, such as a silicon wafer, as it is processed into electronic devices, such as ICs.

ICs and similar devices are typically fabricated by growing, doping, depositing, etching, or otherwise forming a series of patterned layers in or on the substrate. Each layer may have a different pattern from the next. Often, the pattern of an underlying layer is at least partially expressed in the surface of a subsequent layer. An comparative example is when snow falls on a field with mounds and ditches. The location of the mounds and ditches are often visible in the surface of the snow, even if the depth of the snow is greater than the height of the mound or the depth of the ditch. For convenience, surface topology (i.e. deviation from a planar surface) resulting from a structure or structures underlying the surface will be referred to as residual surface topology.

In some semiconductor processing steps, it is desirable to have a flat surface on the substrate. One example is during photolithography processing when it is desirable to obtain a sharp focus on the surface of the substrate. Residual surface topology affects the depth-of-focus budget, meaning that some portions of the surface of the substrate will be in focus, while others might not be. A typical sequence would be to form a conductive layer, for example, cover the conductive layer with a photoresist, expose and develop the photoresist, and etch away the exposed conductor, leaving a patterned conductive layer. Residual surface topology can result in some regions of the

photoresist being exposed differently than others, which in turn affects how the development process. For example, a region of photoresist that is even slightly out of focus might not "harden" as much during the exposure as an in-focus region. When the photoresist is developed, the region that was slightly out of focus might slightly develop out, resulting in less protection for the underlying metal layer and a thinner conductive line after etching.

Depth of focus is an important consideration, especially as device geometries shrink and shorter exposure wavelengths are used to define narrower conductive lines. As described above, residual surface topology can cause the width (i.e. current-carrying capacity) of a conductive trace to vary, resulting in thin regions where current crowding, localized heating, accelerated corrosion, or similar effects may occur. The results of an inconsistent width in the conductive layer can include device failure or reduced reliability.

One approach to limit residual surface topology is to select processes with minimal topological variation. For example, many techniques for isolating devices, or "cells", on an IC chip exist, such as local oxidation of silicon ("LOCOS") and shallow trench isolation ("STI"). Topological variation might be one consideration in choosing one isolation technique over another. However, a compromise might have to be made in another factor, such as isolation effectiveness, processing time, or chip area required to achieve isolation.

Another approach to limit residual surface topology is to "planarize" the surface of a substrate after a process step has created some topology. Some techniques apply a liquid layer and harden it, such as photo-resist, or temporarily liquefy an applied layer, such as low-melting-point spin-on glass, to form a flat surface over the residual surface topology. In some instances, a subsequent layer is built directly on this flat layer, in other instances the flat layer is etched or otherwise removed and the underlying layer is planarized.

An example of the latter instance is where a layer of photoresist is applied and hardened to form a flat surface, and then a non-selective etch process, such as a reactive ion etch, is performed to remove the photoresist and portions of the underlying layer in a uniform manner. A non-selective etch removes the underlying material at essentially the same rate as the planarizing material, so the planar nature is preserved as the surface is etched back.

Another type of technique that has been developed to planarize the surface of a substrate is generally known as chemical-mechanical polishing ("CMP"). CMP generally uses a pad, similar to what is used to polish semiconductor wafers for example, in conjunction with a CMP fluid to remove residual topological features until a desired planar surface is achieved. For the purposes of this discussion, "CMP fluid" may include a solid-liquid mixture commonly referred to as a slurry. The substrate is moved relative to the pad, with the surface of the substrate being pressed against the pad. Some CMP fluids include a mild abrasive, while others rely on the chemical action of the CMP fluid and mechanical removal characteristics of the pad. In some systems, the CMP fluid converts the surface of the material being removed into a softer material that the pad removes by mechanical action. CMP is desirable because it can planarize substrates without additional masking or coating steps.

However, the pads used with a CMP process typically are slightly compliant and/or the chemical action of the CMP fluid is a function of pattern density. An undesirable result is that the planarization achieved is a function of the pattern being planarized. In other words, an area of the substrate with large, dense features may properly become planarized, while "dishing" occurs in the low regions. Dishing might inadvertently and undesirably remove or damage underlying structures, such as conductive traces. Dishing often occurs in memory cell arrays, such as are used in dynamic random access memories ("DRAMs") when trying to planarize regions using shallow-trench isolation ("STI") as well as during inter-level dielectric ("ILD") planarization. Dishing is particularly severe in DRAM IC manufacturing processes where very dense regions in the memory cell array region are planarized simultaneously with significantly less dense regions in the peripheral circuitry.

Another concern associated with CMP is "micro scratching" of the surface of the substrate. While micro scratching has probably always occurred with at least some CMP processes, micro scratching is increasingly a concern in the fabrication of sub-micron-sized (e.g., critical dimensions of 0.25 μm and less) devices which use CMP planarization. Accordingly, CMP is severely limited for today's state-or-art devices.

From the above, it is seen that a technique for planarizing a surface of an integrated circuit structure without pattern sensitivity of conventional CMP processes is

highly desirable. It would be further desirable to provide a CMP process and apparatus with improved micro-scratching for use with fine-geometry devices.

SUMMARY OF THE INVENTION

The present invention provides a technique, including a method and resulting structure, for planarizing integrated circuits. More particularly, the present invention provides a chemical mechanical polishing method which incorporates advantages offered by a selective slurry, while overcoming problems conventionally associated with using selective slurries.

According to one aspect of this invention, a method is provided for fabricating an integrated circuit on a semiconductor substrate. The method includes a series of steps such as forming a "CMP stop layer" over a layer, such as a patterned layer, on a substrate prior to forming a blanket layer that is CMP'd. The blanket layer is CMP'd by a first spatially selective polishing process, which removes substantial portions of any step differences, and a second material selective polishing process, which removes the blanket layer to the stop layer. This provides a substantially planarized blanket layer, which can be used as an interlayer dielectric structure, shallow trench isolation structure, or the like.

In one application, a steep-sided trench or array of trenches has been defined in the substrate. The trench is filled with a conformal layer or layers of an appropriate material, such as a dielectric material if the trench is an isolation trench. The substrate is then planarized in a multi-step (e.g., two-step, three-step) chemical mechanical polishing process. For example, the first step is carried out on a first dedicated polish platen and removes approximately 75 +/- 15% of the conformal layer of trench filling material in the regions not subtended by the trench (i.e. the "field" of the substrate between the trenches) with a relatively non-selective CMP fluid. A relatively high-speed (e.g., 25-90 RPM for 32 inch platen), low-down force (e.g., 2-5 psi) polish process is appropriate for this step. A second step is carried out on a second dedicated polish platen and selectively removes the trench filling material above the protective material in the regions not subtended by the trench by a standard lower-speed (e.g., 10-40 RPM for 32 inch platen), higher down force (e.g., 4-9 psi) polish process and a selective slurry. The combination of these steps selectively removes material extending above the planar surface ("field") of the substrate and the layer of protective material, i.e. the polish stop layer. The first step produces a globally planar surface planar, which might not be

achieved with a selective CMP fluid due to dishing and other factors, while the second step provides precise control of the end-point of the CMP material removal.

Thus, general planarization with rapid material removal and without substantial dishing is accomplished by the first step, while problems with pattern-sensitivity of the selective slurry are generally prevented in the second step by providing a near-planar starting surface for polishing. The high selectivity of the second polish step provides a robust polish process. The step-height differential between the field oxide and the device well (e.g., the active area of a device) beneath the gate electrode regions can be controlled by the deposited thickness (i.e. the initial thickness) of the polish stop layer. The two slurry types are kept from cross-contaminating each other by using a multi-table or multi-station process, for example. The multi-step process provides enhanced control of material removal and superior planarization while efficiently removing the necessary material. A further cleaning step, such as a rinsing step, could be incorporated as an intermediate process step between the first and second table processes to further avoid cross-contamination of the slurries. Accordingly, dishing is often avoided in the wider trenches during chemical mechanical polishing by the two-step selective process, the first step providing a near-planar surface for the high-selectivity second polish step.

Further variations and modifications can be implemented without departing from the spirit and scope of this invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention will now be described by way of example, with reference to the accompanying drawings, in which:

FIGS. 1 to 6 show simplified schematic cross-sectional views of part of a partially fabricated integrated circuit structure at successive stages in forming a trench isolation region according to a first embodiment of the present invention;

FIGS. 7 to 10 show simplified schematic cross-sectional views a partially fabricated integrated circuit structure at successive stages in forming an interconnect with planarized ILD according to a second embodiment of the present invention;

FIG. 11 is a simplified flow chart of a process according to an embodiment of the present invention;

FIG 12 is a simplified flow chart of a process according to an embodiment of the present invention showing additional process steps; and

FIG 13 is a simplified flow chart of a process according to another embodiment of the present invention showing alternative additional process steps.

DESCRIPTION OF THE SPECIFIC EMBODIMENTS

The present invention provides a method and an apparatus for planarizing substrates, such as silicon wafers used for IC fabrication. However, the technique can be applied to other types of substrates, such as semiconductor-on-insulator substrates or other semiconductor substrates with appropriate choice of CMP fluids and processing conditions. The application of the present invention to the fabrication of an STI structure is an example to illustrate the present invention.

One way to fabricate an STI structure is to according to the following fashion:

1. Trenches of appropriate width and depth are etched in field isolation regions. Those skilled in the art will appreciate that the depth, width, set-back, and other aspects of the STI process is a function of many factors, such as semiconductor material and doping, intended operating voltages, and so forth;

2. The trenches are then filled with a dielectric (i.e. electrically insulating) material, typically silicon dioxide or the like. A passivation treatment may be included, or adequate passivation of the trench walls and floor may be provided by the dielectric filling process ; and

3. Planarizing the surface of the substrate.

In conventional STI processes, the planarizing step (step 3) has been performed by a variety of methods. Examples of these methods include:

1. Block resist and resist etch back;
2. Block resist, reactive ion etch and chemical mechanical polishing;
3. Spin-on glass and reactive ion etch;
4. Various combinations of the above.

Additionally, CMP techniques have been used for the planarizing step in STI fabrication. As discussed above, pattern density can affect the CMP process. To avoid dishing or other problems, "dummy features" have been formed during the lithographic process to create a more uniform pattern density. However, even using dummy features, the problem of polishing through at least a portion of the desired layer of

material or into an underlying material arises. This problem is referred to by some as "run-out". To mitigate the problem of run-out, a polish stop layer has been added in some STI fabrication processes. The polish stop layer is typically a layer of a material that is not removed as quickly as the overlying material. In other words, the CMP process selectively removes the overlying material compared to the polish-stop layer. Unfortunately, use of a polish-stop layer can exacerbate the dishing problem, and the selective CMP process is often less efficient than non-selective CMP processes.

Additionally, conventional slurries, such as silica-based slurries, when used with conventional polish stop layers, such as a silicon nitride layer, are not particularly selective, and therefore are not very effective in providing a true polish stop. For example, the selectivity between a silicon oxide overburden layer and a silicon nitride polish stop layer is typically not better than 2:1 or 3:1 when a conventional silica-based CMP fluid is used. Control of the final polish stop layer thickness during planarization is important to controlling the step height differential of the field oxide and device well (active area) beneath the gate electrode regions. It is desirable to keep the step height differential as low as possible. One way to do this is to form a relatively thick polish stop layer, and then CMP a portion of this layer off. Forming a relatively thick polish stop layer is almost mandated by the relatively low selectivity of conventional "selective" CMP fluids; however, this approach nearly obviates the purpose of having a polish stop layer in the first place. In comparison, the present invention provides higher selectivity, allowing a thinner polish stop layer, which results in a lower step height differential between the active regions and the isolation regions.

A particular problem associated with STI arises when the surface of the oxide under the gate electrode is below the plane of the surface of the substrate. What typically happens in such a situation is that the thickness of the gate dielectric is reduced in the corner region produced by the intersection of the trench sidewall and the surface of the substrate. The thinning is produced by a phenomenon known as stress-induced oxidation retardation. This thinning can cause lowering of the transistor threshold voltages, degradation of the sub-threshold characteristics, and early breakdown or wear out of the gate dielectric in the corner region.

In an effort to improve the selectivity of the silicon nitride polish stop to the silicon oxide overburden material, and avoid the aforementioned limitations of controlling the step height differential of the field oxide and device well (e.g., active area) beneath the gate electrode regions, higher selectivity slurries have been developed. In

one example, cerium oxide is used as an abrasive component of a CMP fluid. Such slurry (commonly referred to as"Ce-based" or "ceria-based" slurry) is sold as XSHD3562™ by RODEL of Phoenix, AZ. This slurry has produced stop layer to overburden selectivity of greater than 100:1. While the potentially high selectivity of this slurry is appealing as a way of addressing some of the limitations discussed above, other issues limit its application. For example, Ce-based slurries often exhibit a low or variable removal rate when used to CMP with patterned wafers. This limitation may be severe enough to prevent commercialization of the slurry on a large scale until the issues and mechanisms of this slurry are understood and solved. Fortunately, it has been observed that the low or variable removal rate issue is typically not as severe when Ce-based slurries are used to CMP "blanket" layers.

FIGS. 1 to 6 are simplified cross sections of a portion of a substrate 5 being processed according to an exemplary fabrication sequence. In this sequence, an STI structure is being fabricated; however, those skilled in the art will appreciate that the techniques described in association with this exemplary sequence can be applied to other fabrication sequences and structures.

FIG. 1 shows a substrate 10 suitable for fabricating an integrated circuit. The substrate could be a p-type, <100> single-crystal silicon wafer, for example, but is not limited to such a wafer, or even to silicon. A stress-relief layer 12 has been formed over the substrate 10. The stress-relief material can be thermal silicon oxide or deposited silicon oxide, for example. A polish stop layer 14 has been formed over the stress-relief layer 12. In this instance, the polish stop layer 14 is silicon nitride, boron nitride or other material that can be selectively CMP'd in relation to an overlying layer. Those skilled in the art will appreciate that the stress-relief layer 12 may be optional, depending on the characteristics of the substrate material and/or the polish stop material, as well as acceptable device operation characteristics, among other factors. Those skilled in the art will also appreciate that the choice of a polish stop layer material can depend on the material of the overlying layer and the CMP system or systems being used, among other factors.

Trenches 16 and 18 are formed in the substrate 10 by anisotropic etching or other suitable etching or milling techniques. The trenches 16 and 18 were defined on the substrate with a conventional photoengraving step involving coating with photoresist, and patterning. The wide trench has an aspect ratio of about 1×10^{-4}, which may be less in some embodiments. The narrow trench has an aspect ratio of about 1-2, which also may

be less in some embodiments. A particular device may have both wide and narrow trenches, only wide trenches, or only narrow trenches.

FIG. 2 shows the substrate 10 after a conformal layer 22 of a dielectric material, such as silicon dioxide, has been deposited over the substrate surface and the polish stop layer 14 to fill the trenches 16 and 18. The dielectric material is, for example, silicon dioxide deposited using a chemical vapor deposition ("CVD") process. The conformal layer 22 completely fills both the narrow trench 16 and the wide trench 18. The thickness of the conformal layer 22 is sufficient to fill the wide trench 18 to a level 19 above the substrate surface layer 20, and completely fills the narrower trench 16. It is understood that the thickness' of the layers are not to scale, and that the sections of the layers, e.g. the square corners, are representative only, and that actual layers may have rounded corners, dimples, voids, or other artifacts. The conformal layer 22 extends over the polish stop layer 14 adjacent to the trenches, i.e., the level 19 of the conformal layer 22 in the wide trench 18 is "above" the polish stop layer 14.

FIG. 3 is a simplified cross section of the portion of the substrate 5 after a first planarizing step. In the first planarizing step, a first platen and CMP fluid is used to remove a first portion of the conformal layer 22 in the regions overlying the substrate surface layers 20 and narrow trench 16. A low-selectivity CMP fluid, such as SS25™ or SC-112™ sold by the CABOT CORPORATION of Boston, MA, is suitable for the first planarizing step. With the exemplary silicon nitride polish stop layer and a silicon dioxide-based conformal layer, an example of a low-selectivity slurry includes an alkali-bearing compound and a silica-bearing abrasive. The conformal layer 22 lies over the polish stop layer 14. In such an arrangement, the conformal layer or a similar layer is commonly referred to as "overburden". Selective removal of the overburden can be achieved for example by using a relatively high platen RPM and relatively low spindle down force during the first, planarization step, which partially planarizes the substrate. Typical values of platen RPM would range from 40 RPM to 150 RPM, and typical down force values would range from 2 PSI to 7 PSI. Other values may be used, depending on the overburden material, size of the substrate, type of CMP fluid, type of polishing pad, and other factors. In other embodiments, the platen RPM is as low as about 20 RPM; hence, the platen RPM can be between about 20-150 RPM and greater.

A selected amount of dielectric material from the conformal layer is removed during the first CMP step, which is a feature-selective CMP process. The characteristics of the feature-selective CMP process is to more quickly remove material

from the surface of the wafer in regions where a surface artifact extends "above" the general plane of the substrate. The selected amount is chosen to leave between about 0.2 -1 micrometers of dielectric material above the stress relief layer, and hence does not strictly depend on the initial (deposited) thickness of the conformal layer. In other embodiments the selected amount can range from about 1 micrometer and greater, depending upon the application. Of course, the amount of material removal depends upon the application, including the subsequent processing.

After the first polish step, the conformal layer becomes a partially planarized dielectric layer 32. Dielectric material remains in regions overlying the polish stop layer and the trenches. The dielectric material over the narrow trench 16 has been partially polished off, while some of the dielectric material over the wide trench 18 has not been polished during the first polish step. A rinse or other cleaning step(s) may be performed between the first and second polish step, depending on the polishing systems and CMP fluids being used. In some instances, a rinse or clean is desirable to prevent cross-contamination of the second polish system with slurry or other artifacts of the first polish system.

FIG. 4 shows the portion of the substrate 5 after a second polish step. The second polish step was performed on a second platen under CMP conditions different from the first polish step. The second polish step is material selective step because it preferentially removes one material faster than another. A Ce-based high-selectivity slurry was used with the silicon nitride and silicon oxide layers. Such slurries are available from various suppliers, such as RODEL and CABOT CORPORATION. The second polish step exposes the polish stop layer 14. The high selectivity of the CMP slurry removes little, essentially none, of the polish stop layer, while polishing the dielectric material 46 down to the level of the polish stop layer, resulting in a planarized substrate.

During the second polish step, uniform material removal is achieved using relatively lower platen speed and higher down force, compared to the first polish step. Typical values of platen RPM would range from about 10 RPM - 50 RPM, and typical down force values would range from about 4 PSI - 11 PSI. Selectivity of oxide: nitride removal rate achieved with this type of slurry typically ranges from 15:1 to more than 200:1.

Material removal by a highly selective chemical mechanical polishing process provides a dielectric layer surface 42 adjacent to the substrate surface layer 20 having a surface which is co-planar to the surface 44 of the polish stop layer 14. The step

height differential between the dielectric layer surface 42 and the adjacent substrate surface layer 20 is primarily determined by the combined thickness' of the polish stop layer 14 and the optional stress relief layer 12.

FIG. 5 is a simplified cross section of the portion of the substrate 5 after the polish stop layer and an additional portion of the dielectric layer has been removed with an etch process. The polish stop layer 14 can be removed by any of a variety of processes, such as a non-selective plasma etch, a selective plasma etch, or a wet-chemical dip. The method of choice depends on the desired resultant cross section, among other factors, and is facilitated by the planar surface obtained by the two-step CMP process. In this instance, the surface 50 of the dielectric material is level with the surface of the stress relief layer 52. The plasma etch process can be stopped when the effluent stream from the processing chamber indicates that silicon nitride is no longer being removed by the etch process, for example. Alternatively, the plasma etch could be continued until the material of the substrate 10 is reached. In that instance (not shown), the surface of the dielectric material would be level with the surface 20 of the semiconductor substrate. In yet another instance, the polish stop layer may be left on the substrate to be incorporated into the eventual device structure, or may be chemically altered or alloyed, or otherwise dealt with.

FIG. 6 shows the portion of the substrate 5 after additional, and in some instances optional, processing. The stress relief layer has been removed and a high-quality dielectric material 60 for use as a gate dielectric layer has been formed. Typical processes for the formation of such a material include thermal oxidation, including steam oxidation, or nitride-oxidation, and other suitable methods. A conductive layer 61 has been formed and patterned using conventional techniques to form a gate electrode 62. Typically, the dielectric material in the trenches is about 0.3-0.7 μm thick. The dielectric material may be deposited in a deposition process, or series of deposition processes, or an initial layer of silicon oxide may be thermally grown prior to depositing the remainder of the dielectric layer. Similarly, the surface of the dielectric material may be thermally treated, such as during the gate dielectric formation processor other process, or a capping layer may optionally be formed over the dielectric material in the trenches.

The present method can be performed on a variety of processing tools. For example, the process may be performed on multiple CMP tools, such as multiple single-table (single-platen) tools, or on a multi-table processing tool, such as are available from STRASBAUGH, located in San Luis Obispo, CA.

FIGS. 7-10 are simplified cross sections of a portion of a semiconductor substrate 70 illustrating an embodiment of the present invention applied to an ILD structure. FIG. 7 shows a first dielectric layer 72 supporting a metal structure 74, such as an electrical trace (wire). The first dielectric layer 72 can lie above an inferior patterned conductive layer or on the surface of a silicon wafer or other substrate, for example. A polish stop layer 76 has been formed over the metal structure 74, and a second dielectric layer 78 has been formed over the polish stop layer. In a particular embodiment, the polish stop layer is a layer of silicon-rich silicon dioxide formed in a high-density plasma ("HDP") chamber by adjusting the relative flows of silicon-containing gas or vapor, such as tetraethylorthosilane ("TEOS) vapor, and oxygen into the deposition chamber. Such silicon-rich oxide films exhibit a polishing selectivity of up to 30:1 compared to conventional HDP silicon oxide films. The cross-sections are not to scale, and the thicknesses are shown for illustrative purposes only.

FIG. 8 shows the portion of the substrate 70 after a feature-selective CMP step. A standard alkali slurry was used in conjunction with a relatively high downforce, similar to as described above in relation to FIG. 3. The feature-selective polish step results in a partially planar surface 80 of the second dielectric layer 78. The surface is referred to as partially planar because some portions 82 of the dielectric material lie below the CMP'd surface.

FIG. 9 is a simplified cross section of the portion of the substrate 70 after a material-selective CMP step, which is separate from the feature-selective CMP step and is performed on a different platen. The second dielectric layer 78 has been polished even with the polish stop layer 76. The selectivity of the material-selective CMP to polish stop layer material allows planarization across the wafer without over-polishing in certain regions of the wafer, such as near the wafer edges. The resulting planar surface provides a suitable surface for subsequent wafer fabrication steps, especially the formation and patterning of a fine-line patterned metal layer requiring a low depth-of-focus budget. The ILD thickness between the metal structures 74 and a subsequent conductive layer (not shown) is essentially equal to the thickness of the polish stop layer 76, which in some cases is essentially the thickness of the as-deposited polish stop layer. Naturally, this thickness can be increased or decreased, as desired. However, silicon-rich oxide has a slightly higher dielectric constant than conventional silicon oxide, which may increase coupling between metal layers.

FIG. 10 is a simplified cross section of a portion of a substrate 70 with an additional low-dielectric-constant layer 79 deposited over the planarized surface 84 (represented by dotted lines where an interface occurs between the second dielectric layer 78 and the low-dielectric-constant layer 79. The low-dielectric-constant layer could be, for example, silicon oxide, porous silicon oxide, or fluorine-doped silicon oxide. Additional layers, such as a capping layer (not shown) may also be incorporated.

FIG. 11 is a simplified flow chart 110 of a portion of a wafer fabrication process according to the present invention:

1. Transfer wafers to table 1 (step 112);
2. Polish wafers on table 1 using a low selectivity slurry and high-speed, low-down force process conditions: 30 to 120 sec, approx. (step 114);
3. Transfer wafers to table 2 (step 116);
4. Polish wafers on table 2 using a high selectivity slurry using low-speed, high downforce process conditions: 30 to 120 sec, approx. (step 118);

FIG. 12 shows an optional process sequence:

5. Transfer wafers to table 3 (optional) (step 119);
6. Polish wafers using DI, soft pad (optional): 30 sec, approx. (step 120).

FIG 13 shows a second optional process sequence:

5. Transfer wafers to a rinse station or to a third polish platen for DI rinsing or buff polish (step 121);
6. Transfer wafers back to table 1 (step 122);
7. Polish wafers using low selectivity slurry: 15 to 60 sec, approx. (step 123).

Other variations in the polish sequence can be applied to this process to produce a final planar surface appropriate to the IC process being used, and this process may be applied to alternative substrates or device structures, such as an ILD layer.

In an alternative embodiment using, for example, a MIRRA™ CMP tool, available from APPLIED MATERIALS, INC. of Santa Clara, CA, the process flow would be as follows:

1. Polish wafers on table 1 using low selectivity slurry, at high table speed and low downforce: 15 to 120 sec, approx.;

2. Polish wafers on table 2 using low selectivity slurry, at high table speed and low downforce: 15 to 120 sec, approx.;

3. Polish wafers on table 3 using high selectivity slurry, low speed and high downforce, 15 to 60 sec, approx.;

Alternatively, the third table on the MIRRA™ system could be used for a final deionized ("DI ")water buff polish process on a soft pad (e.g., felt, foam polymer). Optimization of the process on this tool for high throughput may dictate other variations in the process.

In a further alternative embodiment using, for example, an AURIGA™ CMP tool available from SPEEDFAM CORPORATION of Chandler, AZ, the process flow would be as follows:

1. Polish wafers on table 1 using low selectivity slurry, low speed and high downforce: 30 to 120 sec, approx.;

2. Polish wafers on table 2 using high selectivity slurry, low speed and high downforce 15 to 120 sec, approx.

Other variations in this process for the tools mentioned above, as well as others, might include polishing wafers on a single table using the low selectivity slurry, and switching to a high selectivity slurry on the same table while continuing to polish the wafers. Yet another variation on this process would be using a hard pad (e.g., polyurethane) on the first table, and soft pad on the second table, or a pad with embedded abrasive particles. Variations due to different tool configurations may be used or required without departing from the scope of the invention.

Although particular embodiments of the invention have been described in detail, it should be appreciated that numerous modifications, variations and adaptations may be made without departing from the scope of the invention as defined in the claims.

WHAT IS CLAIMED IS:

1. A method of fabricating an integrated circuit comprising:

providing a semiconductor substrate having a surface, the surface being defined by a trench region and an upper surface region defined around a periphery of the trench region, a stress relief material defined over the upper surface region, and a first chemical mechanical polish resistant material over the stress relief material;

filling the trench region with at least a dielectric material overlying the first chemical mechanical polish resistant material, the thickness of the dielectric material being sufficient to fill the trench region to a level above the upper surface region, the dielectric material forming a step difference from a first level, which is above the substrate surface to a second level, which is an upper surface of the dielectric material;

transferring the substrate to be polished by a first polishing platen on a chemical mechanical planarization apparatus and partially planarizing the dielectric material using a first chemical mechanical polishing ("CMP") step on the first polishing platen by a spatially selective removal of the dielectric material overlying the semiconductor substrate to reduce the step difference between the first level and the second level without substantial removal of dielectric material defining the second level;

transferring the partially planarized substrate from the first polish platen to be polished by a second polishing platen and planarizing the partially planarized dielectric layer using a second CMP step on the second polish platen by a material selective removal of the dielectric material overlying the semiconductor substrate not subtended by the trench to expose the chemical mechanical polish resistant material using a high selectivity slurry, whereupon the chemical mechanical polish resistant material overlying the semiconductor substrate defines at least a thickness of the dielectric layer planarized by the second CMP step.

2. The method according to claim 1 wherein the first polish step comprises a high-speed, low-down force polish process on a stacked polish pad comprising a hard upper pad overlying a soft lower pad.

3. A method according to claim 1 wherein the first polish step comprises a low-speed, high down force polish process on a hard pad and the second polish step comprises a lower speed, higher down force polish process on a soft pad.

4. The method according to claim 1 wherein the stress relief material comprises silicon dioxide.

5. A method according to claim 1 wherein the first chemical mechanical polish resistant material comprises silicon nitride.

6. The method according to claim 1 wherein the trench is provided by anisotropic etching.

7. A method according to claim 1 wherein the trench comprises an aspect ratio of at least 1 $x10^{-4}$ and greater.

8. The method according to claim 1 wherein the low selective slurry comprises an alkali bearing compound.

9. A method according to claim 1 wherein the low selective slurry comprises a silica bearing abrasive particle.

10. The method according to claim 1 wherein the high selective slurry comprises a Ce based slurry.

11. A method according to claim 1 wherein the high selective slurry comprises a Ce bearing abrasive particle.

12. A method according to claim 1 wherein the first polish platen and the second polish platen are provided on a common platform to improve efficiency of the method.

13. The method according to claim 1 wherein the first polish platen and the second polish platen are adjacent to each other and are coupled to each other through a handling means.

14. A method according to claim 1 wherein the first polish step is provided using a hard upper pad overlying a soft lower pad, the hard upper pad comprising a polyurethane bearing material and the soft lower pad comprising a foam polymer bearing material.

15. The method according to claim 1 wherein the soft lower pad comprising a felt.

16. A method of fabricating an integrated circuit, comprising:

providing a substrate having an upper surface, the upper surface having formed thereon a stress relief material and an overlying first polish resistant material, the substrate having defined therein a first trench of a first width and a second trench of a second width, the first trench region and the second trench region being surrounded by and extends to the upper surface, the first trench being filled with at least a dielectric layer overlying the first polish resistant material to a thickness sufficient to fill the first trench to a first level above the upper surface, the second trench being filled with the dielectric layer to a thickness sufficient to fill the trench to a second level above the upper surface, whereupon the dielectric layer overlying the first trench comprises a recessed region overlying a portion of the first trench and the dielectric layer overlying the first trench is substantially planar with a region of the dielectric layer overlying the upper surface, the first width being wider than the second width;

removing a first portion of the dielectric material using a first chemical mechanical polishing ("CMP") step on a first polish platen of a CMP tool by a spatially selective removal of the dielectric layer overburden overlying the substrate not subtended by the first trench, the first CMP step partially planarizing the dielectric material; and

removing a second portion of the partially planarized dielectric layer using a second CMP step on a second polish platen of the CMP tool by a selective removal of the dielectric layer overlying the semiconductor substrate not subtended by the first trench regions and exposing the polish resistant material using a high selectivity slurry;

wherein the polish resistant material overlying the upper surface defines a thickness of the dielectric material overlying the stress relief material, the polish resistant material and dielectric layer having a continuous and substantially planarized surface from the second CMP step.

17. The method according to claim 16 wherein the first polish step comprises a high-speed, low-down force polish process on a stacked polish pad comprising a hard upper pad overlying a soft lower pad.

18. The method according to claim 17 wherein the high speed ranges from about 40 to about 150 revolutions per minute.

19. The method according to claim 17 wherein the downforce ranges from about 2 to about 7 pounds per square inch.

20. A method according to claim 16 wherein the first polish step comprises a low-speed, high downforce polish process on a hard pad and the second polish step comprises a lower speed, higher downforce polish process on a soft pad.

21. The method according to claim 20 wherein the low speed ranges from about 20 to about 70 revolutions per minute.

22. The method according to claim 20 wherein the downforce ranges from about 2 to about 7 pounds per square inch.

23. A method of fabricating an integrated circuit, comprising:

providing a substrate having an upper surface, the upper surface having an overlying stress relief material and an overlying first polish resistant material, the substrate having defined therein a first trench of a first width and a second trench of a second width, the first trench being filled with at least one layer of dielectric material overlying the first polish resistant material to a thickness sufficient to fill the trench to a first level above the upper surface, the second trench being filled with at least the one layer of the dielectric layer to a thickness sufficient to fill the trench to a second level above the substrate surface layer, whereupon the dielectric layer overlying the first trench comprises a step difference from a first level, which is above the upper surface, to a second level, which is even with an upper surface of the dielectric material overlying the first polish resistant material, the dielectric layer overlying the second trench is substantially planar with the upper surface of the dielectric layer overlying the first polish resistant material, the first width being wider than the second width, the first width is at least three times more than a depth of the first trench; transferring the substrate to be polished by a first polishing platen on a chemical mechanical planarization apparatus and partially planarizing the dielectric material using a first chemical mechanical polishing ("CMP") step on the first polishing platen by a spatially selective removal of the

dielectric material overlying the semiconductor substrate to reduce the step difference between the first level and the second level without substantial removal of dielectric material defining the second level; and transferring the partially planarized from the first polish platen to be polished by a second polishing platen and planarizing the partially planarized dielectric layer using a second CMP step on the second polish platen by a material selective removal of the dielectric material overlying the semiconductor substrate not subtended by the first trench and to expose the chemical mechanical polish resistant material using a high selectivity slurry whereupon the chemical mechanical polish resistant material overlying the semiconductor substrate defines a thickness of the dielectric layer planarized by the second CMP step.

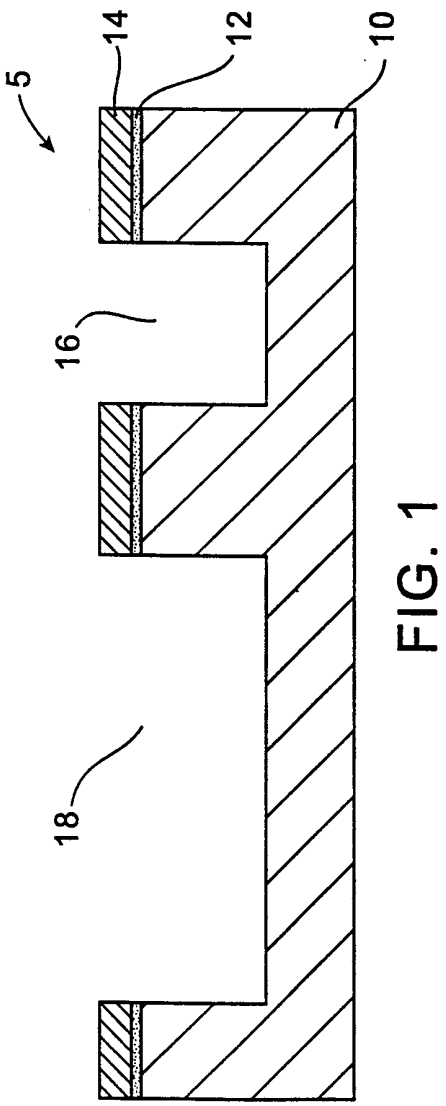

FIG. 1

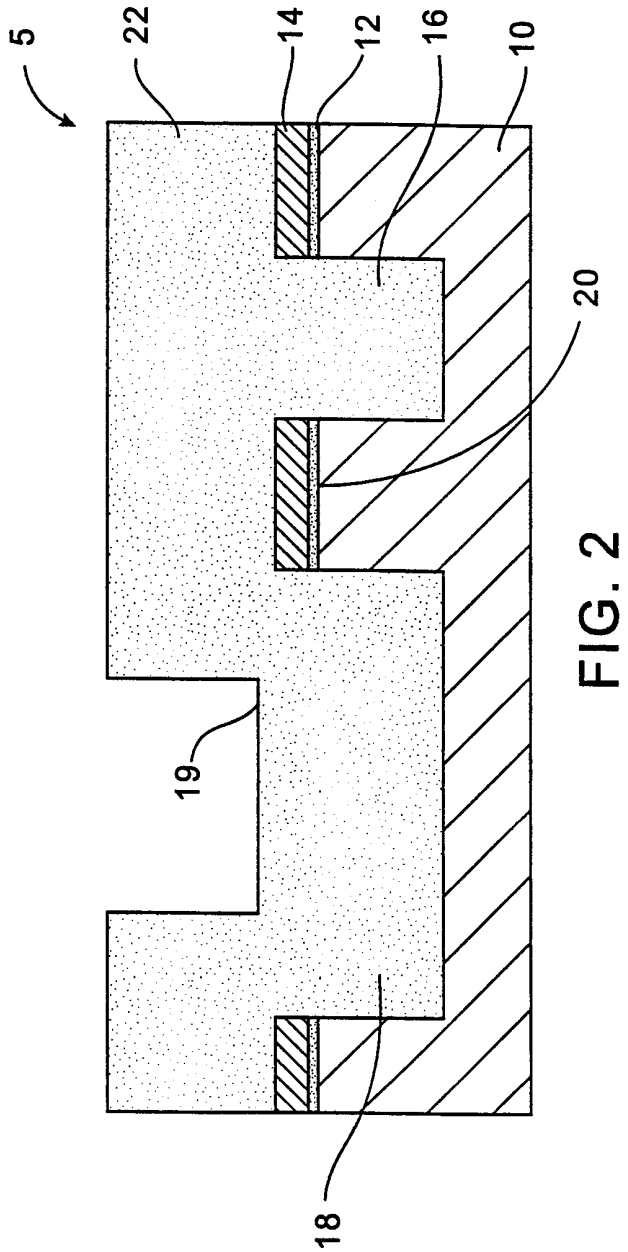

FIG. 2

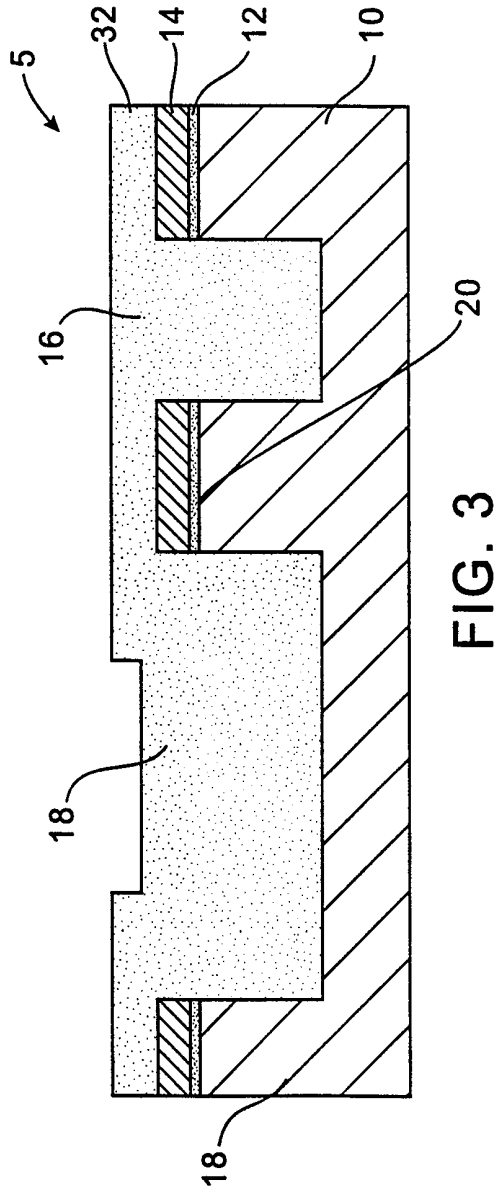

FIG. 3

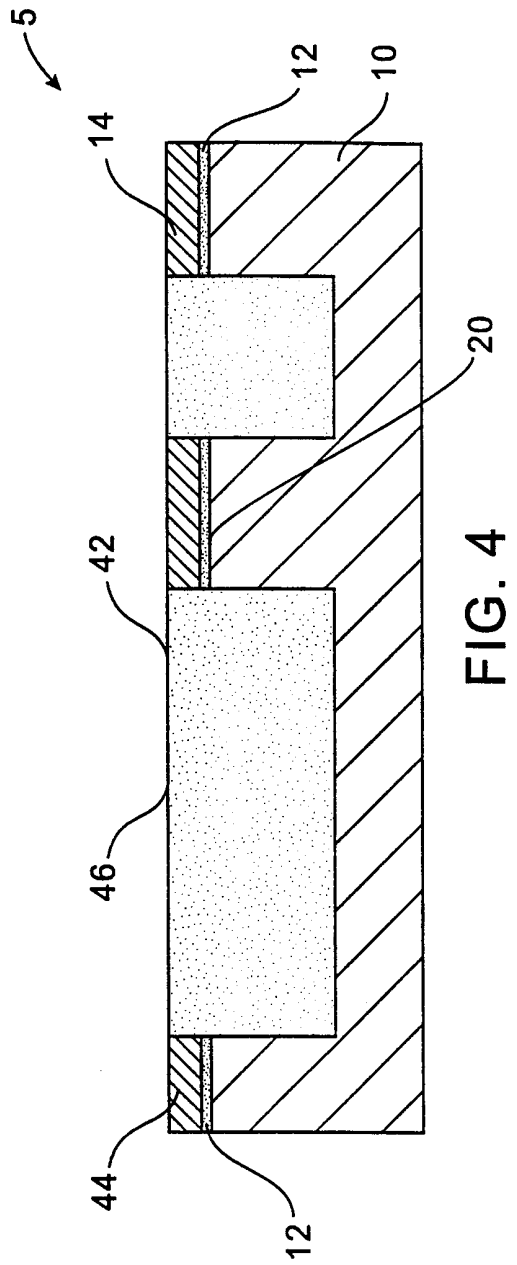

FIG. 4

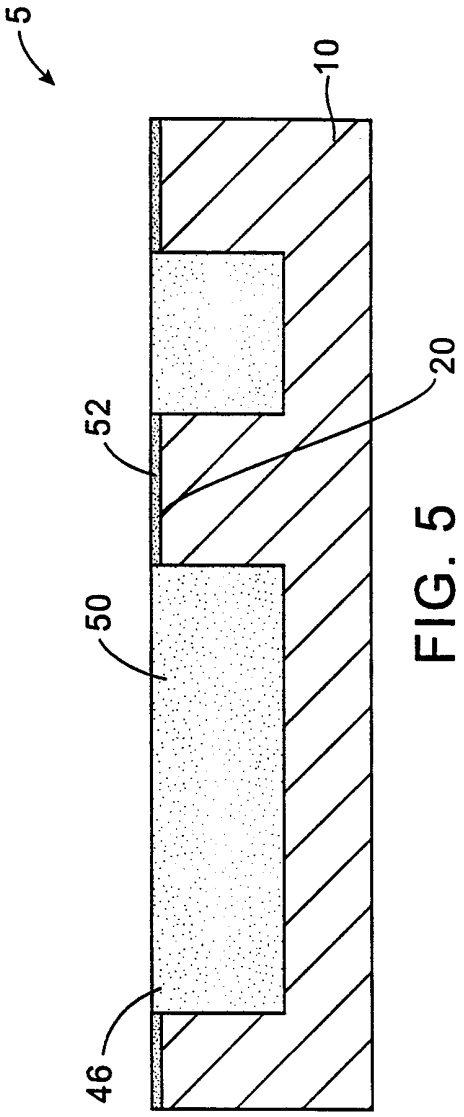

FIG. 5

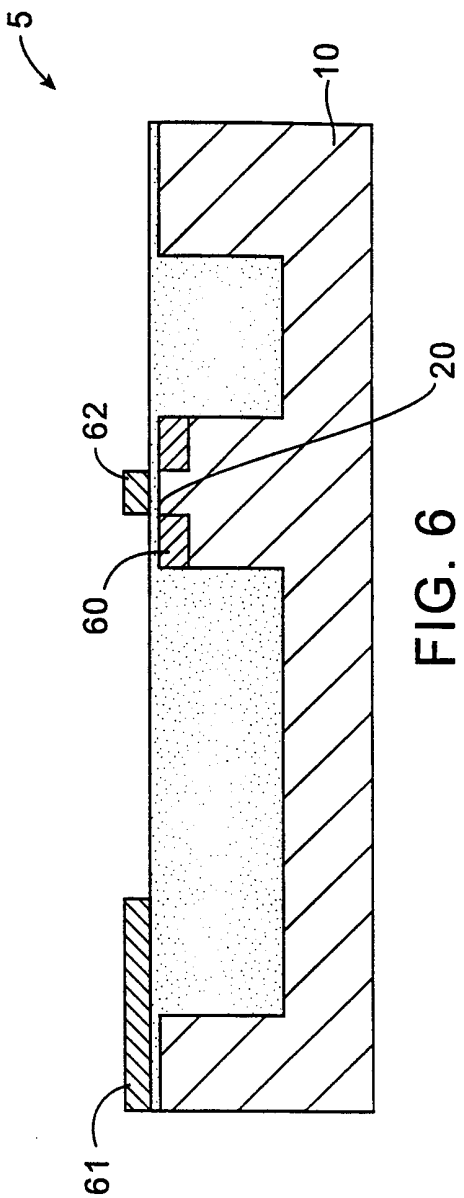

FIG. 6

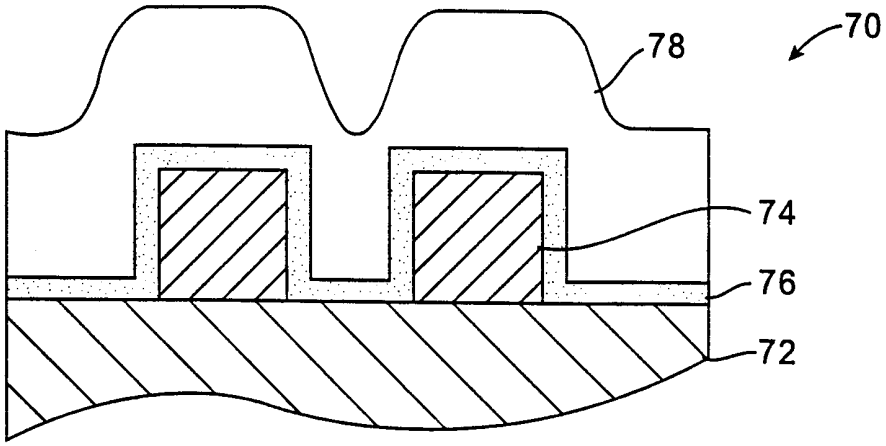

FIG. 7

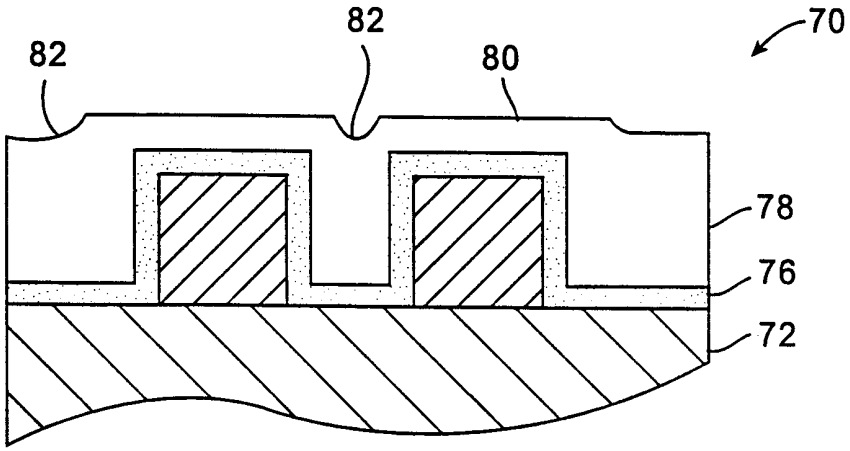

FIG. 8

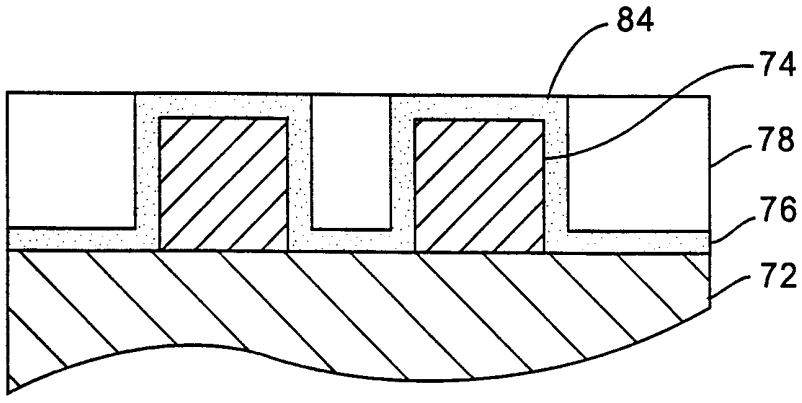

FIG. 9

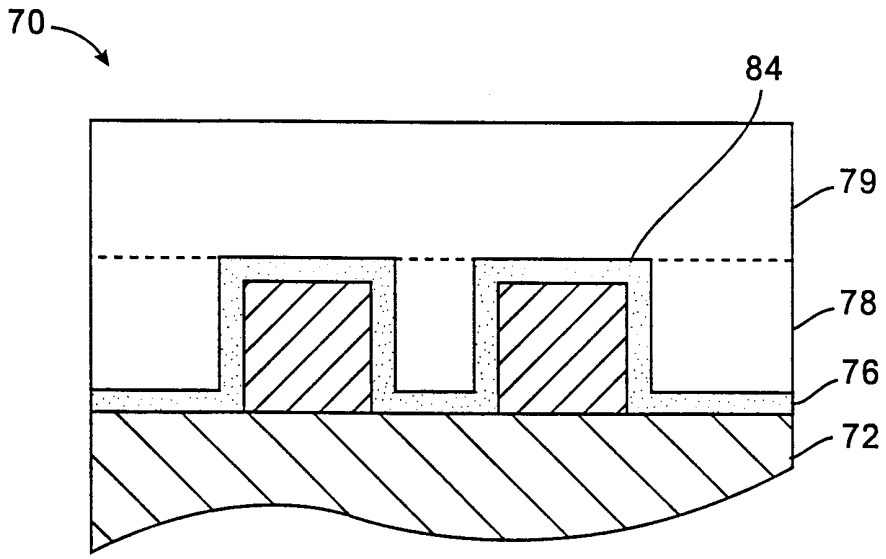

FIG. 10

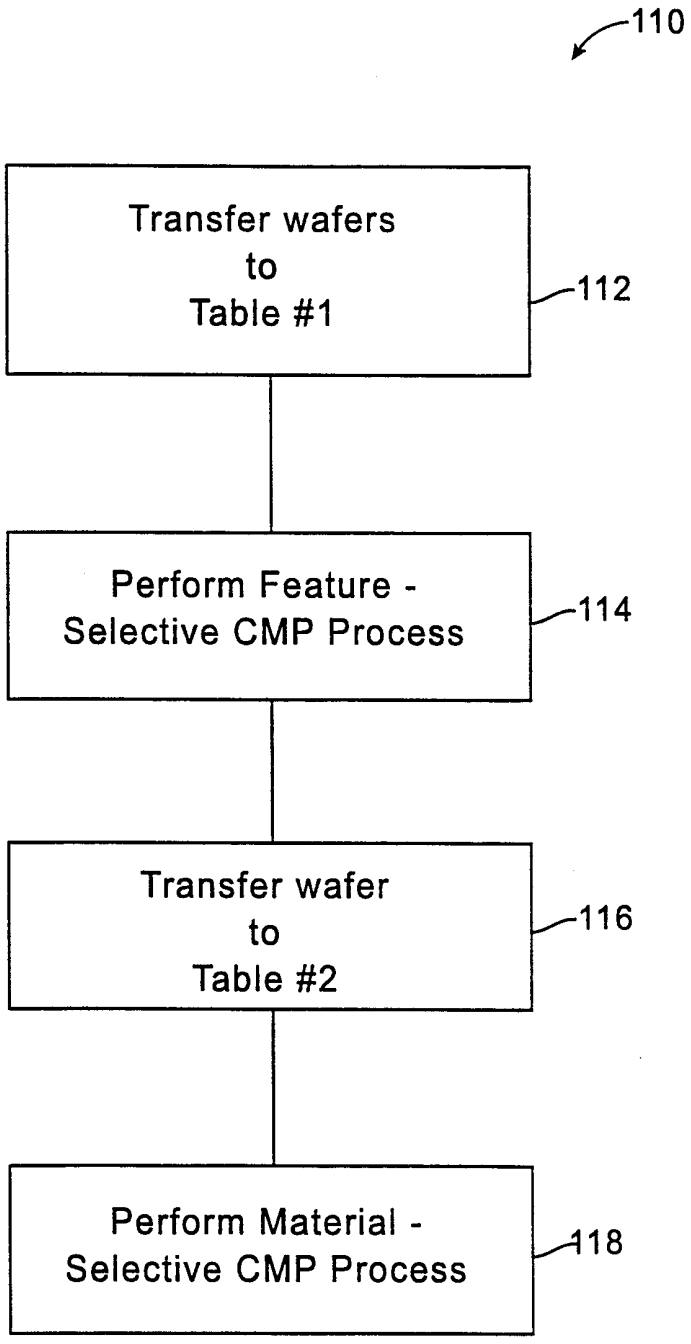
110
Transfer wafers to Table #1
112
Perform Feature - Selective CMP Process
114
Transfer wafer to Table #2
116
Perform Material - Selective CMP Process
118

FIG. 11

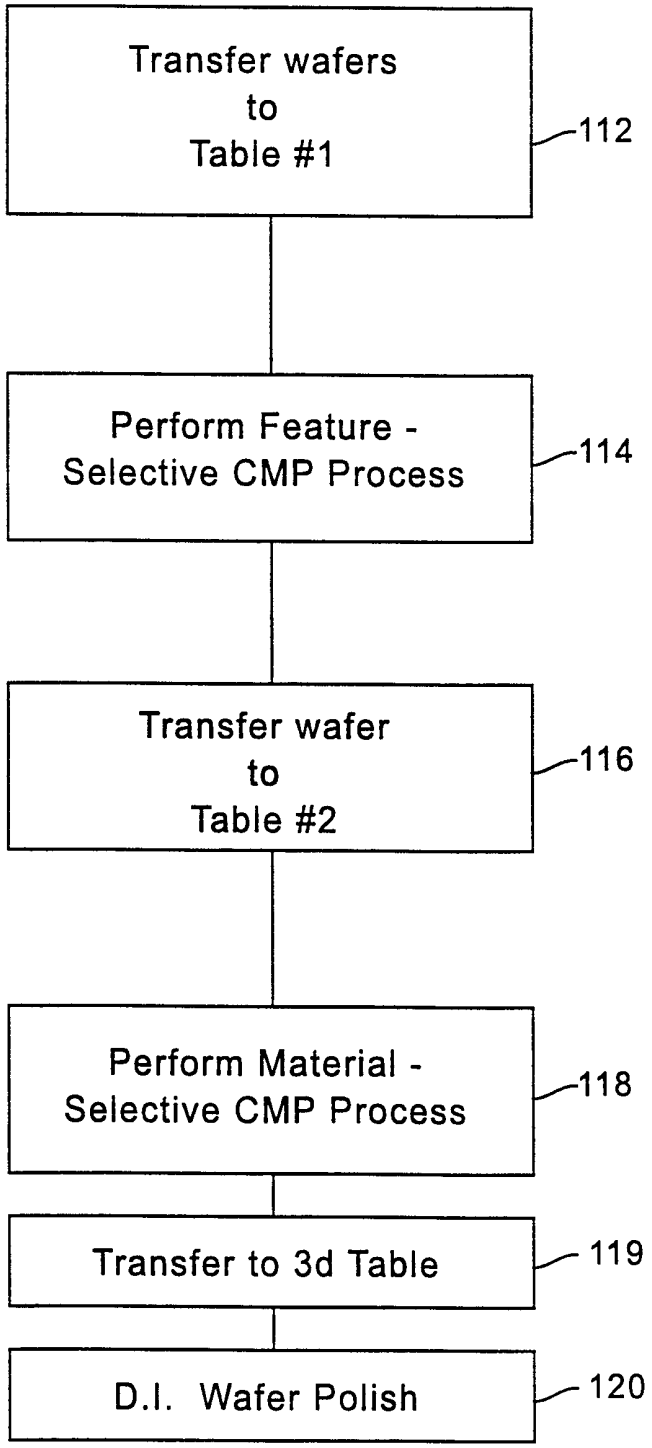
Transfer wafers to Table #1
112
Perform Feature - Selective CMP Process
114
Transfer wafer to Table #2
116
Perform Material - Selective CMP Process
118
Transfer to 3d Table
119
D.I. Wafer Polish
120

FIG. 12

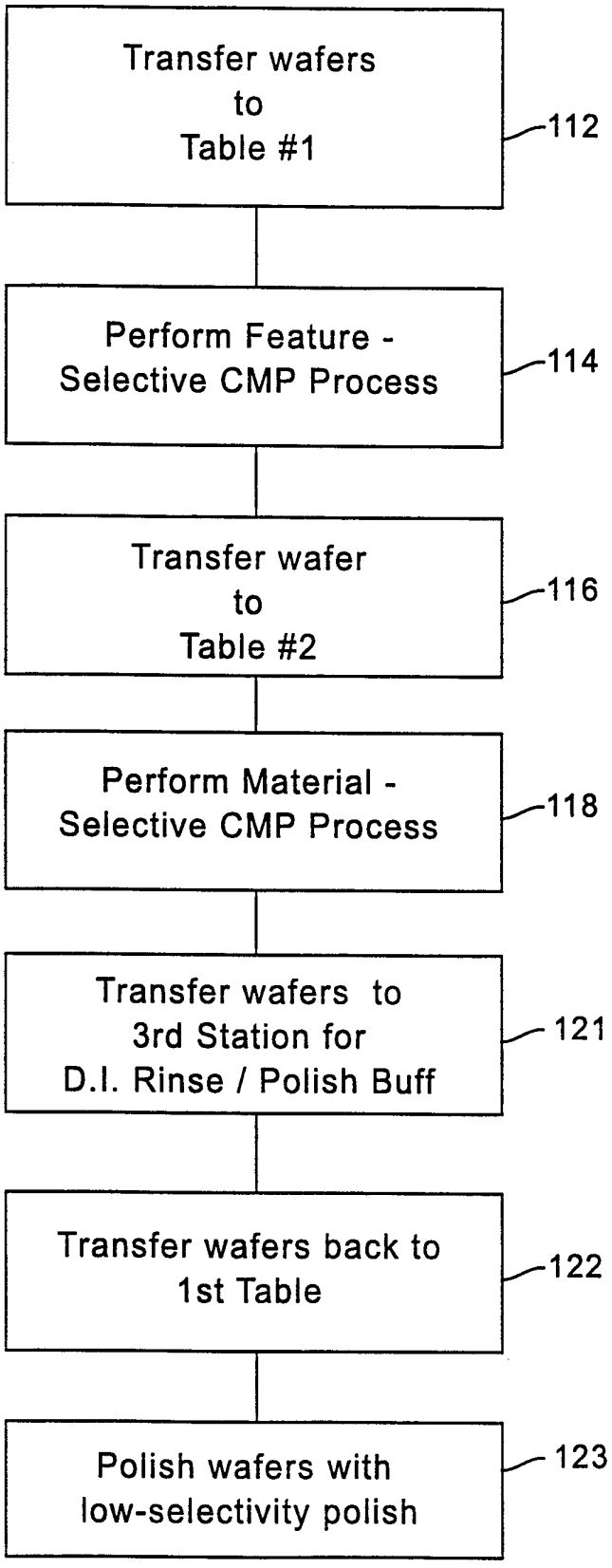
Transfer wafers to Table #1
112
Perform Feature - Selective CMP Process
114
Transfer wafer to Table #2
116
Perform Material - Selective CMP Process
118
Transfer wafers to 3rd Station for D.I. Rinse / Polish Buff
121
Transfer wafers back to 1st Table
122
Polish wafers with low-selectivity polish
123

FIG. 13

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/15156

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01L 21/00, H01L 21/76
US CL :438/692, 693

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 438/692, 693

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

USPTO APS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,573,972 A (Kobayashi) 12 November 1996 (12.11.96), col. 4, lines 49-66	1-15
X,P	US 5,914,275 A (Kodera et al.) 22 June 1999 (22.06.99), col. 27, lines 3-45	17-23

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 21 SEPTEMBER 1999	Date of mailing of the international search report 14 DEC 1999
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer DAVID NELMS Telephone No. (703) 308-4910

Form PCT/ISA/210 (second sheet)(July 1992)★