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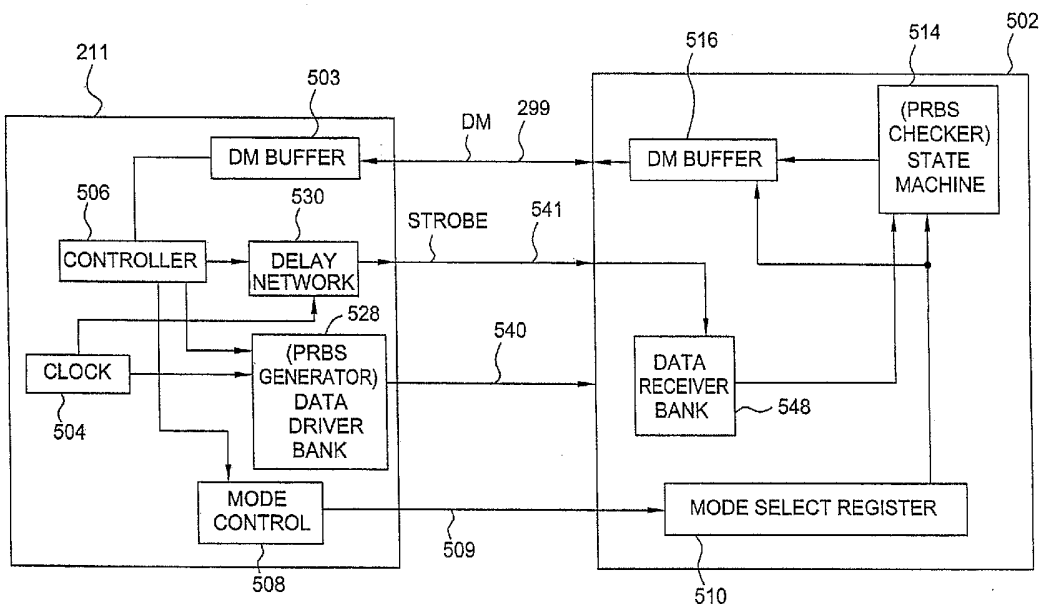
[Continued on next page]

(54) Title: DATA MASK AS WRITE-TRAINING FEEDBACK FLAG



(57) Abstract: Methods and apparatuses that enable memory devices to inform graphical processing systems about the results of WRITE de-skew training. A WRITE-TRAINING mode is added to a memory device. When the WRITE-TRAINING mode is asserted the memory data mask (DM) pin is converted to an output port. Incoming WRITE data is strobed-into the memory device and the resulting data pattern is compared to a desired pattern. If the incoming WRITE data and strobed-in data match, that result is sent to the graphical processing system by setting the DM pin HIGH. If the incoming WRITE data and the strobed-in data do not match, that result is sent to the graphical processing system by setting the DM pin LOW. Beneficially, the incoming data and the desired pattern are derived from pseudo random bit sequence (PRBS) sources.

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DATA MASK AS WRITE-TRAINING FEEDBACK FLAG

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of United States provisional patent application serial number 60/565,973, entitled, Data Mask As Write-Training Feedback Flag, which was filed on April 27, 2004 and which is herein incorporated by reference.

BACKGROUND

[0002] The present invention relates to high speed data interfaces, and more particularly to using a modified Data Mask (DM) pin as an error flag when de-skewing communications.

[0003] Graphics processing is an important feature of modern, high performance computer systems. Some graphical processing systems render high-resolution, real-time graphical images on display devices by using special high-performance computational circuitry that is incorporated into or that is otherwise mated with graphical processing units (GPUs).

[0004] In addition to GPUs and computational circuitry, graphical processing systems also require memory devices, usually high speed static random access memory (SRAM) or dynamic random access memory (DRAM). While SRAM and DRAM devices have been used with GPUs for many years, current demands for high resolution, high performance, real time graphics processing requires very fast memory devices. To that end, faster memory devices, such as double data rate random access memory, have been developed. A double data rate memory device clocks data into or out of memory on both the rising and falling edges of a clocking signal.

[0005] While double data rate memory devices are very useful, the sheer speed required to render high resolution digital images in real time can make the basic task of communicating with memory difficult. This is because high speed data accessing takes place over individual data lines that can differ. For example, individual data lines can have different lengths, distributed impedances, and end terminations. Those differences can cause individual bits of a data byte to arrive at a receiver at different times. Furthermore, individual receivers and drivers have transition speeds that can differ. For example, a GPU could send a data byte to a

memory device with a first pattern, say 1111 0000, which, when clocked into a memory, could be recognized as 1011 0001 because the clock signal arrived before the data byte was ready to be clocked. This temporal problem is referred to as skew.

[0006] In some high speed interface circuits, for example double data rate memory, the actual clocking of data into and out of a memory device is performed using a strobe signal that is derived from a master clock. By selectively delaying the strobe signal relative to the data byte the strobe signal's edges can be shifted such that they occur after the data byte is ready. Reference United States provisional application number 60/539,787 (attorney docket number P001187) filed January 27, 2004, incorporated by reference, which describes how to automatically shift strobe timing such that the strobe edges occur at times that avoid skew.

[0007] While the teachings of United States provisional application number 60/539,787 (attorney docket number P001187) filed January 27, 2004 are beneficial, implementing those teachings are subject to practical constraints. For example, when adjusting strobe timing relative to data packets during WRITE de-skew training, some method of informing the GPU about the results of strobe timing is required. A straightforward way to do that would be to add a new "result" pin to the memory device and another to the GPU. Unfortunately, SRAM and DRAM memory devices, particularly, their input/output (I/O) pin configurations, are relatively standardized. While adding internal circuitry to a GPU and to a memory device to implement de-skew training is relatively straight forward, adding a new I/O pin is contrary to accepted standards.

[0008] Therefore, a method and apparatus that enables a memory device to inform a graphics processing system about the results of de-skew training during WRITE operations would be beneficial. Also beneficial would be a method and apparatus that enables a memory device to signal a graphics processing system about strobe timing relative to data packets during WRITE operations using existing memory pin-outs.

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SUMMARY

[0009] The principles of the present invention enable methods and apparatus that enable memory devices to inform graphical processing systems about results obtained during WRITE de-skew training. Embodiments of the present invention

implement WRITE de-skew training circuitry within the memory device and/or within the graphical processing system. The WRITE de-skew training circuitry enables WRITE de-skew training result notification using the existing memory device pin-out structure.

[0010] Embodiments of the present invention modify the memory device I/O data mask pin to a bi-directional pin and add an operational mode to the memory device that selectively converts the DM pin to an output port. Circuitry provides for a comparison between incoming data and strobed-in data. When the incoming data and the strobed-in data match, that result is made available by setting the DM pin HIGH. When the incoming data and the strobed-in data do not match, that result is made available by setting the DM pin LOW. Beneficially, the incoming data is derived from a pseudo random byte source (PRBS), and the comparison is made using the strobed-in data and another pseudo random byte source (PRBS).

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] So that the manner in which the above recited features, advantages and objects of the present invention are attained and can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to the embodiment thereof which is illustrated in the appended drawings.

[0012] Figure 1 is a block diagram of a computer system that is in accord with the principles of the present invention;

[0013] Figure 2 is a simplified block diagram showing relationships between data and strobe signals;

[0014] Figure 3 helps explain how strobe to data timing results can be used to automatically adjust the delay of a strobe signal to de-skew a communication link;

[0015] Figure 4 illustrates portions of a communication link that is in accord with the principles of the present invention;

[0016] Figure 5 illustrates a pseudo -random byte generator that is suitable for use with embodiments of the present invention; and

[0017] Figure 6 illustrates a pseudo-random byte checker that is suitable for use with embodiments of the present invention.

DESCRIPTION OF A SPECIFIC EMBODIMENT

[0018] Embodiments of the present invention enable memory devices to inform graphical processing systems about the results of WRITE de-skew testing using existing memory device pin-outs. A WRITE-TRAINING mode is added to the operational modes of a memory device. When the WRITE-TRAINING mode is asserted the memory data mask (DM) pin is converted to an output port. Incoming WRITE data is strobed into the memory device and the resulting data pattern is compared to a desired data pattern. If the incoming WRITE data and the strobed in data match, that result is sent to the graphical processing system by setting the DM pin HIGH. If the incoming WRITE data and the strobed-in data do not match, that result is sent to the graphical processing system by setting the DM pin LOW. Beneficially, the incoming data and the desired pattern are derived from pseudo random byte sources (PRBS).

[0019] Figure 1 is a block diagram of a computer system 200 that is in accord with the principles of the present invention. The computer system 200 has a graphical processing system 211 that includes a system platform processor (SPP) 210 and a graphics processor 218. The computer system 200 also includes a media communications processor (MCP) 220, memory device 212 and 214, a central processing unit (CPU) 216, a frame buffer memory 240, a monitor 222, a camera 234, mouse, keyboard, and printer I/O devices 236, hard drives 230, a modem 242, an Ethernet card 246, and an audio system 248.

[0020] The computer system 200 architecture is a distributed processing system that frees the CPU 216 to perform tasks it is best suited for while allowing the graphical processing system 211 to perform the tasks it is best suited for. Specifically, the graphical processing system 211 performs graphics processing tasks that in the prior art were performed by a central processor. While the graphics processor 218 is shown as being external to the SPP 210, in practice it may be beneficial to integrate the graphics processor 218 and the SPP 210 together. Further enhancing distributed processing; the MCP 220 includes an audio processing unit (APU) that performs many of the audio computations that were previously done by a central processor. The MCP 220 also provides for interfacing to USB, modem, and Ethernet devices, another task that was previously performed by a central processor.

[0021] The graphical processing system 211 communicates with the memory devices 212 and 214 over buses 213 and 215 and with the graphics processor 218 over an AGP bus 217. The graphics processor 218 also communicates with the frame buffer 240 via a bus 223. It should be understood that the computer system 200 is exemplary only, and that numerous modifications are possible. For example, the monitor 222 may be driven by the SPP 210 or by a separate display card, there may be more than one monitor 222, various external devices can be added (such as a scanner). In fact, hundreds, possibly thousands of alternatives could exist. However, the computer system 200 is in accord with the principles of the present invention and implements the teachings of United States provisional application number 60/539,787 (attorney docket number P001187) filed January 27, 2004 incorporated herein by reference. Furthermore, the computer system 200 includes bi-directional data mask (DM) lines 299 that extend between the memory devices 212 and 214 and the graphical processing system 211 and between the frame buffer 240 and the graphical processing system 211 (specifically the graphics processor 218). It should be noted that while Figure 1 shows bi-directional data mask (DM) lines 299 that extend between specific memory devices (the frame buffer is a memory) and the graphical processing system 211, in general, the principles of the present invention are also applicable to other portions of computer systems.

[0022] The memory device 212 is a double data rate SRAM while the memory device 214 is a double data rate DRAM. The frame buffer 240 will generally be either an SRAM or a DRAM, but other types of random access memory are contemplated. While those memory devices 212, 214 and 240 are described in more detail subsequently, it should be noted that prior art SRAM and DRAM devices have standardized pin-outs that include read/write strobe lines (DQS) and Data Mask (DM) lines. For simplicity, the read/write strobe lines (DQS) and the signals it propagates are referred to as strobe lines and strobe signals. The strobe lines control the transfer of data to and from the memory devices. In the prior art the DM lines were unidirectional lines that controlled WRITE operation. That is, in prior art memory devices if a DM line is set high, the attached memory device will not WRITE incoming data even when the associated strobe line changed state. If the DM line was LOW, the attached memory device would WRITE incoming data when the associated strobe line changed.

[0023] Figure 2 is a simplified block diagram showing a single data driver 310 that is located within the graphical processing system 211, a bus interface (213; 215; 223), a single receiver 330 that is within a memory device 212, 214 or the frame buffer 240, and exemplary timing relationships between data outputs 312 from a plurality of data drivers 310 and associated strobe signals 314. As suggested in Figure 2, the timing relationship between the data outputs 312 and the strobe signals 314 can be varied. For example, the data signals 312 can be clocked out from the data drivers at fixed times relative to a master clock. Then, the strobe signals 314, which clock the outputs of receivers 330, can be delayed relative to that master clock. The idea is to clock out a special data pattern on the data drivers 310, delay slightly, and then strobe out the same data pattern from the receivers 330. Unfortunately, how much to delay the strobe signals 314 relative to the master clock such that a correct output is obtained from receivers 330 is not readily known, nor in the prior art was there any automated method of correctly determining the correct delay.

[0024] For example, if in Figure 2 a known data pattern was clocked out of data drivers 310, and if the strobe signal 314 changed state before the inputs to corresponding receivers 330 had stabilized for the required minimum time, the receivers 330 would output incorrect data because one or more of the bits from a data driver 310 becomes skewed, that is, temporally offset, before it is clocked into a receiver 330. This condition is suggested by the left side of Figure 2. However, if the strobe signal is properly delayed, the inputs to the receivers 330 would have stabilized and the correct pattern would result. This condition is suggested by the right side of Figure 2. Accordingly, it is desirable to optimize the delay of the strobe signals 314, preferably automatically.

[0025] To automatically optimize the delay, United States provisional application number 60/539,787 (attorney docket number P001187) filed January 27, 2004 discloses a training sequence that trains the graphical processing system 211 to properly delay the strobe signals 314. Figure 3 helps explain a method of automatically adjusting the strobe signal delay during a WRITE training operation using a special training data pattern 410. In Figure 3, the strobe signals 314 are shifted in discrete steps from a minimum delay to a maximum delay. For example, a sequence of strobe signals 314 (not specifically shown in Figure 4, but they have state transitions that occur just before results 420), separated by the discrete step, is

phase delayed relative to master clocks; say from 60 degrees to 120 degrees. Prior to each strobe signal 314 a special data pattern 410 is sent, say at approximately a 1 GHz rate. The output of the receivers 330 are monitored slightly after each strobe signal 314 (to allow the receiver 330 outputs to stabilize). Those outputs are compared to the special data pattern 410 by a special state machine (which is discussed in more detail subsequently). The result 420 of each compare is obtained. If the outputs of the receivers 330 match the special test pattern 410, the result 420 is a pass (P). Otherwise, the result 420 is a fail (F). It should be noted that discrete stepping is not actually required since a variable step can work, but a discrete step may be more convenient. Usually, as shown in Figure 3, the pass results P will be grouped together between fail results.

[0026] As disclosed in United States provisional application number 60/539,787 (attorney docket number P001187) filed January 27, 2004 the foregoing test process is performed automatically and the strobe signal 314 delay is adjusted to occur at or about mid-way in the pass grouping. While the foregoing is beneficial, in practice, the graphical processing system 211 controls the foregoing processes, which produces a problem. The graphical processing system 211sends the strobe signals 314, sends the special data pattern 410, determines the proper delay between the master clocks and the strobe signals, and adjusts that delay. Thus, the graphical processing system 211 needs to know when the compare results 420 are pass or fail. But, those results are within the memory devices 212, 214, or frame buffer 240. That is, the receivers 330 and the comparing state machines are, in practice, within the memory devices 212, 214 and the frame buffer 240. The compare results must be made available to the graphical processing system 211.

[0027] As previously noted, prior art double data rate SRAM and DRAM devices have standardized pin-outs. Those standardized pin-outs do not include a spare I/O pin. Furthermore, most of the standard pins have fixed functions that should not be disturbed. Industry would be highly reluctant to accept a new pin-out to incorporate the required signaling to the graphical processing system 211. However, the memory 212 (SRAM), the memory 214 (DRAM), and the frame buffer 240 are special memory devices that enable the required compare result signaling without changing the existing pin-out structure and while leaving existing pin functions in tact.

[0028] Figure 4 illustrates a portion of the interface between the graphical processing system 211 and a memory device 502. The memory device 502 generically represents a memory device, such as the SRAM memory device 212, the DRAM memory device 214, or the frame buffer 240. Figure 4 also illustrates various functional blocks within the graphical processing system 211 and within the memory device 502. During WRITE de-skew training, that is, when the time delay between master clocks from a master clock 504 and the strobe signals 314 is being determined for WRITE operations, a controller 506 within the graphical processing system 211 signals a data mask (DM) buffer 503 that WRITE training will be performed. In response, the DM buffer 503 changes its DM I/O pin, which connects to a DM line 299, to act as an input. In the prior art, the DM line 299 was always an output of prior art graphical processing systems and an input to prior art SRAM and DRAM devices. Thus, support pins for the DM line 299 are already in-place. The controller 506 also signals a mode control 508 to shift to a WRITE training mode. The mode control 508 then sends a mode control command on a bus 509 to a mode select register 510 in the memory device 502. Current SRAM and DRAM devices already include a mode select register 510 and I/O pins that support the bus 509. However, the memory device 502 implements a mode that is referred to herein as WRITE TRAINING.

[0029] Upon a mode change to WRITE TRAINING, the mode select register 510 enables the outputs of a state machine 514 and changes a DM buffer 516 to assert that the DM line 299 is an output of the memory device 502. At this time, the DM line 299 is driven LOW. Thus, the DM line 299 which in the prior art was a unidirectional line is a bi-directional line in the computer system 200. After the mode change, the controller 506 causes a data driver bank 528 to begin sending out the special data pattern 410 on a bus 540 when clocked by master clocks from the master clock 504. Additionally, the controller 506 enables a delay network 530 to begin sending out a sequence of strobe signals 314 that are delayed at variable times with respect to the master clocks. The strobe signals are applied to the memory device 502 on a bus 541.

[0030] The data on the bus 541 is applied to a receiver bank 548, which is comprised of a bank of receivers 330. The strobe signals clock outputs from the receiver bank 548, which are applied to a state machine 514. When the state machine 514 recognizes the special data pattern 410 it causes the DM buffer 516 to

output a HIGH signal on the DM line 299. When the state machine 516 does not recognize the special data pattern 410 it causes the DM buffer 516 to output a LOW signal on the DM line 299. The signal on the DM line 299 is received by the DM buffer 503 and applied to the controller 506. The signal on the DM is becomes a WRITE training flag that signals the result of WRITE training.

[0031] Based on the foregoing, the controller can use the state of the WRITE TRAINING flag on the DM line 299 to adjust the delay asserted by the delay network 530 so as to cause the strobe signals 314 to be centered in the pass results as described above. The special data pattern 410 is beneficially derived from a pseudo-random bit sequence (PRBS) generator, while the comparison is beneficially performed by a PRBS checker. Random generators produce random bits that effectively test all lines of a data byte as they might occur during normal operation. By using a matching random generator in the checker a comparison can be made.

[0032] Figure 5 illustrates an exemplary PRBS generator 600 while Figure 6 illustrates an exemplary PRBS checker 700. The random generators are initialized with the same seed value. Thus each next "random" state is the same.

[0033] Turning now to Fig. 5, the PRBS generator 600 is a linear feed-back random noise generator comprised of serially-connected D flip flops 602 and 221 multiplexers 604. The output of the last D flip flop 602 forms a line 610 which produces a pattern output of the random generator 600. The signal online 610 is fed back into an exclusive OR gate 606. The PRBS generator 600 is loaded with the seed value from a memory 608 when the line 612 is held high. Line 612 represents a load seed command. After the seed value has been loaded into the 221 multiplexers 604, clock signals on line 614 cause the output on pin 610 to vary in a pseudo random manner.

[0034] Turning now to Fig. 6, which shows the PRBS checker 700. That checker includes a matching pseudo random noise generator comprised of the D flip flop 602 and the 221 multiplexers 604. The pseudo random noise generator is loaded with the same seed value using the memory 608 and a load seed line 614. The output of the linear noise generator is applied to the input of an exclusive OR gate 606 which feeds into another exclusive OR gate 606. The second exclusive OR gate is connected to the output of the first D flip flop 602. An input pattern is applied on line 704, clock supplied on line 612, the data applied from the data receiver bank 548. PRBS generators in both the PRBS 600 and the checker 700 should be the

same since the same seed value was loaded. The output on a pass fail line 706 goes high when the PRBS checker sees the same pattern output by the PRBS generator 600. For that to occur, skew must have been corrected for.

[0035] The above description of exemplary embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form described, and many modifications and variations are possible in light of the teaching above. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications to thereby enable others skilled in the art to best utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated.

CLAIMS:

1. A random access memory device having a bi-directional data mask pin.

2. The random access memory device of claim 1, further including a data mask buffer for receiving input singles on said bi-directional data mask pin and for applying signals to said bi-directional data mask pin.

3. The random access memory device of claim 1, further including a mode select register that controls the directionality of said bi-directional data mask pin.

4. The random access memory device of claim 3, further including a state machine for applying a state machine output to said data mask buffer, wherein said state machine output controls the state of said bi-directional data mask pin when said bi-directional data mask pin is an output.

5. A network, comprising:

a processing system for receiving a signal on a data mask line; and

a random access memory device having a bi-directional data mask pin connected to said data mask line, said random access memory device including a data mask buffer for selectively impressing said signal on said data mask line.

6. The network of claim 5, wherein said random access memory device includes a mode select register that controls the directionality of said bi-directional data mask pin and a state machine that controls the state of said signal when said bi-directional data mask pin is an output.

7. The network of claim 6, wherein said processing system includes a mode control network for producing a mode control signal on a mode line, wherein said mode control signal controls said mode select register.

8. The network of claim 7, wherein said processing system includes a data generator for generating a sequence of de-skew signals on a bus.

9. The network of claim 8, wherein said random access memory device includes a data checker for comparing said de-skew signals against a predetermined pattern, and where said signal on said data mask line depends on whether said data checker finds said predetermined pattern.

10. The network of claim 8, wherein said processing system includes a circuit that produces timed strobe signals, and wherein said data checker compares said de-skew signals after they are delayed by the time of said strobe signals.

11. A method of WRITE training comprising the steps of:

sending a plurality of predetermined data patterns to a memory device, wherein each predetermined data pattern is sent upon the occurrence of a master clock;

sending a plurality of strobe signals, wherein the strobe signals are delayed relative to the master clock, and wherein the delay of at least two strobe signals are different;

receiving the plurality of data patterns, wherein each data pattern is clocked in by a different strobe signal;

comparing the received plurality of data patterns to the plurality of predetermined data patterns, wherein each received data pattern is compared to an associated predetermined data pattern to determine a comparison result; and

setting the state of a data mask pin based on the comparison results.

12. The method of claim 11, wherein the step of sending a plurality of predetermined data patterns includes the step of generating a pseudo-random bit pattern.

13. The method of claim 12, wherein the step of generating a pseudo-random bit pattern includes applying a predetermined seed value to a pseudo-random generator.

14. The method of claim 13, wherein the step of comparing the received plurality of data patterns to the plurality of predetermined data patterns includes the step of generating a second pseudo-random bit pattern.

15. The method of claim 14, wherein the step of generating the second pseudo-random bit pattern includes the step of applying the predetermined seed value to a second pseudo-random generator.

16. A method of WRITE training, comprising the steps of

setting a memory mode of a memory device to a WRITE TRAINING mode;

converting the status of the memory device data mask pin to an output when the WRITE TRAINING mode is entered;

sending a plurality of predetermined data patterns to the memory device, wherein each predetermined data pattern is sent upon the occurrence of a master clock;

sending a plurality of strobe signals to the memory device, wherein the strobe signals are delayed relative to a master clock, and wherein the delay of at least two strobe signals are different;

receiving the plurality of bit patterns, wherein each bit pattern is clocked in by a different strobe signal;

comparing the received plurality of bit patterns to the plurality of predetermined bit patterns, wherein each received bit pattern is compared to an associated predetermined bit pattern to determine a comparison result; and

setting the state of a data mask pin based on the comparison results.

17. The method of claim 16, wherein the step of sending the plurality of predetermined bit patterns includes the step of generating a pseudo-random bit pattern.

18. The method of claim 17, wherein the step of generating a pseudo-random bit pattern includes applying a predetermined seed value to a pseudo-random generator.

19. The method of claim 18, wherein the step of comparing the received plurality of bit patterns to the plurality of predetermined bit patterns includes the step of generating a second pseudo-random bit pattern.

20. The method of claim 19, wherein the step of generating the second pseudo-random bit pattern includes the step of applying the predetermined seed value to a second pseudo-random generator.

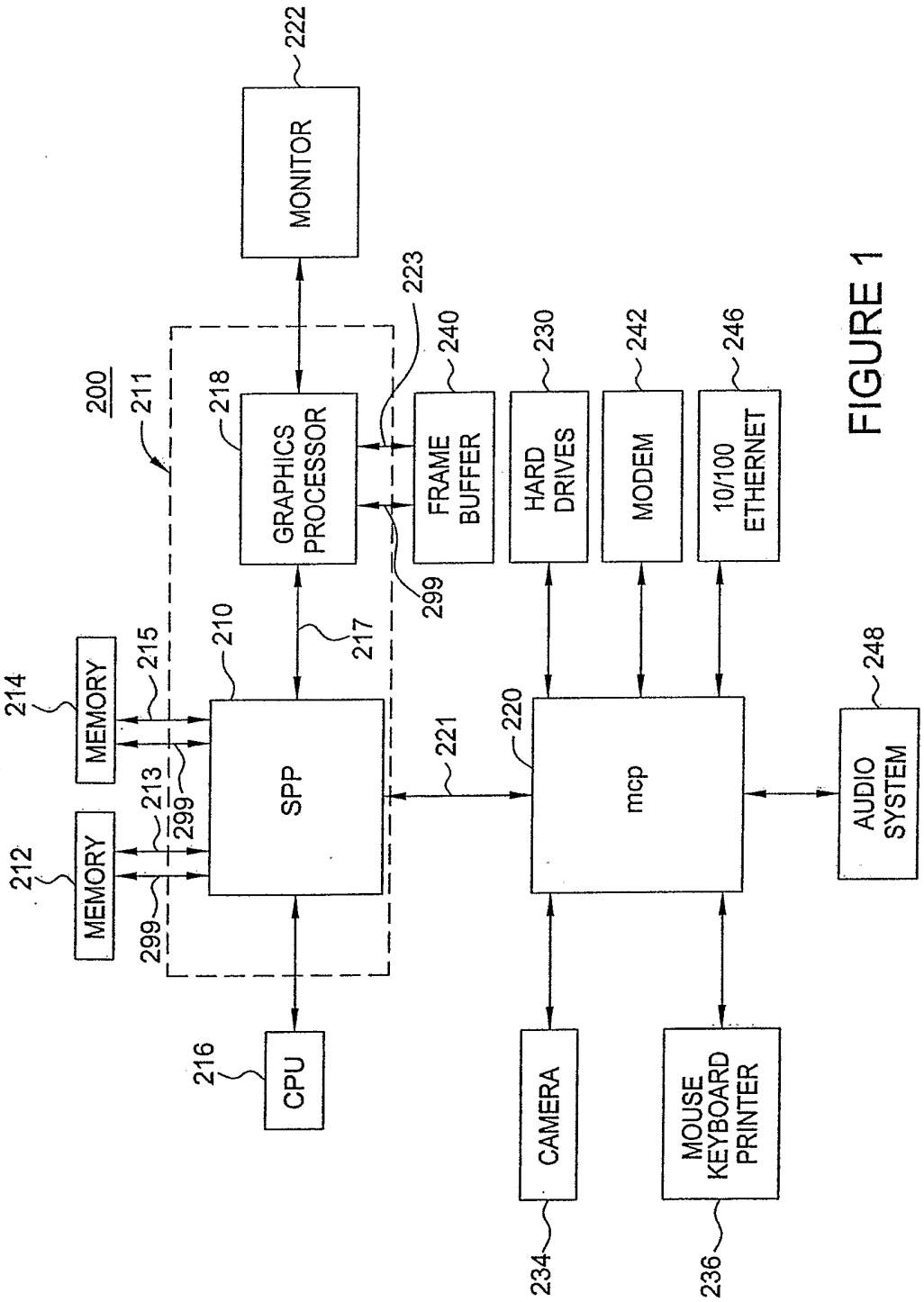
MONITOR
222
GRAPHICS PROCESSOR
218
FRAME BUFFER
240
223
HARD DRIVES
230
MODEM
242
10/100 ETHERNET
246
200
211
299
210
217
SPP
MEMORY
214
215
MEMORY
212
213
299
299
221
220
mcp
AUDIO SYSTEM
248
CPU
216
CAMERA
234
MOUSE KEYBOARD PRINTER
236

FIGURE 1

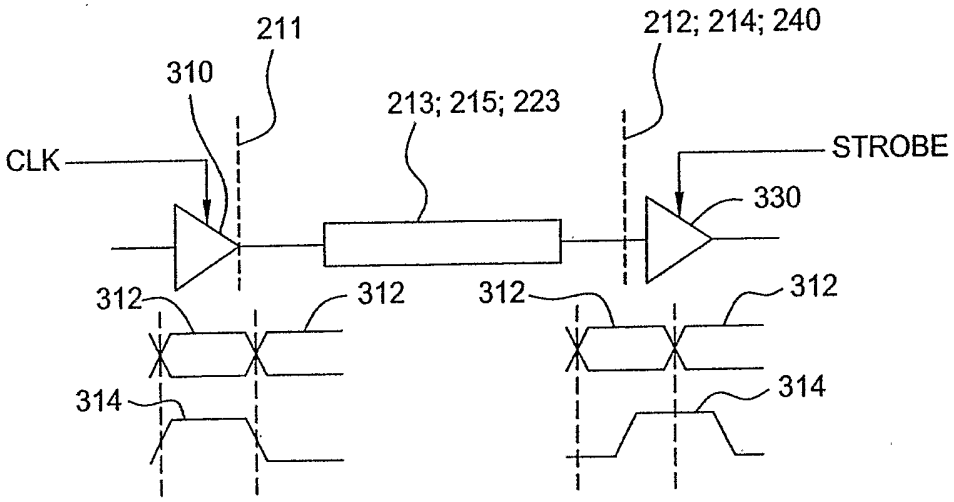
211
212; 214; 240
310
213; 215; 223
CLK
STROBE
330
312
312
312
312
314
314

FIGURE 2

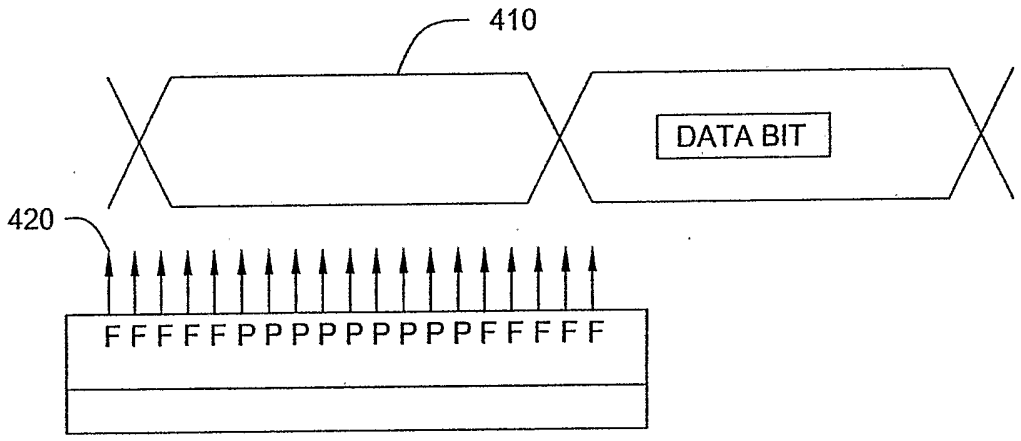

FIGURE 3

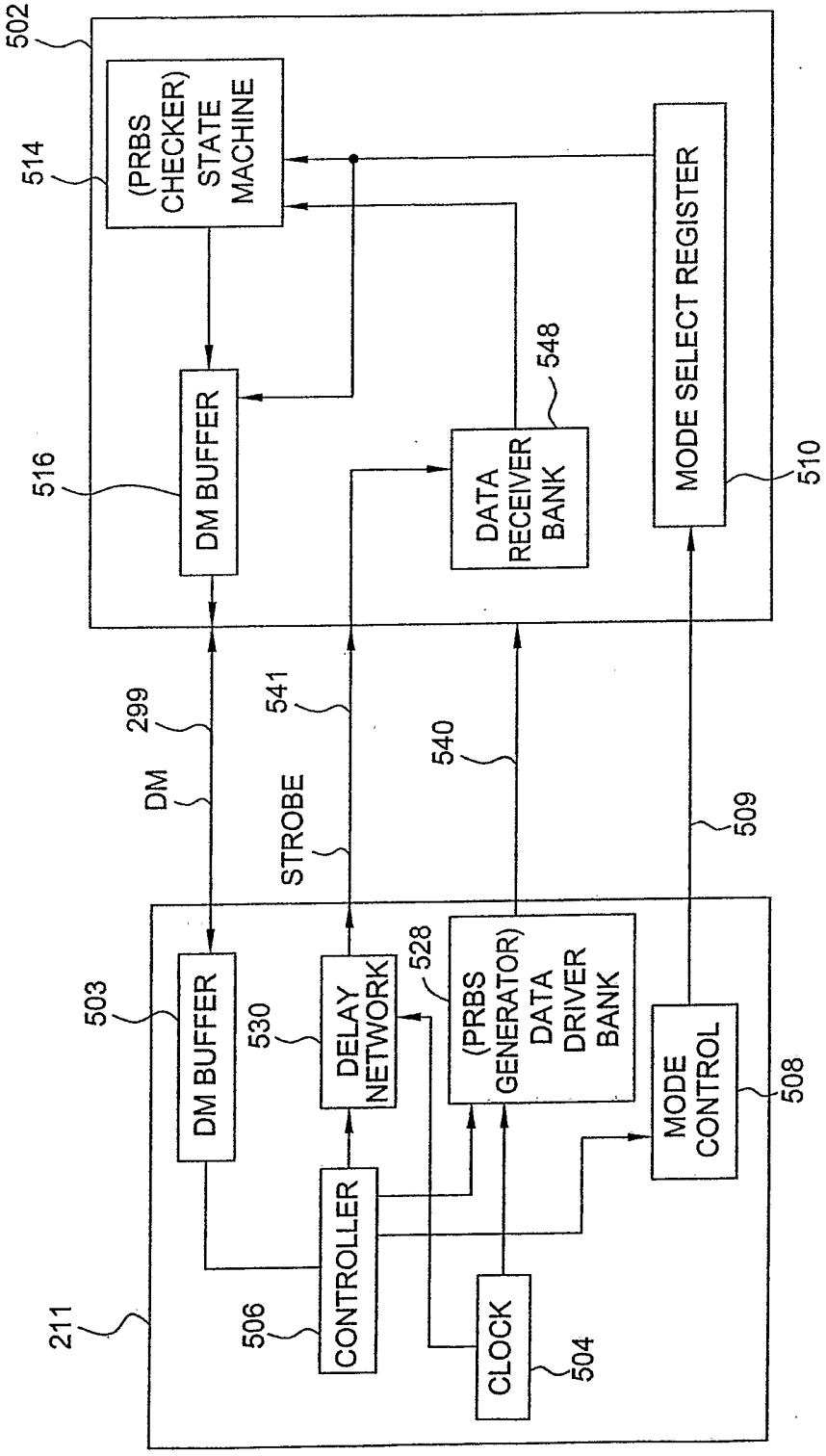
502
(PRBS CHECKER) STATE MACHINE
514
DM BUFFER
516
DATA RECEIVER BANK
548
MODE SELECT REGISTER
510
299
DM
541
STROBE
540
509
503
DM BUFFER
530
DELAY NETWORK
528
(PRBS GENERATOR) DATA DRIVER BANK
MODE CONTROL
508
211
506
CONTROLLER
CLOCK
504

FIGURE 4

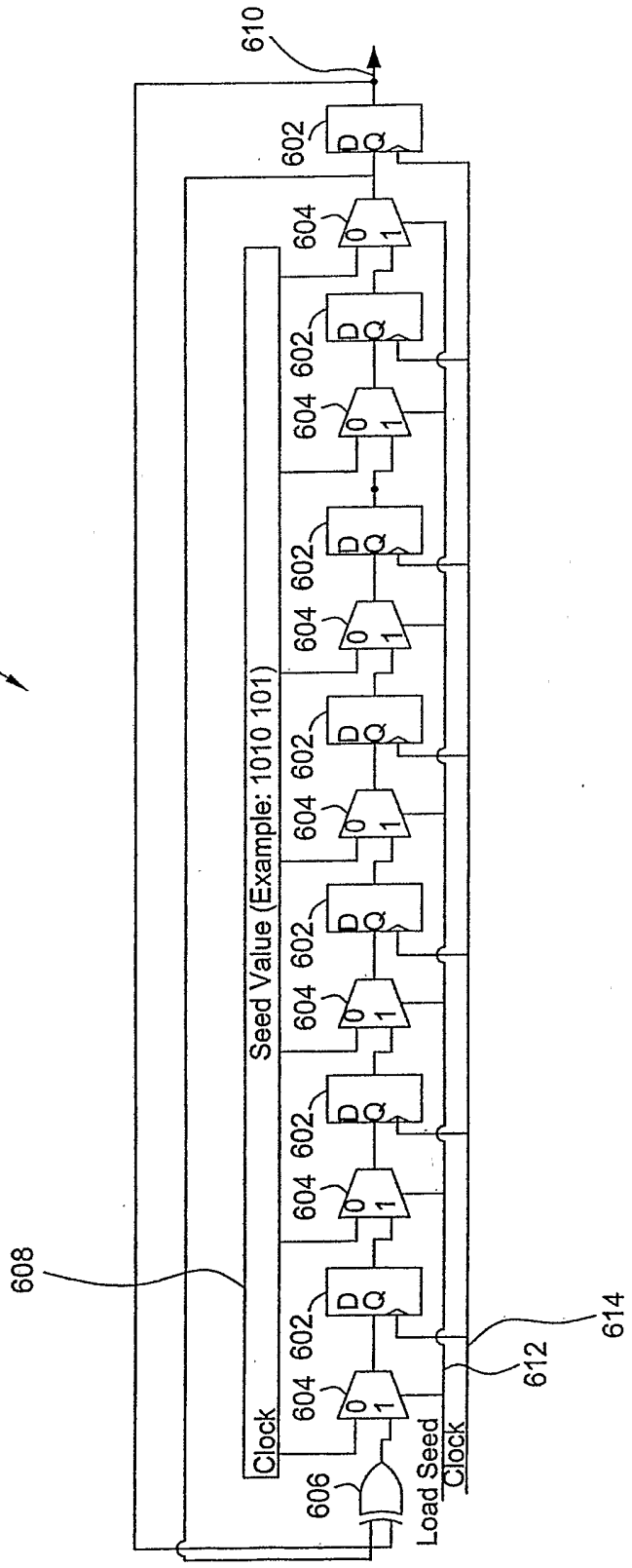
600
610
602
604
608
606
612
614
Seed Value (Example: 1010 101)
Clock
Load Seed
Clock
D
Q
0
1

FIGURE 5

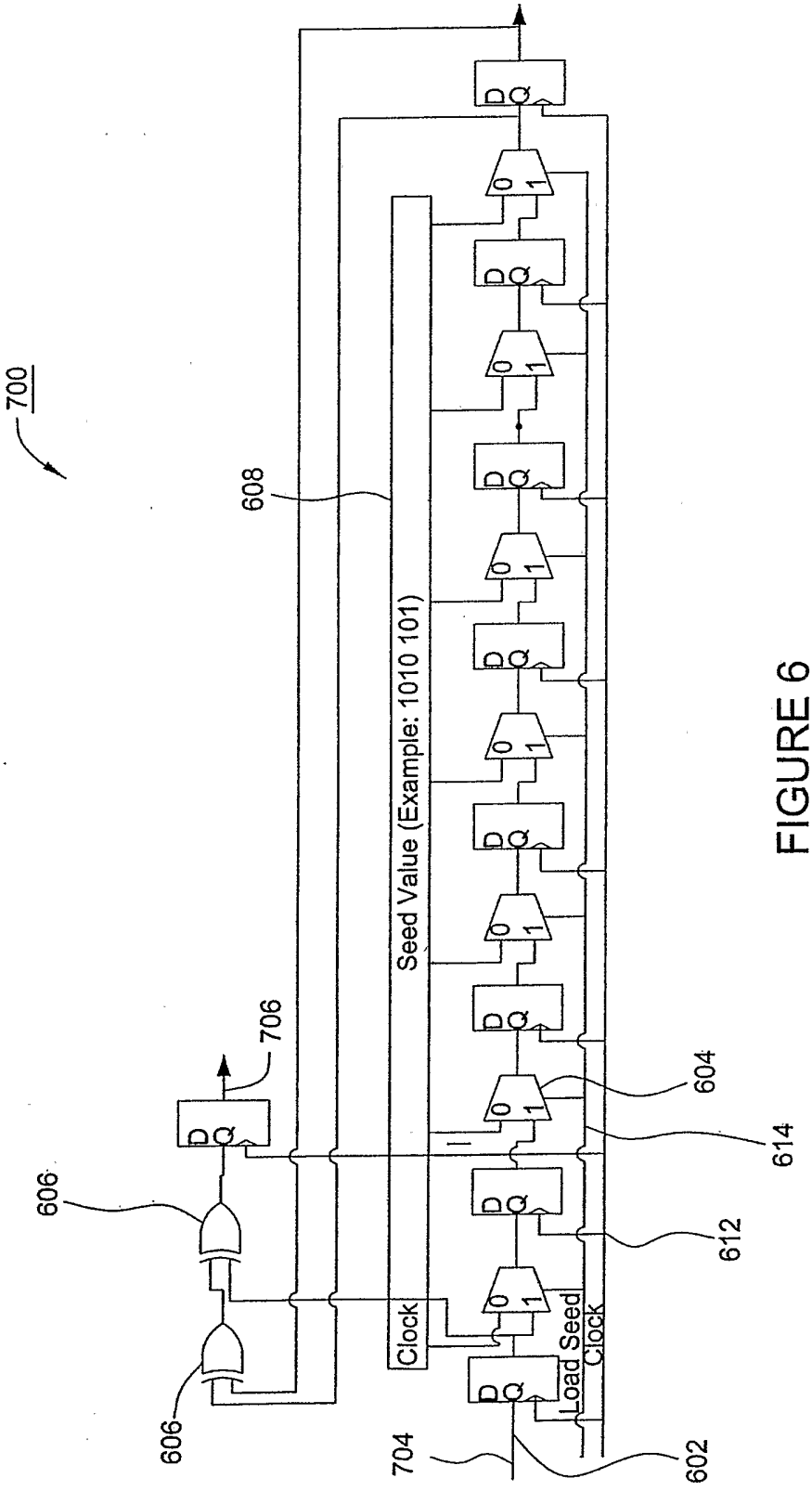
700
608
Seed Value (Example: 1010 101)
706
606
606
604
614
612
Clock
Load Seed
Clock
704
602

FIGURE 6

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2005/013713

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G11C7/10

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2002/034119 A1 (LEE JAE-HYEONG ET AL) 21 March 2002 (2002-03-21) paragraph '0042! - paragraph '0051!; figures 5,6	1-9
X	EP 1 336 972 A (ATI TECHNOLOGIES INC; ELPIDA MEMORY INC) 20 August 2003 (2003-08-20)	1-9
A	paragraph '0014! - paragraph '0022!; figures 2-4	10-20
A	US 6 574 760 B1 (MYDILL MARC) 3 June 2003 (2003-06-03) column 6 - column 11	1-20

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
4 August 2005	11/08/2005

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Colling, P

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US2005/013713

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		CN 1345070 A	17-04-2002
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US 6574760 B1	03-06-2003	NONE	