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CONVENTION APPLICATION FOR A PATENT

610249

We, MICROELECTRONICS AND COMPUTER TECHNOLOGY CORPORATION, a Delaware Corporation of 3500 West Balcones Center Drive, Austin, Texas 78759, United States of America, hereby apply for the grant of a Patent for an invention entitled "CUSTOMIZABLE CIRCUTRY" which is described in the accompanying complete specification.

This application is a Convention application and is based on the Application Numbered 102,172 for a patent or similar protection made in United States of America on 29th September 1987.

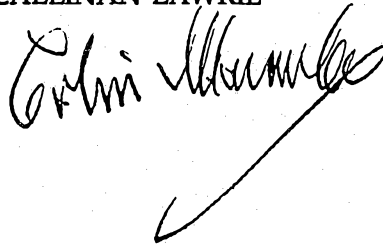
Our address for service is care of CALLINAN LAWRIE, Patent Attorneys, of 278 High Street, Kew, 3101, Victoria, Australia.

D A T E D this 28th day of November, 1990.

MICROELECTRONICS AND COMPUTER
TECHNOLOGY CORPORATION

By their Patent Attorneys:

CALLINAN LAWRIE



To: The Commissioner of Patents.

APPLICATION ACCEPTED AND AMENDMENTS

ALLOWED 26.2.91.

AUSTRALIA
Patents Act 1952-1973

Regulation 11 (1)
Regulation 11 (2)

Declaration in Support of
(a) A Convention Application
(b) An Application
for a Patent or Patent of Addition

In support of the Application/Convention Application made by
(c) Microelectronics and Computer Technology Corporation
(hereinafter termed "said Company")
for a patent/patent of addition for an invention entitled:

(d) "CUSTOMIZABLE CIRCUITRY"

I/~~we~~ (e) Palle F. Smidt

of (f) 3500 West Balcones Center Drive, Austin, Texas,
U.S.A. 78759

do solemnly and sincerely declare as follows:—

1. (g) I ~~am/we~~ ~~are the applicant(s) for the patent/patent of addition~~
or

(h) I am/~~we~~ ~~are authorized by~~ Microelectronics and Computer
Technology Corporation
the applicant for the patent/~~patent of addition~~ to make this declaration on its behalf.

2. (i) The basic application(s) as defined by Section 141 of the Act was/were made
in United States of on the 29th day of September 19 87
America
by
David H. Carey

3. (j) ~~I am/we are the actual inventor(s) of the invention referred to in the basic application.~~
or

(k) I am/we are the actual inventor(s) of the invention referred to in the basic application.
or

(l) David Harrison Carey
of 10306 Yucca Drive, Austin, Texas, U.S.A. 78759
is/~~are~~ the actual inventor(s) of the invention and the facts upon which
I/~~am/we~~ ~~are~~ the said Company is entitled to make the application are as follows:

(m) The said Company is the assignee of the said invention
and of the priority rights from the said actual inventor
who made the application in the United States of
America on the date claimed.

4. The basic application referred to in paragraph 2 of this Declaration was the first
application made in a Convention country in respect of the invention the subject of the
application.

(n) Declared at Austin, Texas, this 7th day of October 1988.
U.S.A.

SIGN

X Palle F. Smidt
Senior Vice-President

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CUSTOMIZABLE CIRCUITRY

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(56) Prior Art Documents
AU 32170/89 H01L 23/12 23/50
AU 30033/89 H01R 23/72 H05K 1/18 3/40
US 4458297

(57) Claim

1. A multi-layer programmable electrical interconnect for connecting electrical components including:

an X-conductor layer comprising a plurality of substantially parallel channels, each channel including a plurality of electrically conductive first set of segments of substantially uniform length arranged end-to-end, a majority of segment ends in said X-conductor layer extending to a customization surface of said interconnect;

a Y-conductor layer comprising a plurality of substantially parallel channels, each channel including a plurality of electrically conductive second set of segments of substantially uniform length non-planar to said first set of segments and arranged end-to-end, a majority of the segment ends in said Y-conductor layer extending to said customization surface,

the X-conductor and Y-conductor layer being positioned so that the channels of the X- and Y-layers overlap;

a plurality of programmable junctions formed on the customization surface in a plurality of programming tracks which extend diagonally with respect to the channels of the X- and Y- layers, each programmable junction comprising segment ends of two adjacent X-conductor layer segments in the same X-conductor layer channel, and segment ends of two adjacent Y-conductor layer segments in the same Y-conductor layer channel, the segment ends in each programmable junction being positioned whereby selective electrical linkage can be accomplished on the customization surface between all combinations of segment ends forming the programmable junction, thereby permitting selective X to X, Y to Y, and X to Y linkage between the segment ends forming each programmable junction, as well as combinations thereof.

Australia

PATENTS ACT 1952

Form 10

COMPLETE SPECIFICATION

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Name of Applicant: MICROELECTRONICS AND COMPUTER TECHNOLOGY CORPORATION

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United States of America

Actual Inventor: DAVID H. CAREY

Address for Service: CALLINANS [REDACTED] Patent Attorneys, of
48-50 Bridge Road, Richmond, State of Victoria, Australia.

Complete Specification for the invention entitled: "CUSTOMIZABLE CIRCUITRY"

The following statement is a full description of this invention, including the best method of performing it known to me:—

* Note: The description is to be typed in double spacing, pica type face, in an area not exceeding 250 mm in depth and 160 mm in width, on tough white paper of good quality and it is to be inserted inside this form.

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CUSTOMIZABLE CIRCUITRY

15 BACKGROUND OF THE INVENTION

20 The present invention relates to customizable circuitry, and particularly to customizable circuitry which includes an interconnect for receiving and electrically connecting electrical devices and tape automated bonding chip designs. The invention relates to an interconnect which can be produced in gross with an undedicated, universal structure and subsequently customized to a specific application with minimal effort and fabrication, and to a tape automated bonding chip design for use therewith. Further, the invention also concerns a method for manufacturing the interconnect and chip design.

25
30 Customizable circuitry, as used herein, refers to that circuitry in which some of the device interconnections are not made during the initial manufacture of the circuitry, but are deferred. This deferral allows the circuitry to be manufactured in large quantities with generic properties, with the specific design details being applied later by the user in a final
35

1 step called "customization". Integral to customizable
circuitry is a generic interconnect structure coupled with
a method of bonding the leads of integrated circuit chips
to that interconnect structure.

5 Interconnects, as building blocks for electronic
circuitry and microcircuitry, typically receive and
support further electrical devices, for example,
substrates, i.e., smaller scale interconnects, integrated
10 chips, capacitors, resistors and so forth, which can be
electrically connected to one another to provide larger,
more complex electrical structures. The interconnects
typically have a sandwich-type structure through which a
series of wires extend. The wires connect the electrical
15 devices attached to the interconnect according to a plan
specified by the interconnect user.

The interconnects are used in a multiplicity of
designs, each requiring unique electrical circuitry.
Presently, in a majority of the interconnects, the wiring
plan is fixed at an early stage of manufacture. In other
20 words, the manufacturer lays down the interconnect wiring
according to a specific, predetermined plan. Such
interconnects will be referred to as "design specific."
As is readily apparent, design specific interconnects
cannot be mass produced and are, therefore, time and cost
25 intensive.

Recognizing the shortcomings of design-specific
interconnects, there arose a need in the interconnect
industry for an interconnect design which could be
mass-produced in an unspecified manner and thereafter
30 programmed to produce whatever wiring plan is required by
the user. Such interconnects will be referred to as
"programmable interconnects" and the final step of
imposing the wiring plan on the interconnect will be
referred to as "customization."

35 A previous attempt at programmable interconnect
design is disclosed in U.S. Patent No. 4,458,297 to Mosaic
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1 Systems, Inc. The Mosaic design provides interconnect
wiring in the form of a grid with wires in one direction
forming one plane and orthogonal wires forming a second
plane. Positioned between the two sets of wires is a
5 layer of amorphous silicon which, though originally
non-conductive, can be rendered conductive at specified
points of wire overlap. The selective conductivity is
achieved through crystallization of the amorphous silicon
by applying a voltage differential across the orthogonal
10 wires. The electric field produced by this voltage
differential causes the silicon in the region of the
overlapped wires to crystallize and become conductive.
Therefore, an electrical path is formed between the
overlapped wires.

15 The Mosaic structure is advantageous in that it
provides for the mass production of undedicated
interconnects which can be customized by the manufacturer
or by the end user at a later stage of manufacture. The
Mosaic interconnect, however, has many drawbacks. For
20 example, because of the electrical properties required, a
limited number of materials can be used. Amorphous
silicon is the only suggested material for use as the
intermediate layer. Also, while a limited number of
metals might be used for the interconnect wiring, aluminum
25 is by far the best candidate because its properties are
compatible with the amorphous silicon. The density of the
Mosaic grid, and specifically the proximity of the wires
in the overlap region, is limited since a sufficiently
large area about the overlap region is required to avoid
30 shorting of adjacent wires during crystallization. In
other words, the electric field forms an area of flux
between the overlapped wires extending into the area
between adjacent overlap regions. If the wires are placed
too close together, this region of flux may cause adjacent
35 regions to bleed together and short the adjacent wires.

1 Another disadvantage of the Mosaic design is that
it is only an additive process. In other words, the wire
routing is formed by adding electrically conductive
segments, i.e., the crystalline silicon bridges. The
5 design is not subtractive. Accordingly, it is very
difficult, if not impossible, to make changes to the
customized interconnect. The difficulty in altering the
customized wiring makes engineering changes impractical.
A further and very crucial disadvantage in the Mosaic
10 design results from the fact that each additive step,
i.e., creation of the silicon bridge, excludes both
affected orthogonal wires from further utilization in the
interconnect plan, except as to this one route. In other
words, if X1 and Y1 wires are bridged to provide an
15 interconnect path, these wires, or segments thereof,
cannot be used to provide another interconnect path, for
to do so would result in a shorting of the two paths
together. This characteristic of the Mosaic interconnect
severely limits the complexity of the interconnect for a
20 given interconnect area. This complexity limit affects the
interconnect efficiency for the available channels, called
channel utilization. It is desirable to have high channel
utilization since a given interconnect can be performed
with fewer channels if high channel utilization is present.

25 In addition to Mosaic's electrical customization
approach, mechanical customization has also been used in
some areas. For example, "Wire-Wrap" involves the use of
an interconnect having a number of metal pins extending
orthogonally from the interconnect surface. After the
30 wiring plan has been specified, the appropriate pins can
be connected by wrapping wires about the appropriate
pins. Because of the forces involved, large, rigid pins
are needed along with large tools to wrap the wire
securely. The process is time consuming, since only one
35 wire is added at a time, and cannot be used for small

1 scale circuits such as integrated circuits because of the
large pins and tools required.

Another mechanical customization approach is the
use of wire bonding to interconnect bonding pads provided
5 on the surface of an integrated circuit. The interconnect
is provided by welding or sputtering a thin wire onto a
metal bonding pad at each end of the desired interconnect
path. This approach has many disadvantages, however,
including very poor area efficiency. For example, the
10 sputtering used requires the use of large bonding pads
with large spaces between them to assure that the
sputtering process does not destroy the pad or cause a
short circuit. Further, because the interconnect wires are
not insulated, the density is restricted to those
15 interconnect paths that do not require crossed wires.
Thus, this procedure has most of the disadvantages of wire
wrap with the additional disadvantage that interconnect
paths cannot cross each other.

Turning now to the problem of mounting the
20 integrated circuit chips, it is conventional practice to
mount such chips on interconnect structures which serve to
electrically connect the chips. The integrated circuit
chips are frequently mounted on carrier film, or tape, by
a process known as "Tape Automated Bonding" (TAB). To
25 achieve efficiency in the resulting customizable circuit,
it is important to match the chip bonding technique used
to the particular interconnect structure.

Accordingly, there exists a need in the art for
an improved customizable circuitry including a
30 programmable interconnect which can be mass produced to
include an unspecified wiring plan and which can be
subsequently specified in the later stages of manufacture
or by the end-user with a minimum of effort and time, and
which can provide a dense interconnect structure which can
35 be practiced at both the printed circuit and integrated

circuit levels, and a tape automated bonding structure compatible with such interconnects.

SUMMARY OF THE INVENTION

It is an object of the present invention is to provide an interconnect
5 for customizable circuitry which can be produced as an undedicated interconnect
and then customized based on user needs.

Another object of the present invention is to provide an interconnect
structure which can be formed into interconnects of a variety of sizes.

Still another object of the present invention is to provide an
10 interconnect which can be formed from a variety of materials.

Yet another object of the present invention is to provide a low cost
interconnect.

According to the present invention there is provided a multi-layer
programmable electrical interconnect for connecting electrical components
15 including:

an X-conductor layer comprising a plurality of substantially parallel
channels, each channel including a plurality of electrically conductive first set of
segments of substantially uniform length arranged end-to-end, a majority of
segment ends in said X-conductor layer extending to a customization surface of
20 said interconnect;

a Y-conductor layer comprising a plurality of substantially parallel
channels, each channel including a plurality of electrically conductive second set
of segments of substantially uniform length non-planar to said first set of
segments and arranged end-to-end, a majority of the segment ends in said Y-
25 conductor layer extending to said customization surface;

the X-conductor and Y-conductor layer being positioned so that the
channels of the X- and Y-layers overlap;



a plurality of programmable junctions formed on the customization surface in a plurality of programming tracks which extend diagonally with respect to the channels of the X- and Y- layers, each programmable junction comprising segment ends of two adjacent X-conductor layer segments in the same X-conductor layer channel, and segment ends of two adjacent Y-conductor layer segments in the same Y-conductor layer channel, the segment ends in each programmable junction being positioned whereby selective electrical linkage can be accomplished on the customization surface between all combinations of segment ends forming the programmable junction, thereby permitting selective X to X, Y to Y, and X to Y linkage between the segment ends forming each programmable junction, as well as combinations thereof.

Further objects, features and advantages of the present invention will be apparent from a review of the detailed description of preferred embodiments which follows, when considered together with the drawings, a brief description of which follows.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is an isometric view of a presently available substrate.

Figure 1A is an enlarged isometric sectional view of a blind via of the prior art non-universal substrates.

Figure 2 is an isometric view of an interconnect according to the present invention.

Figure 2A is an enlarged sectional view of the pillar interconnect between the wiring structure of Figure 2.



1 Figure 3 is a plan view of the interconnect of
Figure 2.

 Figure 4 is an enlarged plan view of the diagonal
interconnect region of Figure 3 according to one
5 embodiment of the present invention.

 Figure 4A is an enlarged plan view of the
diagonal interconnect region of Figure 3 according to
another embodiment of the present invention.

 Figure 5 is an enlarged plan view of the diagonal
10 interconnect region of Figure 3 according to one
embodiment of the present invention.

 Figure 5A is an enlarged plan view of the
diagonal interconnect region of Figure 5 after subsequent
processing.

15 Figure 6 is a plan view of an interconnect
according to the present invention having a chip bonded
thereto.

 Figure 7 is an enlarged cross-sectional view of
the specified area of Figure 6.

20 Figure 8 is an enlarged isometric view of the
area specified in Figure 6 according to one embodiment of
the present invention.

 Figure 8A is an enlarged isometric view of the
area specified in Figure 6 according to another embodiment
25 of the present invention.

 Figure 9 is an enlarged isometric view of the
area specified in Figure 6 according to another
embodiment.

 Figure 10 is a plan view of multiply overlaid and
30 interconnected interconnects according to the present
invention and having chips attached thereto.

 Figure 11 is a cross-sectional view of one
embodiment of the interconnect of the present invention.

 Figure 12 is a cross-sectional view of another
35 embodiment of the interconnect of the present invention.



1 Figure 13 is a cross-sectional view of yet
another embodiment of the interconnect of the present
invention.

 Figure 14 is a schematic view of a carrier film
5 having a chip attached thereto.

 Figure 15A is a schematic representation of OLB's
positioned according to a peripheral bonding scheme.

 Figure 15B is a schematic representation of OLB's
positioned according to an area bonding scheme.

10 Figure 16 is an enlarged plan view of a chip lead
design.

 Figure 17 is an enlarged sectional plan view of a
chip lead design.

 Figure 18 is a plan view of the preferred
15 embodiment of the programming tracks and programming
junctions.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

20 Figure 1 is an isometric, cut-away view
illustrating one type of programmable interconnect design
presently available, i.e., the Mosaic Systems, Inc.
interconnect discussed previously. The substrate 10
includes a set of aluminum wires 12 extending parallel to
25 one another and joined by amorphous silicon programmable
bridges 14 to a set of aluminum wires 16 extending
orthogonally to the wires 12. The silicon bridges are
originally non-conductive amorphous silicon, but through
crystallization under an electric field are rendered
30 conductive. The wires 16 form a plane separate from and
above the plane formed by the wires 12. The programmable
bridges 14 form available electrical pathways between the
wires 12 and 16. The wires are covered by the layer 20.
The layer 20 is provided with a number of pads 22 which
35 are connected electrically to the wires 16 by further

1 bridges 24. The pads 22 are selectively connected to
underlying voltage planes 26, 28 by extended bridges 30,
32, respectively. The pads 22, in turn, are connected to
chips 34 by wire bonds 36 extending from the chips to the
5 pads.

During the original phase of manufacture, the
above design is not specified, i.e., a particular wiring
scheme is not fixed. Once an application is identified and
a specific wiring scheme determined, the programmable
10 bridges can be electrically changed to conductive bridges,
thus producing the requisite customized wiring scheme.
While this design overcomes the limitations inherent in
the design specific interconnects which require complete
customization, it too is limited. First, this prior art
15 structure is limited in the materials which can be used.
Specifically, amorphous silicon must be used in order to
achieve the programmable bridge property necessary for
subsequent programming. As has also been noted, the
density of the Mosaic design is limited by processing
20 characteristics. Additionally, once a wire has been used
to form one wire route, no matter how short a segment is
needed, the entire wire must be used and thereby rendered
incapable of receiving further routing; otherwise, the two
routes would short circuit.

25 The interconnect of the present invention has a
sandwich structure. The actual number and types of layers
depend on the particular application. Figure 2
illustrates one type of interconnect structure according
to the present invention. As illustrated, the
30 interconnect 40 comprises an optional first plane 42.
Plane 42 can be an electrically conductive plane, for
example, a ground plane or a power plane. Additionally,
both power and ground planes may be provided. The actual
number and type of planes will depend upon user needs.
35 For present purposes, the planes will simply be referred



1 to as conductive planes. The conductive planes, besides
their specific purposes, also help to control the
impedance of the interconnect.

Extending above plane 42 is a plurality of wires
5 44 which are labeled as y-axis wires for the sake of
convenience and later reference. The wires 44 extend
essentially parallel to one another and are coplanar.
Though not shown, an insulation layer is typically
positioned between the plane 42 and the wires 44, when
10 plane 42 is present.

A second set of wires 46 is positioned above the
wires 44 and extends essentially perpendicularly thereto.
These wires have been marked as x-axis wires for the sake
of convenience and later reference. The wires 46, like
15 wires 44, extend essentially parallel to one another and
are coplanar. The wires 44 and 46 form what will be
referred to as y- and x-planes, respectively. An
insulation layer, not shown in this view, is provided
between the x- and y-planes. While the wires described
20 here are orthogonally positioned, this is not required.
Any relationship between the wires is possible, the only
requirement being that the wires not be parallel so that
the wires do overlap.

Finally, a customization plane 48 is positioned
25 above the wires 46. The customization plane 48 generally
provides a surface on which additional structures can be
attached for carrying out other electrical processes.
These structures include device attach pads, test pads,
and facilities for engineering changes, defective line
30 rerouting and overflow connections. The plane is formed
so as to allow access to the terminal portions of the
wires 44 and 46, as will be described in more detail
immediately below.

As Figure 2 illustrates, the x-and y-wires are
35 formed into line segments by terminating the wires at



1 certain select areas of wire overlap 50. For example,
wire 52, extending in the y-direction, terminates in the
area of overlap 50 with wire 54, extending in the
x-direction. The terminal portions 56, 58 of the y-wire
5 52 and the terminal portions 60, 62 of the x-wire 54
extend upward in the z-direction. Access areas 63 are
provided in the customization plane 48 to provide access
to the ends 56, 58, 60, 62 of the wires.

The terminal ends 56, 58, 60 and 62 comprise what
10 will be referred to hereinafter as a "programmable
junction." The ends of the wires are linked to one
another at the programmable junctions to establish the
required wiring sequence in the interconnect, commonly
referred to as routing. The access areas 64 in the
15 customization plane 48 allow the end user to access the
terminal ends and interconnect same to achieve any routing
scheme desired.

It has been discovered, in accordance with the
present invention, that preferable and advantageous wiring
20 results are achieved by forming the programmable junctions
in a diagonally-extending pattern. As Figure 2
illustrates, a diagonal track 64 has been formed through
and across the customization plane 48 and the underlying
diagonally-extending programmable junctions 66 are
25 accessible therethrough. These diagonally-extending
regions will be referred to as "programming tracks."

Figure 3 is a plan view of the upper
customization plane 48 and interconnect 40 shown
isometrically in Figure 2. The programming tracks 64 and
30 programming junctions 66 can be seen in Figure 2. The
programming tracks can extend in the same direction (a
single pattern) or can be perpendicularly positioned to
extend diagonally across the interconnect in either
direction (a "double" pattern). The double track pattern,
35 on the one hand, is advantageous since it provides a



1 greater number of programmable junctions and therefore,
greater flexibility for routing purposes. However, for
most applications, the single track pattern will be
sufficient. This is true for a variety of reasons.

5 First, the single track pattern is simpler to design.
Second, it is more compatible with integrated chips having
tape automated bonding (TAB), a common means of chip
bonding to be discussed below. Also, the single pattern
typically offers more than enough programmable junctions
10 for wiring purposes, both as to flexibility and
directional changes, i.e., bus-type structures. Also,
because the "single" track pattern utilizes fewer
programmable junctions than the "double" track pattern, it
is advantageous because excessive programmable junctions
15 may detrimentally affect the electrical properties, as
well as the yield, i.e., manufacturing defects.

The programming tracks extend diagonally across
the interconnect. Preferably, and especially with
orthogonal wiring, the programming tracks extend
20 diagonally across the interconnect at a 45 degree angle.
However, the tracks can assume any angle depending solely
on user needs. Also, the programming tracks do not have
to be linear. The tracks can assume any geometry, again
depending on user needs. Saw-tooth tracks serpentine
25 tracks and others are possible. The pitch (P), as a
measure of the distance between successive programming
tracks, is determined by the required flexibility of
interconnect routing. The selection of the pitch is
determined by the balance of the advantage of more
30 locations at which directions may be changed and increased
customization layer surface for attachment, testing, and
additional wiring. The pitch (P) as a measure of the
distance between successive x-wires or y-wires is as small
as possible in order to increase the number of possible
35 programmable junctions.

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1 Figure 18 illustrates a preferred embodiment of
the programming tracks 64, and especially the programmable
junctions 66 therein. As shown, the programmable
junctions of adjacent wires are offset from one another
5 along the programming track. This design allows higher
line density in cases where the via diameter is greater
than the line width, or in any similar situation where the
programmable junction tends to limit the line-to-line
spacing. This configuration also allows wiring to pass
10 between the programmable junctions on the upper
(customization) plane.

The diagonal programmable tracks are also
advantageous because the length of connections between the
wires is minimized. As Figure 3 illustrates, the
15 programmable junctions 66 position the four wire ends from
the x-and y-wires in close proximity to one another.

The connections between the wires are
illustrated, for example, in Figure 2A. Figure 2A is an
enlargement of an area of overlap, such as overlap 50 of
20 Figure 2. For reference purposes, the same reference
numbers will be used. As shown, wire 52, extending in the
y-direction, and wire 54, extending in the x-direction,
terminate at overlap 50. The wires extend in different,
but parallel, planes. Extending upward from the wires are
25 electrically conductive pillars 70. These pillars 70
extend upward to a plane which forms the programmable
junctions. As Figure 2A shows, because wire 54 is in a
plane above the wire 52, the length of the pillars from
wire 54 to the interconnect plane is less than from wire
30 52 to the plane. The plan view of the pillars as shown in
Figures 2A and 3 place the terminal ends thereof in
essentially a T-shape. Advantageously, the pillars may
extend along a diagonal orthogonal to the programming
tracks. Such a layout facilitates routing access across
35 programming tracks for wiring on the customization plane.



1 The final component in the interconnect region is
the link 72 between the pillars 70. The link 72 extends
from the upwardly facing ends of the pillars and provides
an electrical connection between the pillars, and thus the
5 underlying wire structure.

 The process of specifying and then forming the
interconnections between the wires represents the
customization of what is an otherwise undedicated
interconnect. Through customization, the various wire
10 segments can connect in a variety of different manners as
depicted by Figures 4, 4A, 5 and 5A. Figures 4 and 4A
parallel one another in the type of connections made, but
differ in the design of the customization plane, a matter
to be discussed in more detail below. For reference
15 purposes, the ends of the pillars will be numbered in a
fashion similar to Figure 2, with the customization y-wire
end (Y1) being end 56, the lowermost y-wire (Y2) being end
58, the leftmost x-wire (X1) being 60 and the rightmost
x-axis wire end (X2) being 62. As the figures illustrate,
20 the wire ends can be connected in a variety of different
arrangements, for example, X1-X2, X1-Y1, X1-Y2, X2-Y2, or
any combination thereof. The application of the links to
the wires is known as "additive" customization. This
configuration also allows the use of the same programmable
25 junction for two independent nets, often called
"knock-knee" connections.

 Figures 5 and 5A show another embodiment of the
interconnect design, i.e., "subtractive" customization, in
which a continuous connection shorting all four wire ends
is provided. The interconnect can undergo a subtractive
30 process, e.g., laser etching, to disconnect select ends,
thus defining the specific links. Subtractive
customization also allows the simultaneous formation of
programmable links, attachment pads, additional wiring,
35 etc.

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1 The interconnect plane formed by the terminal
wire ends can be positioned at a variety of heights
measured in the z direction. As shown in Figure 2, the
interconnect plane can be parallel to the customization
5 plane 48. In this embodiment the programming tracks 65
are formed in the customization plane and aligned with
the diagonally-extending programmable junctions. In
another embodiment, the interconnect plane is parallel to
the plane formed by the upper set of wires. Figure 12
10 illustrates this embodiment. In order to provide the
necessary access to the interconnect region, a
personalization "trench" 76 is formed in the upper layers
of the interconnect 40. The base of the trench terminates
in the plane formed by the upper set of wires 46. Such an
15 arrangement offers advantages over the embodiment in which
the programming tracks are coplanar with the upper
customization plane. As a result of the design of Figure
12, the pillars extending upward from wires 46, i.e., the
top set of wires, are eliminated. In addition, the pillars
20 extending from the lower set of wires 44 are reduced in
length. The result is, in effect, a 66% reduction in the
pillars necessary to bring the wire segment ends to the
interconnect plane.

25 The personalization trench can even be extended
downwardly to the lower set of wires. This embodiment
completely eliminates the need for pillars. In yet
another embodiment of interconnect design, as illustrated
in Figure 11, a separate reference plane 78 is positioned
between the upper set of wires 46 and the customization
30 layer 48. The additional reference plane 78 provides for
the separation of the electrical connections between
programmable junctions and the chip attach pads,
engineering changes, overflow wiring, etc.

35 In other embodiments, a first and second
reference plane are provided on either side of the wires,



1 for example, in Figure 11, planes 78 and 79 on either
sides of wires 44 and 46.

Figure 11 also reflects the provision of
insulation 80 between the various interconnect layers.
5 Typically, the interconnect sandwich, in cross-section,
comprises metal separated by insulation. A variety of
metals, for example, gold, copper, tungsten, are useful.
A particularly preferred metal is copper. Also, the
various layers can utilize different metals. Though not
10 illustrated by the figures, it is also envisioned that,
rather than an entire insulative layer, insulative strips
may be used between the wire segments. Any electrically
insulative material may be used. Preferred insulative
materials include polyimide, ceramic, glass-epoxy
15 laminates, and PTFE-glass boards. The polyimides are
particularly preferred where the desired construction of
the invention is for smaller interconnects.

Figure 13 shows another embodiment of the
interconnect according to the present invention. The
20 interconnect includes multiple power planes 82 and 84.
The exact number of power planes is determined by
interconnect application. As illustrated, pillars 86, 88
extend upward through the interconnect to electrically
connect the power planes 82 and 84, respectively, to the
25 customization layer 48. Should these additional pillars
overly complicate the interconnect structure, it is
possible to address the power concerns by using the two
reference planes, or an external structure onto which the
interconnect may or may not be attached.

30 The determination of which of the various
interconnect topologies to utilize will depend upon a
comparison of the user needs and the tradeoffs in
fabrication ease, customization ease, cost, performance,
etc.

35



1 The areas for passage of the pillars to the
interconnect plane and/or customization plane are commonly
referred to as "vias". The present interconnect design is
such that the vias do not block the various wiring
5 channels since the wires terminate in the areas of x-y
intersection and the vias are positioned in the
termination areas. The design further allows for
advantageous wiring compactability, for example, more than
500 lines per inch per layer are possible using 15 micron
10 lines and 30 micron spaces. Higher line densities are
possible with the only limitation being the lithographic
capabilities.

 The present vias are accessible from the exterior
of the interconnect and are designed such that the
15 programmable junctions therein can be accessed to
customize the routing. Figure 2 illustrates the prior art
via design, known as a "blind via". In the prior art, as
each successive layer is applied, the lower layers become
buried, making it impossible to access the interconnect
20 structure externally. Since the vias used to interconnect
lower layers are buried in the same process, they are
inaccessible for further customization and are known as
blind vias. While blind vias are not disadvantageous per
se, they can create difficulty in situations requiring
25 further changes or modifications as well as complicate the
testing process. For these reasons, it is advantageous,
where possible, to eliminate blind vias by providing
access to all vias.

 The use of wire segments in the interconnect
30 allows for infinite pitch flexibility in the programming
tracks. Also, since a series of wire segments are used
rather than one continuous wire, use of a segment for one
routing purpose does not disable use of the other wire
segments in that wiring channel for other purposes. As

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1 was pointed out, disabling of entire wires is a drawback
of the Mosaic electrically programmable design.

5 The customization layer 48 of the interconnect is
shown in more detail in Figures 7-9. A review of these
figures reflects the variety of designs the layer can
assume. Figure 8, for example, shows a layer 48 having
the continuous diagonal access tracks 81 which provide
access to the programming tracks 65 previously described
and illustrated in Figures 2 and 3. The tracks correspond
10 to and overlay onto the underlying diagonally-extending
programmable junctions 66. Figure 4A illustrates a
customization layer 48 having access regions in the form
of cut-away portions 64 which provide access to the wire
segment ends. Other modifications of the customization
15 layer topography are possible, the primary objective
simply being to allow access to the wire segment ends so
that the necessary customization of the wiring routing can
be achieved.

Besides providing for wire connections, the
20 customization layer includes pads 82, see, for example,
Figure 7, for bonding to the leads from the integrated
circuit chips. The pads can be formed in the same plane
as the wire interconnect region, and can be arbitrarily
placed within the space separating the diagonal tracks or
25 cut-aways. As shown in Figure 7, a chip 90 attaches to
the customization layer 48. The chip includes leads 92
which extend from the chip and bond to the interconnect at
the bonding pads 82. This process is referred to as outer
lead bonding (OLB). The connection can, for example, be
30 by means of a solder bump extending from the bond pad to
the lead. The pads 82, in turn, are electrically
connected, as part of the customization of the
interconnect, to select wire segment ends. As shown in
Figure 7, a connector 94 extends from the pad 82 to the
5 wire end 96. Figure 8 is an isometric representation of

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1 the interconnect of Figure 7. The structures are
similarly referenced.

Figure 8A illustrates a further design of the
customization layer 48 and OLB pads 82. The pads are
5 circumferential, resembling islands in the customization
layer, and the customization layer is contoured in a
similar fashion. The customization layer includes the
diagonal tracks. Figure 9 shows a lead 98 extending from
the chip 86 to the bonding pad 82.

10 The interconnect of the present invention, and
particularly the customization layer thereof, is
compatible with a variety of OLB techniques, for example,
tape automated bonding (TAB), wire bonding, C4 bonding,
etc. TAB-type bonding is particularly preferred and will
15 be described in more detail below.

The selection of bonding pad sites is part of the
interconnect customization. If only one outer lead bond
is to be formed between diagonal access areas, the pads
can be arranged in a straight line. If more than one bond
20 is going to be present between programming tracks, the
pads can be staggered. The interconnect is compatible
with either area or peripheral bonding.

As noted above, TAB-type bonding is a
particularly preferred means for bonding the interconnect
25 to integrated circuit chips. TAB-type bonding involves the
mounting of the integrated circuit chips on a carrier film
or tape. The tape, for example, may comprise a very thin
polyimide strip. The chip is affixed to the tape by means
of the chip's outer signal and power leads. These leads
30 are generally formed of copper and typically plated with
tin, or noble metals such as gold, platinum, etc.

Typically, the leads extend from the centrally
positioned chip in all directions. The leads generally
have inner and outer lead bondsites. The inner lead
35 bondsites (ILB's) connect the lead to the chip; the outer

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1 lead bondsites (OLB's) connect the leads to the
interconnect. Because of the small scale at which the
bonding must be performed, it is desirable to have
center-to-center distances between adjacent OLB's
5 sufficient to prevent overlap of the bonding connections
between two bondsites which result in shorting the
connection. This design objective, however, must be
balanced against the need to use as little bonding area as
possible in order to allow compact chip mounting. In
10 other words, if one were to spread out the OLB's over an
interconnect to facilitate the bonding of the individual
leads to the interconnect, it would result in the adjacent
chip being positioned at greater distances from one
another and thus fewer chips per unit area could be
15 accomodated.

The present interconnect circuitry also includes
the provision of a tape design for improved tape automated
bonding for use with the present interconnect. The
present tape design provides an improved means for bonding
20 between the tracks and for maximizing the number of
bondsites along a staggered row of sites. The tape design
of the present invention also allows for more dense
packing of chips onto an interconnect due to the shorter
outer lead bonding length.

25 Figure 14 schematically illustrates a typical
"Tape Automated Bonding" (TAB) chip. As illustrated, a
semiconductor integrated circuit chip 110 is affixed to a
carrier film, or tape, 112 by means of outer leads 114.
The tape is formed from an insulative material, for
30 example, a polyimide. The polyimide tape is then covered
on one side with a conductive metal, for example, copper.
The copper layer is then etched to form the desired lead
pattern, with the non-etched copper areas forming the
resultant leads. The polyimide tape is also etched or
35 stamped to form an area for receiving the chip 110. This



1 etch or stamp is generally performed in the center of the
tape at the inner terminations of the leads. The
non-etched leads are typically then plated with tin, gold
or other noble metals. The chip is then placed onto the
5 tape and ILB's (inner lead bonds) are formed between the
chip and the inner terminal portions of the leads. The
OLB's of Figure 1 have a peripheral design. As Figure 14
depicts, the leads fan-out from the ILB's to the OLB
bondsites which are essentially aligned in a row parallel
10 to the chip edge. It should be noted that the lead design
depends on the number of ILB's. In some designs in which
a limited number of leads are present, the leads may not
need to fan-out.

Figures 15A and 15B schematically represent
15 peripheral and area bonding, respectively. The outer
leads 114 comprise bondsites 116. The peripheral bonding
of Figure 15A parallels that used in Figure 14. Figure
15B illustrates how the OLB's can be arranged in rows in a
manner which spaces the center-to-center distances between
20 bondsites to an optimal distance (r).

Figure 16 further illustrates the inner leads and
the lead design according to the present invention. The
leads 130 are shown extending from a TAB chip. The chip
itself is not shown, but would be positioned, as
25 previously described, in the center of the structure.
Starting from the center and working outwardly along the
leads, a lightened lead area 124 is shown along the inner
edge of the rectangular rim 118. This portion of the
leads is the inner lead bonding area which attaches to the
30 chip. The rectangular rim 118, in fact, represents the
polyimide tape. As previously described, the polyimide
tape is removed in the area where the chip is to be
located. Typically, the area where the tape is removed is
larger in size than the chip itself leaving a gap between
35 the chip and tape across which the inner leads 124



1 extend. The cross-hatched area 120 represents the
underlying interconnect. The diagonal lines 122
schematically represent the diagonally-extending
programming tracks or interconnect regions at which the
5 signal scheme is selected.

Continuing outwardly from the inner leads 124 and
onto the tape section 118, the leads are depicted by
alternating dark sections 126 bounding a lighter shaded
area 128. As shown, the areas 128 of successive leads are
10 staggered along a center-line axis which parallels the
diagonal programming tracks 122 and places the areas 128
between the programming tracks. The areas 128 represent
the OLB's for bonding the leads to the underlying
substrates. As designed, the bondsites do not overlap or
15 interfere with the programming tracks 122.

In order to form the bond between the leads 130
and interconnect 120, it is necessary to form a staggered
window between the leads and interconnect at the staggered
bonding areas 128. A preferred approach is to form the
20 window in the polyimide tape by removing the tape from the
underneath side of the leads along the staggered bondsites
128 of Figure 16. For example, parallelogram-shaped
"boxes" 132 could be formed as shown. Alternatively, the
tape could be removed only in the area of the bonds 128.
25 Another option is to form a solder mask over the
interconnect 120 in which the mask is designed to
correspond to the bondsites 128.

Figure 17 is an enlarged representation of a
section of leads 130 of the lead design of Figure 16. The
30 leads, as previously discussed, comprise inner lead bond
sections 124 which form ILB's with the chip 110, and OLB's
128 which are staggered in adjacent leads. The outer lead
bondsites 128 have not been cross-hatched though they are
sections along a continuous lead. The absence of
35 cross-hatching allows for further representing that the

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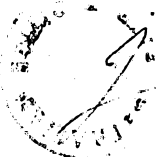


1 tape 112 has been removed at each bondsite 128. Figure 17
also illustrates that the staggered positioning of the
bondsites 128 increases the center-to-center distance of
adjacent bondsites. The increased distance allows for
5 improved operation. For example, because the bondsites
are farther apart, there is less opportunity for a solder
bump of one outer lead bondsite to bleed over to the
adjacent site and short circuit the leads. Also, the
present staggered OLB design decreases chip footprint
10 size, while still maximizing center-to-center distance to
the extent possible. The design also positions a number
of outer lead bondsites between adjacent programming
tracks of the underlying interconnects.

Figure 10 illustrates the interconnect 40 with
15 the diagonally-extending programming tracks 65 and a
plurality of different-sized chips 90 attached thereto.
The figure also illustrates that interconnects having
differing pitches of diagonal programming tracks can be
interconnected. For example, top interconnect 40 is
20 attached to middle interconnect 100 which in turn is
attached to lower interconnect 102. This figure is used
to show the applicability of the invention to numerous
levels or layers of an overall package scheme.

Figure 6 is a plan view of the chip 90 bonded to
25 the interconnect 48 through the access areas 64. The
Figure illustrates the use of square Kapton supports which
are employed with staggered OLB pads which align to
diagonal spaces between the diagonal access areas.

Additionally, though not shown by the figures,
30 the customization layer can also support overflow wiring,
engineering changes (EC), test pads and defective line
rerouting. Also, to improve electrical performance of the
multiple vias present in the interconnect, ground vias can
be added in the spare space of the customization layer.
35 The vias serve to lower inductance, realign characteristic



1 impedance and reduce coupling. Also, the vias from the
ground and power planes extend to the customization plane,
preferably in the areas of the bonding pads. The
customization layer between the programming tracks 65
5 serves as a high frequency shield to reduce coupling and
impedance imbalance between x-and y-layers.

It is also envisioned that the customization
plane can support wiring connecting programmable
junctions. In other words, the present interconnect
10 provides for a limited amount of design-specific wiring on
the customization layer. For example, referring to Figure
2, a wire could extend on the customization plane from a
programmable junction at one point along the programming
track to a programmable junction at another point along
15 the programming track.

The final step in the interconnect production is
the customization of the undedicated interconnect.
Customization embodies chip footprint, chip connections,
and the links between the underlying wiring. More
20 specifically, customization refers to the process by which
the standard interconnect is customized for a specific
end use. The wiring schemes to be established include (1)
the underlying wire circuitry, (2) the bonding pads to the
select wiring ends, (3) the ground or power vias and (4)
25 any test pads or overflow wiring. The customization can
be achieved through a single processing step, thus
avoiding multiple patterning steps which are expensive.
The single processing step can include single pattern
lithographic techniques and laser-assisted techniques, for
30 example, either direct or indirect write. The process can
be subtractive or additive. In other words, the links can
be selectively applied to achieve the desired interconnect
pattern, i.e., additive, or lines can be applied
universally throughout the interconnect and then removed,



1 for example, by laser-etching, to achieve the desired end product, i.e., subtractive.

The customization can be done quickly, for example, in the order of a few hours or less. This is a
5 marked improvement over the presently available interconnects, some of which require days or months to develop. The customization can be performed by the end user, with the undedicated interconnect structure being mass produced.

10 The interconnect of the present invention can be produced by a variety of methods. The manufacturing method described below is used to form an interconnect having a reference layer below the lower layer of
15 conducting wires, two layers of conducting wires and a top customization layer. As will become apparent from the discussion below, the various steps can be excluded or repeated to produce the specific interconnect designs previously discussed. In accordance with the present method, a supporting interconnect, such as ceramic or
20 other material, is selected to receive the conducting layers of the interconnect. The support may be rigid or flexible. A conductive material is then deposited on the interconnect to form a lower reference plane for the conductive wires. The conductive material can be
25 deposited by sputtering, electroless plating, electroplating or lamination. Optionally, a dielectric layer may be formed between the supporting interconnect and the lower reference plane. An additional dielectric layer is placed on top of the lower reference layer to
30 separate this layer from the interconnect layers which follow.

The lower layer of conductive wires is formed by etching of a blanket layer of metal which is applied in the same manner as the lower reference layer.
35 Alternatively, a lift-off technique or plating method may

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1 be used to form the conductors. Vias are required to
connect the lower layer of conductive wires or the
underlying reference or voltage planes to the top surface
where customization occurs. A stacked via approach is
5 preferred such that the area of via cluster is minimized,
and thus line density is maximized. Formation of the
stacked via may be achieved through anisotropic etch, or
for filled vias by electroless plating or electroplating.
For the latter method, a plating interconnect is necessary
10 at the layer preceding the via level.

A further dielectric layer is used to separate
the lower conductive layer from the upper conductive
layer. This dielectric may be spun on top of the existing
layers in liquid form and cured to a hardened state. If
15 electroplating is used to form the stacked via, this
dielectric must flow around the plated-up via structure.
In order to create a planar surface for additional layers,
it is convenient to planarize the cured dielectric layer
through which the vias protrude. This can be accomplished
20 by several well-known planarization techniques, including
etchback and mechanical polishing.

The second layer of conductive wires is formed in
a manner identical to that for forming the first layer of
conductive wires, with the appropriate vias from the
underlying layers connecting to the second conductor
25 layer. The preceding steps for forming the vias,
dielectric and planarization are repeated to continue the
migration of the upper and lower (X and Y) wire segments
ends up to the topmost surface where customization
occurs. A top reference layer is formed according to the
30 same process as used for forming the other reference
planes. This top reference plane may be a final layer, or
alternatively, the above steps may be appropriately
repeated to bring the wire segment ends to a layer above
35 the top reference plane.

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As can be understood from the above discussion, these various techniques can be repeated or modified to produce a variety of specific interconnect structures, depending on user needs.

As a result of the present design, the resulting interconnect is scalable to whatever technology with which it is to be used. Less dense interconnects are used in printed circuit applications and more dense interconnects are used in integrated circuit applications. This results from the fact that the construction of the interconnect utilizes the construction of the technology. Only the design remains constant. Thus, as circuitry construction becomes more sophisticated, the interconnect construction will keep pace.

In addition to the advantages of the present structure discussed above, the consistent interconnect pattern of the present invention provides for ease in testing the wiring and makes for predictable discontinuity effects. The interconnect also allows for similar crossover loading for all lines, as well as for good plating characteristics. Also, the lines provide for high-speed signal transport with controlled impedance. The ground vias can be mixed with personality vias to reduce via discontinuity.

The design also provides inherent fault-tolerance by allowing route-around of non-functional line segments. A test and repair strategy can be employed at each step of the interconnect processing, allowing potential yields of finished product to be quite high.

The regularity of the interconnect design may also allow "tiling" of good interconnect sections to achieve larger interconnects. The interconnect can be used as a first level packaging or can be extended to generic interconnect vehicles at higher levels of

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1 packaging, e.g., as an interconnect for modules and
printed circuit boards.

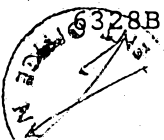
The primary application of the present
interconnects is to provide high performance multi-chip
5 customizable circuitry. The high cost typically associated
with such interconnects is lowered dramatically by the
present universal interconnect. By avoiding the use of
fully custom wiring, volume and yield are increased and
the end user is thus responsible for only a small fraction
10 of the overall fabrication. By taking advantage of a
compatible chip bonding design, density and flexibility of
the resulting customizable circuitry is greatly enhanced.

The present invention, therefore, is well adapted
to carry out the objects and obtain the ends and
15 advantages mentioned, as well as others inherent therein.
While presently preferred embodiments of the invention
have been described for the purpose of disclosure,
numerous changes in the details of construction and
arrangement of parts may be made without departing from
20 the spirit of the present invention and the scope of the
appended claims.

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The claims defining the invention are as follows:-

1. A multi-layer programmable electrical interconnect for connecting electrical components including:

an X-conductor layer comprising a plurality of substantially parallel channels, each channel including a plurality of electrically conductive first set of segments of substantially uniform length arranged end-to-end, a majority of segment ends in said X-conductor layer extending to a customization surface of said interconnect;

a Y-conductor layer comprising a plurality of substantially parallel channels, each channel including a plurality of electrically conductive second set of segments of substantially uniform length non-planar to said first set of segments and arranged end-to-end, a majority of the segment ends in said Y-conductor layer extending to said customization surface;

the X-conductor and Y-conductor layer being positioned so that the channels of the X- and Y-layers overlap;

a plurality of programmable junctions formed on the customization surface in a plurality of programming tracks which extend diagonally with respect to the channels of the X- and Y- layers, each programmable junction comprising segment ends of two adjacent X-conductor layer segments in the same X-conductor layer channel, and segment ends of two adjacent Y-conductor layer segments in the same Y-conductor layer channel, the segment ends in each programmable junction being positioned whereby selective electrical linkage can be accomplished on the customization surface between all combinations of segment ends forming the programmable junction, thereby permitting selective X to X, Y to Y, and X to Y linkage between the segment ends forming each programmable junction, as well as combinations thereof.

The interconnect of claim 1, wherein all combinations of electrical



linkage formed between segment ends within a single programmable junction are formed on the customization surface without overlap of electrical linkages in the same programmable junction.

3. The interconnect of claim 1, wherein the segment ends forming a programmable junction are in close proximity to one another,

4. The interconnect of claim 3, wherein the segments are long with respect to an area of the programmable junction.

5. The interconnect of claim 1, wherein the programming tracks are essentially parallel to each other, and extend at essentially a 45° angle to the Y-conductor layer channels.

6. The interconnect of claim 1, wherein the X-conductor channels and the Y-conductor layer channels are substantially orthogonal to one another.

7. The interconnect of claim 1, further comprising means for electrically insulating the Y-conductor layer segments and X-conductor layer segments where they overlap.

8. The interconnect of claim 1, wherein the Y-conductor layer and customization surface are substantially coplanar.

9. The interconnect of claim 1, further comprising a carrier film bonded to the interconnect; and

an electronic component bonded to the carrier film by a plurality of leads extending from the carrier film to the interconnect.

10. The interconnect of claim 1, wherein substantially all of the electrical linkage formed on the customization surface between segment ends are formed without crossing over other electrical linkage on the customization surface.

11. The interconnect of claim 1, wherein substantially all of the electrical linkage on the customization surface between segment ends are formed with a single pattern on the customization surface.

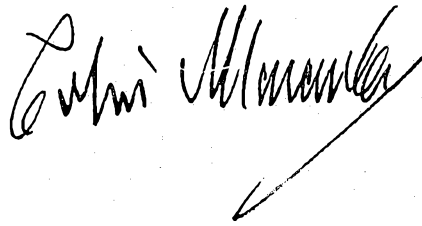
12. A multi-layer programmable electrical interconnect for connecting electrical components substantially as hereinbefore described with reference to the accompanying drawings.

D A T E D this 22nd day of February, 1991.

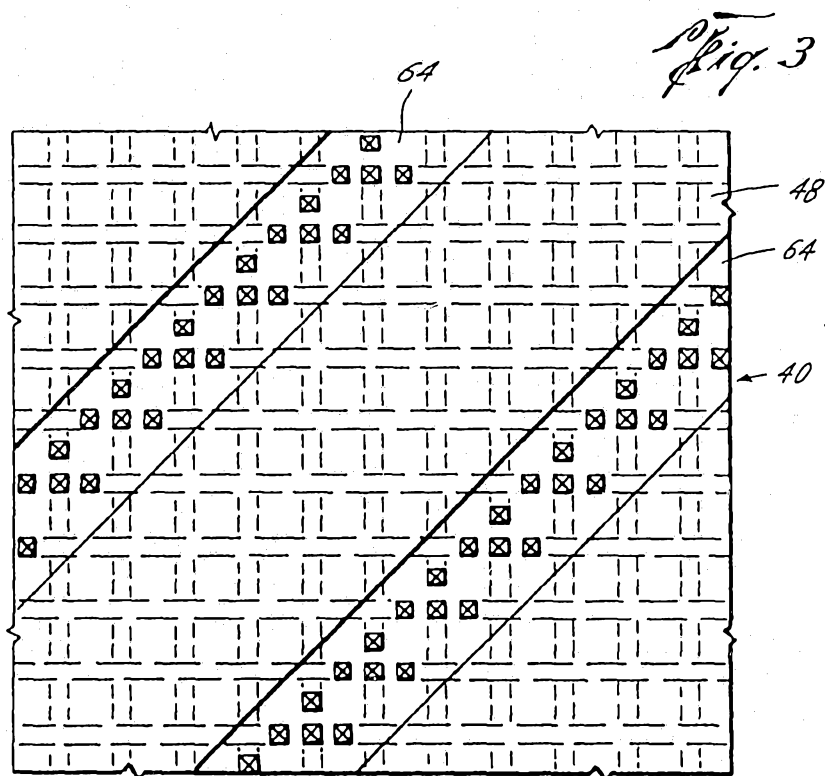
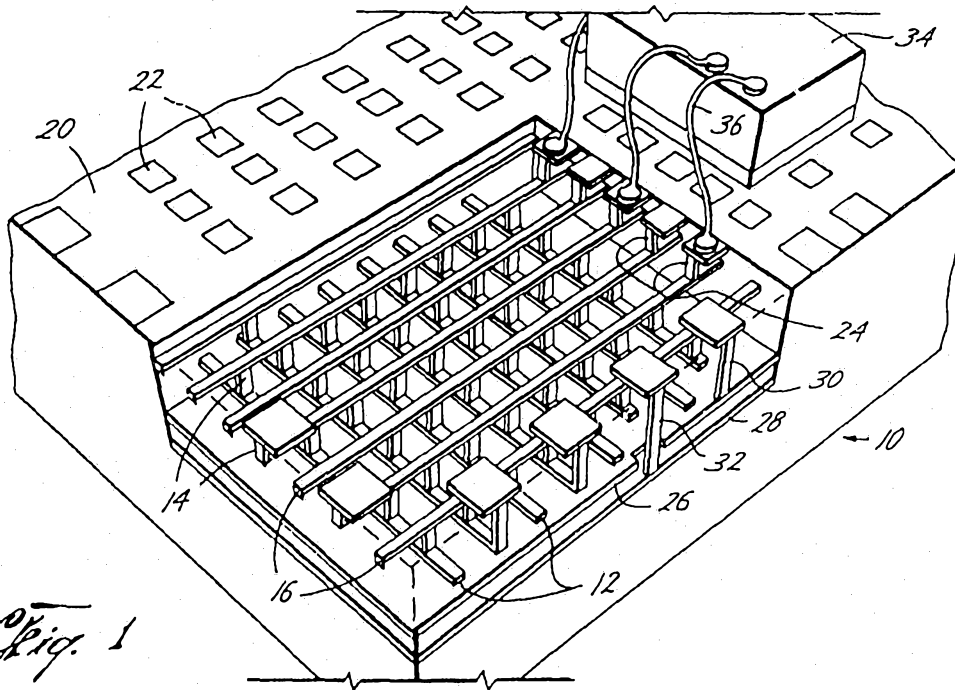
MICROELECTRONICS AND COMPUTER
TECHNOLOGY CORPORATION

By their Patent Attorneys:

CALLINAN LAWRIE



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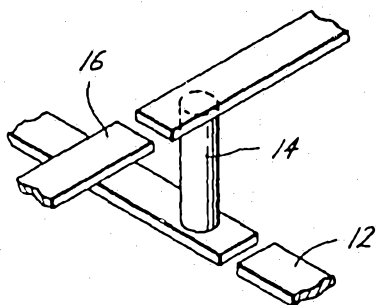


Fig. 1A
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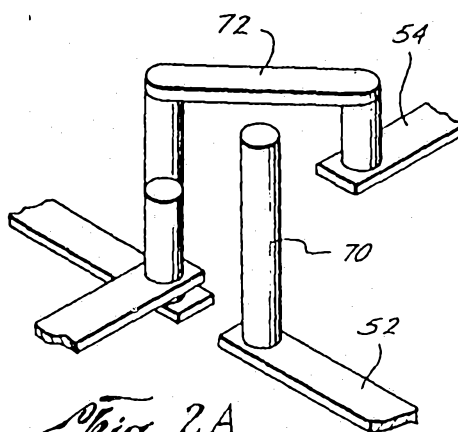


Fig. 2A

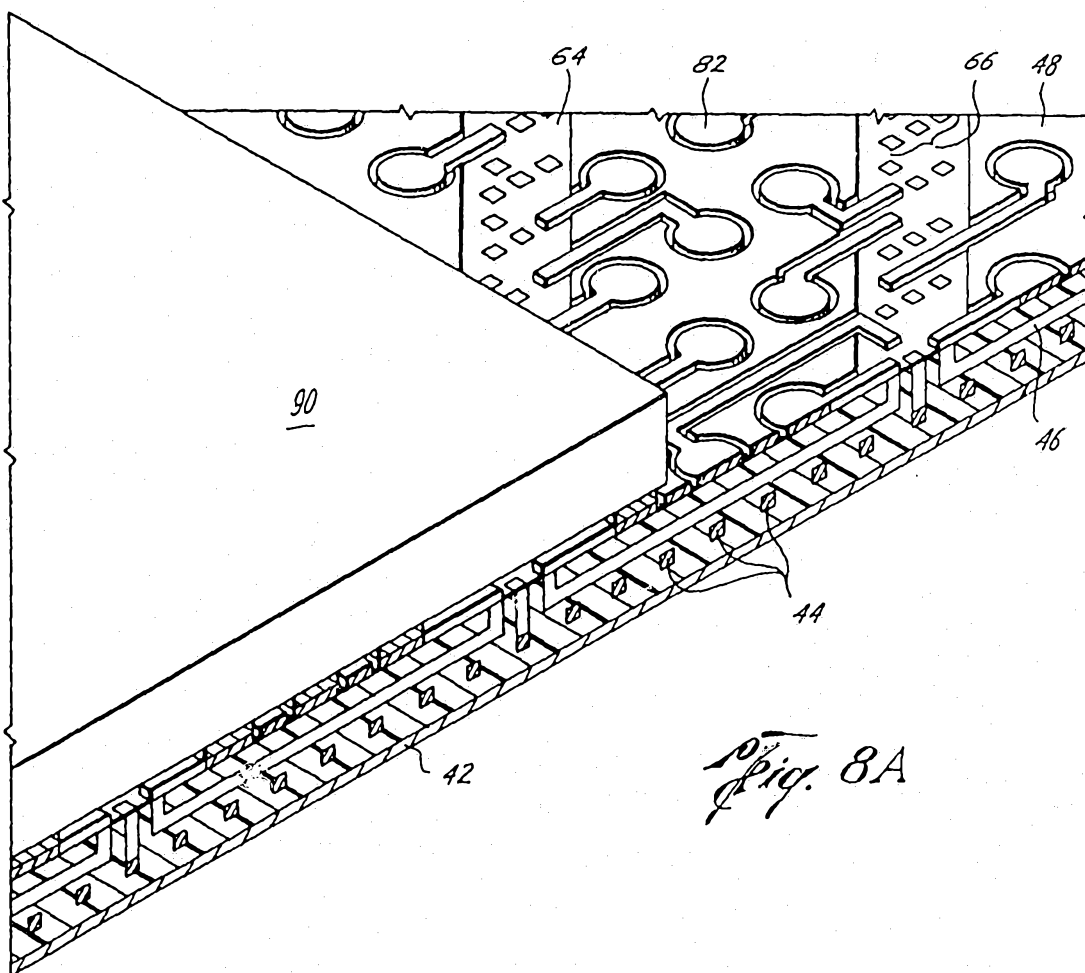


Fig. 8A

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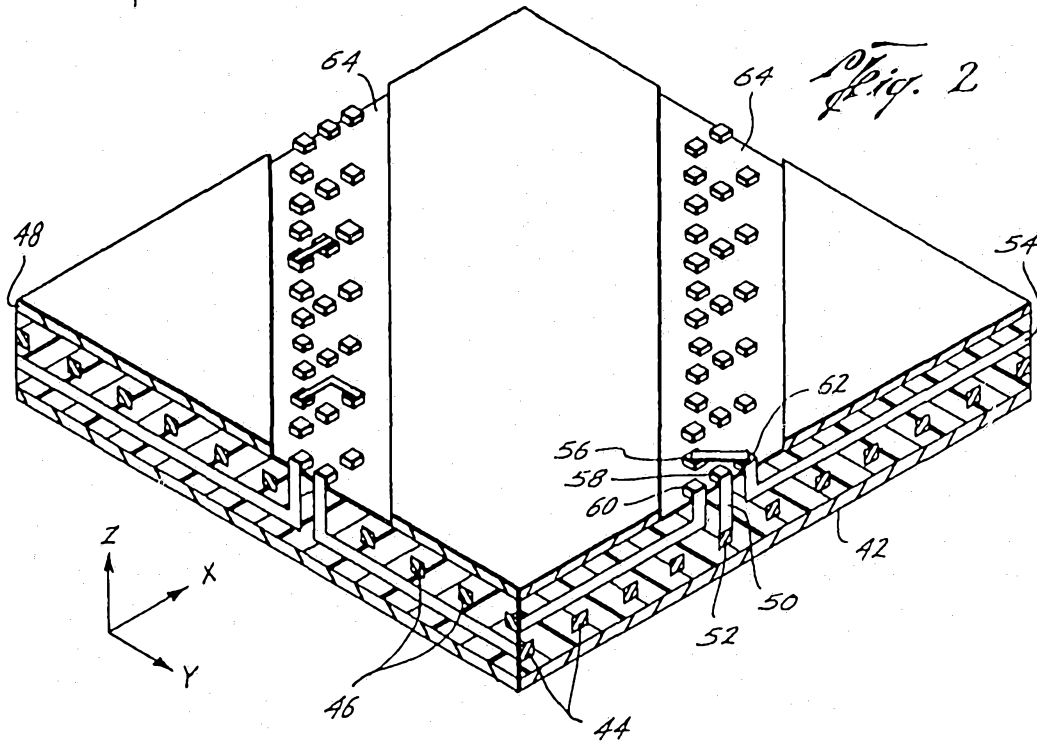


Fig. 4

Fig. 4A

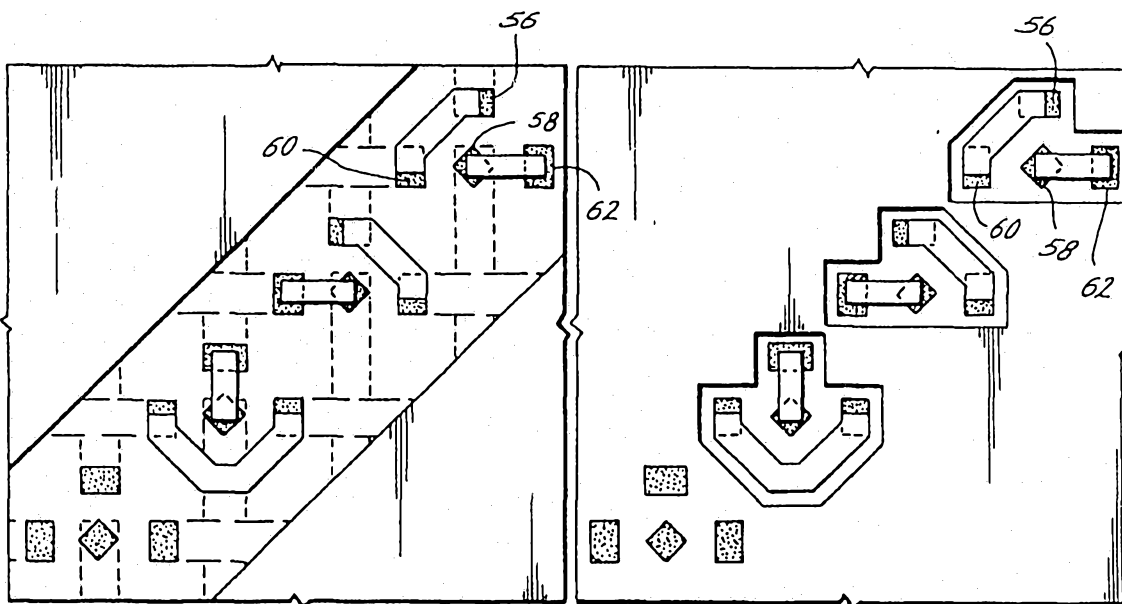


Fig. 5

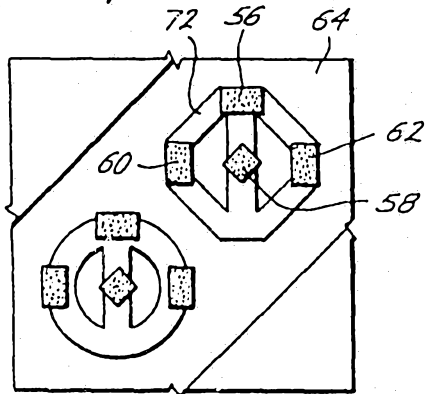


Fig. 5A

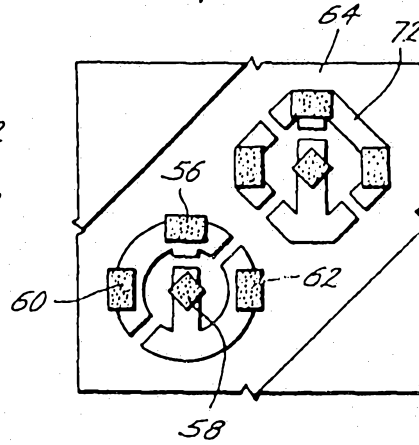
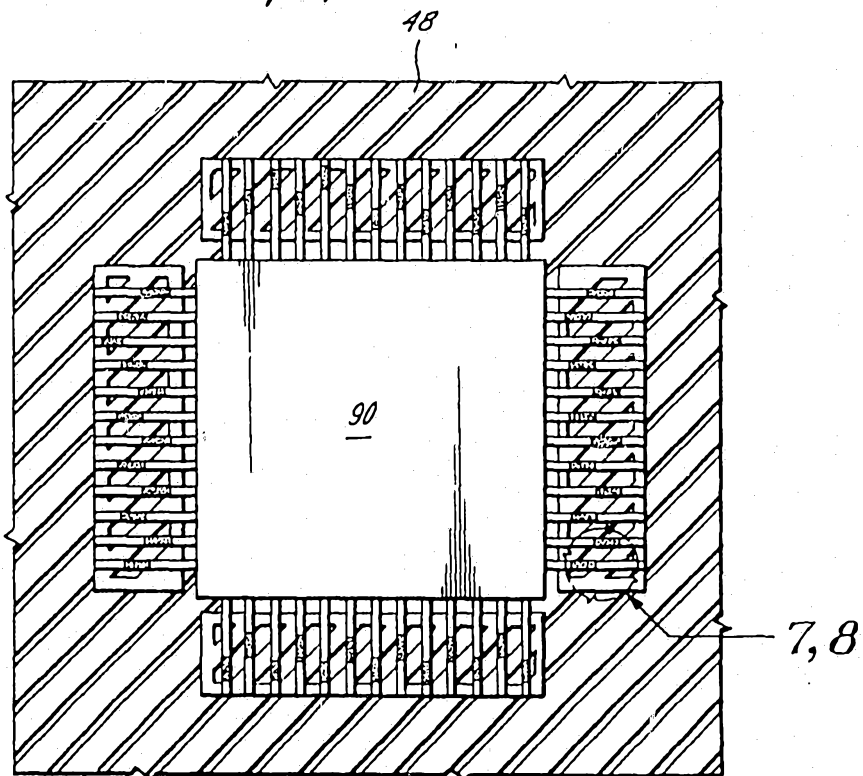


Fig. 6



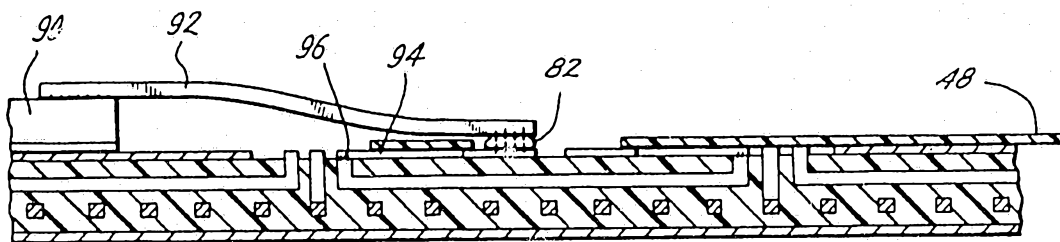


Fig. 7

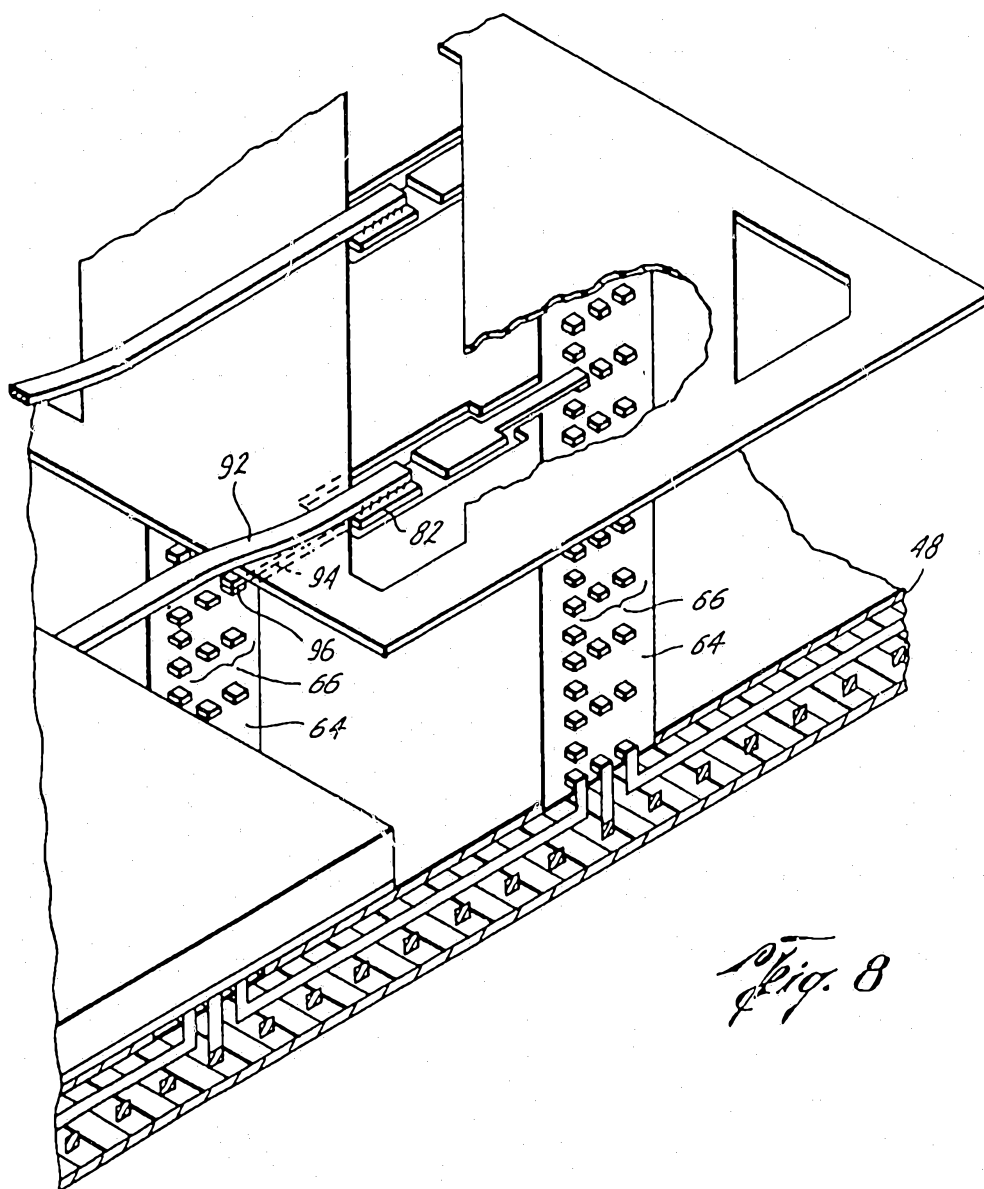


Fig. 8

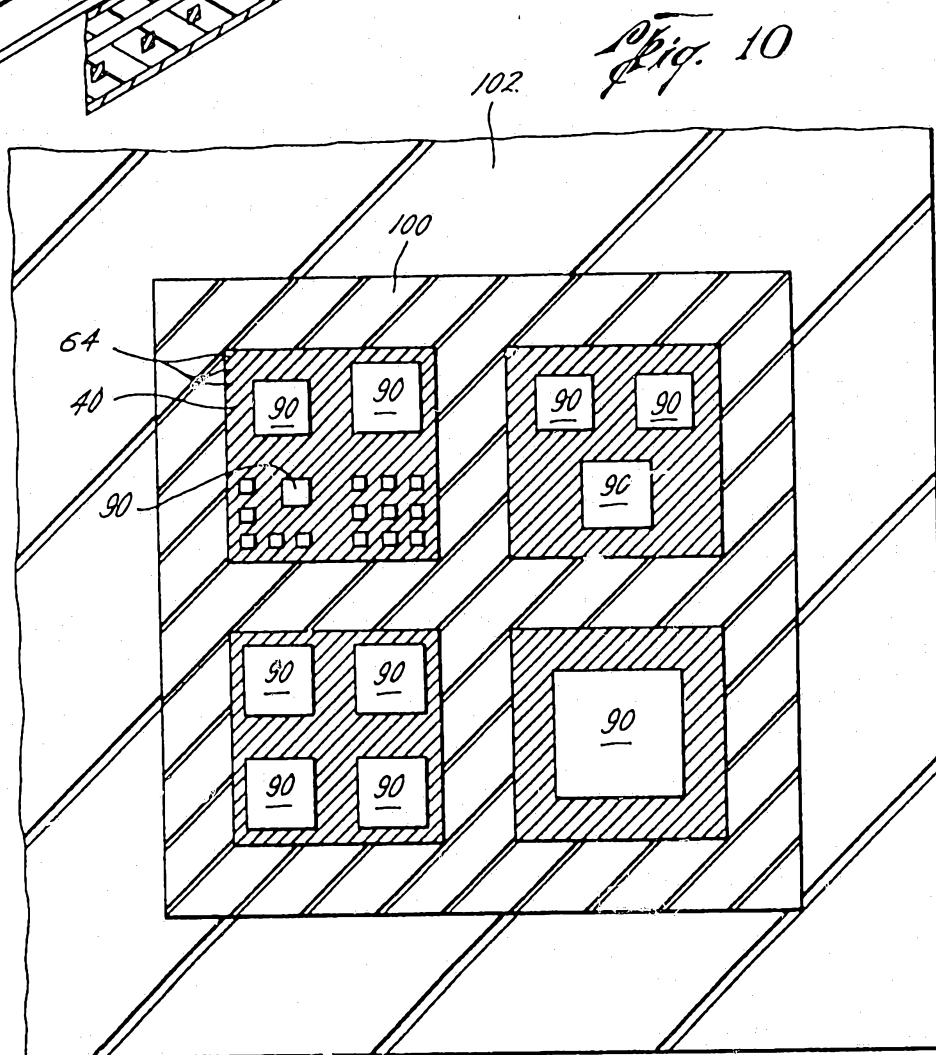
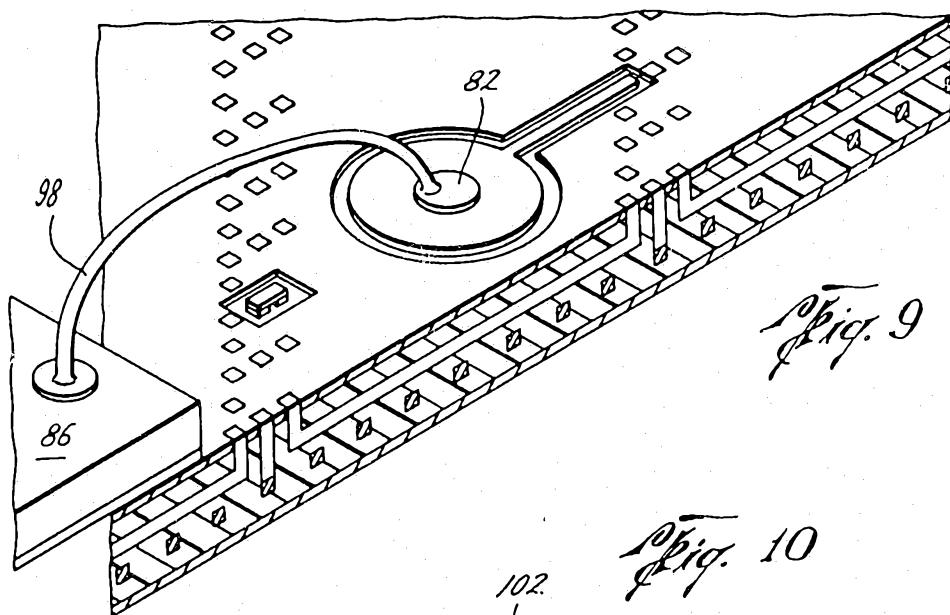


Fig. 11

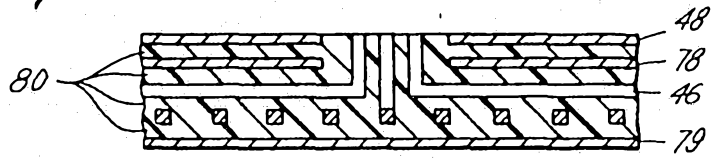


Fig. 12

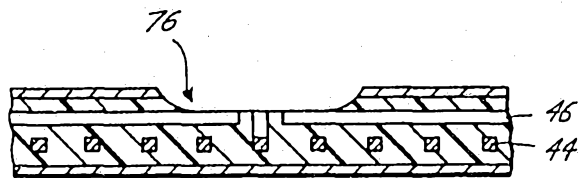
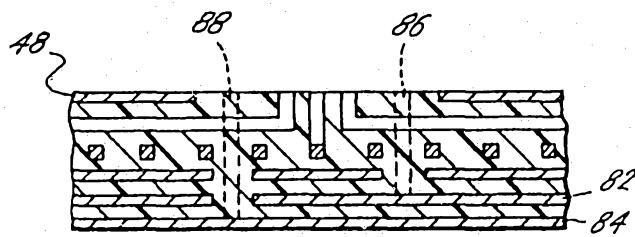


Fig. 13



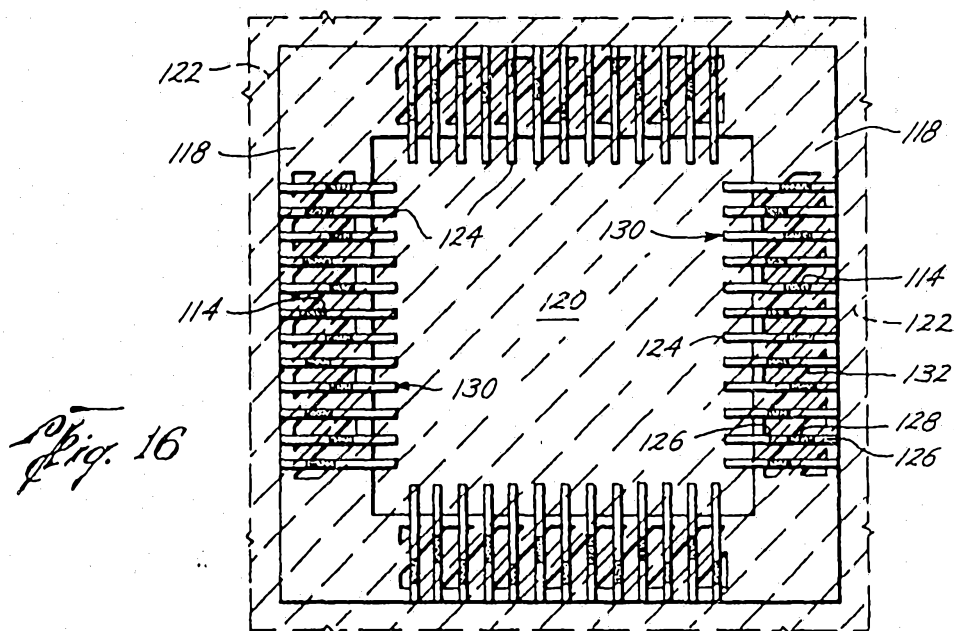
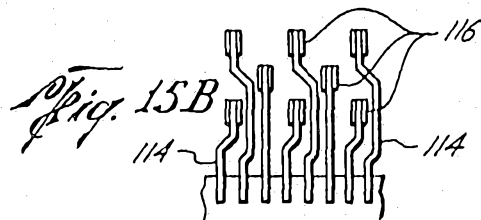
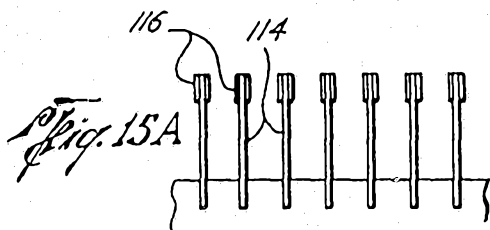
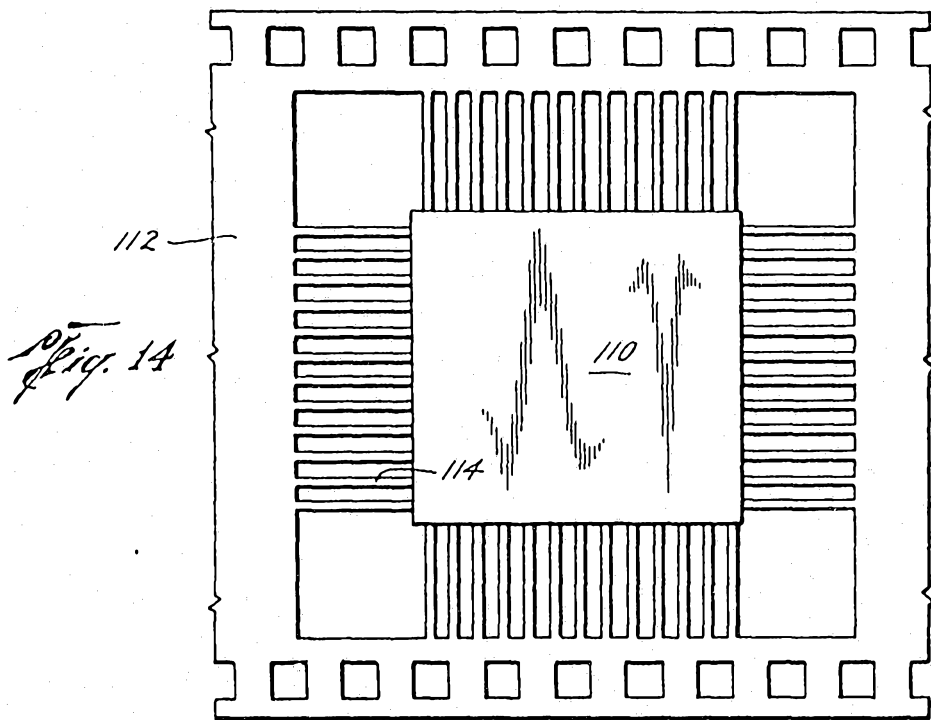


Fig. 17

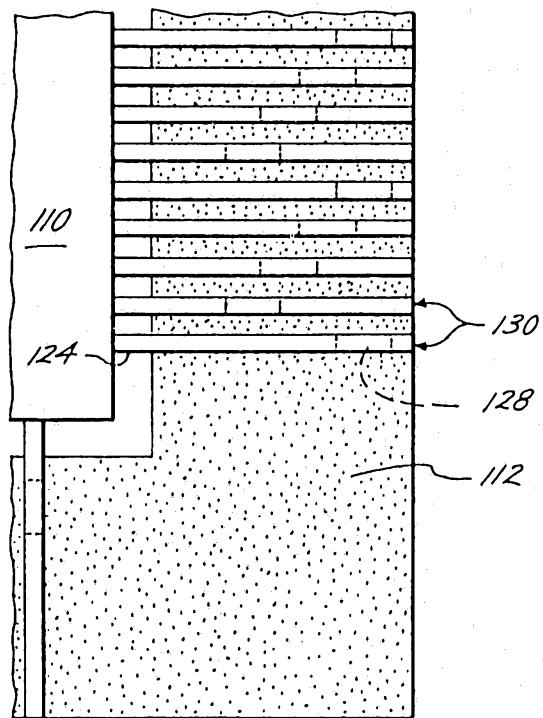


Fig. 18

