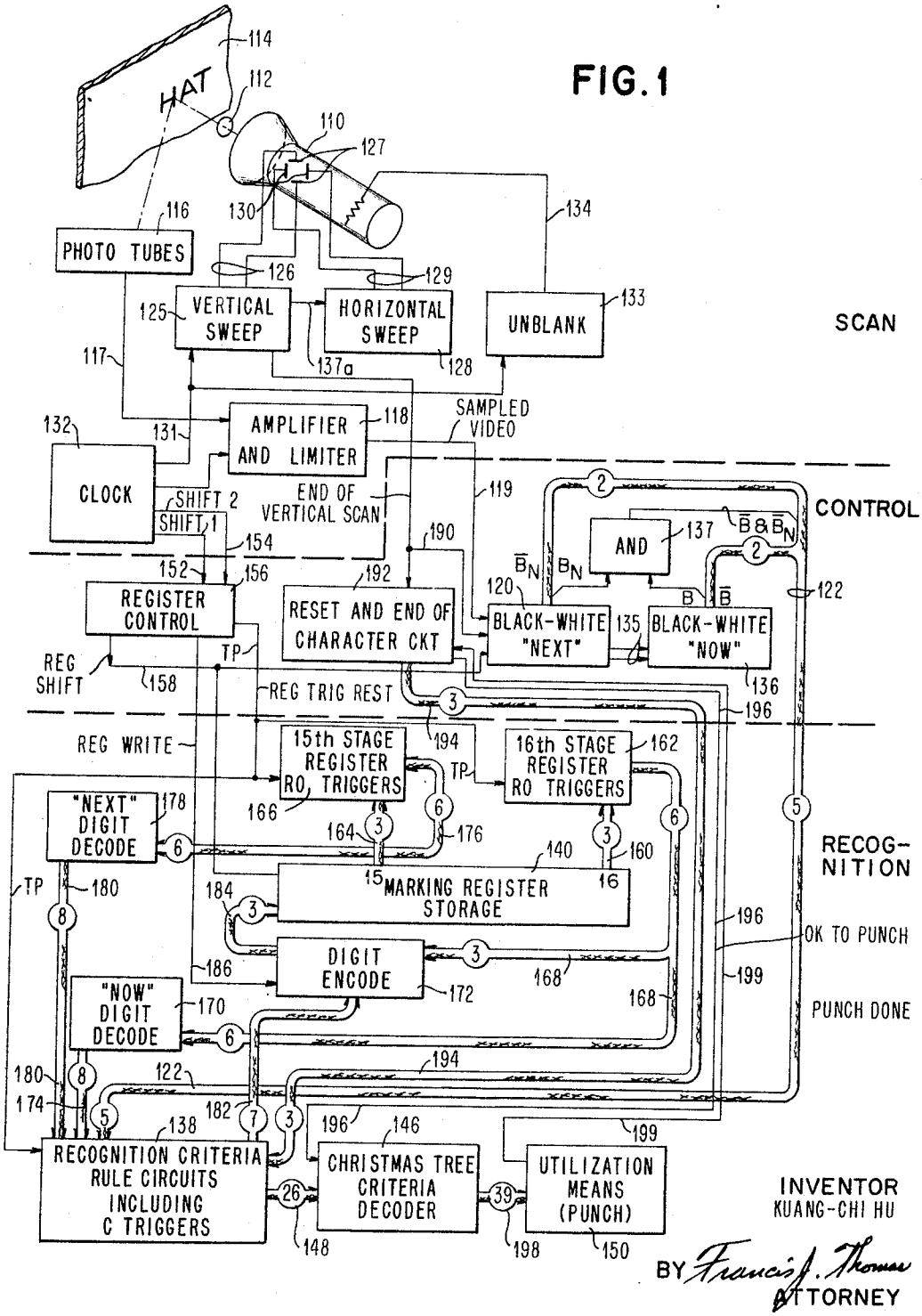
Sept. 6, 1966 KUANG-CHI HU 3,271,761

CURVATURE AND SHAPE DETECTION

Filed Nov. 29, 1963 69 Sheets-Sheet 1

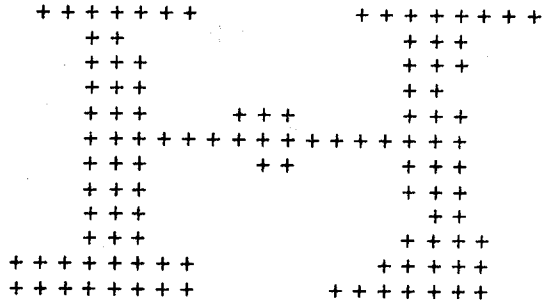
FIG. 1



INVENTOR
KUANG-CHI HU

BY Francis J. Thomas
ATTORNEY

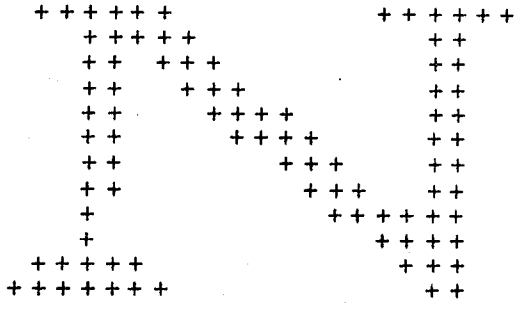
FIG. 2A



SOUTH BAY

H = 6
W = 9
K = 2/3
A = 43
K·H·W = 36
A > K·H·W

FIG. 2B



SOUTH BAY

H = 8
W = 10
K = 2/3
A = 45
K·H·W = 53 1/3
A < K·H·W

FIG. 3A

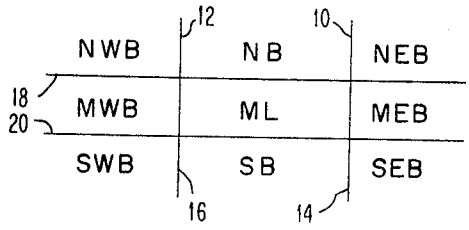


FIG. 3B

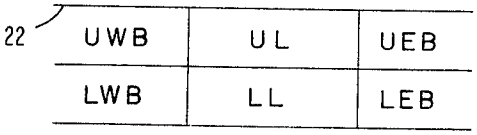


FIG. 4

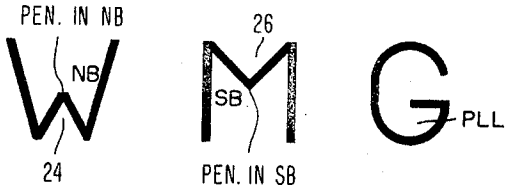


FIG. 5

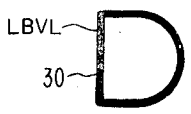


FIG. 6

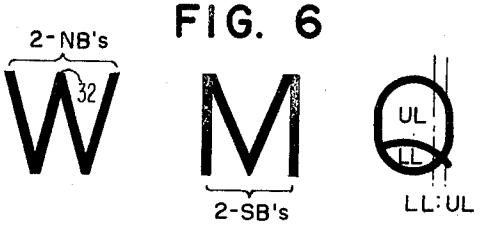


FIG. 7

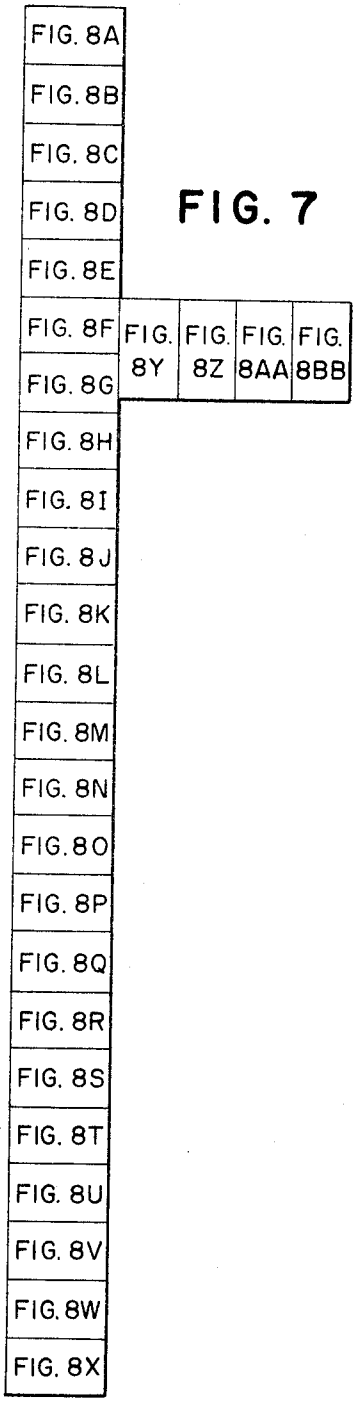
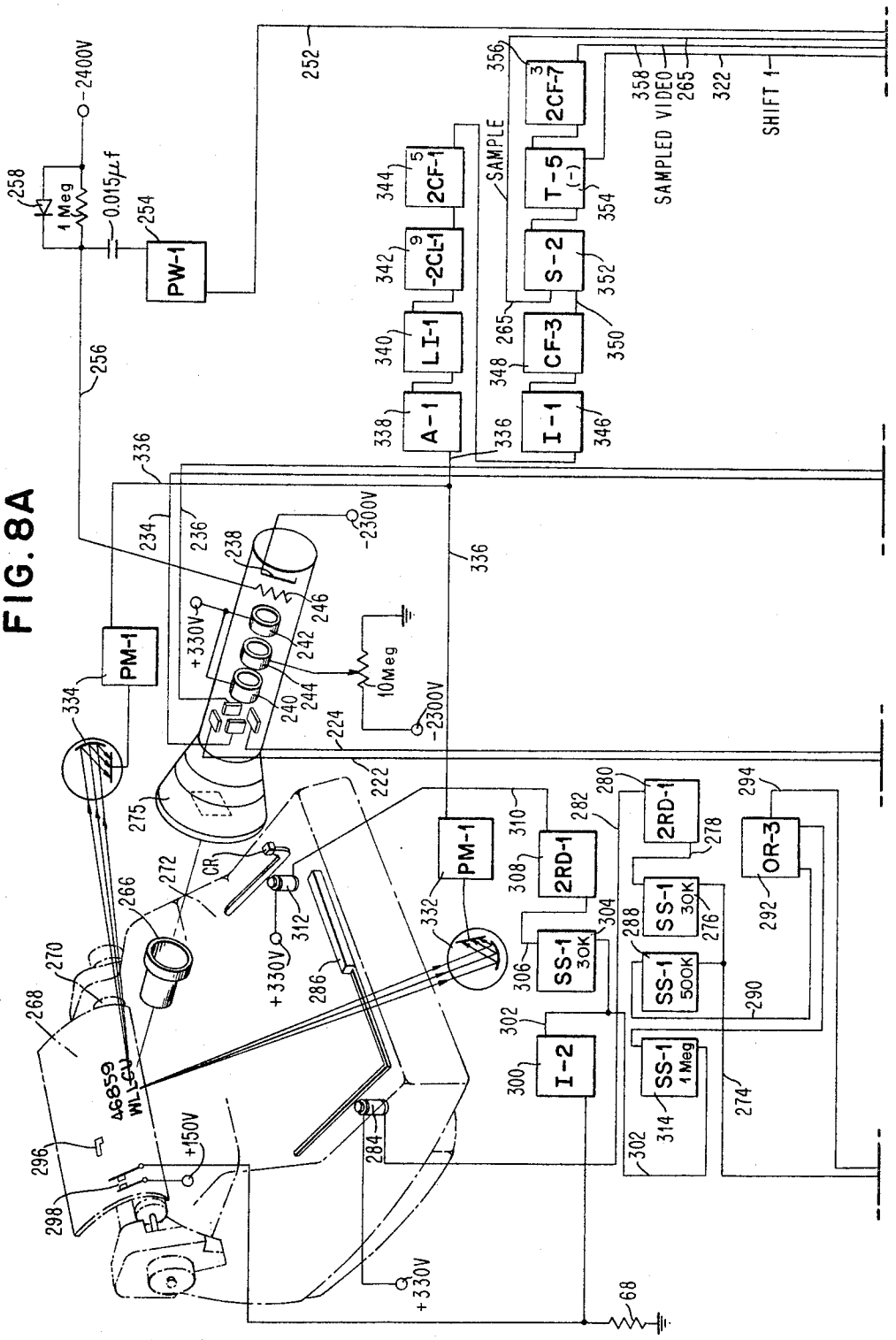


FIG. 8A


-2400V
1 Meg
0.015μf
PW-1
PM-1
+330V
-2300V
10Meg
CR
+150V
46859 MILEU
2CF-7
T-5 (-)
S-2
CF-3
I-1
2CF-1
-2CL-1
LI-1
A-1
SAMPLE
SAMPLED VIDEO
SHIFT 1
2RD-1
SS-1 30K
SS-1 500K
SS-1 1 Meg
I-2
OR-3
68

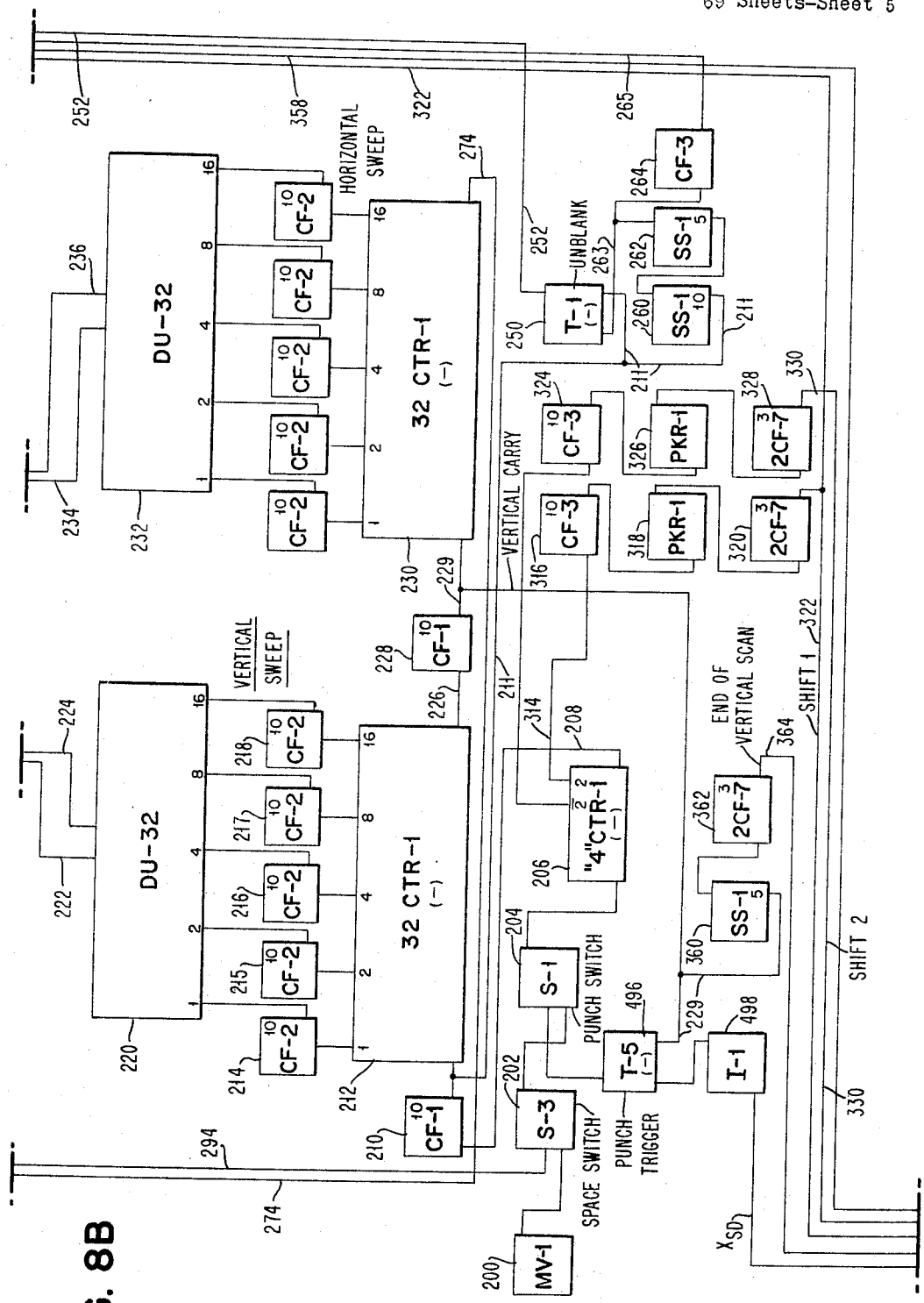

DU-32
32 CTR-1 (-)
CF-2
CF-1
CF-3
HORIZONTAL SWEEP
VERTICAL SWEEP
VERTICAL CARRY
"4"CTR-1 (-)
PKR-1
2CF-7
SS-1
T-1 (-)
UNBLANK
S-1
PUNCH SWITCH
S-3
SPACE SWITCH
T-5 (-)
PUNCH TRIGGER
I-1
MV-1
END OF VERTICAL SCAN
SHIFT 1
SHIFT 2
X_{SD}

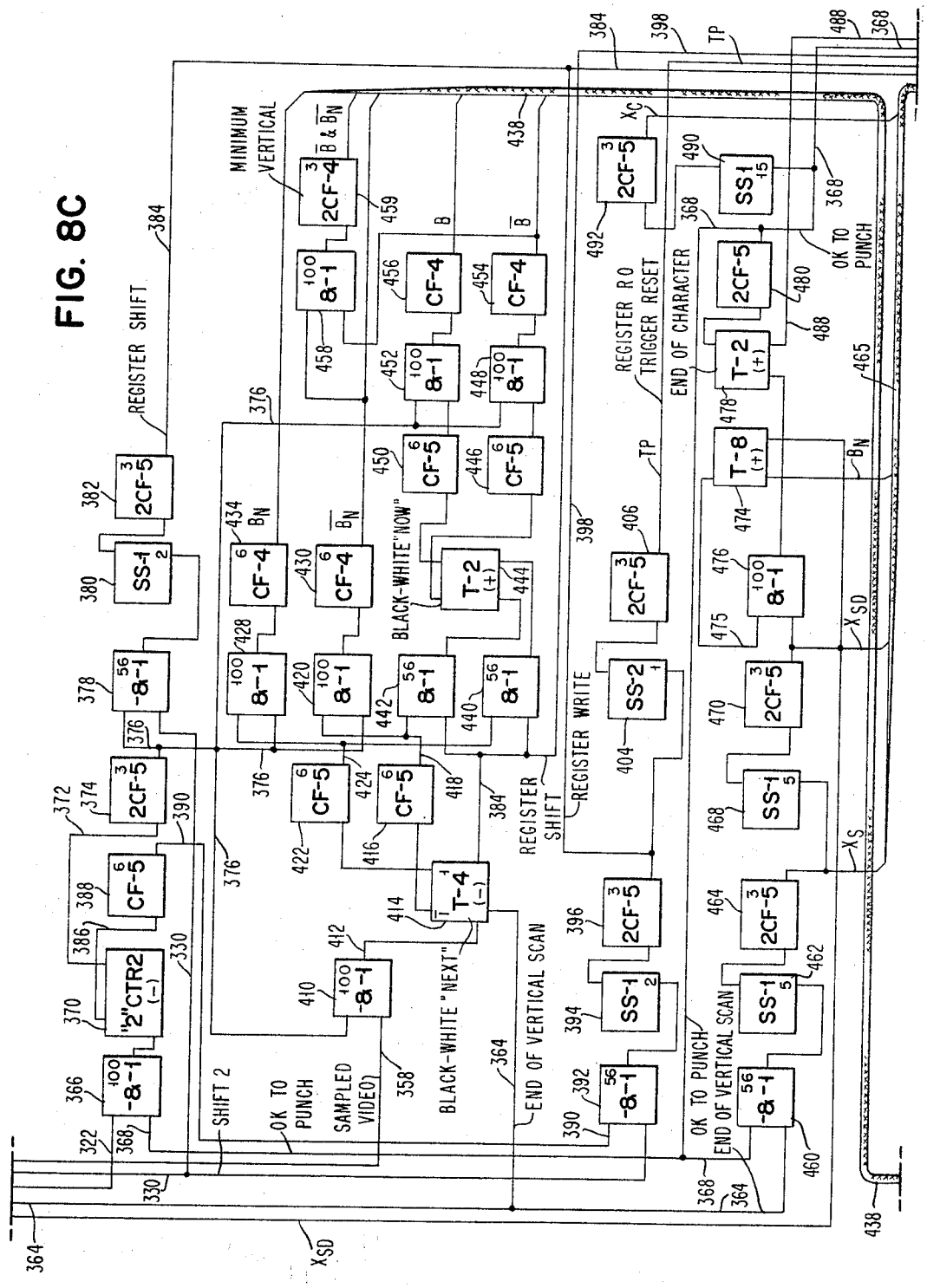
FIG. 8B

Sept. 6, 1966 KUANG-CHI HU 3,271,761

CURVATURE AND SHAPE DETECTION

Filed Nov. 29, 1963 69 Sheets-Sheet 6

FIG. 8C



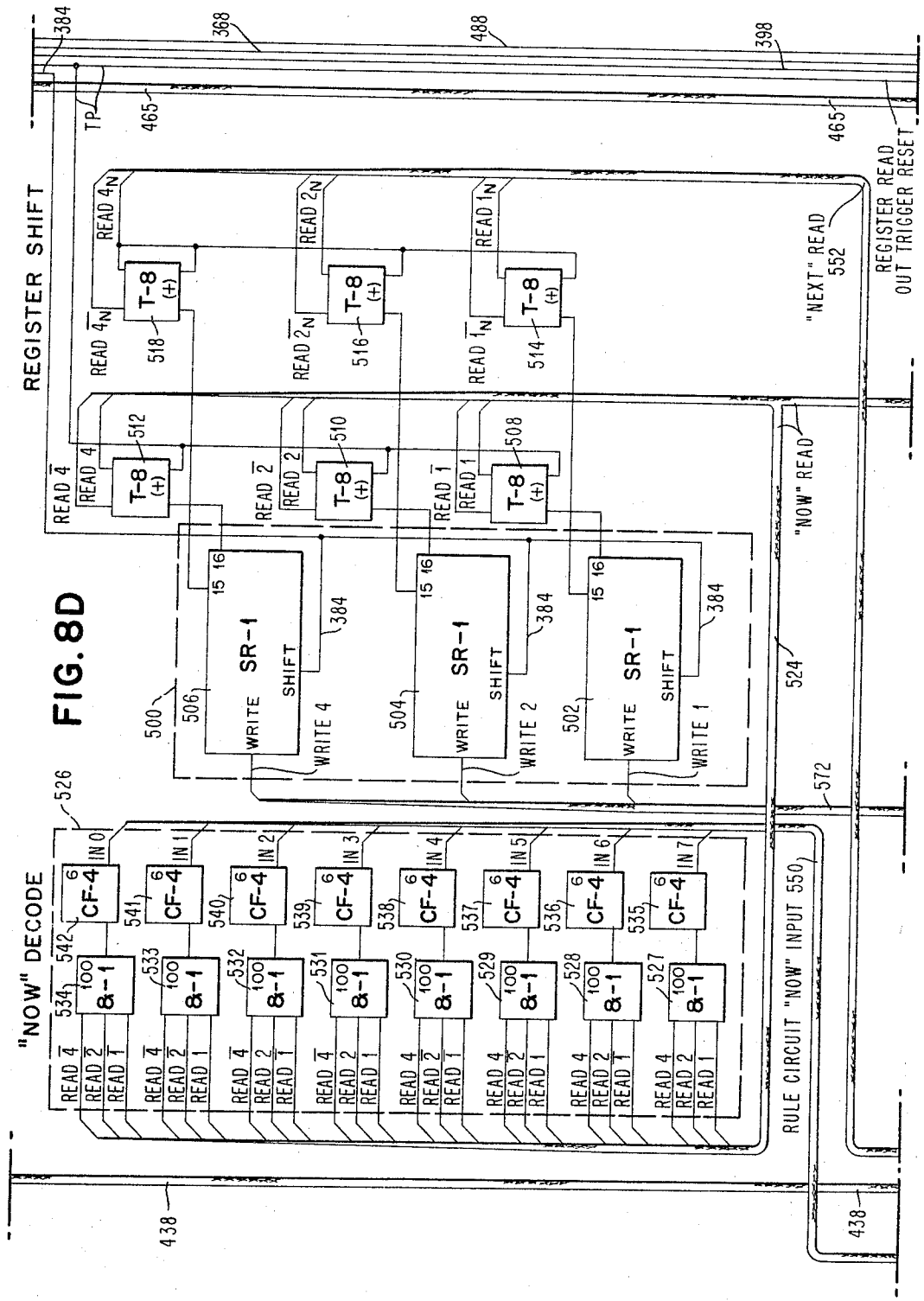

REGISTER SHIFT
"NOW" DECODE
RULE CIRCUIT "NOW" INPUT 550
"NEXT" READ 552
"NOW" READ
REGISTER READ OUT TRIGGER RESET
SR-1 SHIFT
WRITE 4
WRITE 2
WRITE 1
T-8 (+)
CF-4
8-1

FIG. 8D

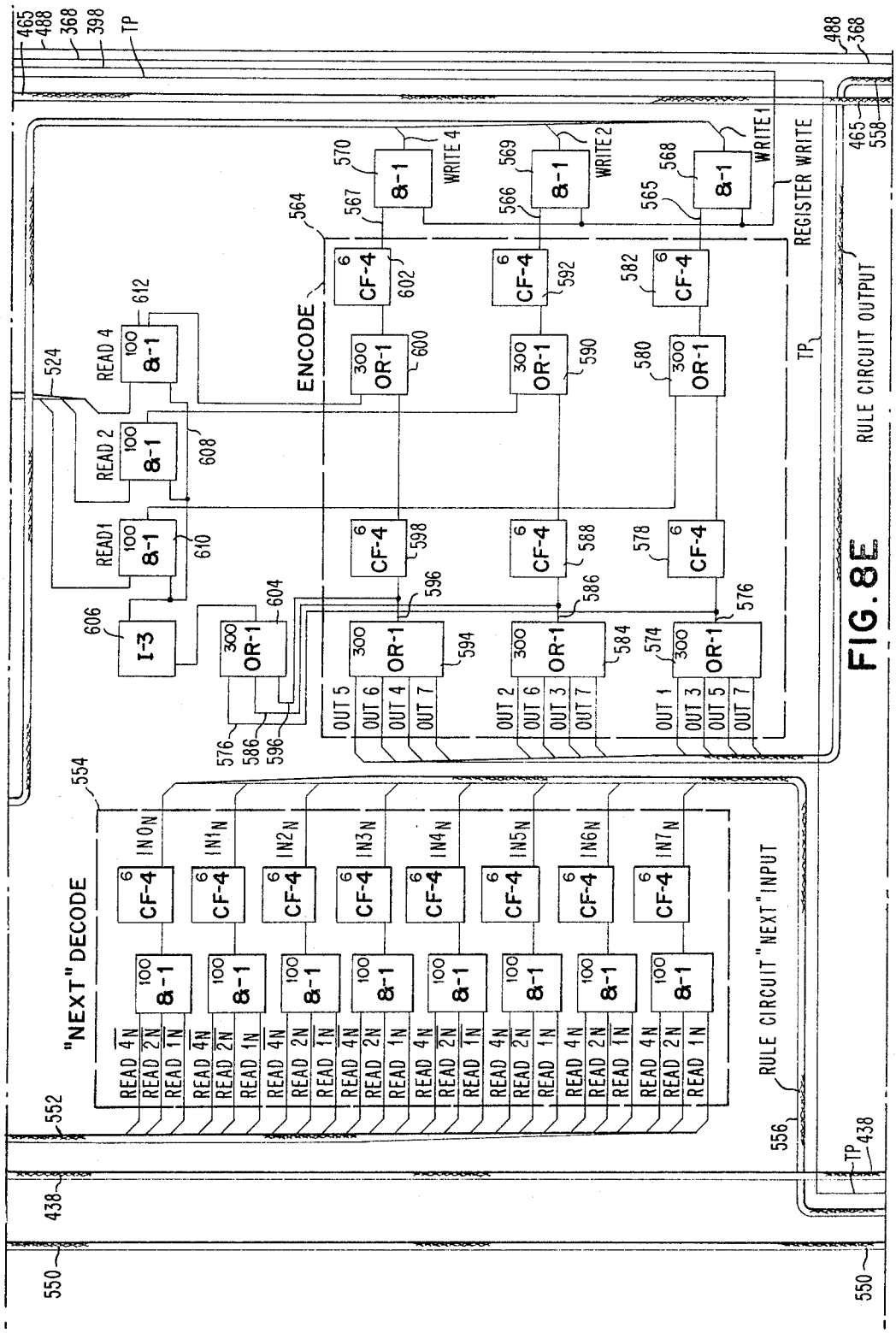
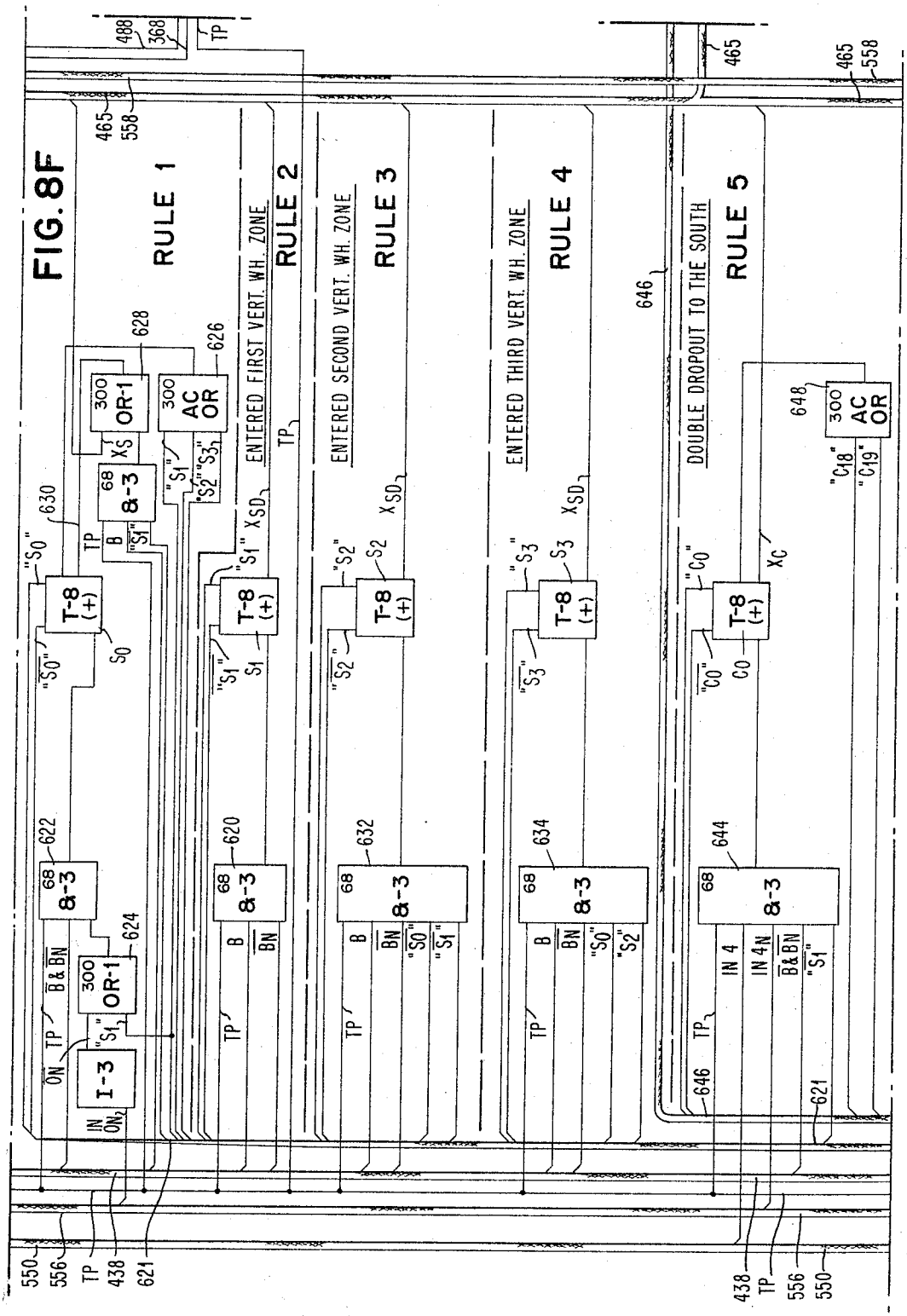

"NEXT" DECODE
ENCODE
REGISTER WRITE
RULE CIRCUIT OUTPUT
RULE CIRCUIT "NEXT" INPUT
CF-4
8-1
OR-1
I-3
WRITE 1
WRITE 2
WRITE 4
READ 1
READ 2
READ 4
TP

FIG. 8E

FIG. 8F


RULE 1
RULE 2
RULE 3
RULE 4
RULE 5
ENTERED FIRST VERT. WH. ZONE
ENTERED SECOND VERT. WH. ZONE
ENTERED THIRD VERT. WH. ZONE
DOUBLE DROPOUT TO THE SOUTH
T-8 (+)
8-3
I-3
OR-1
AC OR
TP
550
556
438
621
465
558
646
648

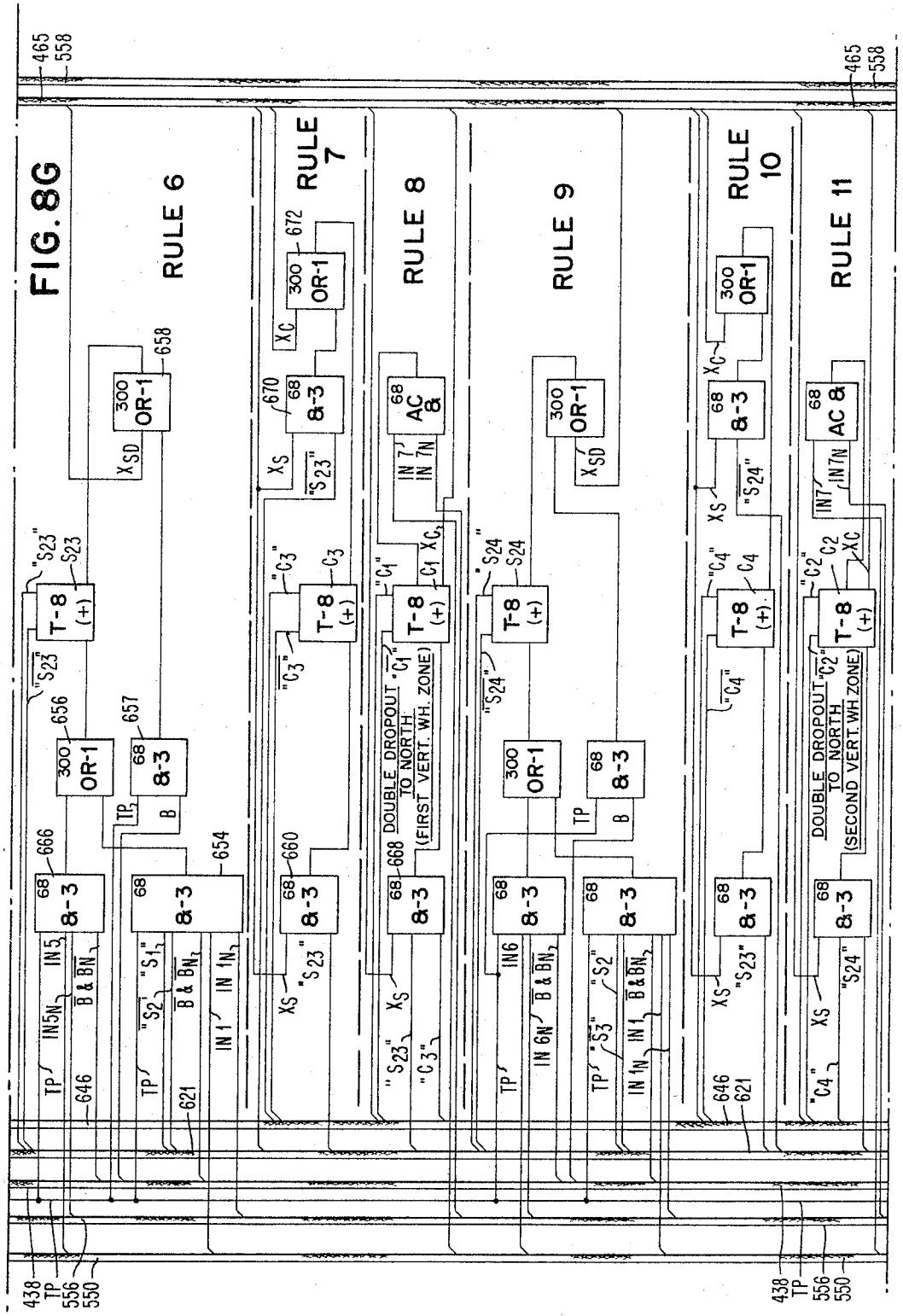

FIG. 8G
RULE 6
RULE 7
RULE 8
RULE 9
RULE 10
RULE 11
DOUBLE DROPOUT TO NORTH (FIRST VERT. WH. ZONE)
DOUBLE DROPOUT TO NORTH (SECOND VERT. WH. ZONE)
T-8 (+)
8-3
AC 8
OR-1
300
68
465
558
438
TP
556
550
646
621

FIG. 8H

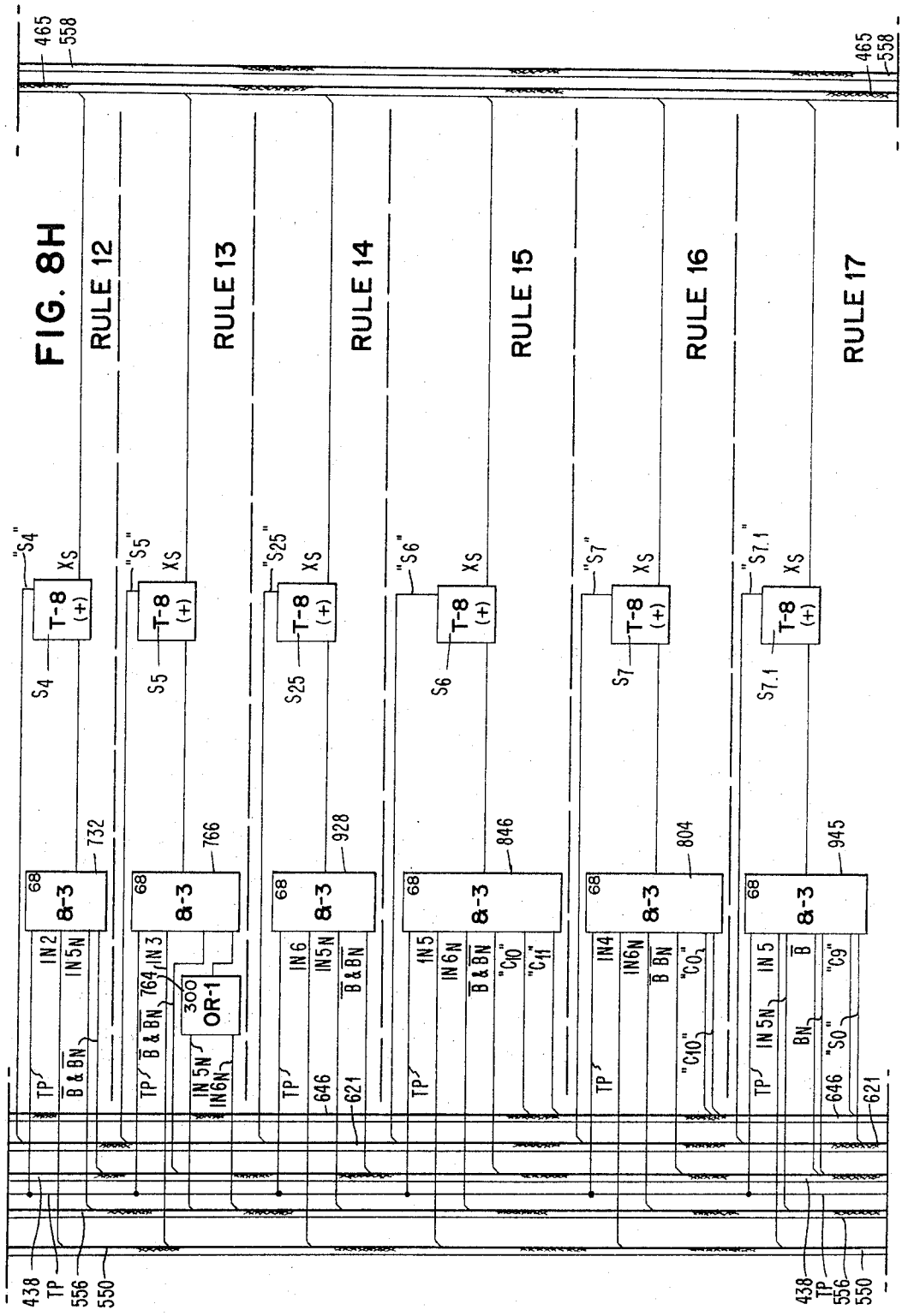

RULE 12
RULE 13
RULE 14
RULE 15
RULE 16
RULE 17
465
558
"S4"
"S5"
"S25"
"S6"
"S7"
"S7.1"
XS
T-8 (+)
S4
S5
S25
S6
S7
S7.1
68
8-3
732
766
928
846
804
945
IN 2
IN 5N
IN 3
IN 6
IN 5
IN 6N
IN 4
B & B̄N
B̄ & BN
B̄ BN
B̄
BN
TP
764
300
OR-1
IN 5N
IN 6N
646
621
"C10"
"C11"
"C0"
"C9"
"S0"
438
556
550

FIG. 8I

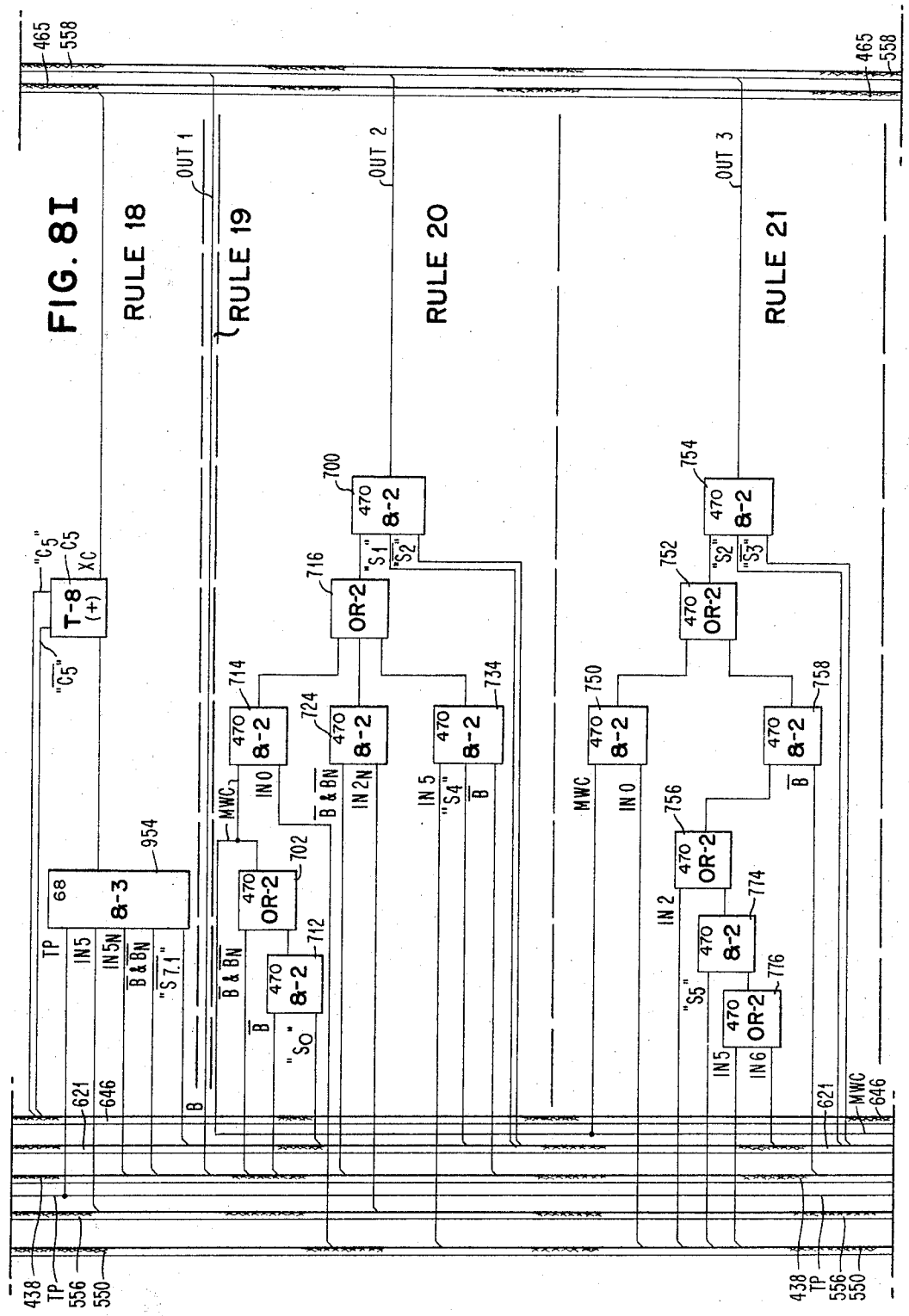

RULE 18
RULE 19
RULE 20
RULE 21
OUT 1
OUT 2
OUT 3
T-8 (+)
8-3
8-2
OR-2
470
465
558
954
700
702
712
714
716
724
734
750
752
754
756
758
774
776
MWC
IN 0
IN 2
IN 5
IN 6
IN 2N
IN 5N
TP
621
646
438
556
550

FIG. 8J

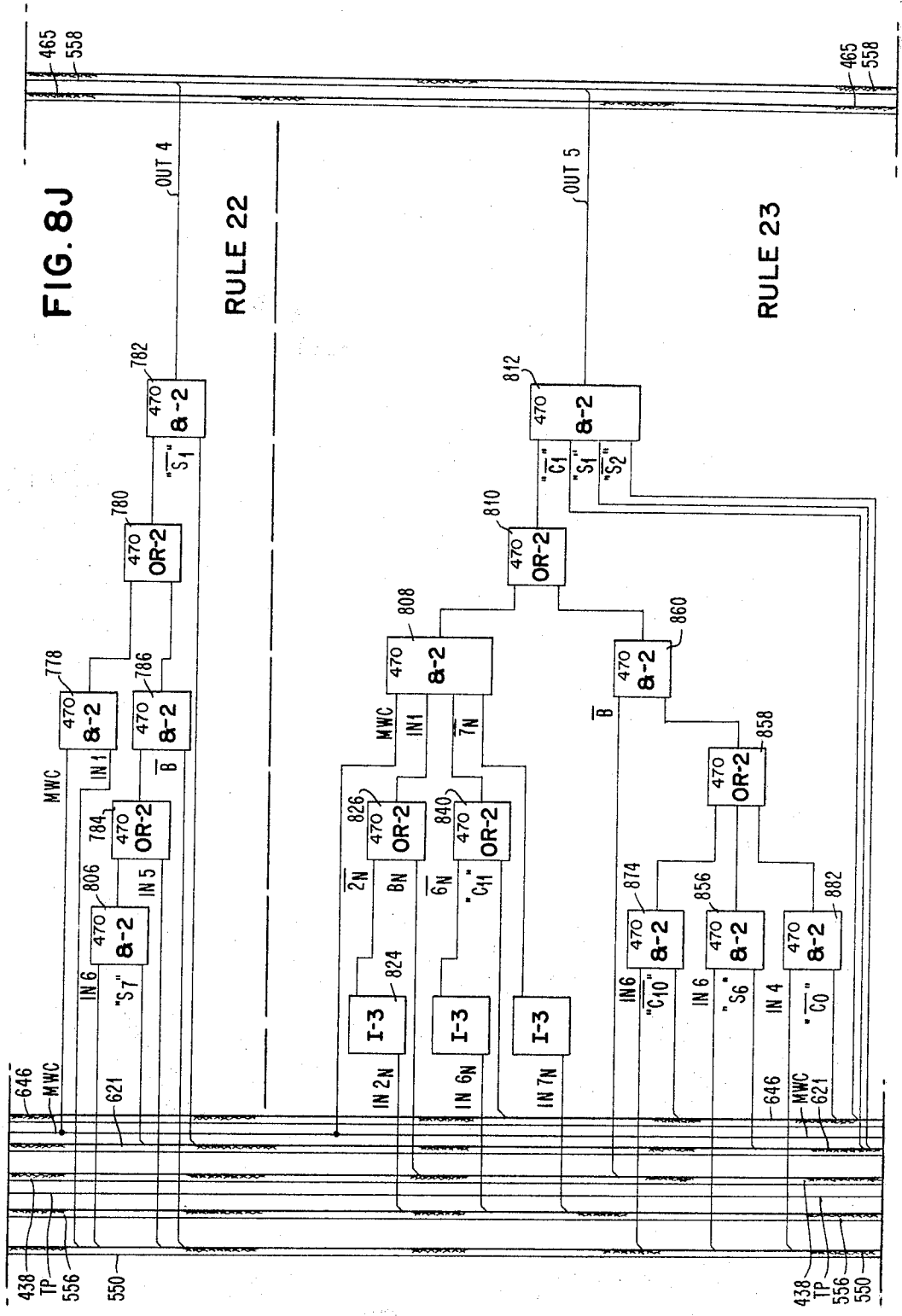
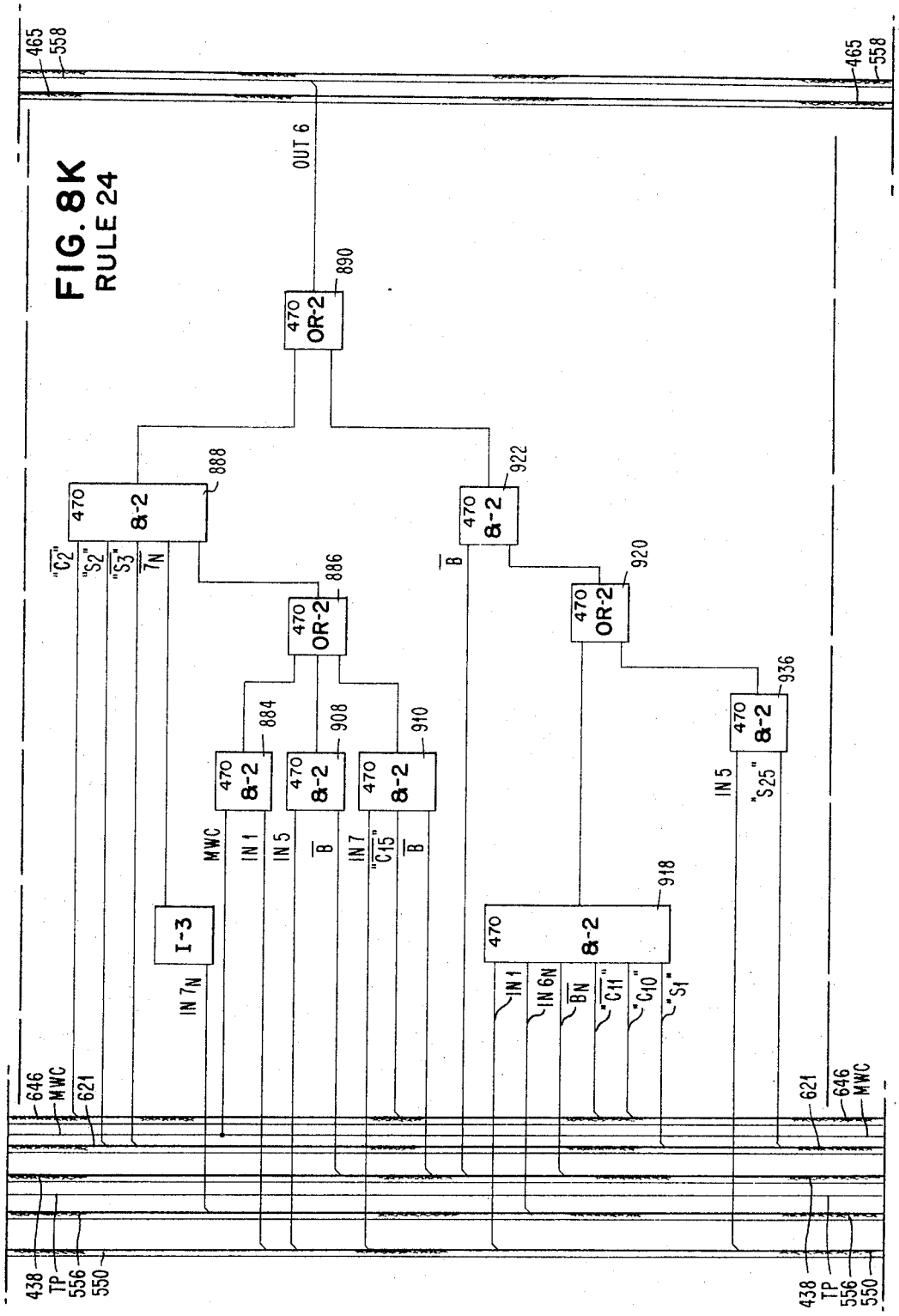

RULE 22
RULE 23
OUT 4
OUT 5
465
558
782
780
778
786
784
806
808
810
812
826
840
824
858
860
856
874
882
646
621
438
TP
556
550
MWC
IN 1
IN 2N
IN 6N
IN 7N
IN 5
IN 6
IN 4
470
8-2
OR-2
I-3

FIG. 8K
RULE 24



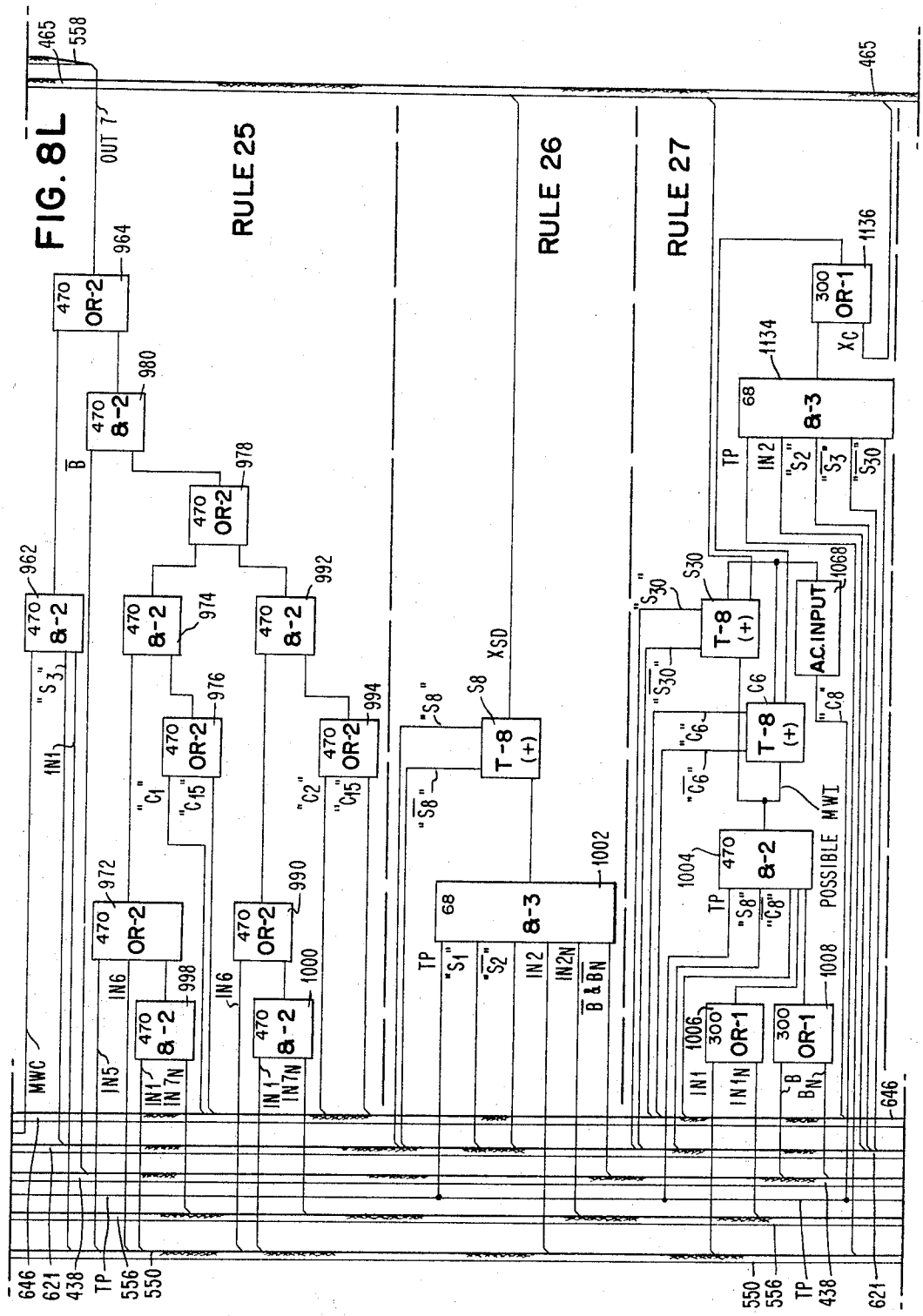

FIG. 8L
RULE 25
RULE 26
RULE 27
OUT 7
OR-2
a-2
a-3
T-8 (+)
OR-1
AC.INPUT
POSSIBLE MWI
MWC
TP
IN1
IN2
IN5
IN6
IN7N
IN2N
B & B̄N
646
621
438
556
550
465
558
964
980
978
962
974
992
976
994
972
990
998
1000
1002
1004
1006
1008
1134
1136
1068

FIG. 8M

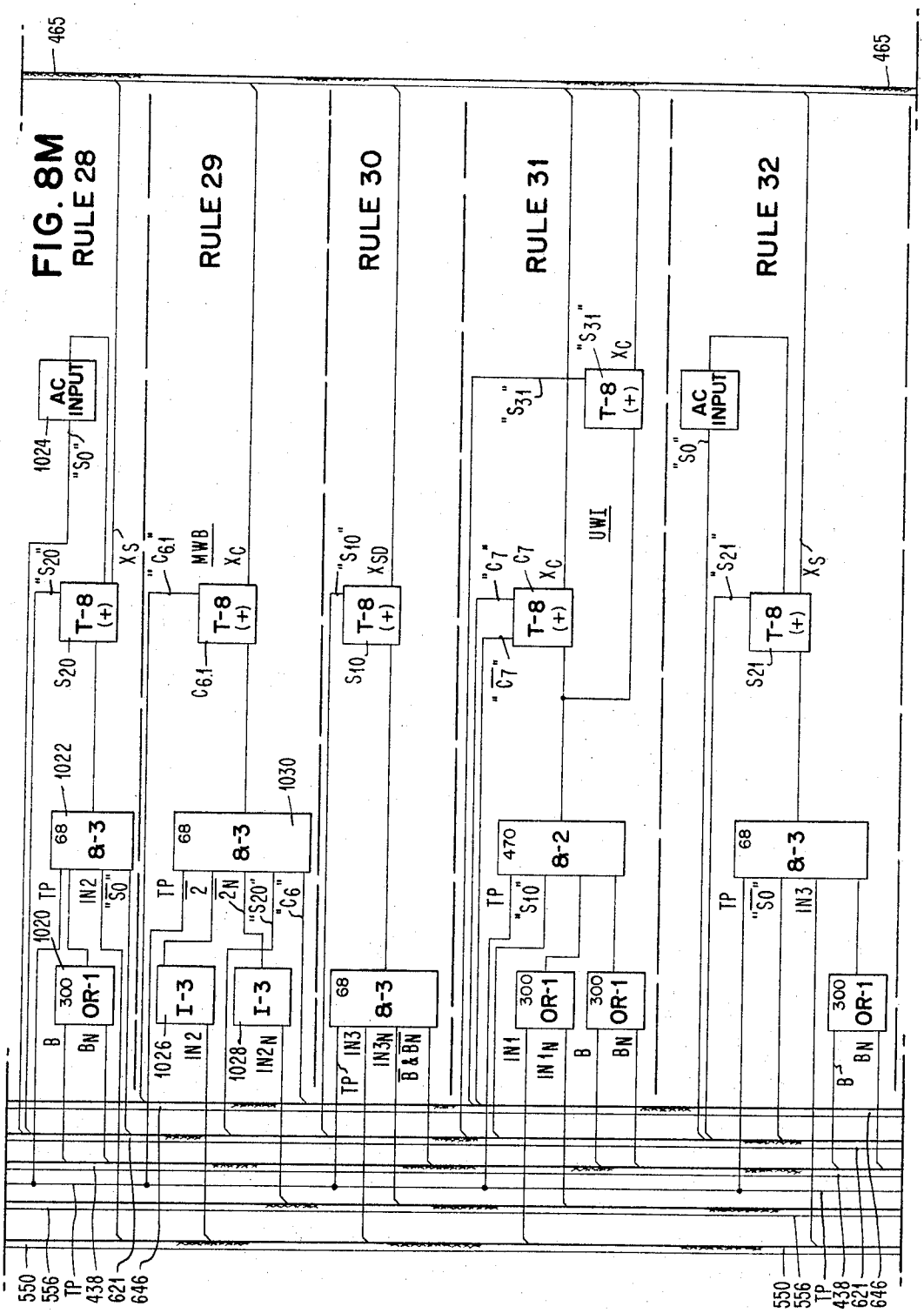

RULE 28
RULE 29
RULE 30
RULE 31
RULE 32
465
AC INPUT
T-8 (+)
8-3
8-2
I-3
OR-1
1024
1022
1020
1026
1028
1030
470
300
68
"S0"
"S20"
"C6.1"
"S10"
"C7"
"S31"
"S21"
MWB
UWI
TP
IN1
IN2
IN3
B
BN
550
556
438
621
646

FIG. 8N

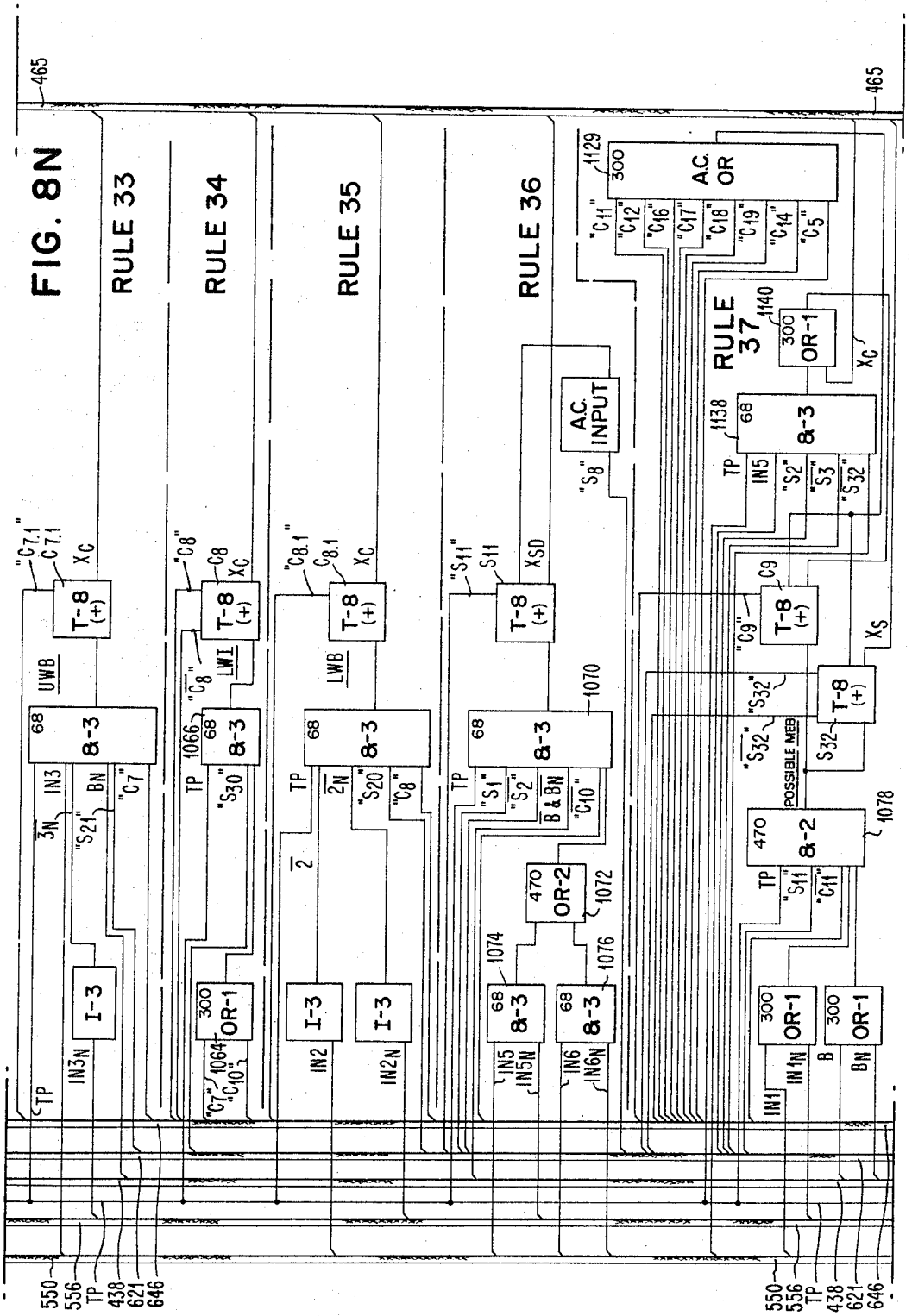

RULE 33
RULE 34
RULE 35
RULE 36
RULE 37
A.C. INPUT
A.C. OR
T-8 (+)
8-3
I-3
OR-1
OR-2
8-2
UWB
LWB
LWI
TP
POSSIBLE MEB
465
550
556
438
621
646
1070
1072
1074
1076
1078
1138
1140
1129

FIG. 8 O

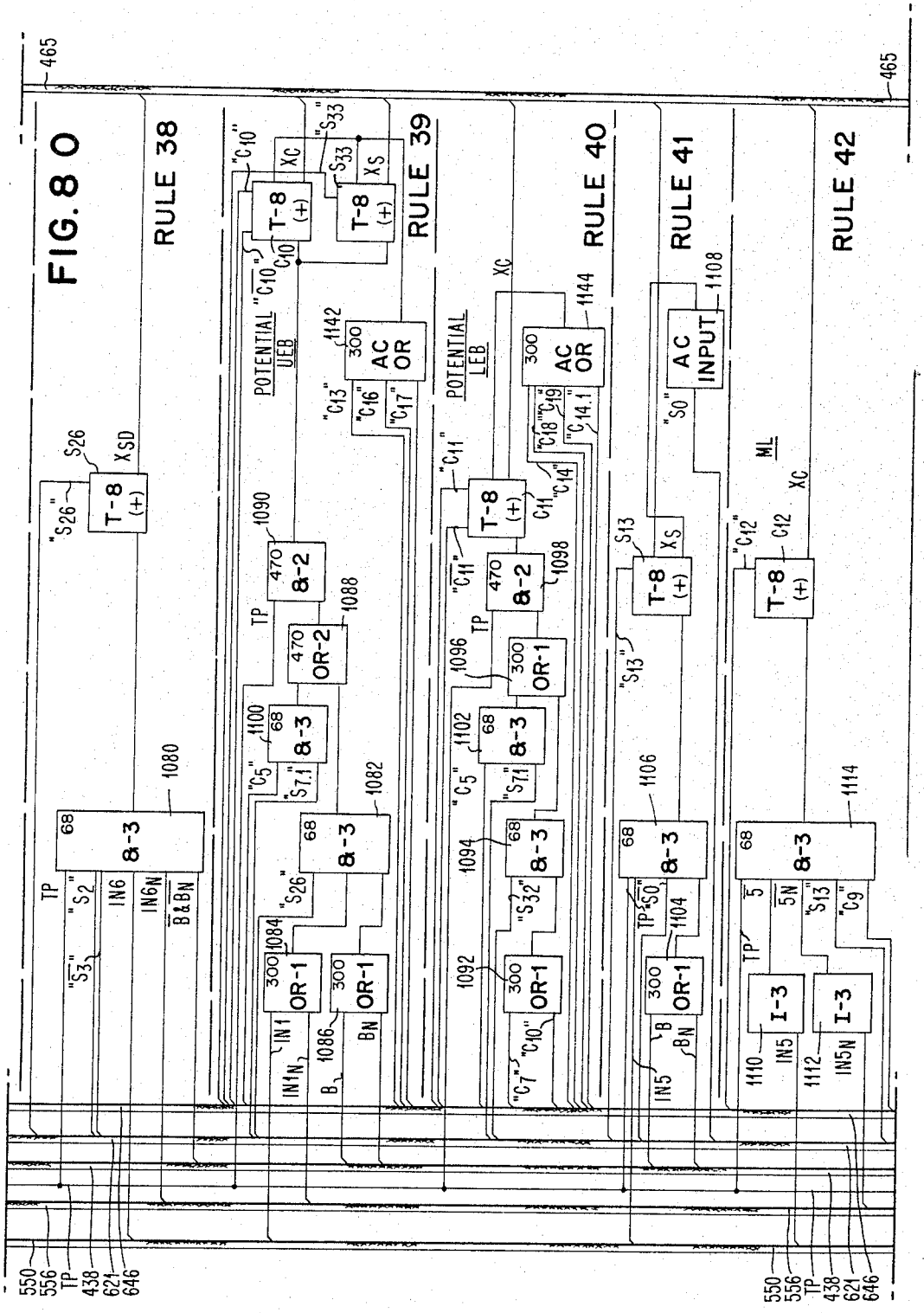
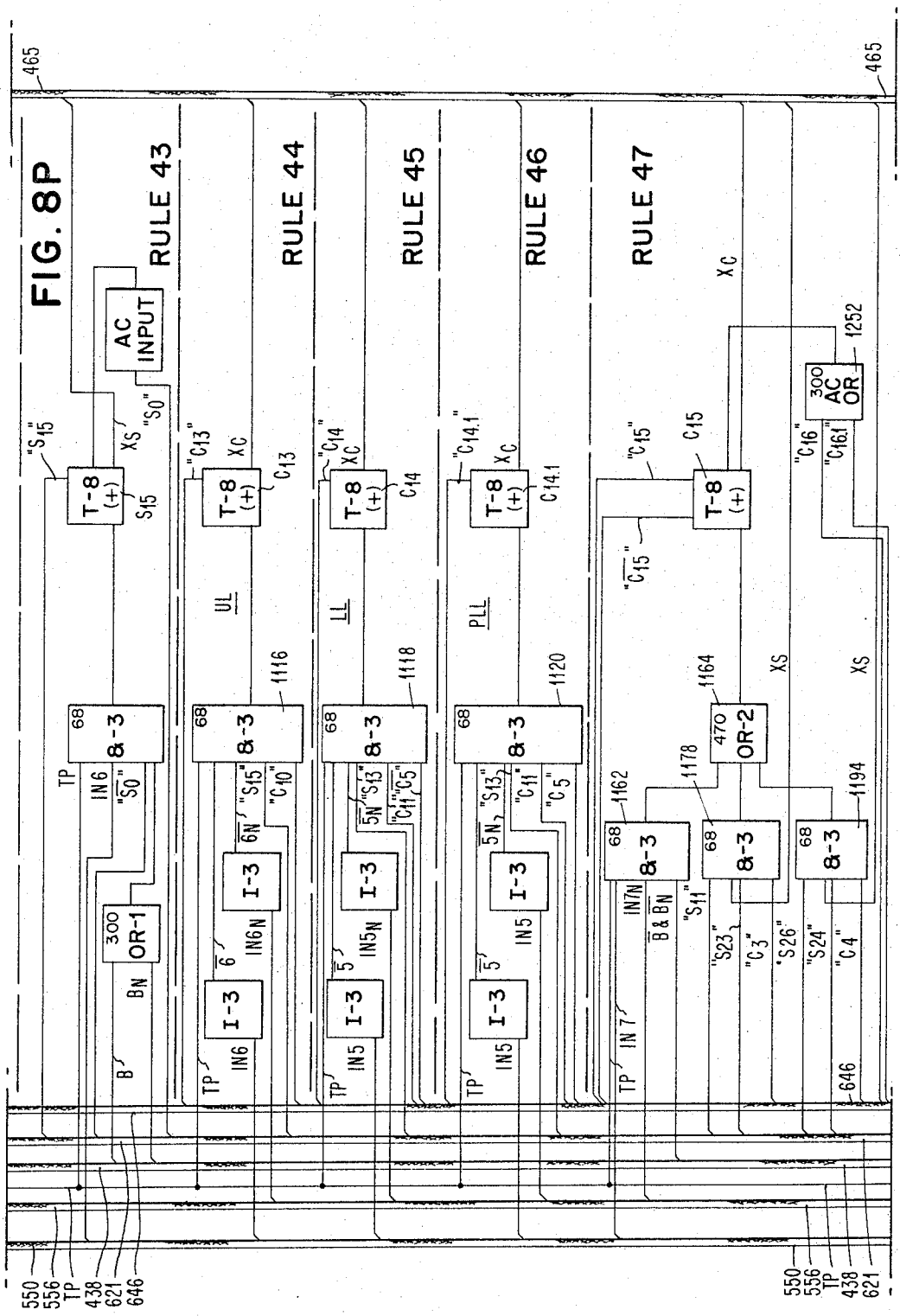

RULE 38
RULE 39
RULE 40
RULE 41
RULE 42
465
T-8 (+)
XSD
XC
XS
AC OR
AC INPUT
8-3
8-2
OR-1
OR-2
I-3
POTENTIAL UEB
POTENTIAL LEB
ML
TP
IN6
IN6N
B&BN
IN1
IN1N
B
BN
IN5
IN5N
5
5N
550
556
438
621
646
1080
1082
1084
1086
1088
1090
1092
1094
1096
1098
1100
1102
1104
1106
1108
1110
1112
1114
1142
1144

FIG. 8P


RULE 43
RULE 44
RULE 45
RULE 46
RULE 47
AC INPUT
T-8 (+)
8-3
I-3
OR-1
OR-2
AC OR
UL
LL
PLL
XC
XS
TP
465
550
556
438
621
646
1116
1118
1120
1162
1164
1178
1194
1252

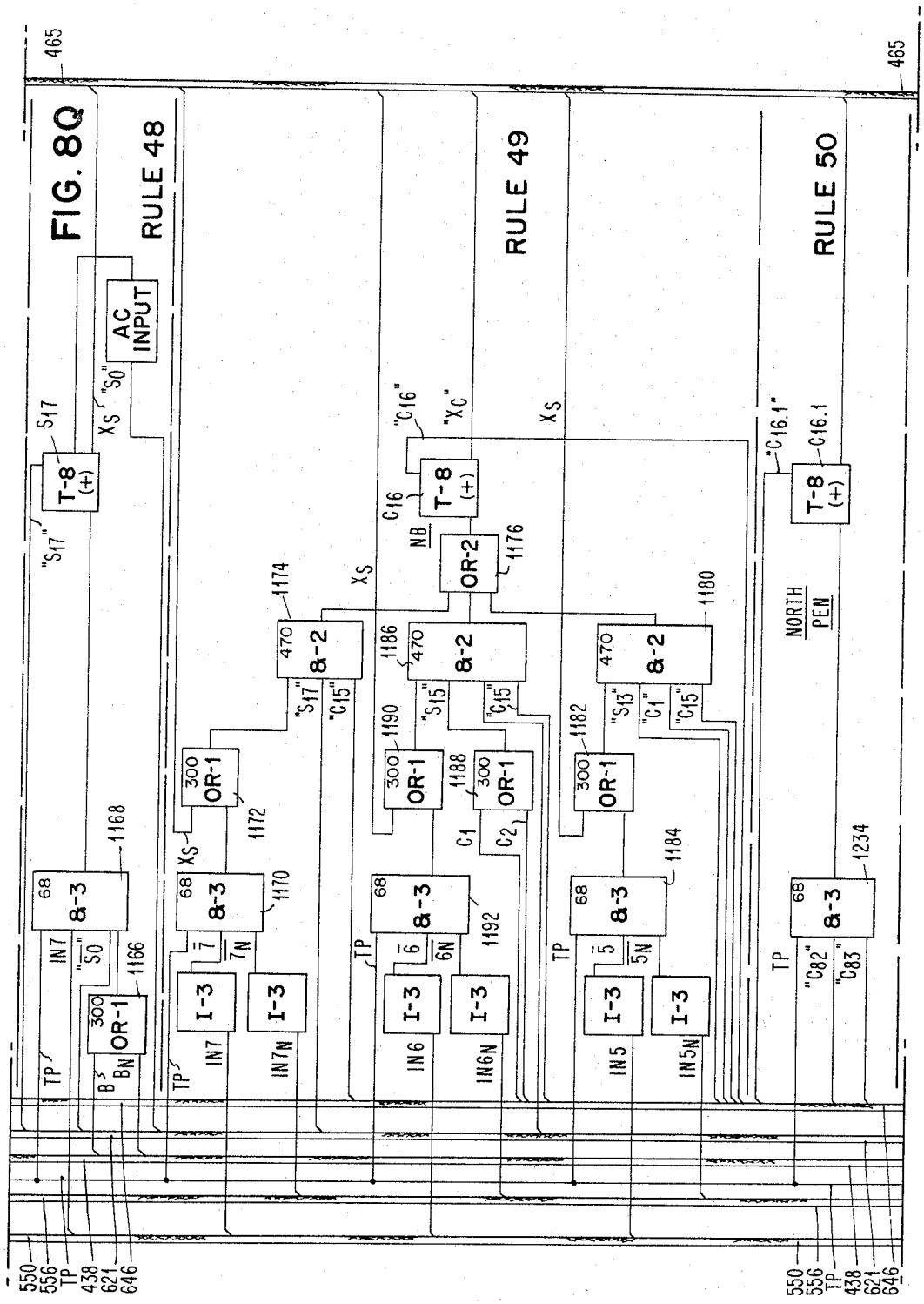
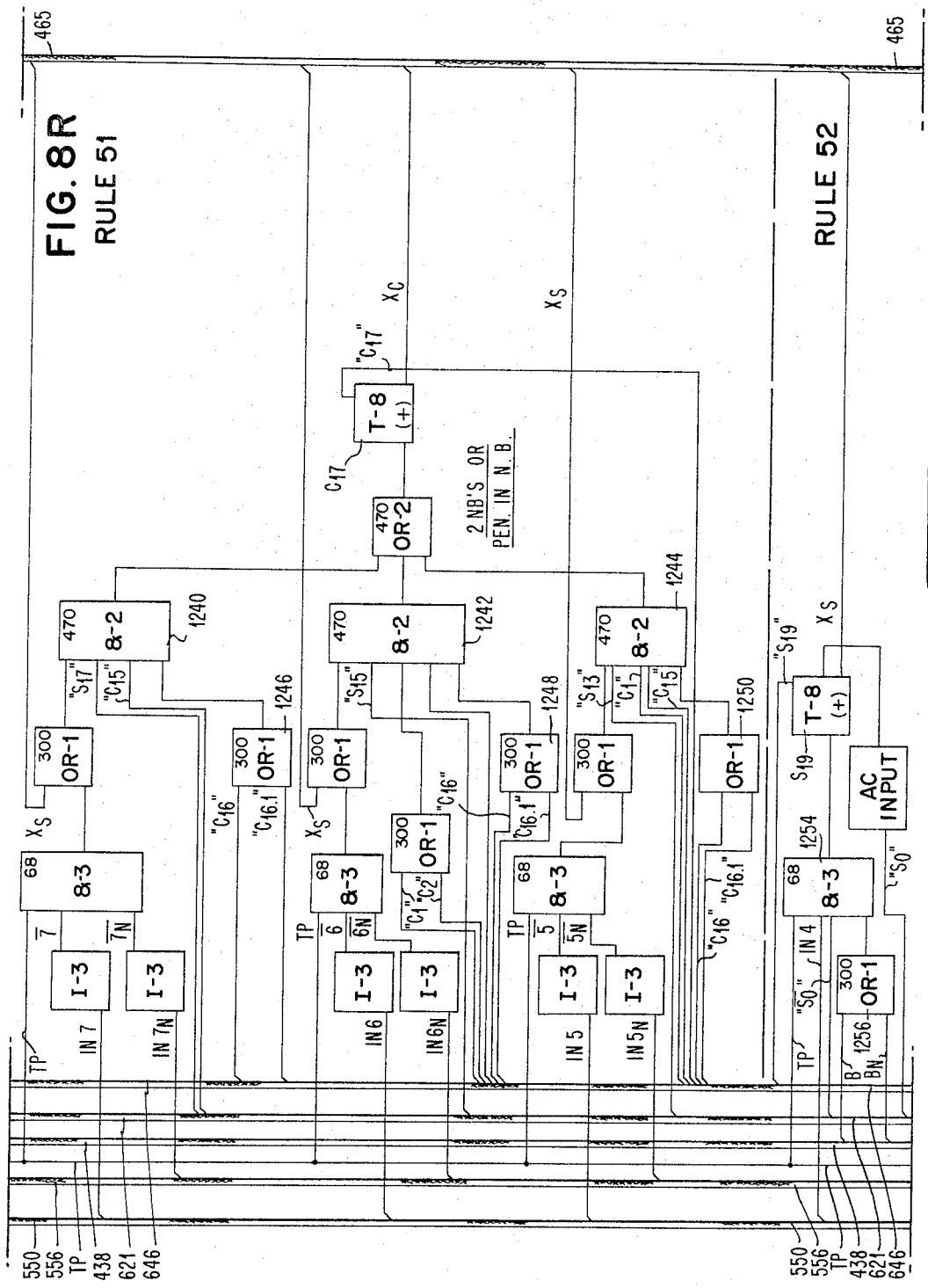
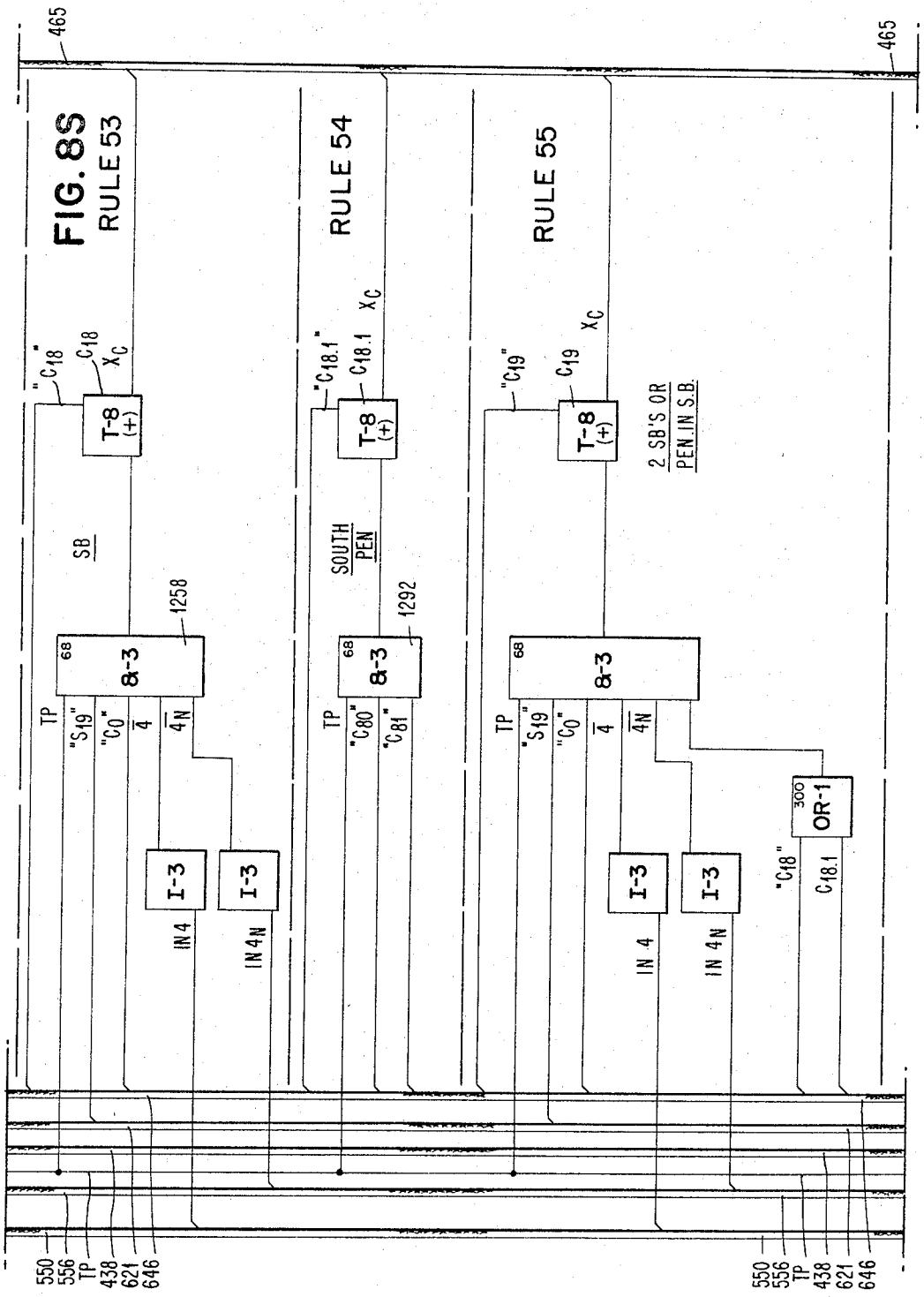

FIG. 8Q
RULE 48
RULE 49
RULE 50
AC INPUT
T-8 (+)
OR-1
OR-2
8-3
8-2
I-3
NORTH PEN
TP
465
550
556
438
621
646

FIG. 8R


RULE 51
RULE 52
465
465
T-8 (+)
2 NB'S OR PEN. IN N. B.
470 OR-2
470 8-2
1240
1242
1244
1246
1248
1250
300 OR-1
68 8-3
I-3
IN 7
IN 7N
IN 6
IN 6N
IN 5
IN 5N
IN 4
AC INPUT
1254
1256
TP
550
556
438
621
646


FIG. 8S
RULE 53
RULE 54
RULE 55
465
"C18" C18 XC
"C18.1" C18.1 XC
"C19" C19 XC
T-8 (+)
SB
SOUTH PEN
2 SB'S OR PEN. IN S.B.
1258
1292
68
8-3
TP
"S19"
"C0"
4
4N
"C80"
"C81"
I-3
IN 4
IN 4N
300
OR-1
"C18"
C18.1
550
556
TP
438
621
646

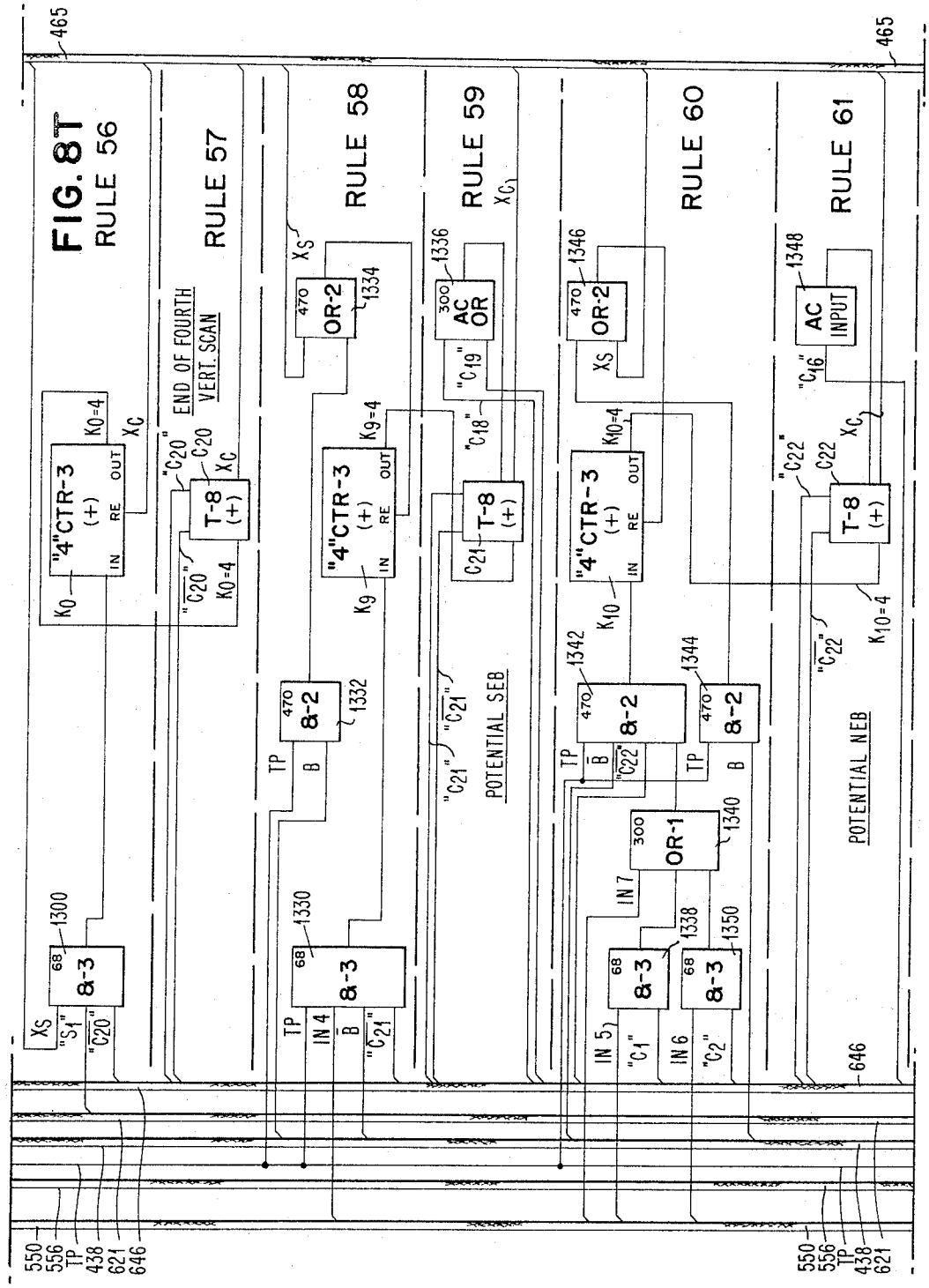
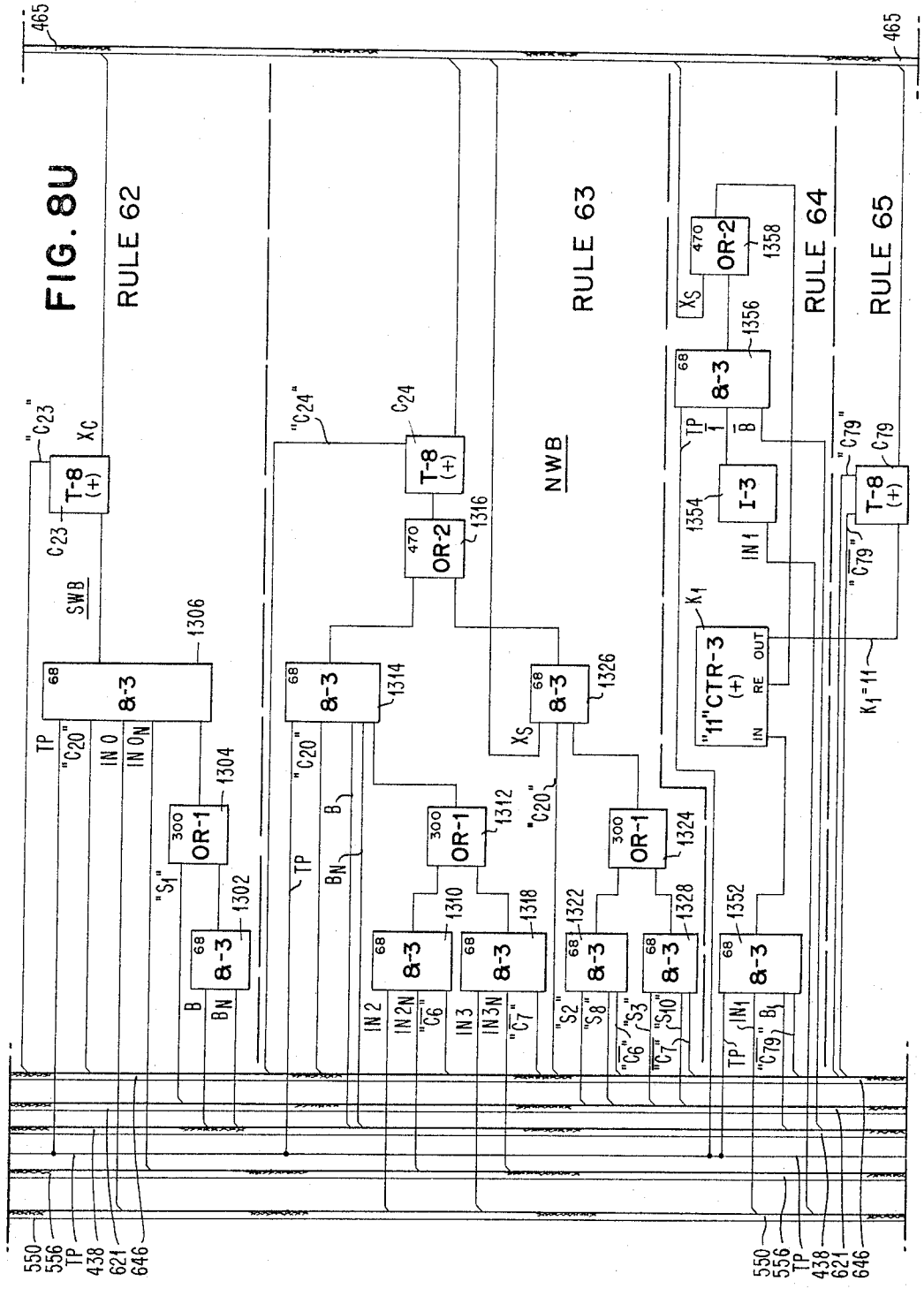

FIG. 8T
RULE 56
RULE 57
RULE 58
RULE 59
RULE 60
RULE 61
END OF FOURTH VERT. SCAN
POTENTIAL SEB
POTENTIAL NEB
"4"CTR-3 (+)
T-8 (+)
AC OR
AC INPUT
OR-2
OR-1
8-2
8-3
465
550
556
TP
438
621
646

FIG. 8U


RULE 62
RULE 63
RULE 64
RULE 65
NWB
SWB
465
T-8 (+)
OR-1
OR-2
I-3
8-3
"11" CTR-3 (+)
IN
RE
OUT
TP
IN 0
IN 0N
IN 2
IN 2N
IN 3
IN 3N
IN 1
550
556
TP
438
621
646

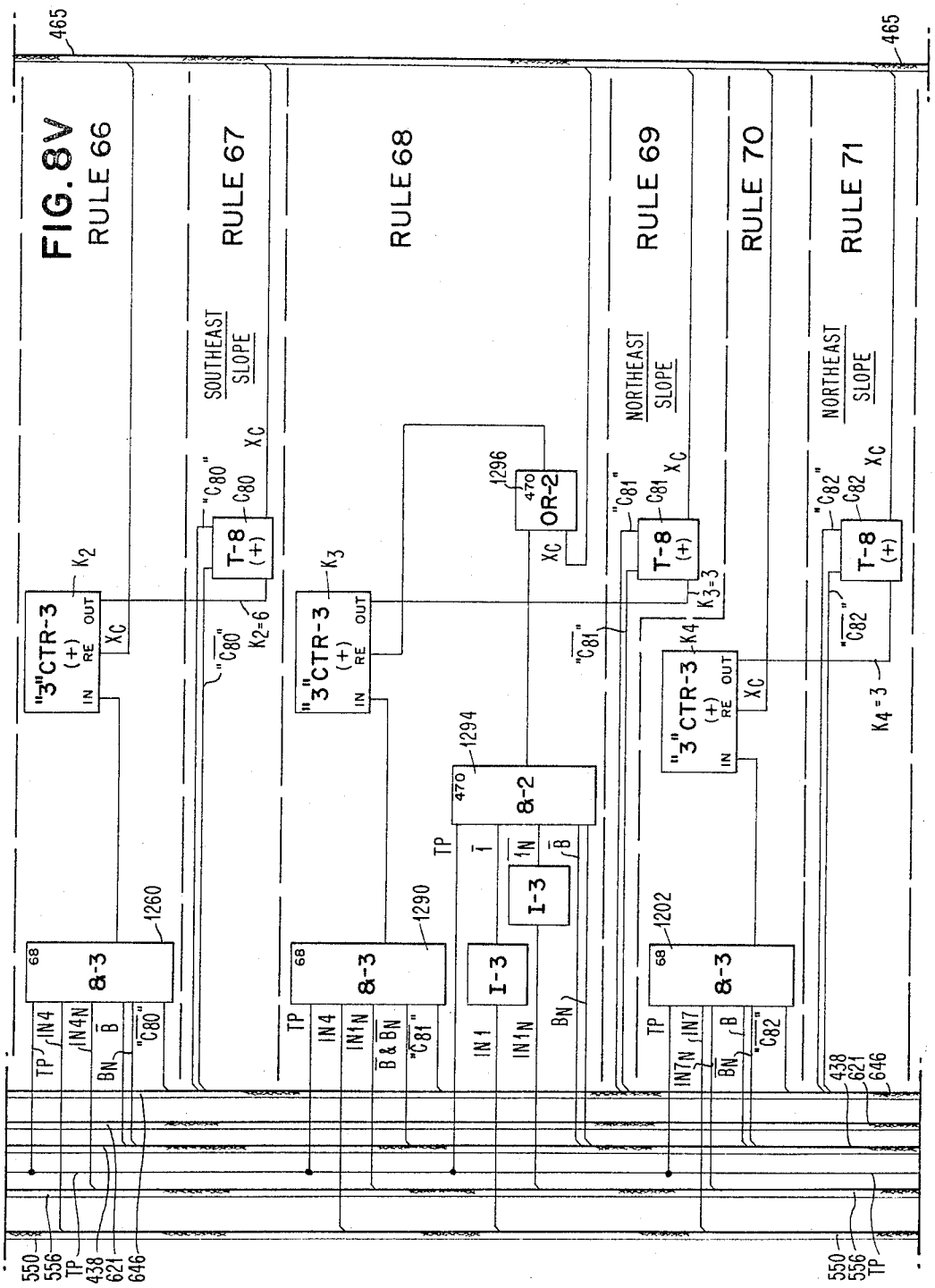

FIG. 8V
RULE 66
RULE 67
RULE 68
RULE 69
RULE 70
RULE 71
SOUTHEAST SLOPE
NORTHEAST SLOPE
"3"CTR-3
T-8 (+)
OR-2
8-3
8-2
I-3
465
1260
1290
1294
1296
1202
K2=6
K3=3
K4=3
K4
XC
TP
IN4
IN4N
BN
B
"C80"
C80
"C81"
C81
"C82"
C82
IN1
IN1N
B & BN
IN7
IN7N
438
621
646
550
556

FIG. 8W

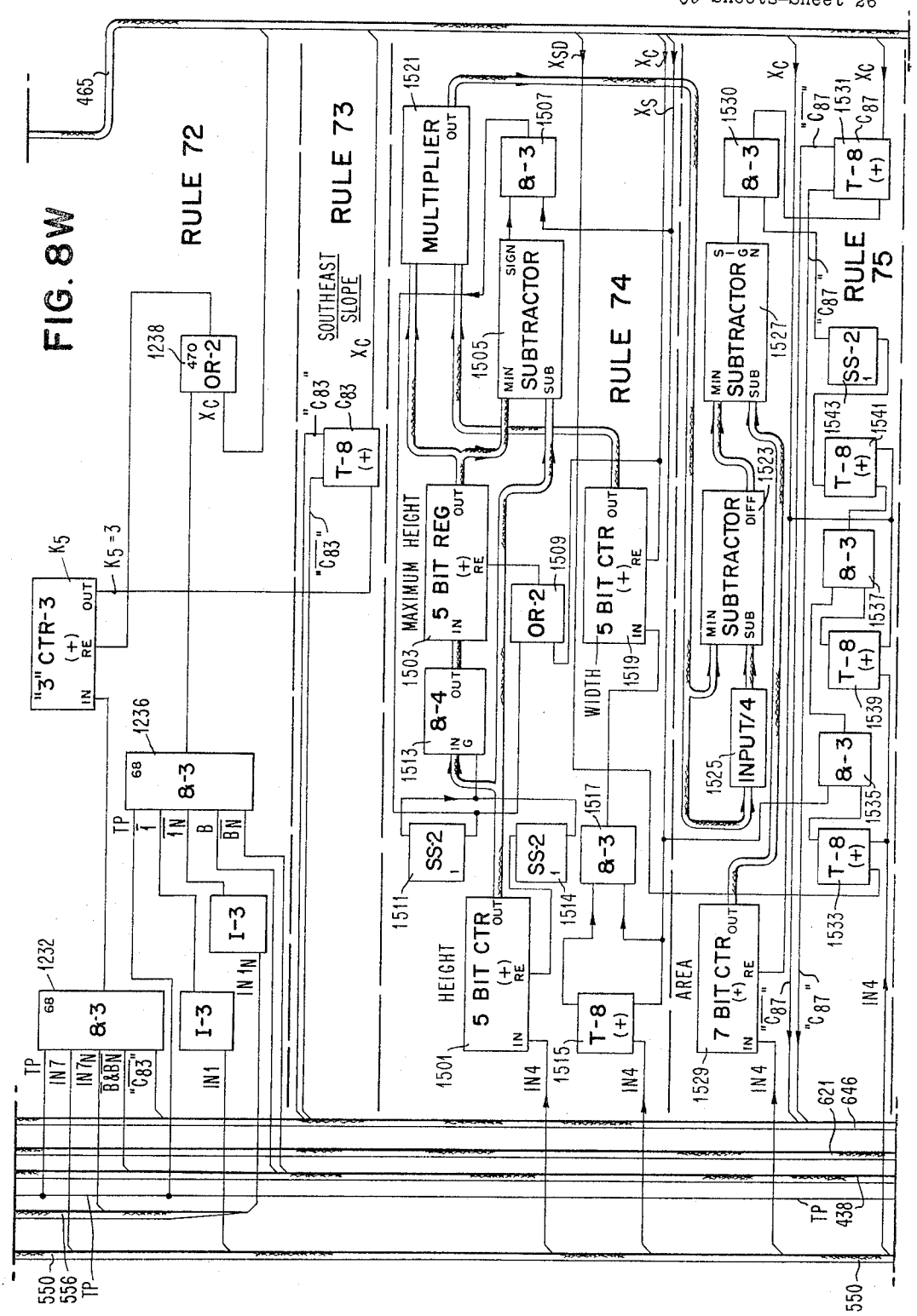
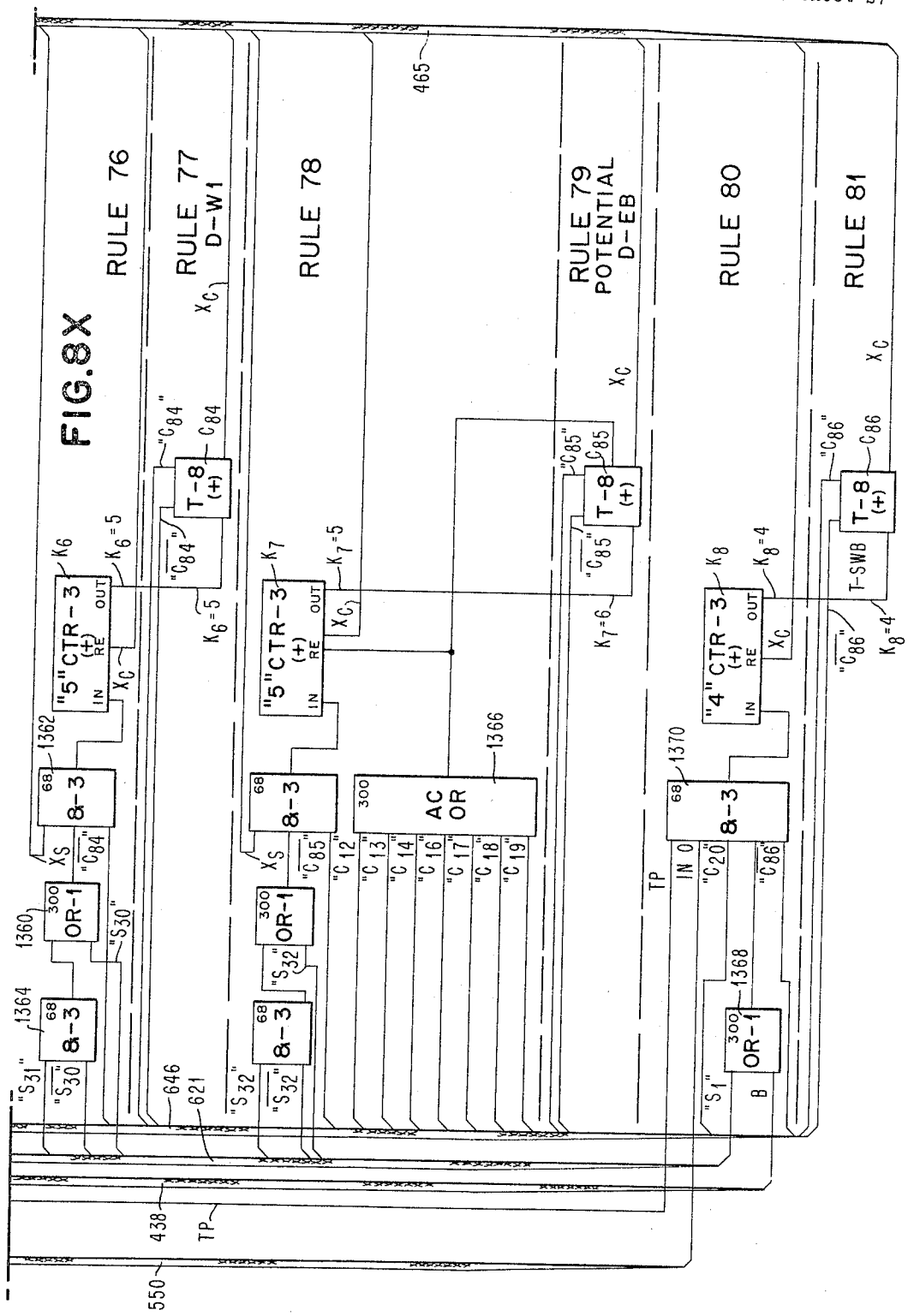

RULE 72
RULE 73
RULE 74
RULE 75
SOUTHEAST SLOPE
MAXIMUM HEIGHT
HEIGHT
WIDTH
AREA
MULTIPLIER
SUBTRACTOR
INPUT/4
"3" CTR-3
OR-2
I-3
T-8
SS-2
5 BIT REG
5 BIT CTR
7 BIT CTR
465
1238
1236
1232
1503
1505
1507
1509
1511
1513
1514
1515
1517
1519
1521
1523
1525
1527
1529
1530
1531
1533
1535
1537
1539
1541
1543
1501
550
556
TP
438
621
646

FIG. 8X


RULE 76
RULE 77 D-W1
RULE 78
RULE 79 POTENTIAL D-EB
RULE 80
RULE 81
465
"5" CTR-3 (+)
"4" CTR-3 (+)
T-8 (+)
T-SWB
8-3
AC OR
OR-1
IN
OUT
RE
646
621
438
550
TP

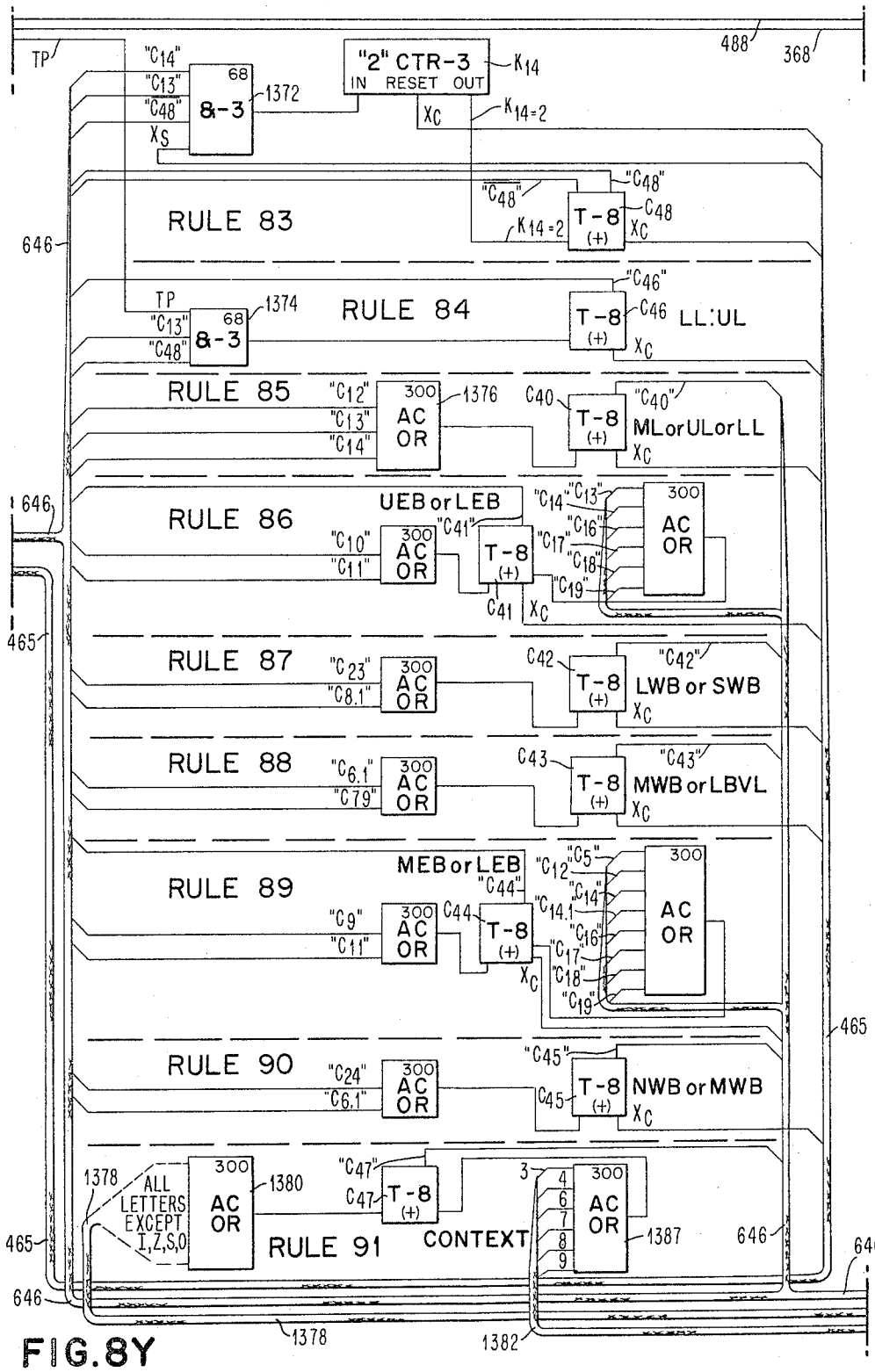

TP
"C14"
"C13"
"C48"
XS
68
&-3
1372
"2" CTR-3
IN RESET OUT
K14
XC
K14=2
488
368
RULE 83
"C48"
T-8
(+)
C48
646
RULE 84
"C46"
C46
LL:UL
1374
RULE 85
"C12"
"C13"
"C14"
300
AC
OR
1376
C40
"C40"
MLorULorLL
RULE 86
UEB or LEB
"C41"
"C10"
"C11"
"C15"
"C16"
"C17"
"C18"
"C19"
C41
465
RULE 87
"C23"
"C8.1"
C42
"C42"
LWB or SWB
RULE 88
"C6.1"
"C79"
C43
"C43"
MWB or LBVL
RULE 89
MEB or LEB
"C44"
"C9"
"C11"
C44
"C5"
"C12"
"C14"
"C14.1"
"C16"
"C17"
"C18"
"C19"
RULE 90
"C24"
"C6.1"
"C45"
C45
NWB or MWB
1378
ALL
LETTERS
EXCEPT
I,Z,S,O
1380
"C47"
C47
RULE 91
CONTEXT
3
4
6
7
8
9
1387
1382

FIG.8Y

FIG. 8Z

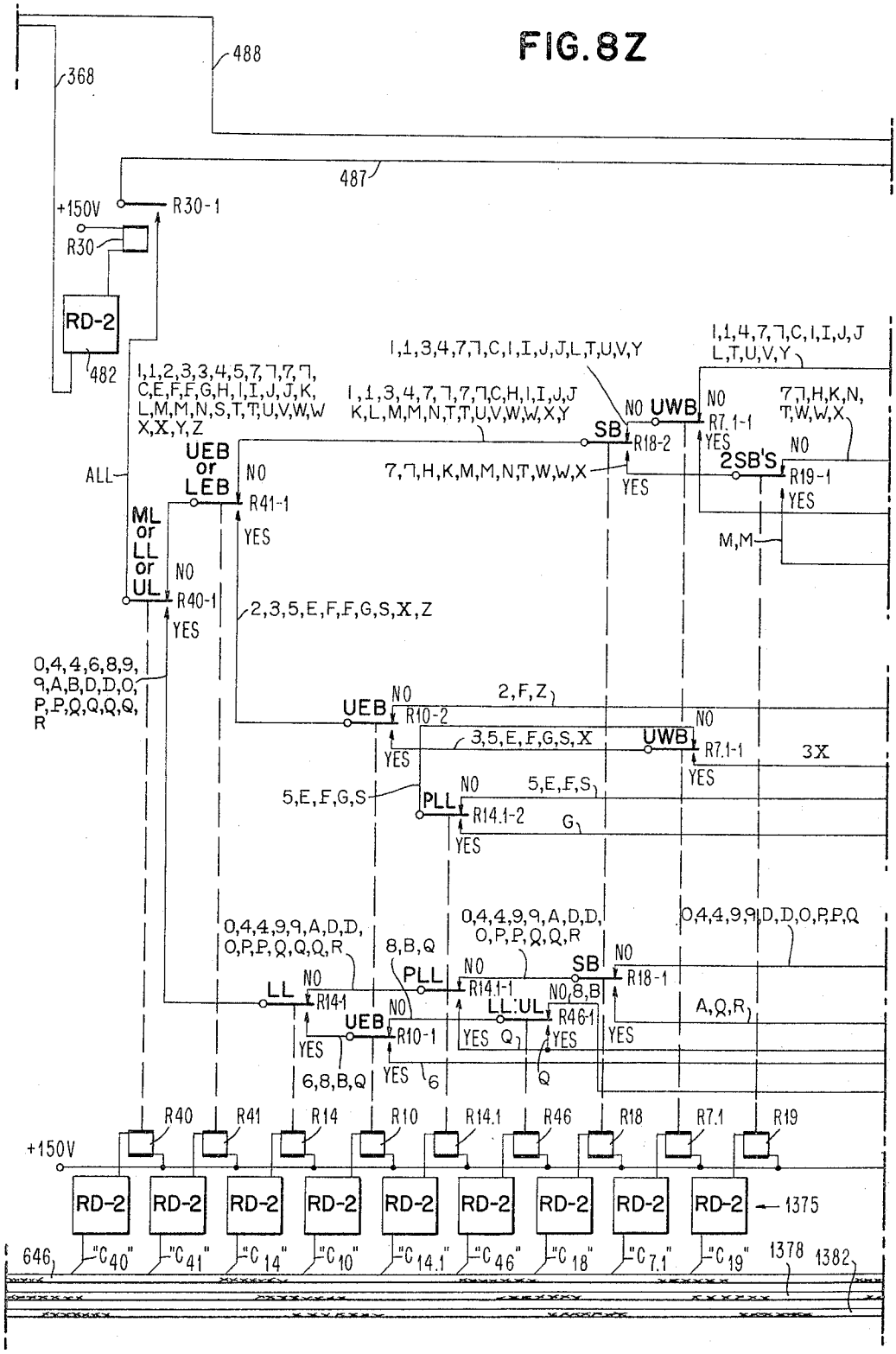

368
488
487
+150V
R30-1
R30
RD-2
482
ALL
UEB or LEB
NO
YES
R41-1
ML or LL or UL
R40-1
2,3,5,E,F,F,G,S,X,Z
0,4,4,6,8,9,9,A,B,D,D,O,P,P,Q,Q,Q,Q,R
UEB
R10-2
2,F,Z
3,5,E,F,G,S,X
UWB
R7.1-1
3X
PLL
R14.1-2
5,E,F,G,S
G
0,4,4,9,9,A,D,D,O,P,P,Q,Q,Q,R
8,B,Q
LL
R14-1
LL:UL
R46-1
R10-1
6,8,B,Q
A,Q,R
SB
R18-1
R18-2
2SB's
R19-1
M,M
R40
R41
R14
R10
R14.1
R46
R18
R7.1
R19
1375
646
"C40"
"C41"
"C14"
"C10"
"C14.1"
"C46"
"C18"
"C7.1"
"C19"
1378
1382

FIG.8AA

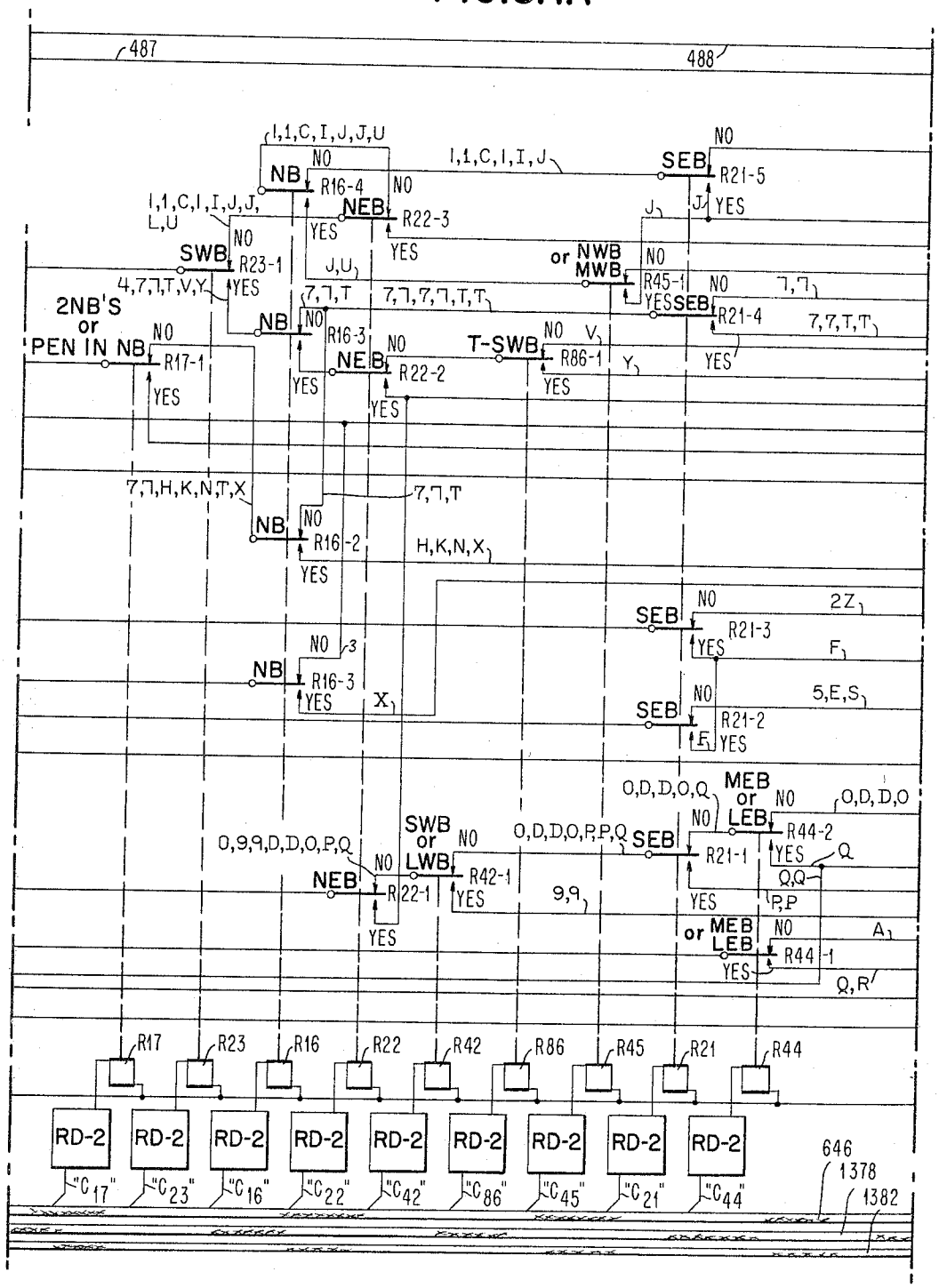

487
488
NB
R16-4
NEB
R22-3
SWB
R23-1
2NB'S or PEN IN NB
R17-1
NB
R16-3
NEB
R22-2
NB
R16-2
NB
R16-3
SEB
R21-5
or NWB MWB
R45-1
SEB
R21-4
T-SWB
R86-1
SEB
R21-3
SEB
R21-2
MEB or LEB
R44-2
SEB
R21-1
SWB or LWB
R42-1
NEB
R22-1
or MEB LEB
R44-1
R17
R23
R16
R22
R42
R86
R45
R21
R44
RD-2
"C17"
"C23"
"C16"
"C22"
"C42"
"C86"
"C45"
"C21"
"C44"
646
1378
1382

FIG.8BB

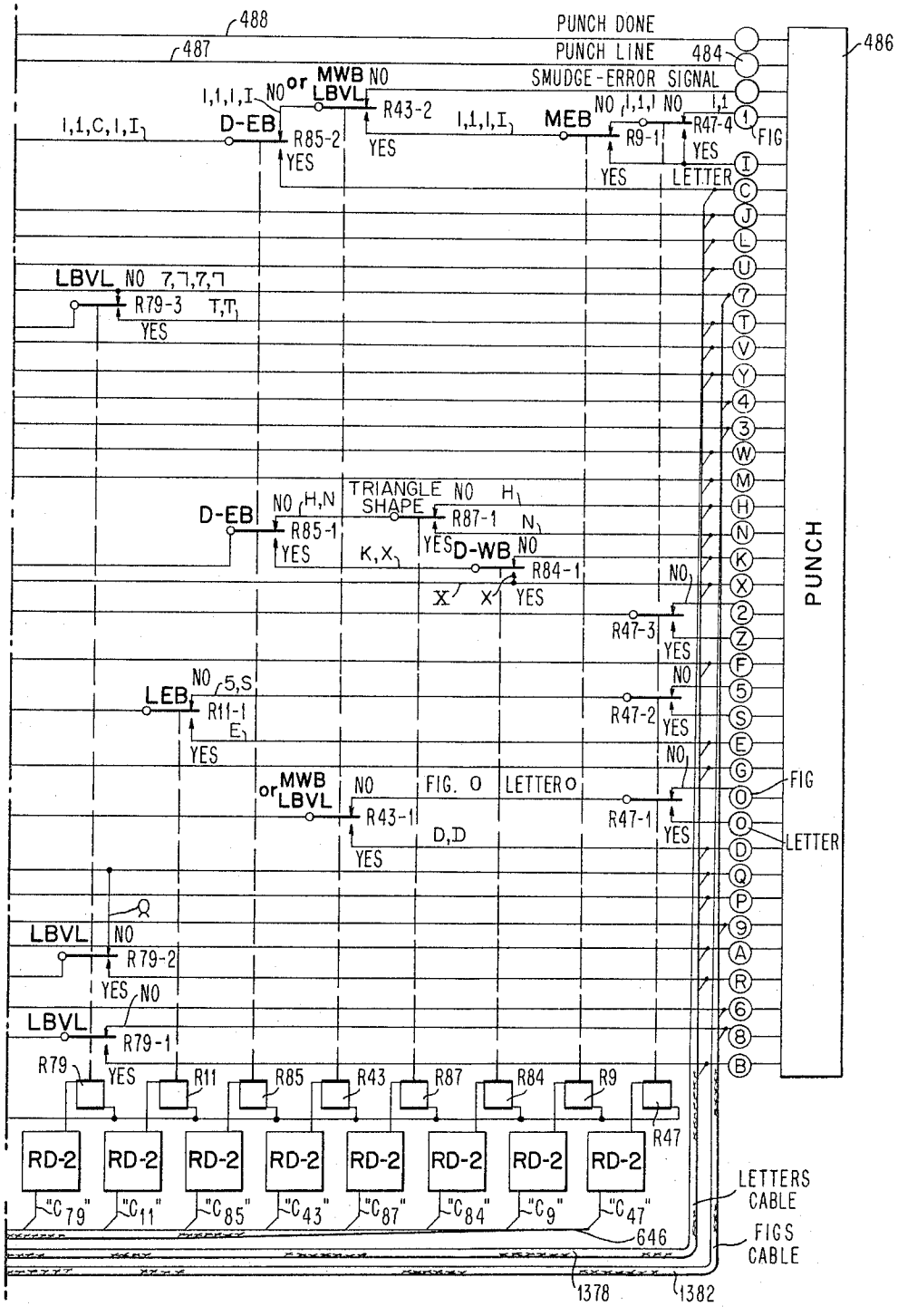
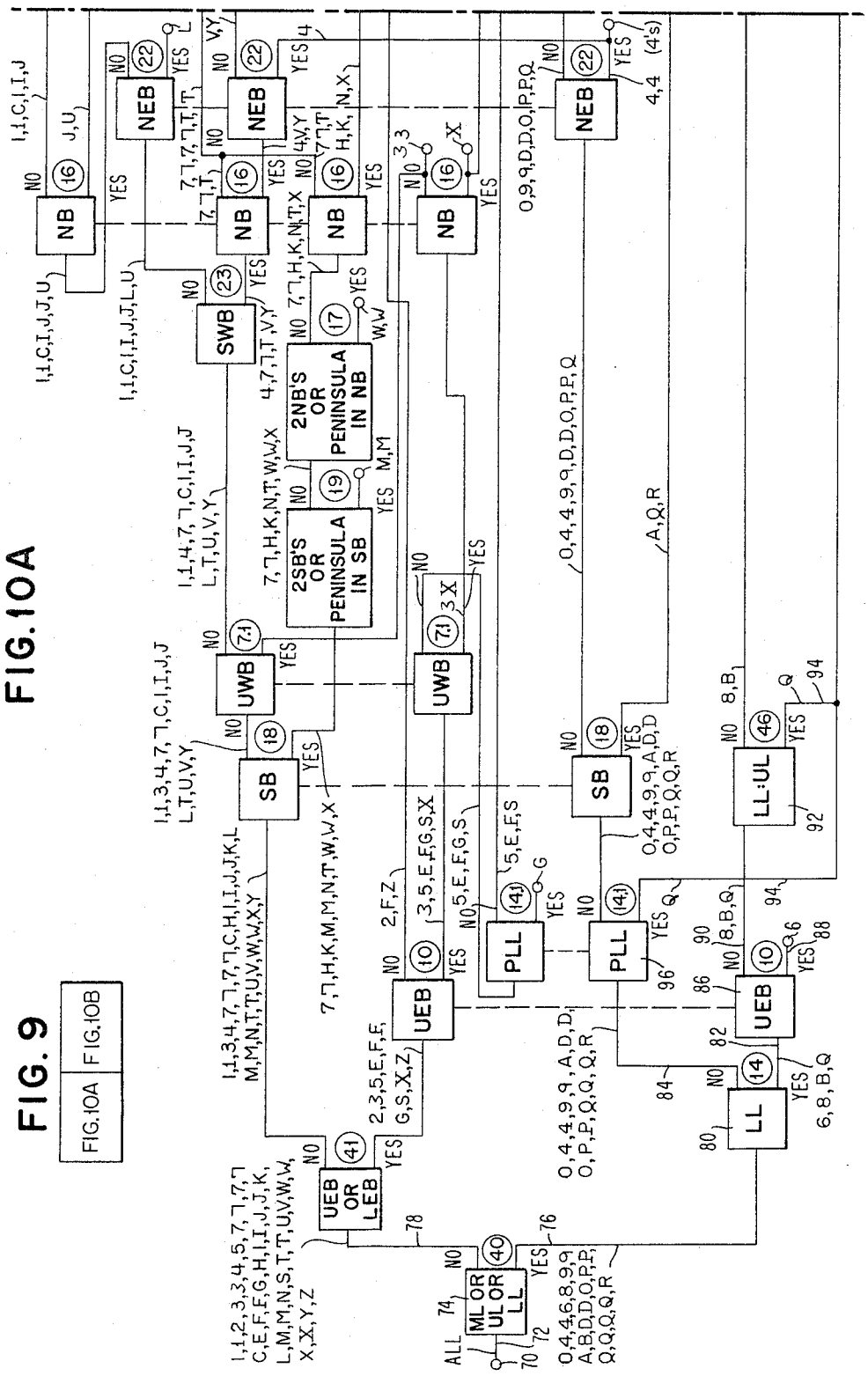

488
487
PUNCH DONE
PUNCH LINE
SMUDGE-ERROR SIGNAL
484
486
PUNCH
D-EB
R85-2
YES
MWB or LBVL
NO
R43-2
YES
MEB
R9-1
R47-4
FIG
LETTER
LBVL
R79-3
YES
D-EB
R85-1
YES
TRIANGLE SHAPE
R87-1
D-WB
R84-1
YES
R47-3
R47-2
LEB
R11-1
YES
MWB or LBVL
FIG. O
LETTER O
R43-1
YES
R47-1
LBVL
R79-2
LBVL
R79-1
R79
R11
R85
R43
R87
R84
R9
R47
RD-2
"C79"
"C11"
"C85"
"C43"
"C87"
"C84"
"C9"
"C47"
646
LETTERS CABLE
FIGS CABLE
1378
1382

FIG. 9

FIG. 10A | FIG. 10B

FIG. 10A



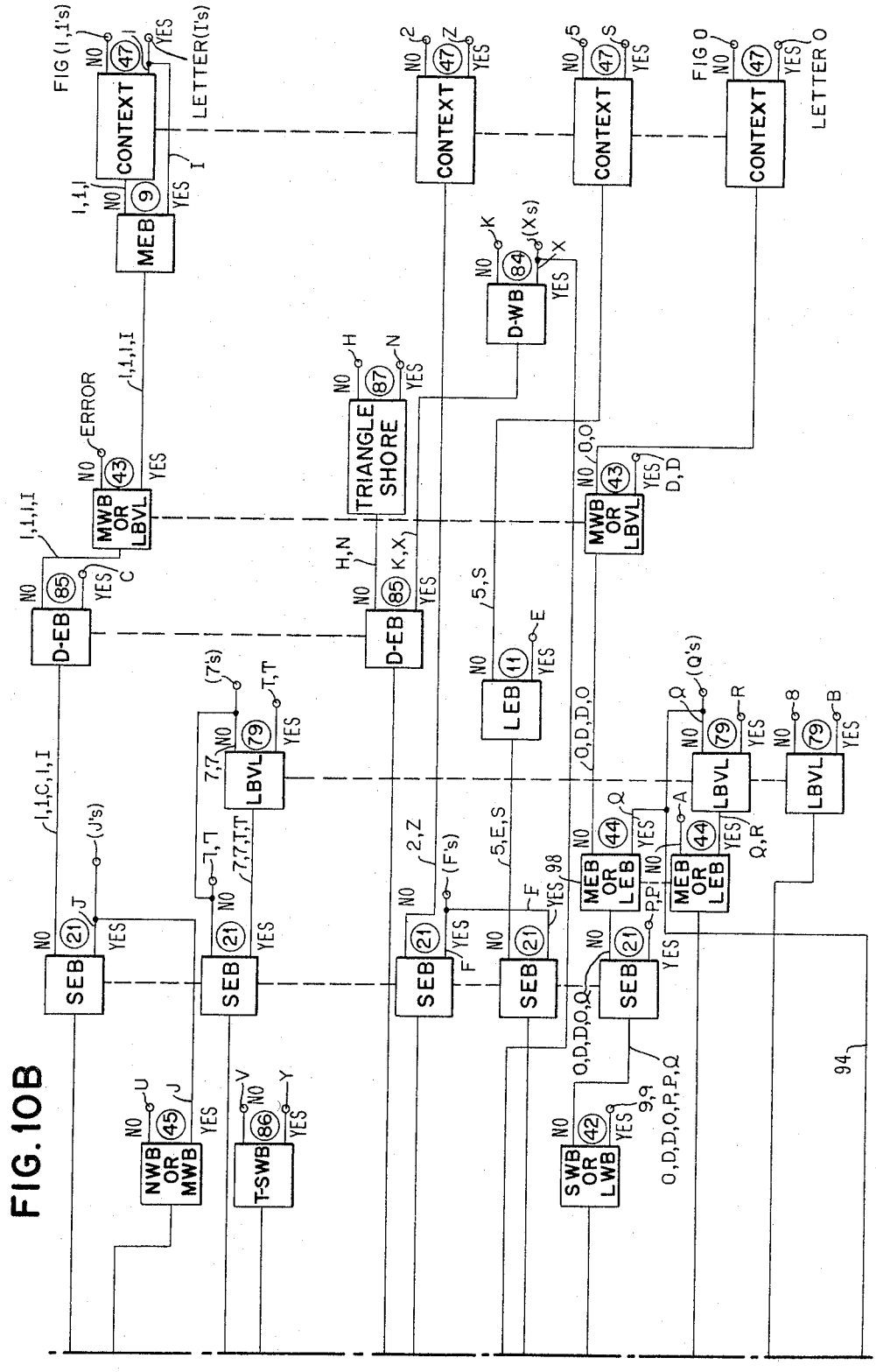
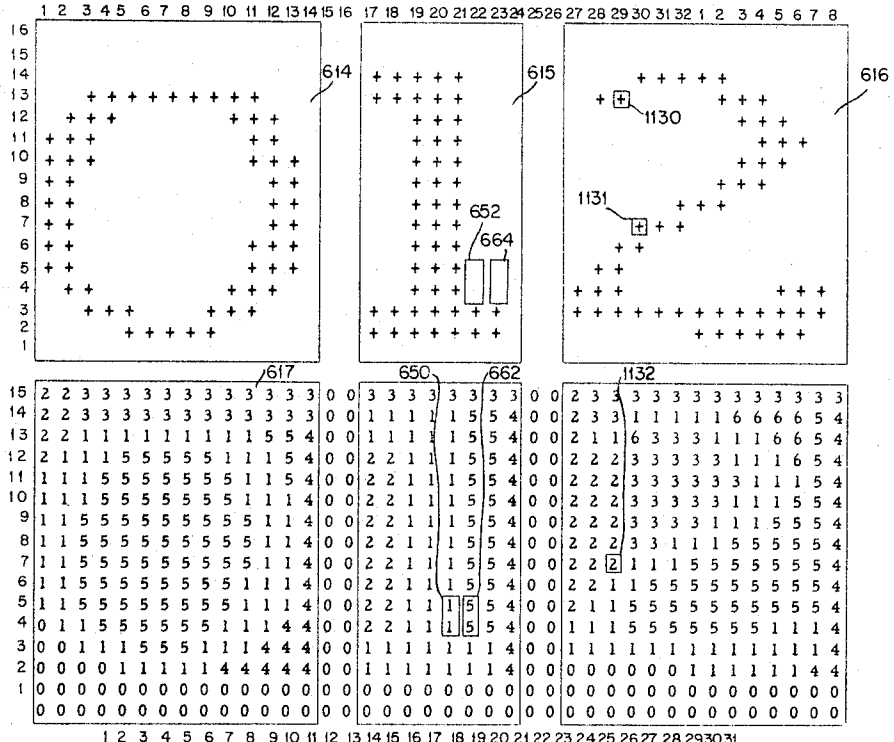

FIG(I,1's)
LETTER(I's)
CONTEXT
MEB
ERROR
MWB OR LBVL
D-EB
SEB
NWB OR MWB
T-SWB
LBVL
LEB
D-WB
TRIANGLE SHORE
SWB OR LWB
MEB OR LEB
FIG 0
LETTER O
94

FIG. 10B

FIG. 11


A
ML
SB
B
LBVL
UL
LL
C
D-EB
D
LBVL
42
ML
D
46
44
MWB
ML
46
E
UEB
LEB
F
MEB
48
SEB
F
56
UEB
50
54
SEB
52
G
UEB
PLL
H
NB
RECTANGLE SHAPED SB
I
LBVL
J
LBVL
MWB
MEB
NWB
NB
J
MWB
SEB
K
NB
DEB
SB
L
NEB
M
NB
SB
SB
2SB
M
NB
PEN IN SB
N
NB
TRIANGLE SHAPED SB
O
ML
P
ML
SEB
P
UL
40
SEB
Q
UL
LEB
SB
64
Q
UL
PLL
64
Q
ML
MEB
64
Q
UL
LL:UL
LL
64
R
LBVL
UL
LEB
SB
S
UEB
T
SWB
SEB
T
SB
SEB
U
NB
V
NB
SWB
W
2 NB
NB
NB
W
PEN IN
NB
SB
X
NB
D-WB
D-EB
SB
X
960
958
DWB
NB
UWB
UEB
SB
Y
NB
T-SWB
Z
LEB
1
LBVL
MWB
2
LEB
3
62
UWB
3
60
UWB
UEB
4
NEB
ML
4
UL
NEB
4
NB
NEB
SWB
5
UEB
6
UEB
LL
7
SWB
SEB
7
LBVL
SWB
7
SB
SEB
7
LBVL
SB
8
UL
LL
9
UL
LWB
9
ML
SWB
0
ML

FIG. 12


614
615
616
652
664
1130
1131
617
650
662
1132

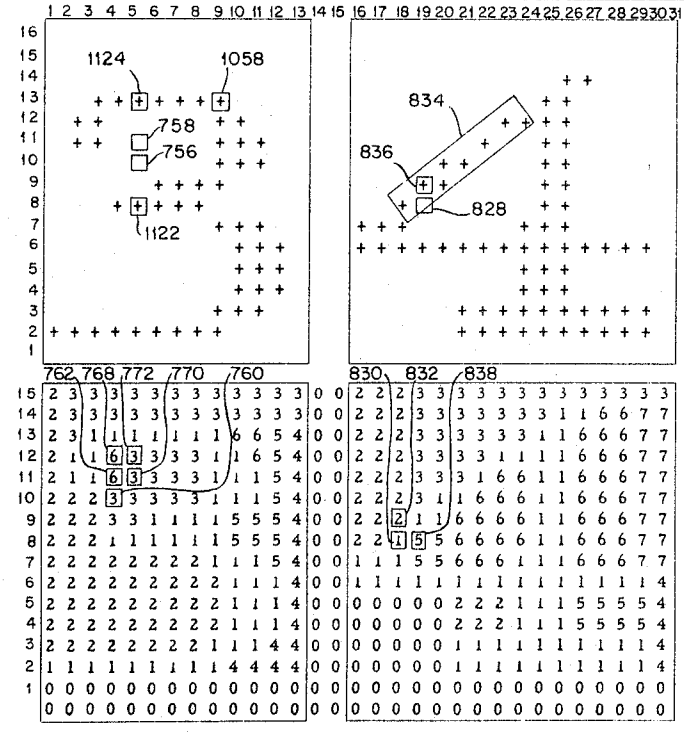

1124
1058
758
756
1122
834
836
828
762
768
772
770
760
830
832
838

FIG. 13

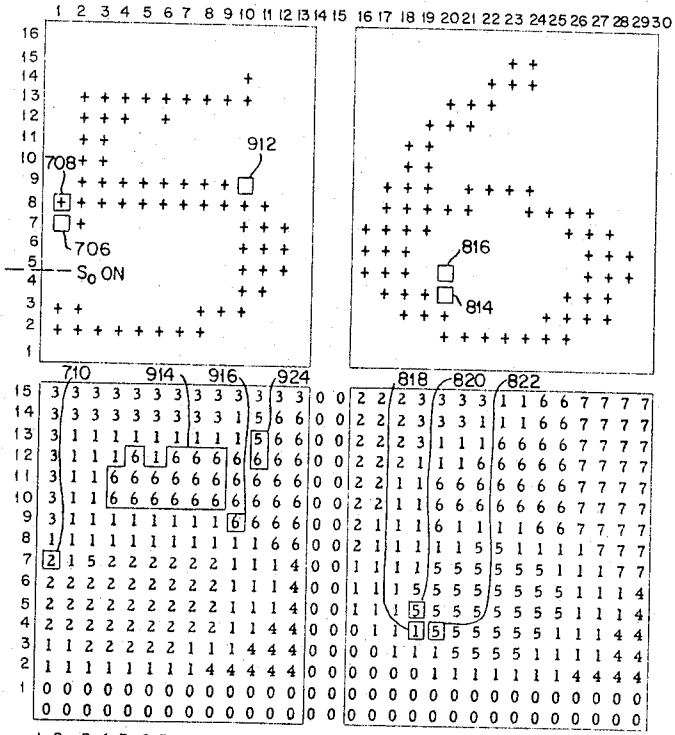


FIG.14

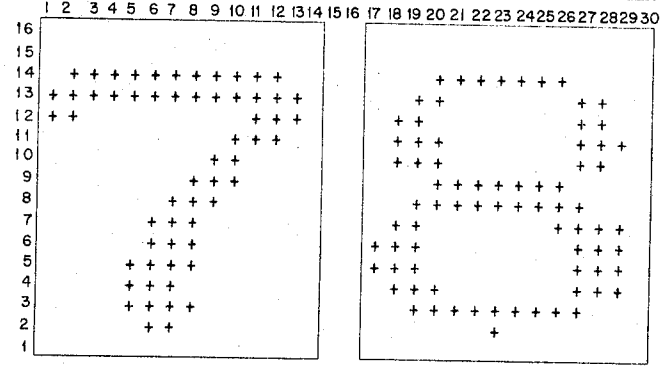
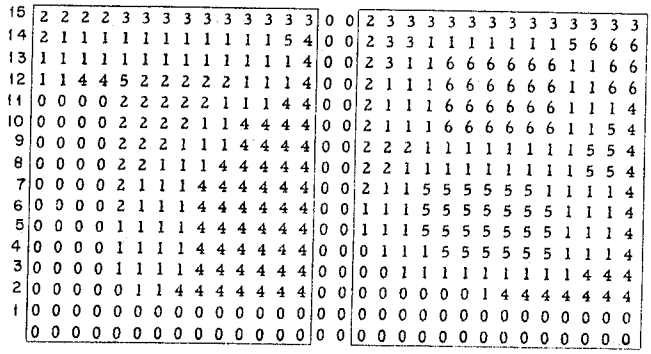


FIG.15



Sept. 6, 1966 KUANG-CHI HU 3,271,761

CURVATURE AND SHAPE DETECTION

Filed Nov. 29, 1963

69 Sheets-Sheet 37

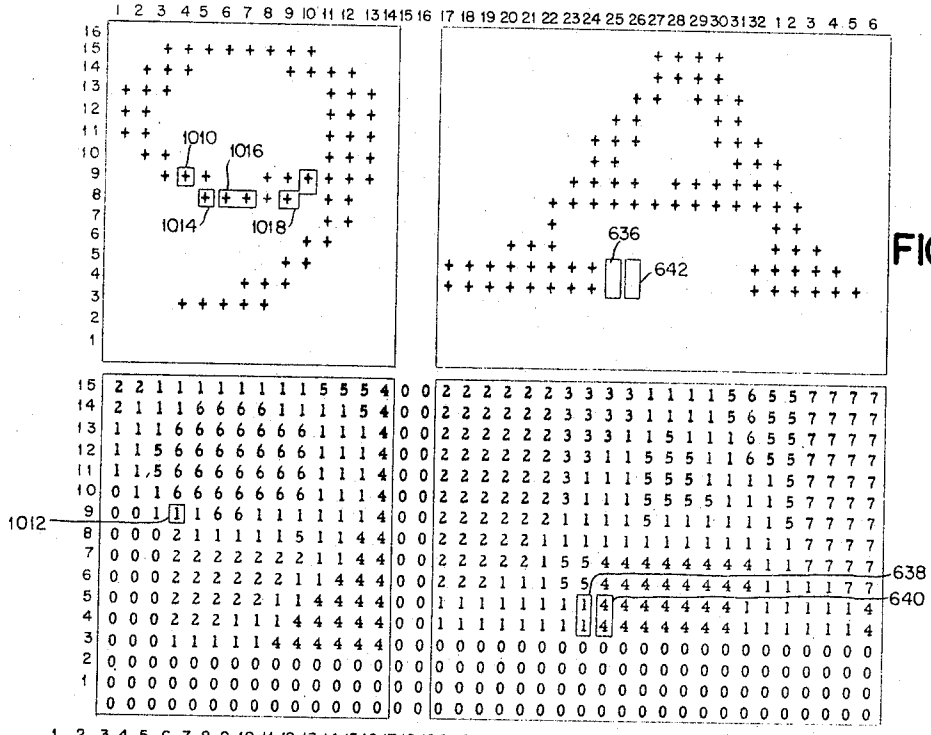


FIG.16

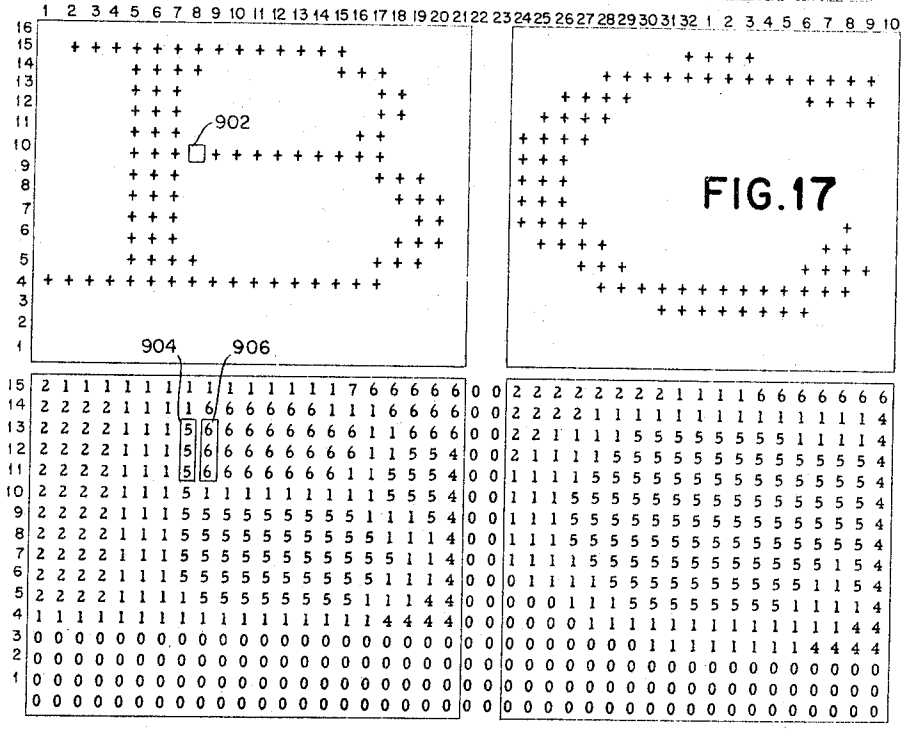
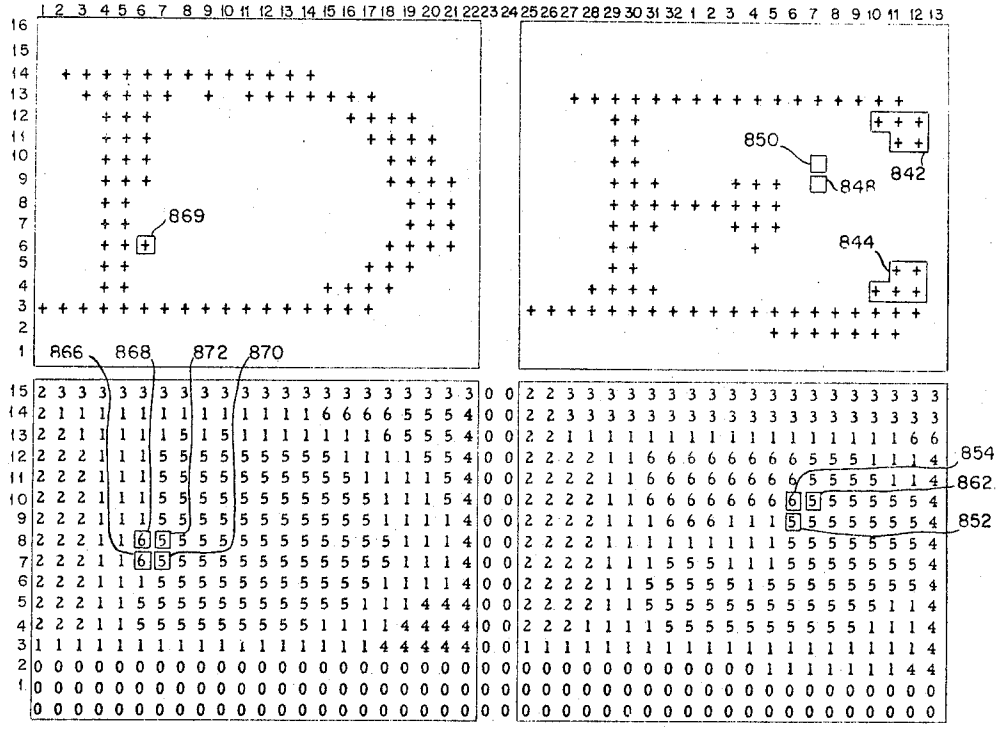


FIG.17

FIG. 18


866
868
872
870
869
850
848
842
844
854
862
852

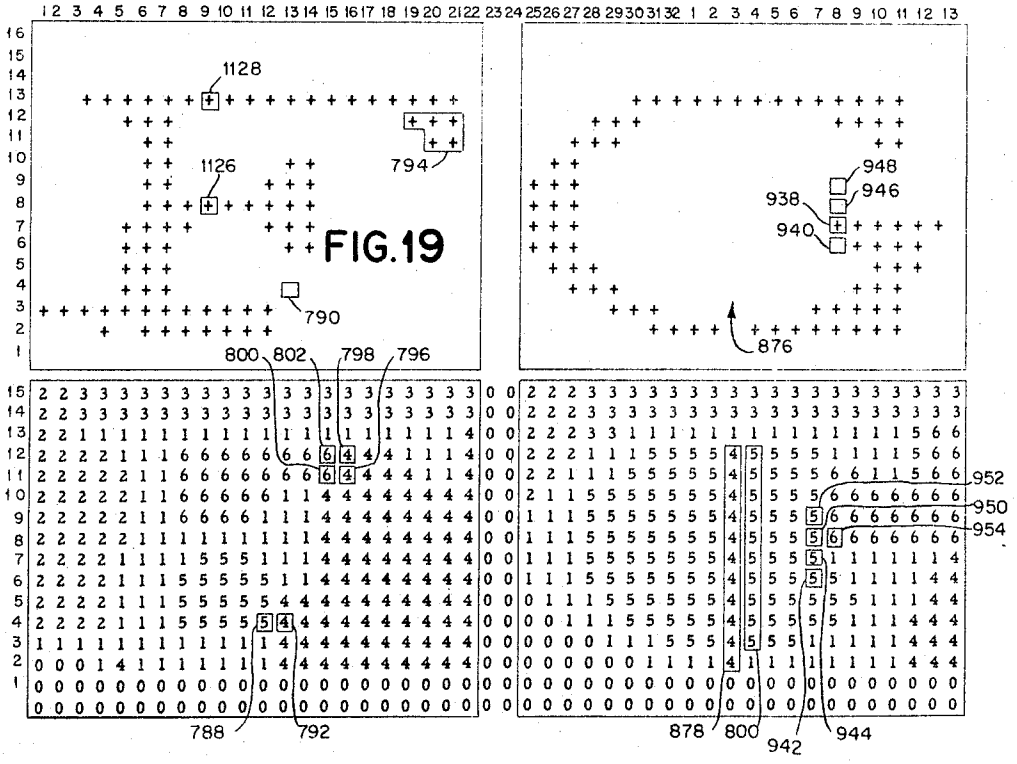

1128
1126
794
790
800
802
798
796
788
792
948
946
938
940
876
878
942
944
952
950
954

FIG. 19

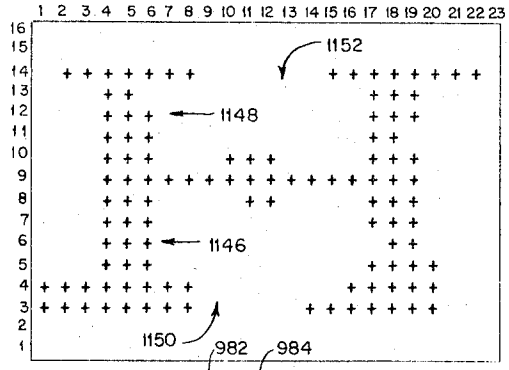
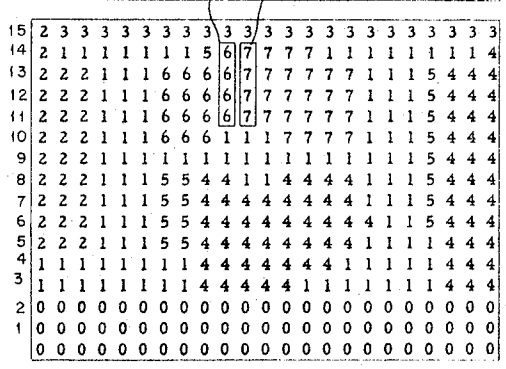


FIG. 20



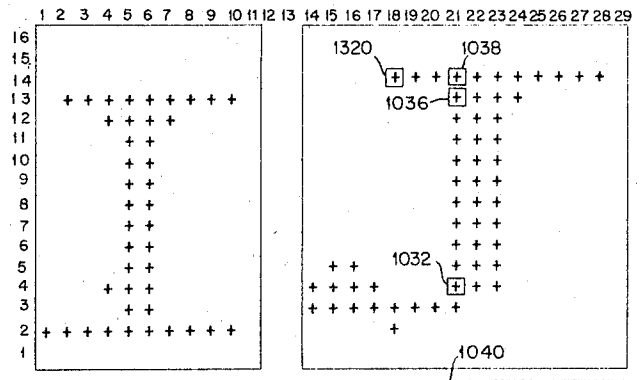
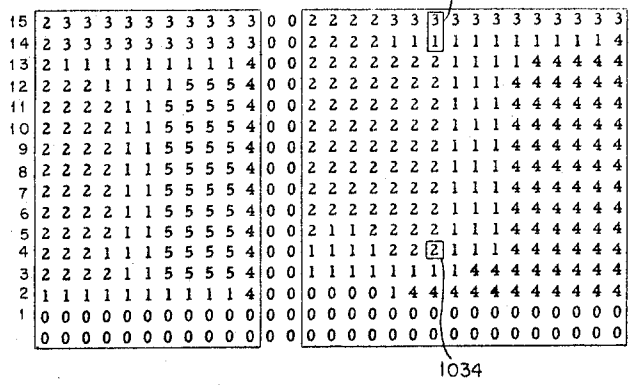


FIG. 21



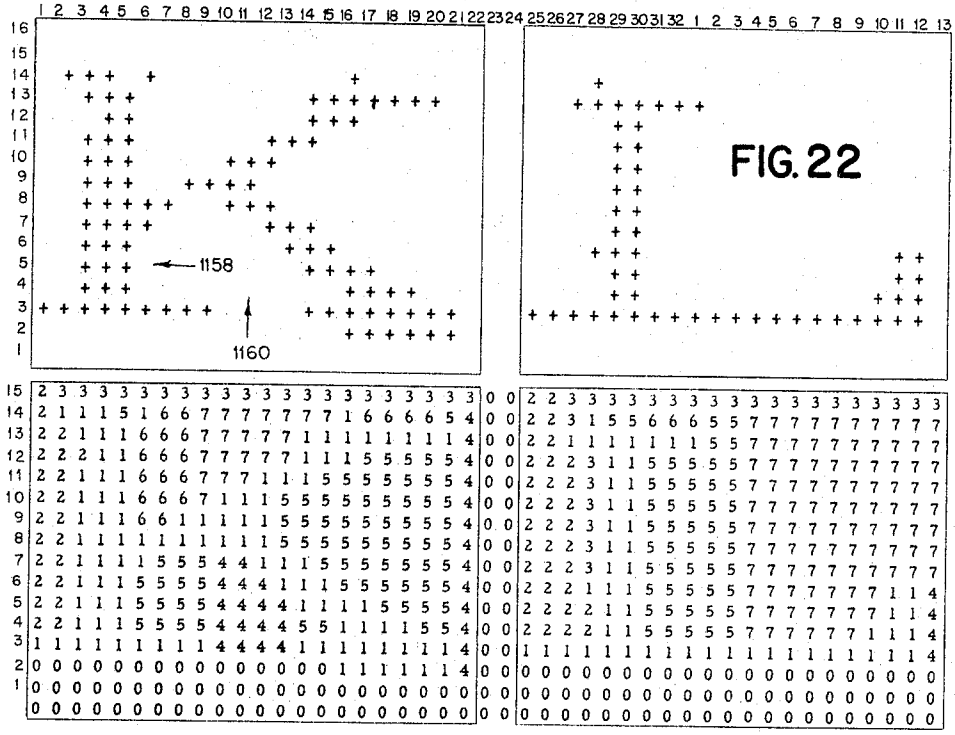

1158
1160

FIG. 22

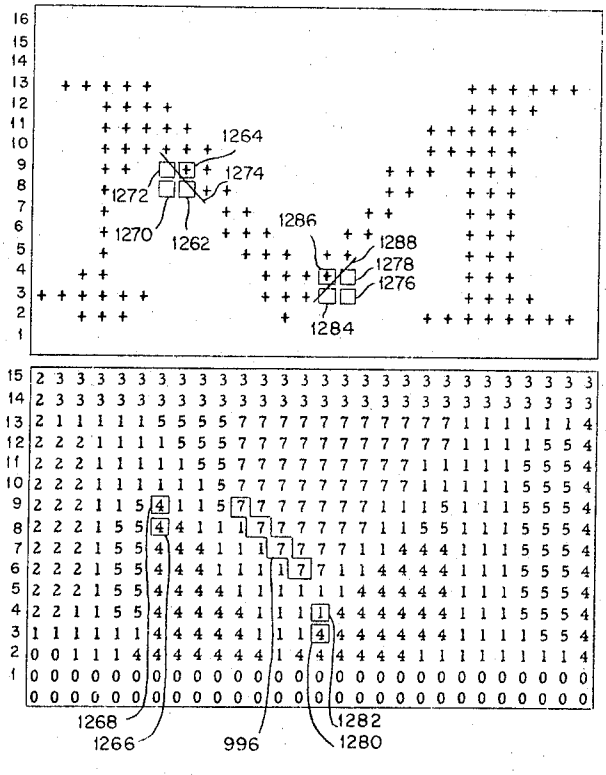
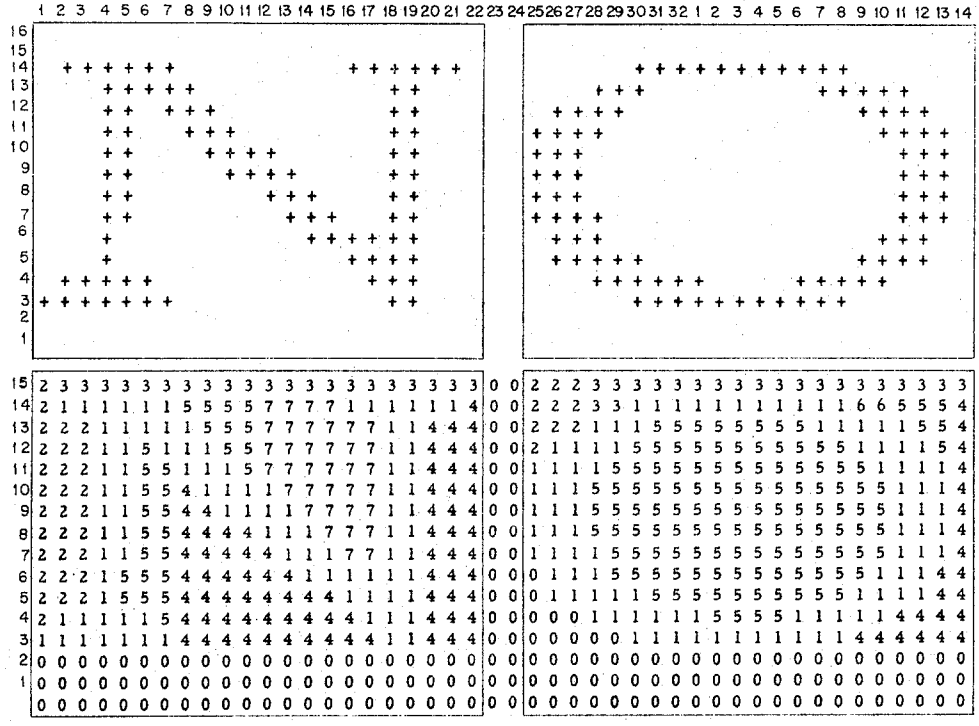

1264
1274
1272
1270
1262
1286
1288
1278
1276
1284
1268
1266
996
1282
1280

FIG. 23

FIG. 24



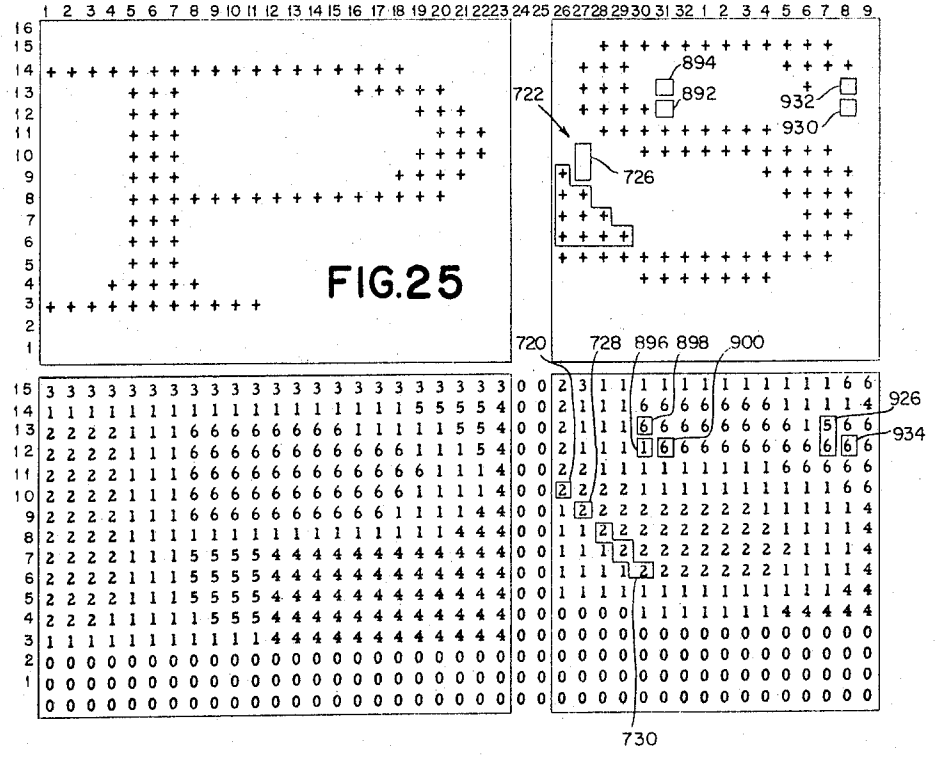


FIG. 25

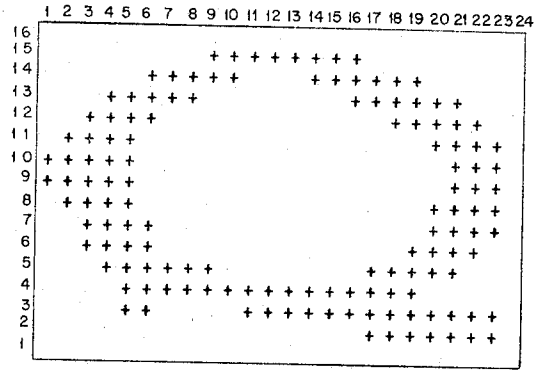


FIG. 26

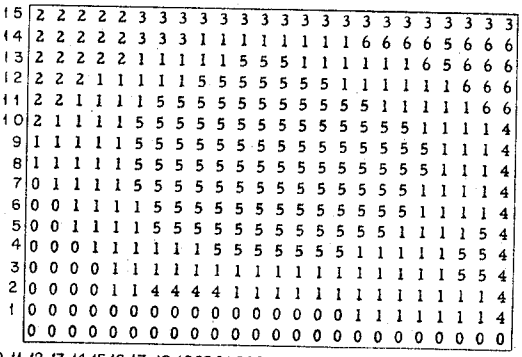


FIG. 27

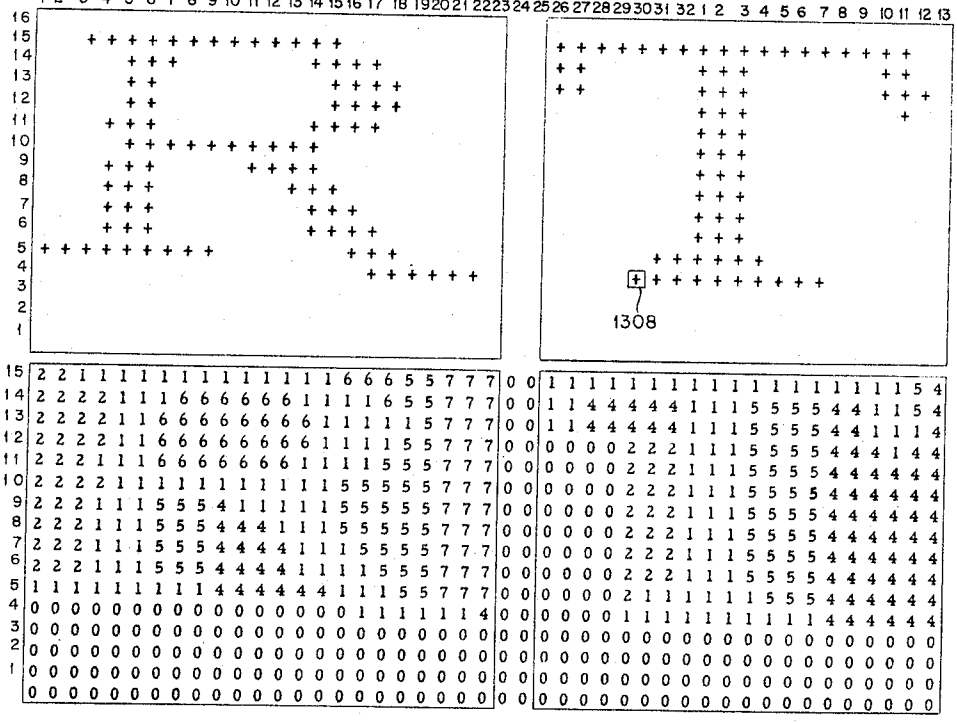
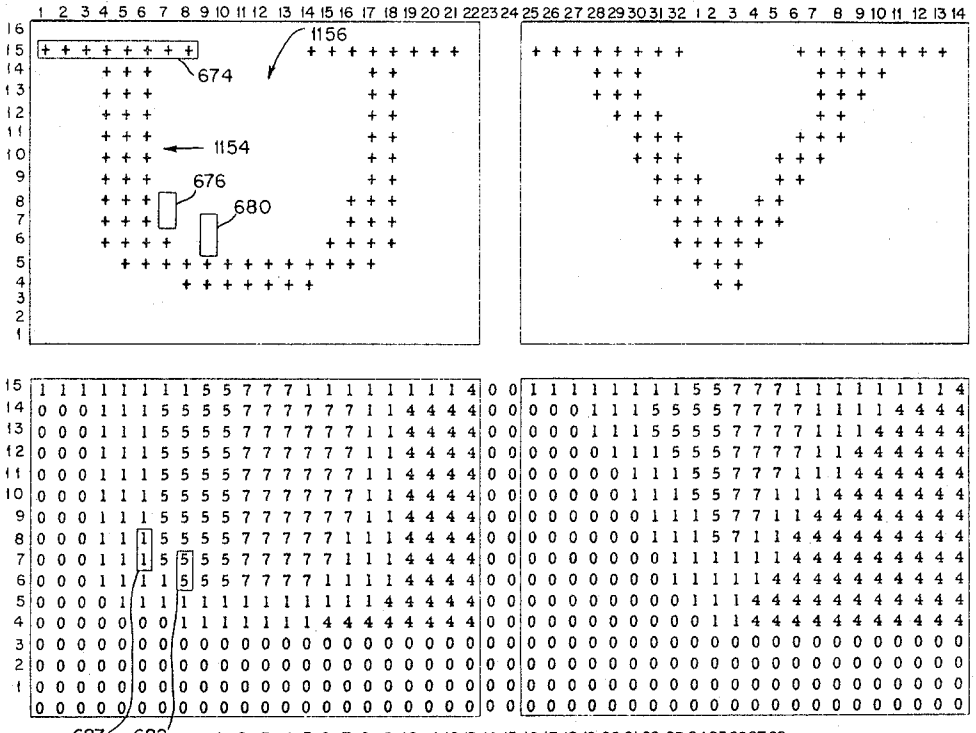


FIG.28


1156
674
1154
676
680
687
682

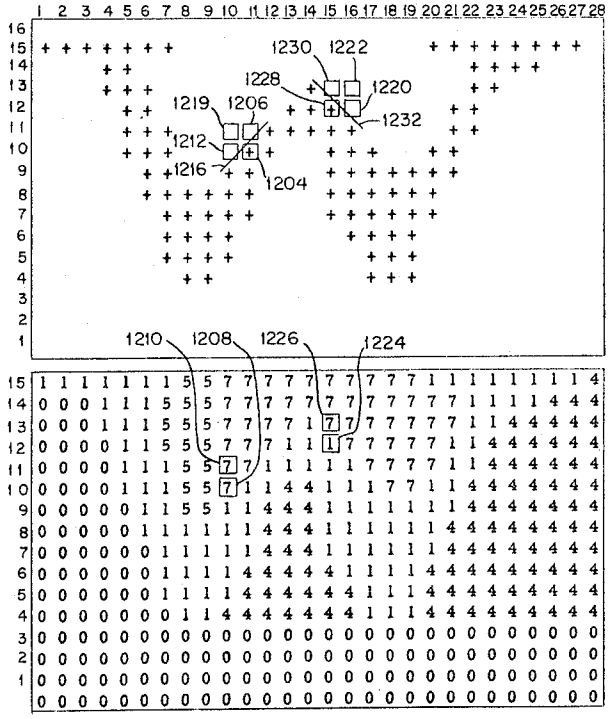

1230
1222
1228
1220
1219
1206
1232
1212
1216
1204
1210
1208
1226
1224

FIG.29

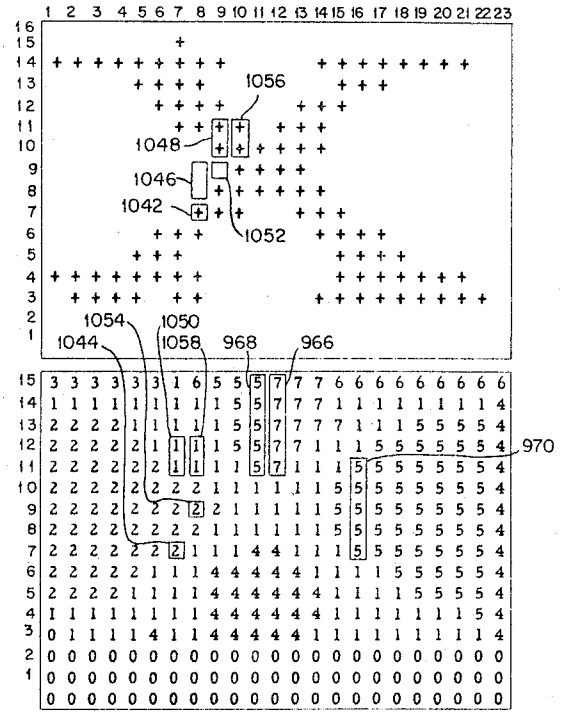

1056
1048
1046
1042
1052
1054
1050
1044
1058
968
966
970

FIG. 30

FIG. 31

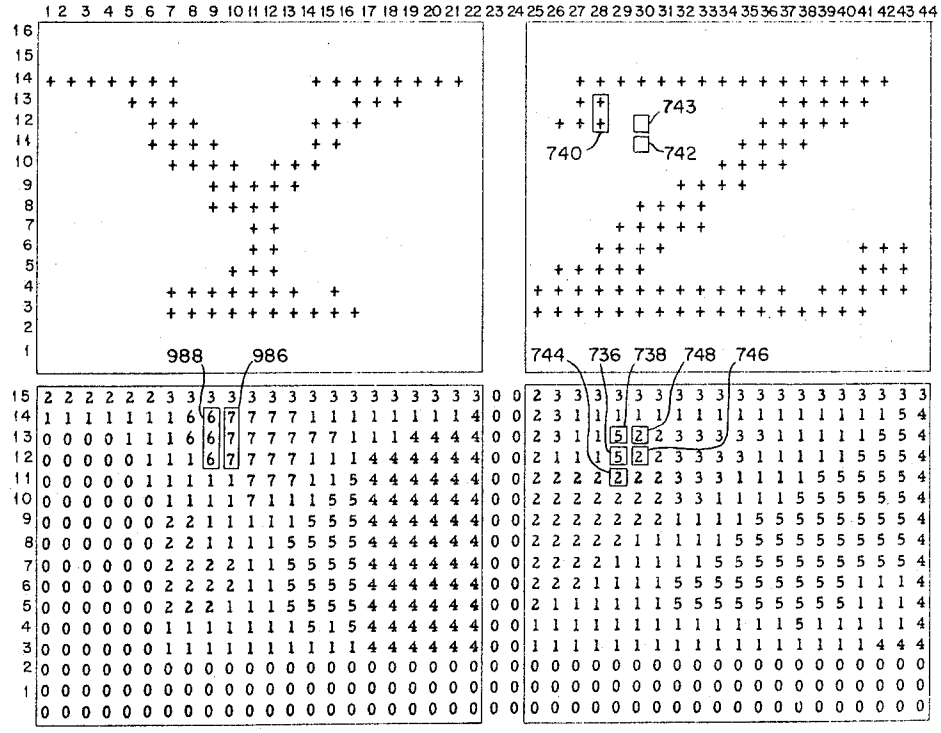

743
740
742
988
986
744
736
738
748
746

FIG. 32

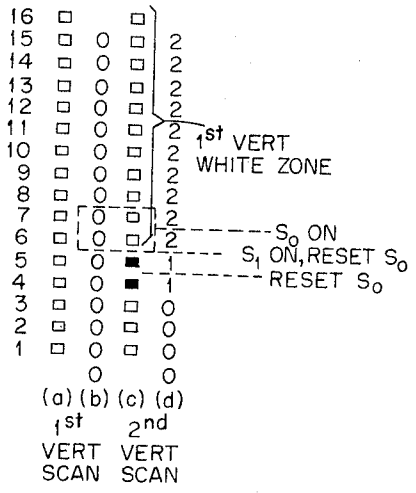


FIG. 33

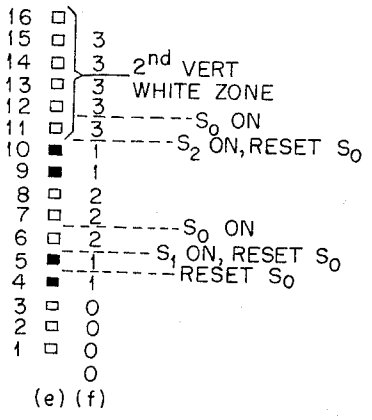


FIG. 34

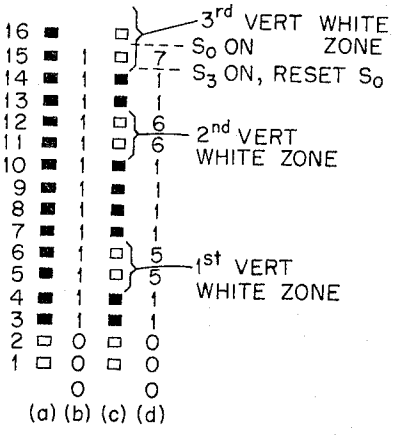


FIG. 35

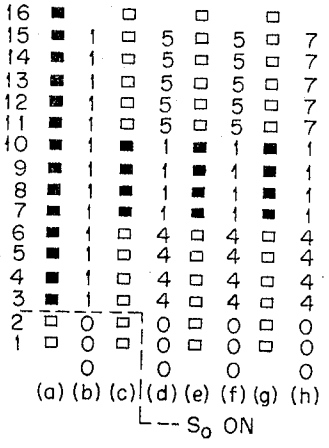


FIG. 36

FIG. 37A	FIG. 37B	FIG. 37C	FIG. 37D	FIG. 37E	FIG. 37F	FIG. 37G	FIG. 37H	FIG. 37I

FIG.37A

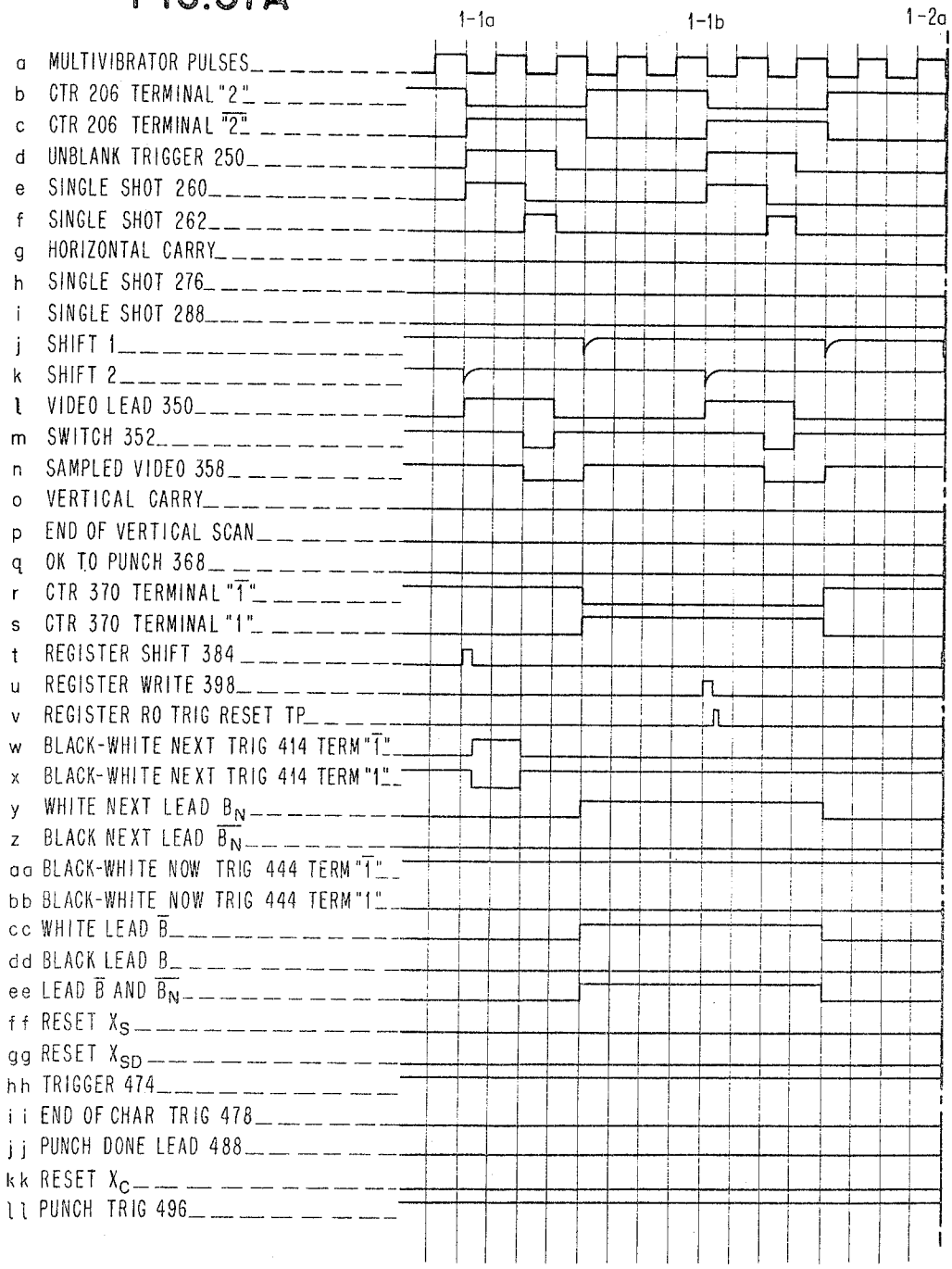

1-1a
1-1b
1-2a
a MULTIVIBRATOR PULSES
b CTR 206 TERMINAL "2"
c CTR 206 TERMINAL "$\overline{2}$"
d UNBLANK TRIGGER 250
e SINGLE SHOT 260
f SINGLE SHOT 262
g HORIZONTAL CARRY
h SINGLE SHOT 276
i SINGLE SHOT 288
j SHIFT 1
k SHIFT 2
l VIDEO LEAD 350
m SWITCH 352
n SAMPLED VIDEO 358
o VERTICAL CARRY
p END OF VERTICAL SCAN
q OK TO PUNCH 368
r CTR 370 TERMINAL "$\overline{1}$"
s CTR 370 TERMINAL "1"
t REGISTER SHIFT 384
u REGISTER WRITE 398
v REGISTER RO TRIG RESET TP
w BLACK-WHITE NEXT TRIG 414 TERM "$\overline{1}$"
x BLACK-WHITE NEXT TRIG 414 TERM "1"
y WHITE NEXT LEAD B_N
z BLACK NEXT LEAD $\overline{B_N}$
aa BLACK-WHITE NOW TRIG 444 TERM "$\overline{1}$"
bb BLACK-WHITE NOW TRIG 444 TERM "1"
cc WHITE LEAD $\overline{B}$
dd BLACK LEAD B
ee LEAD $\overline{B}$ AND $\overline{B_N}$
ff RESET X_S
gg RESET X_{SD}
hh TRIGGER 474
ii END OF CHAR TRIG 478
jj PUNCH DONE LEAD 488
kk RESET X_C
ll PUNCH TRIG 496

FIG. 37B

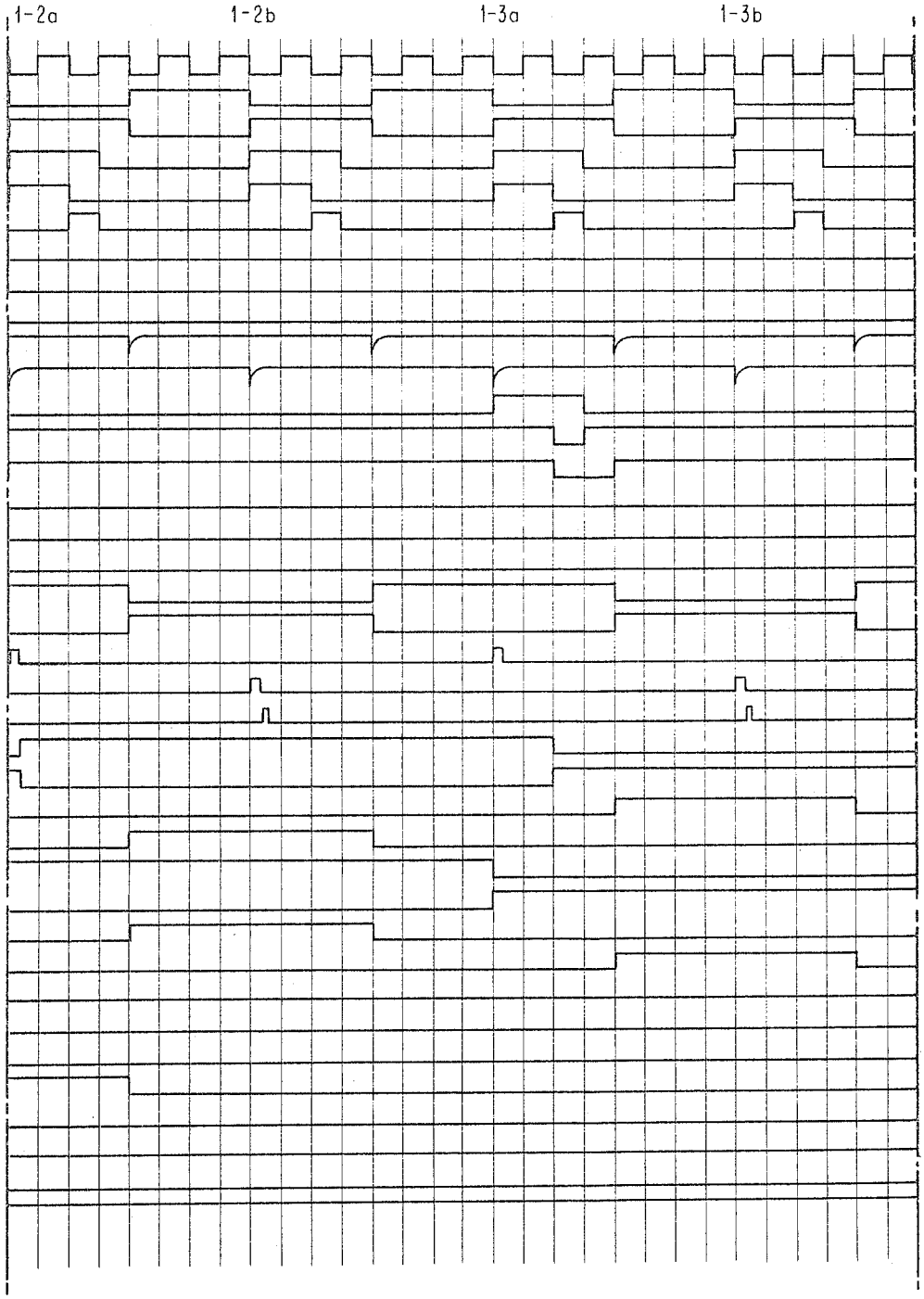


FIG.37C

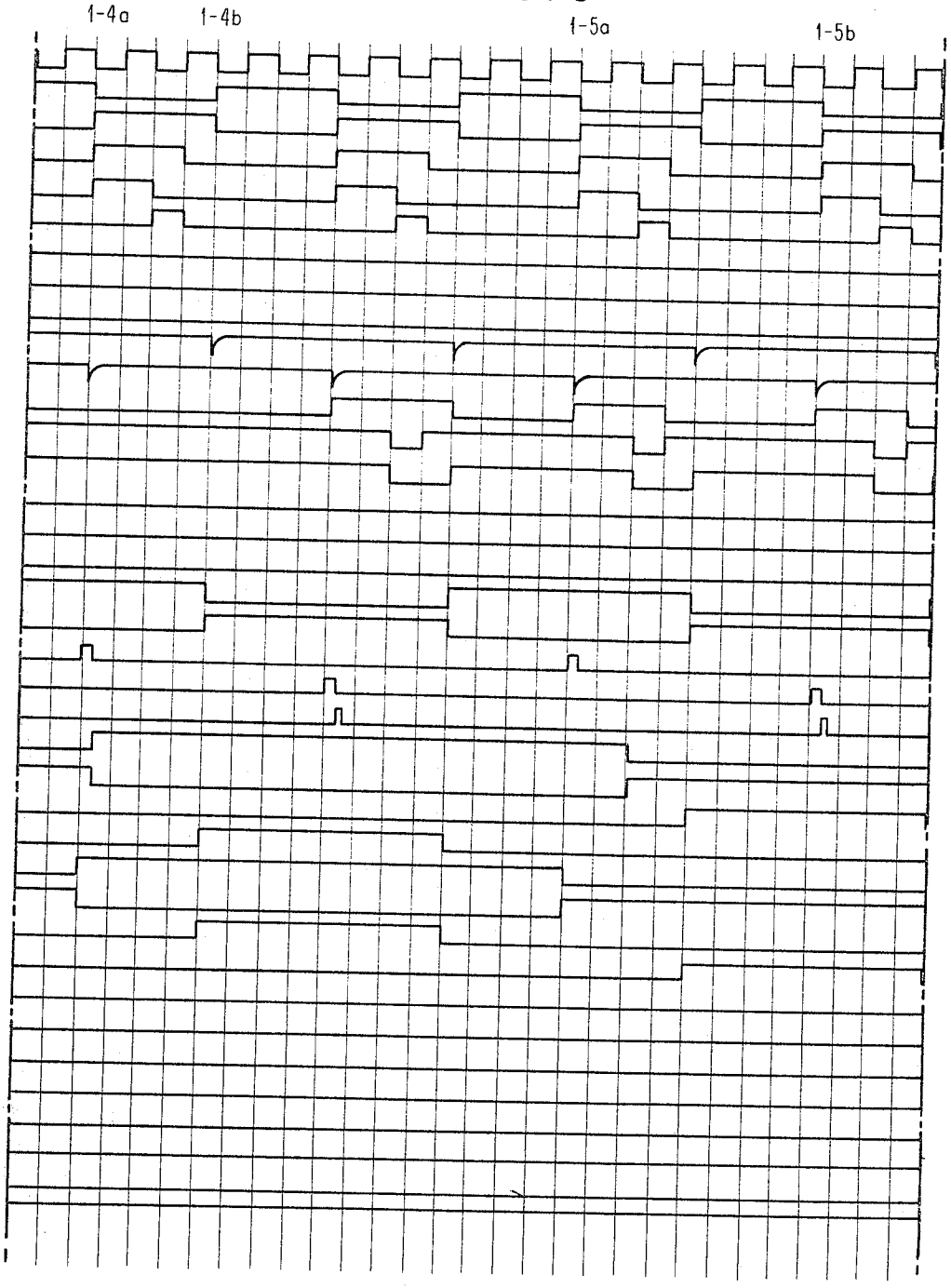


FIG.37D

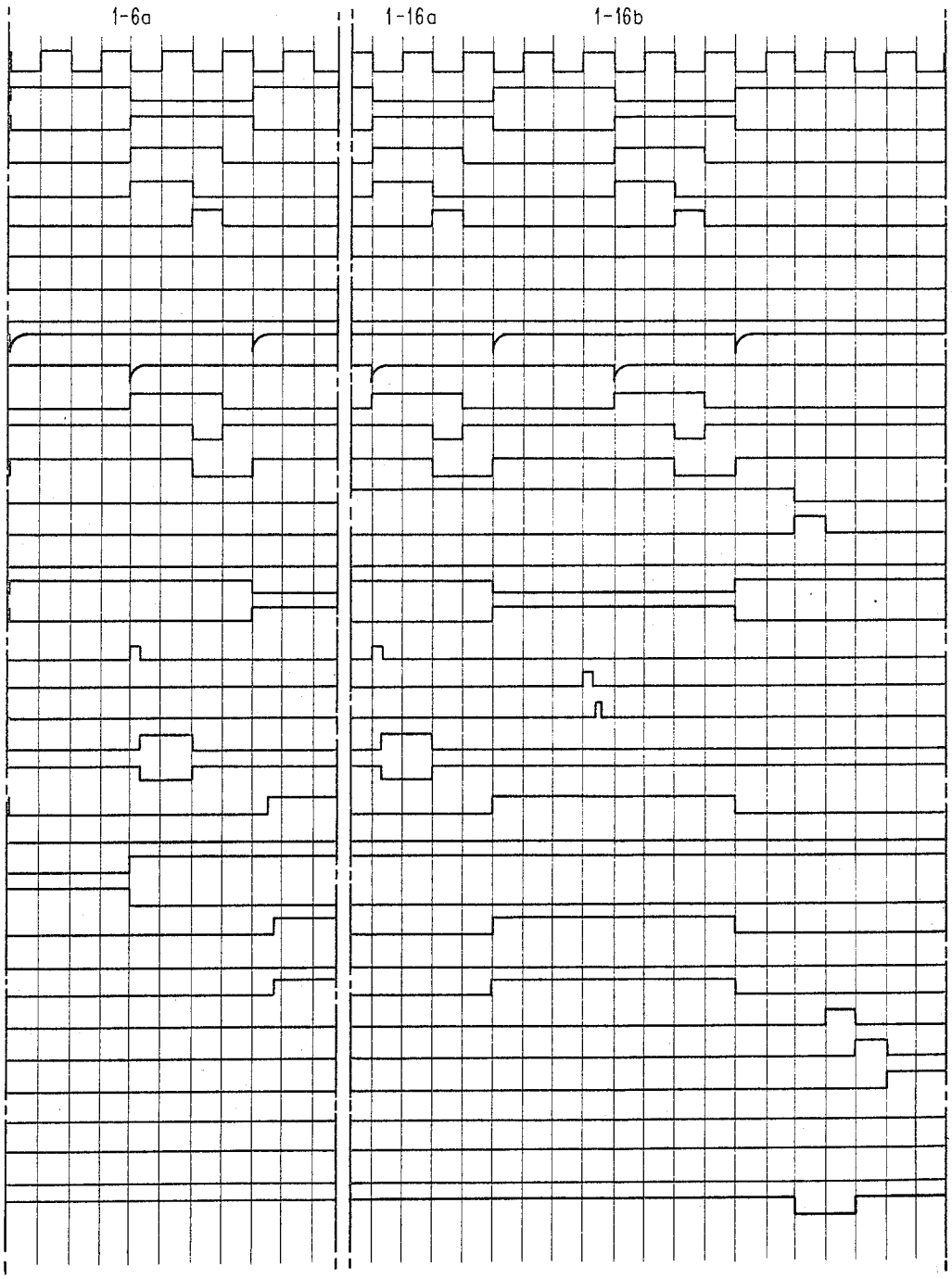


FIG.37E

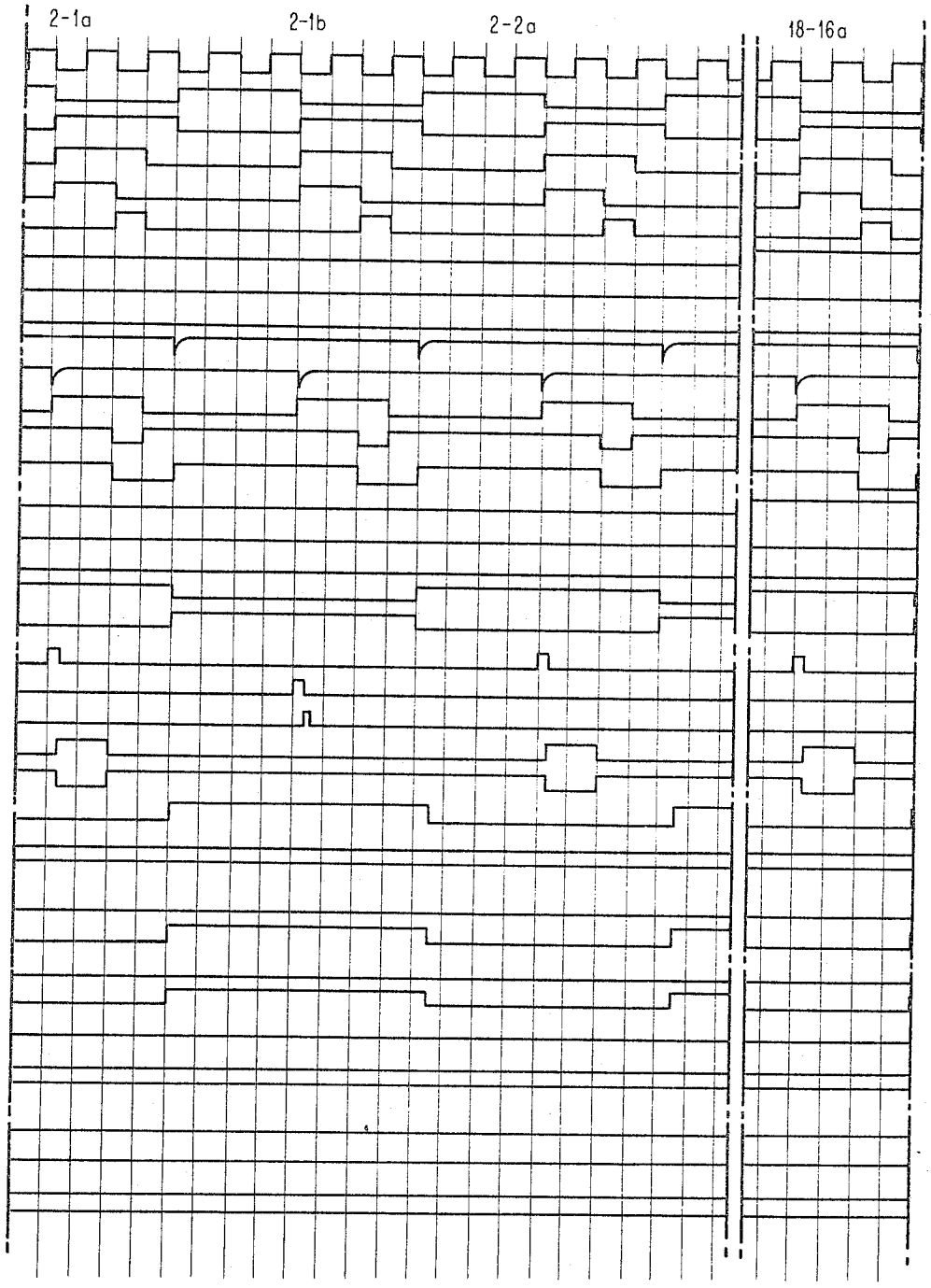


FIG.37F

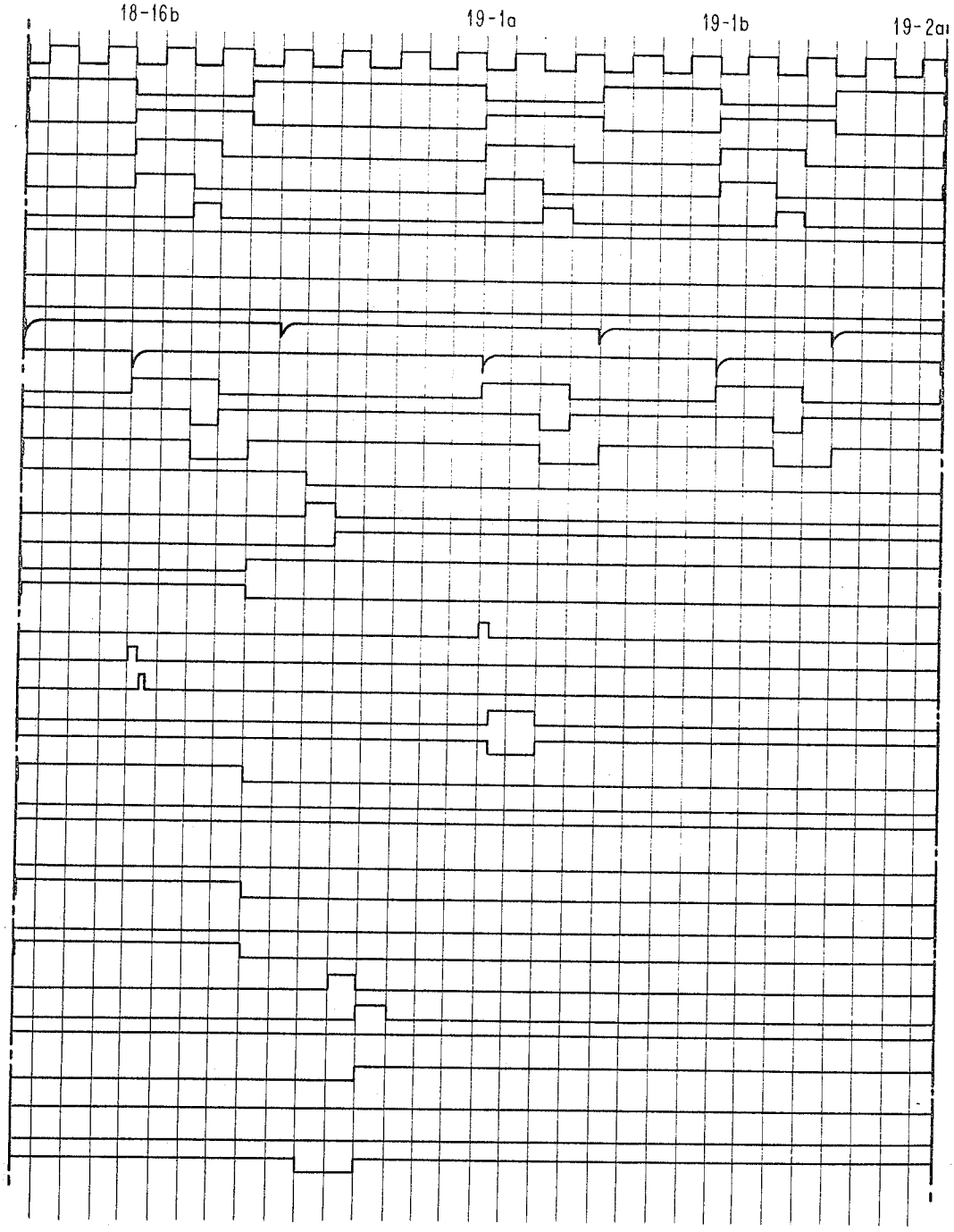


FIG.37G

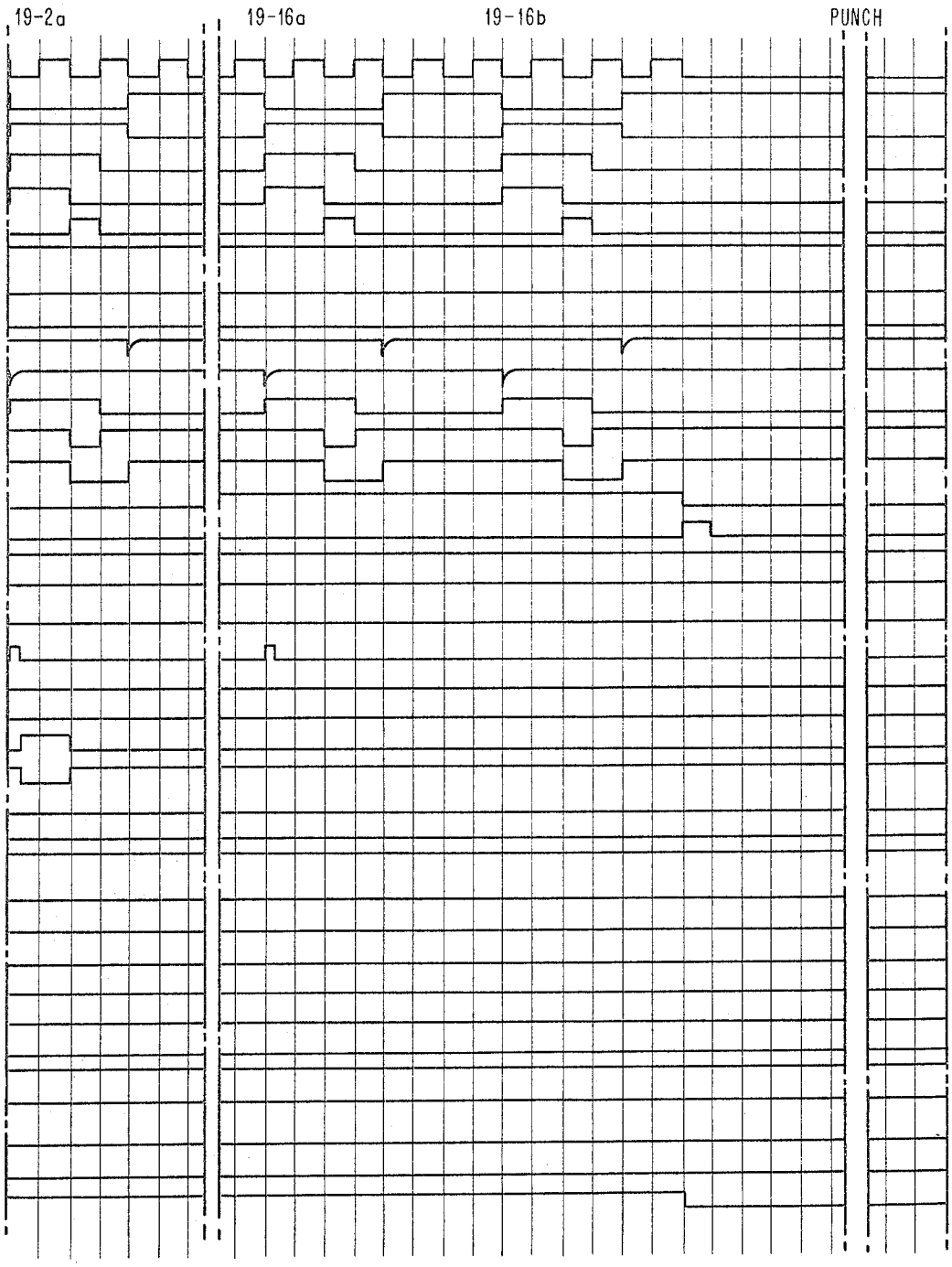


FIG.37H

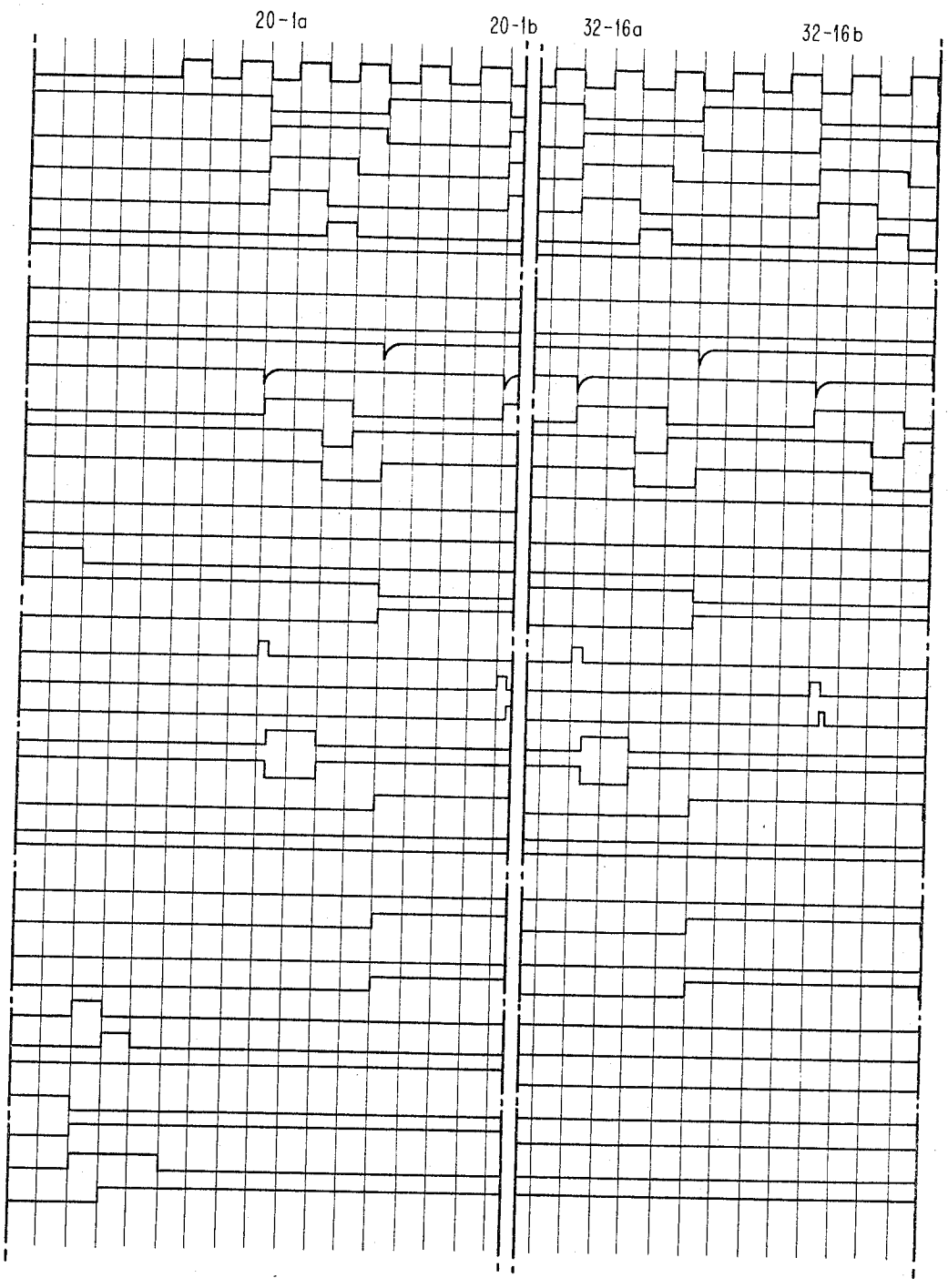
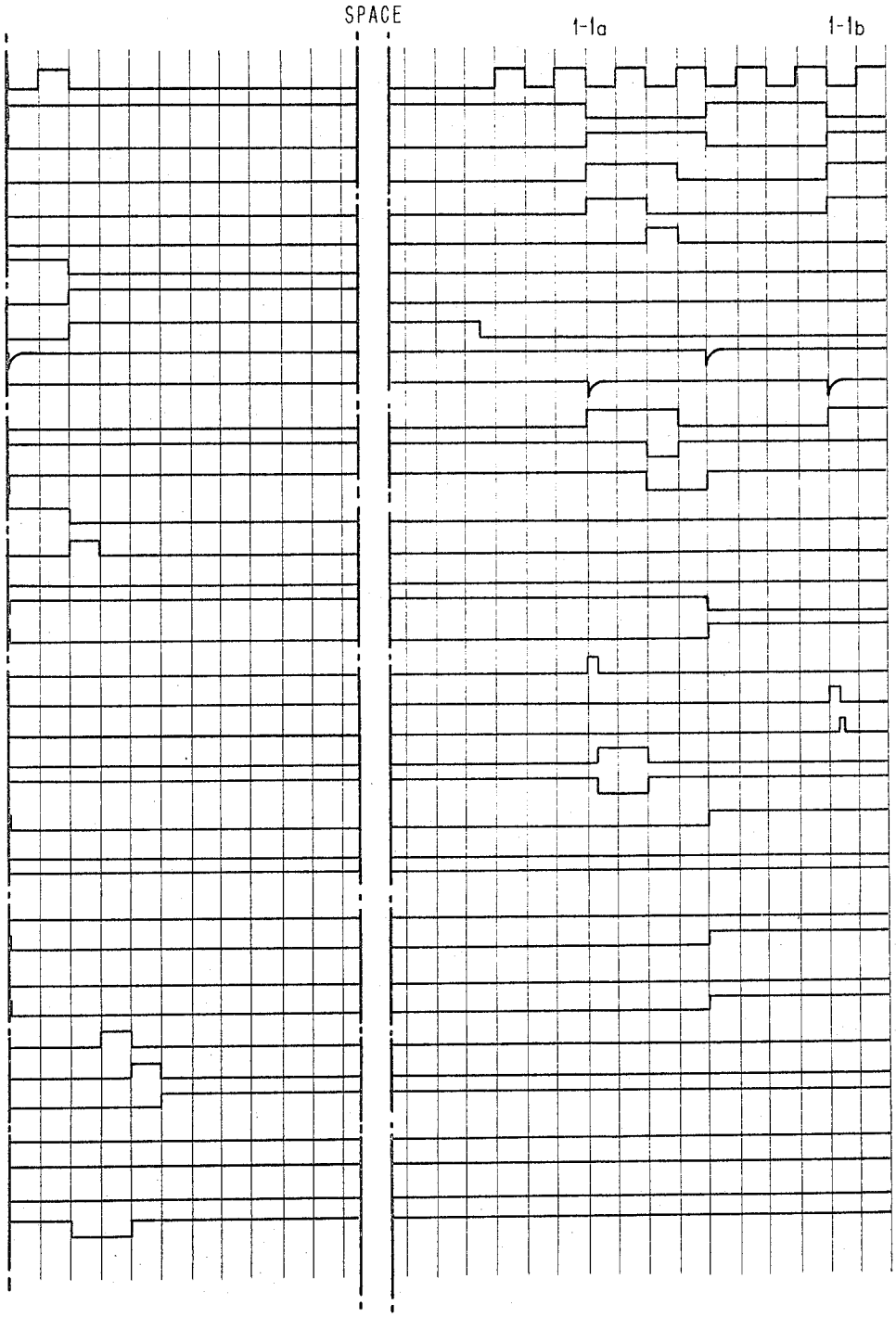


FIG.37I



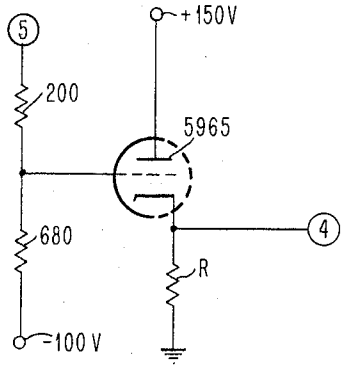
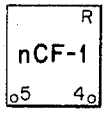


FIG. 38



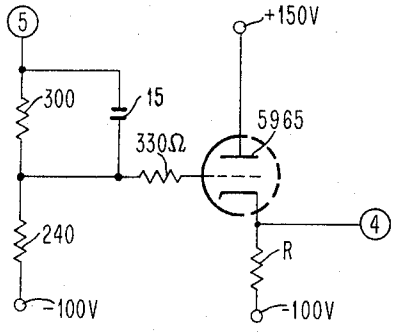
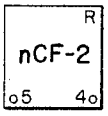


FIG. 39



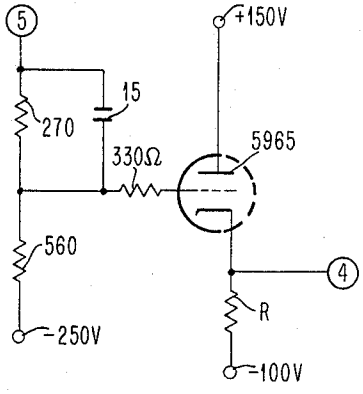


FIG. 40

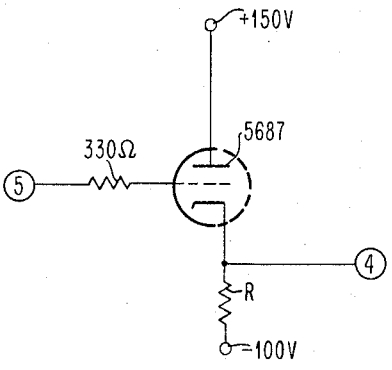
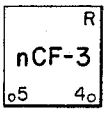
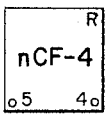


FIG. 41





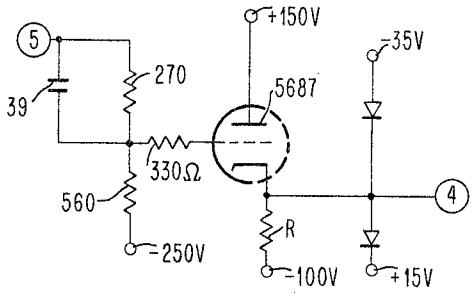
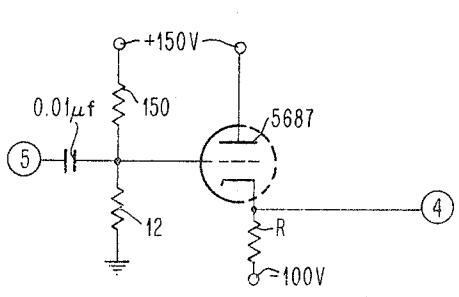


FIG. 42



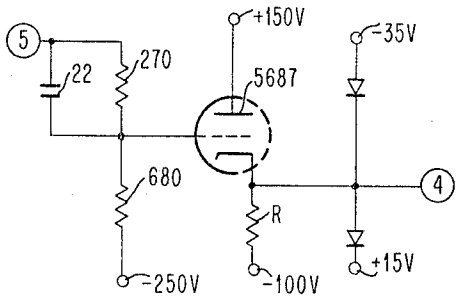


FIG. 43

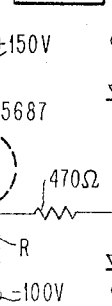


FIG. 44

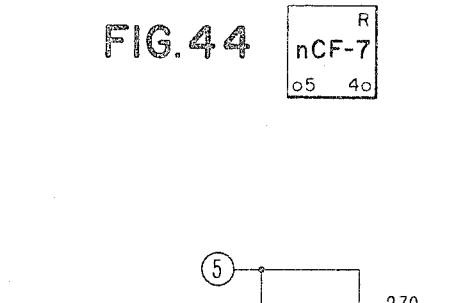


FIG. 45



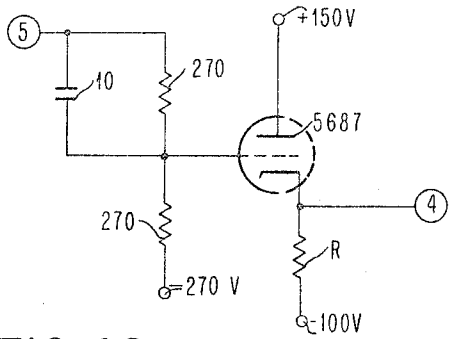


FIG. 46



Sept. 6, 1966 KUANG-CHI HU 3,271,761

CURVATURE AND SHAPE DETECTION

Filed Nov. 29, 1963 69 Sheets-Sheet 57

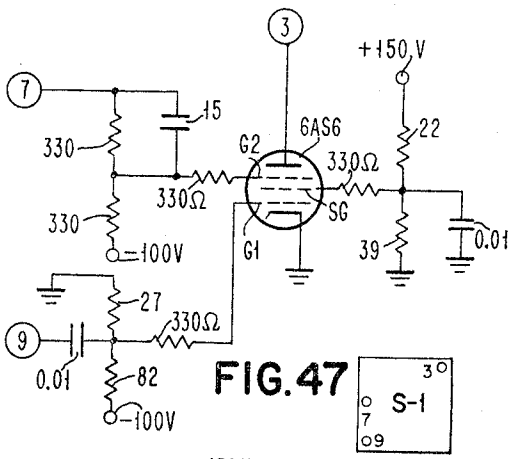
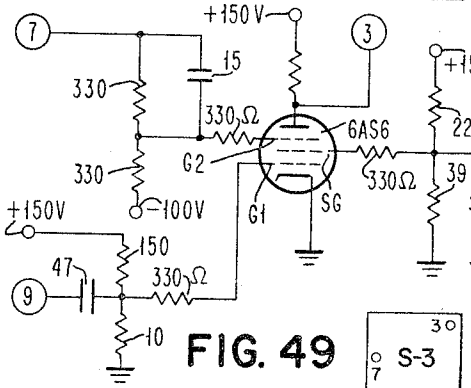


FIG. 47



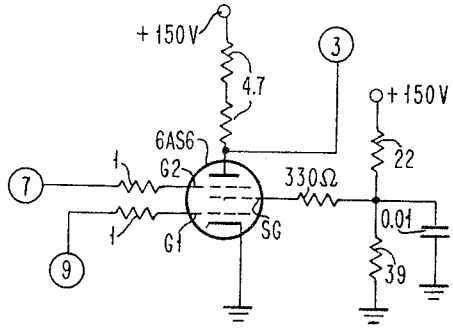


FIG. 48

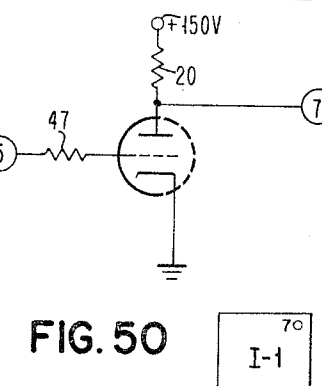


FIG. 49

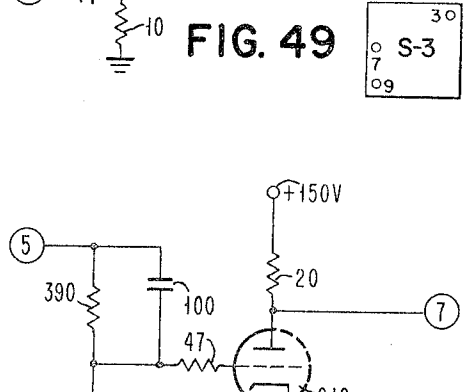


FIG. 50

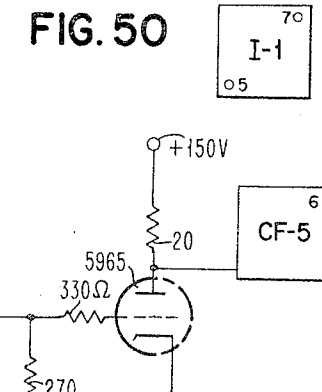


FIG. 51

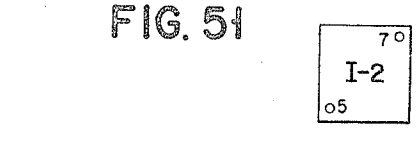
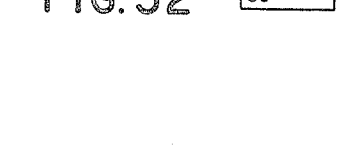


FIG. 52



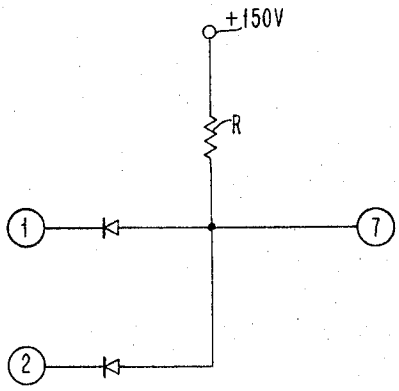
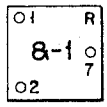


FIG. 53



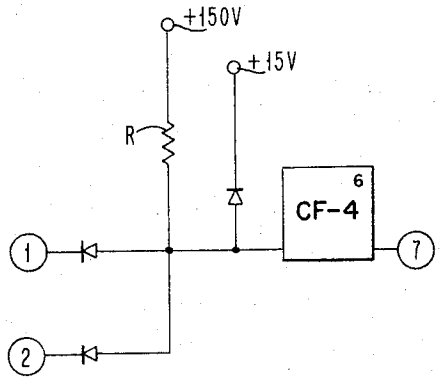
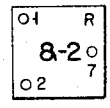


FIG. 54



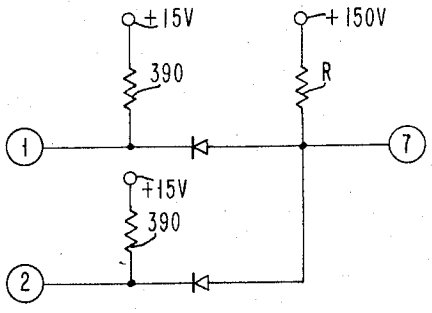
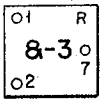


FIG. 55



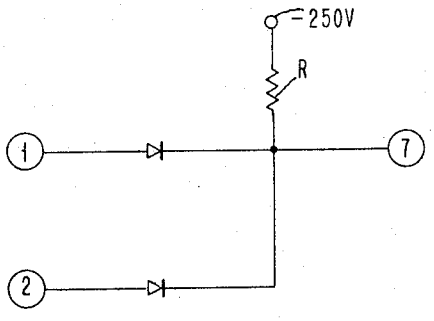
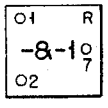


FIG. 56



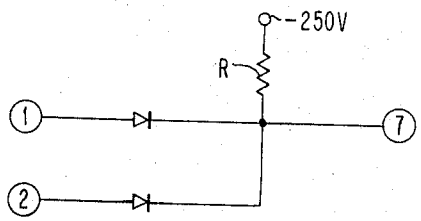
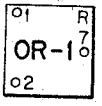


FIG. 57



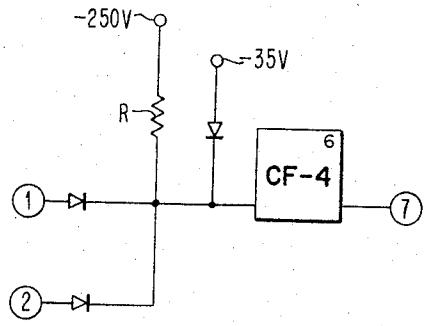


FIG. 58

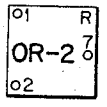
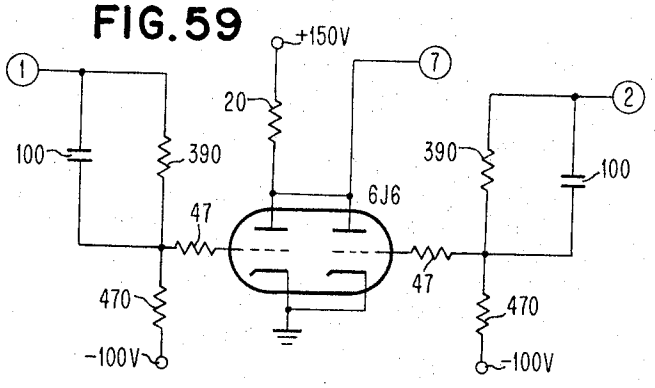


FIG. 59





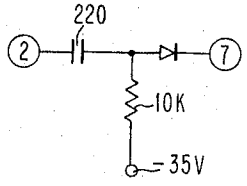
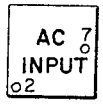


FIG. 60



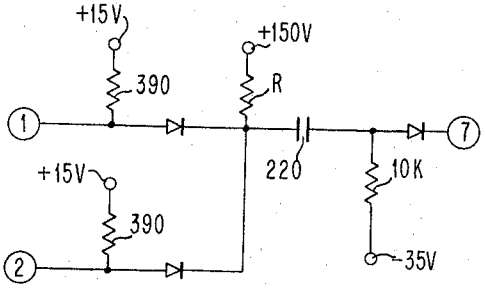


FIG. 61



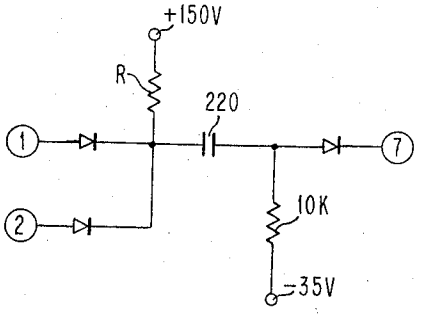


FIG. 62



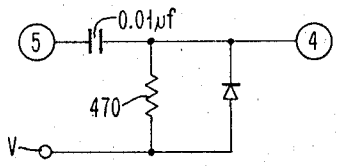
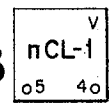


FIG. 63



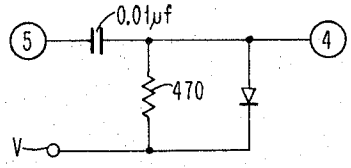


FIG. 64

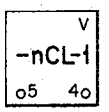


FIG. 65

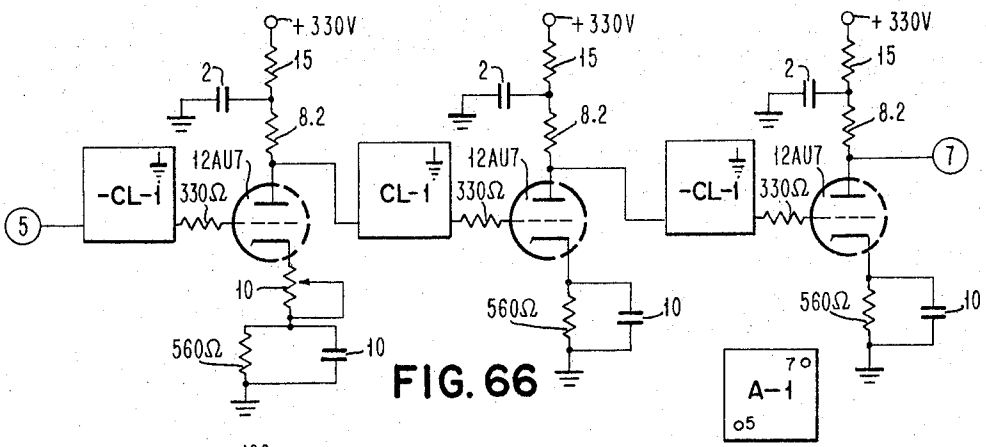


FIG. 66

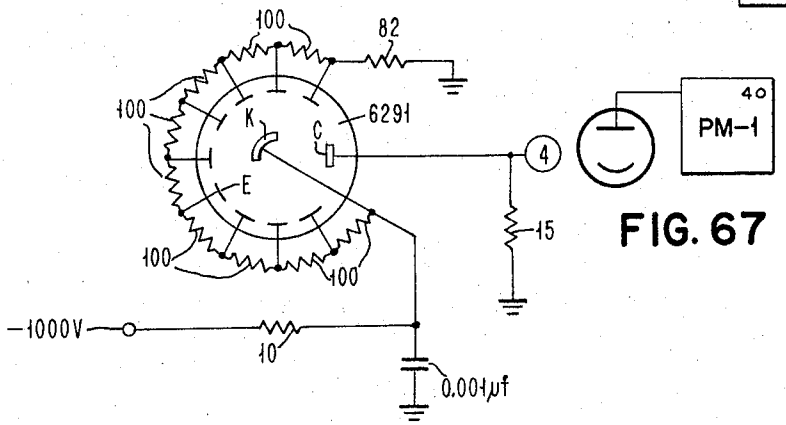


FIG. 67

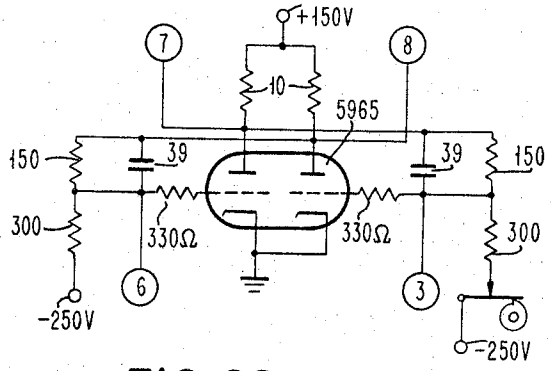


FIG. 68

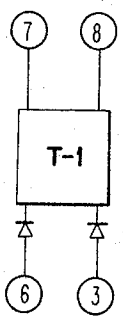


FIG. 69

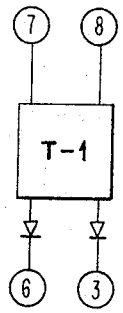
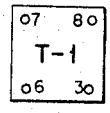
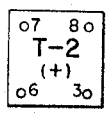
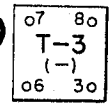


FIG. 70







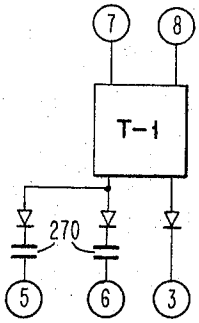


FIG. 71

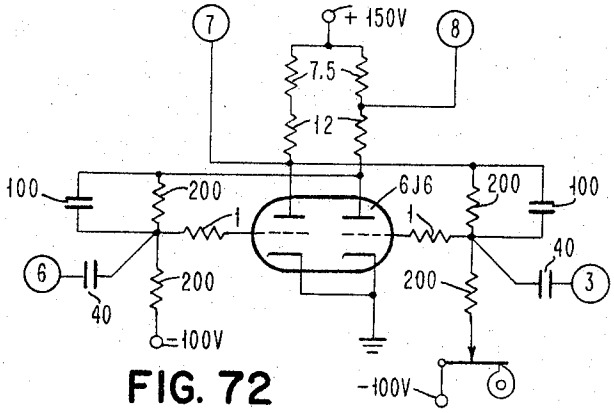
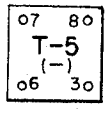


FIG. 72



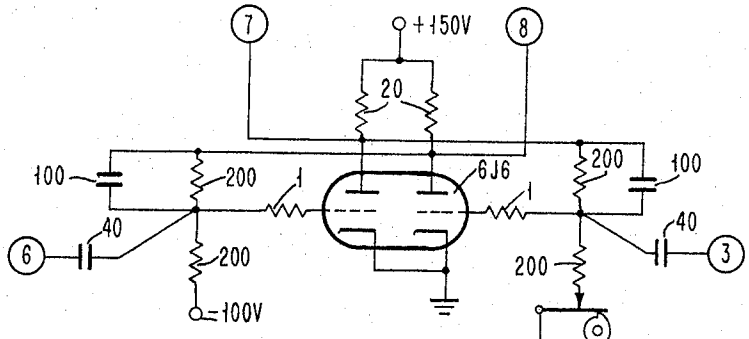


FIG. 73

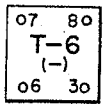


FIG. 74

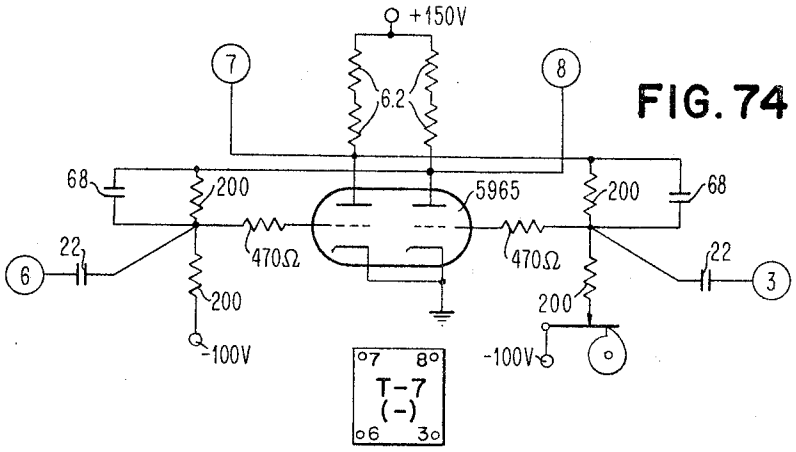
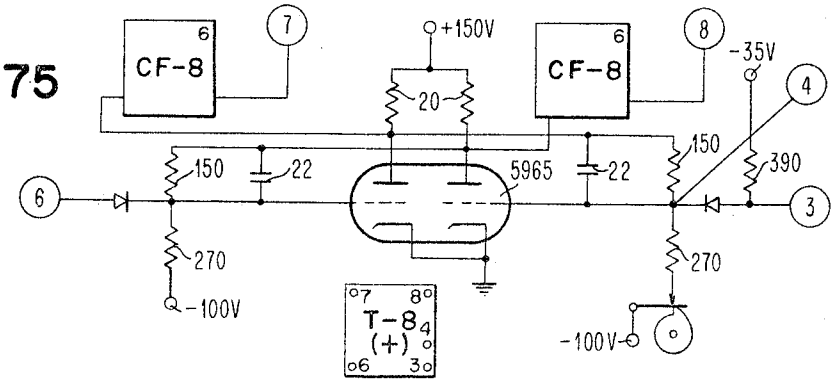


FIG. 75



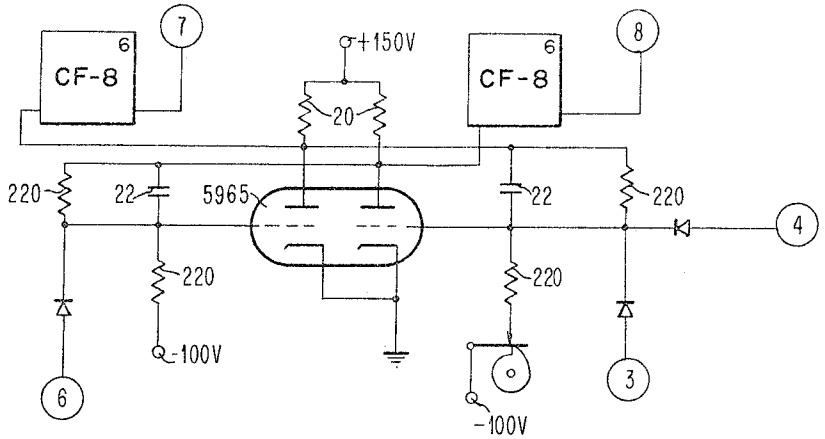
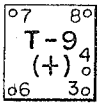


FIG. 76



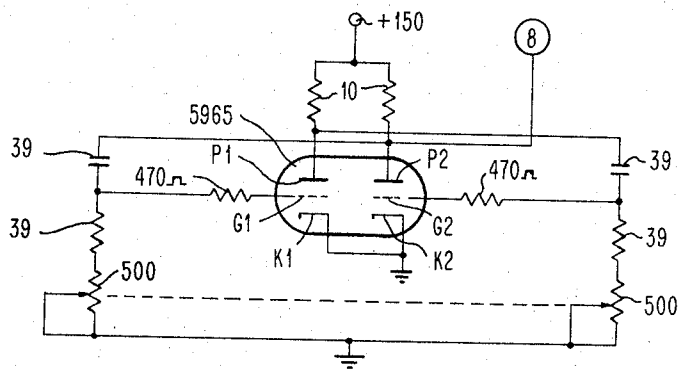


FIG. 77 MV-1

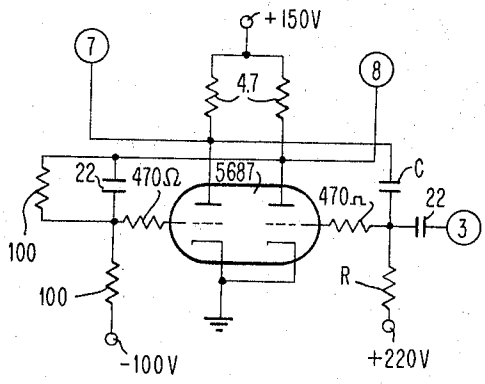


FIG. 78 SS-1

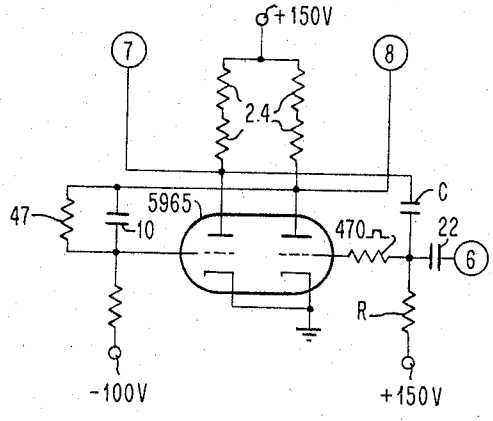


FIG. 79 SS-2

t-μ Sec	R	C
2	130	20
5	330	20
10	680	20
30K	5.1Meg	0.02μf
500K	4.4Meg	0.02μf
1 Meg	4.4Meg	0.1μf

t-μ Sec	R	C
1	22	50

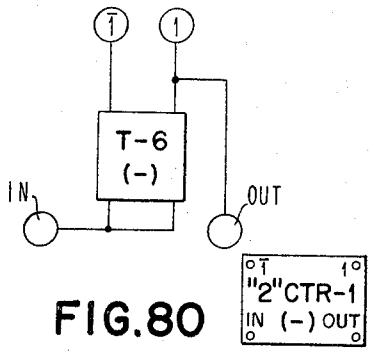


FIG.80

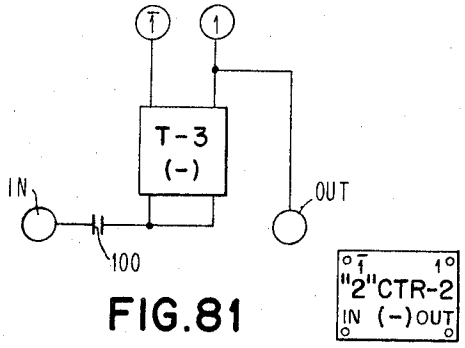


FIG.81

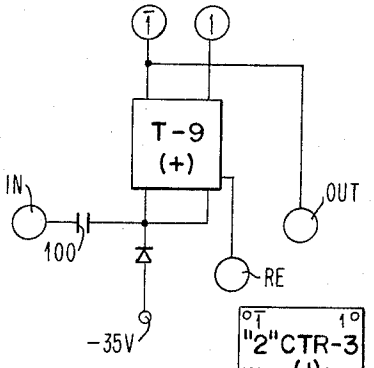
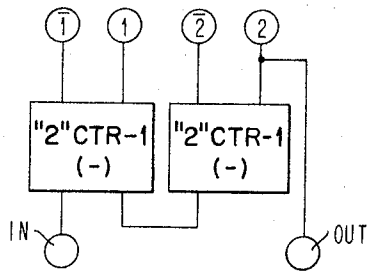


FIG.82



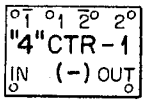


FIG.83

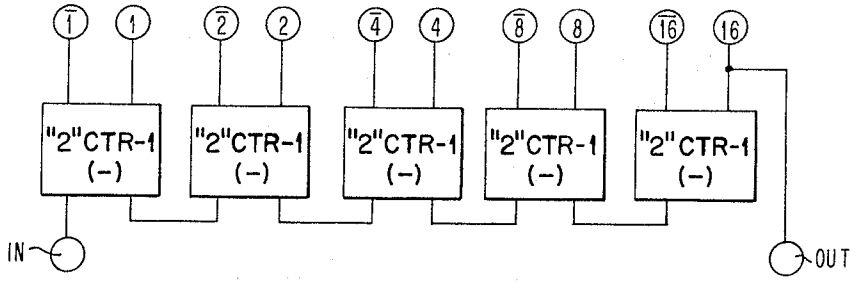
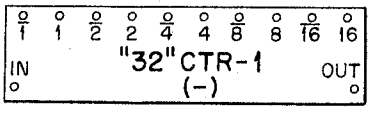


FIG.84



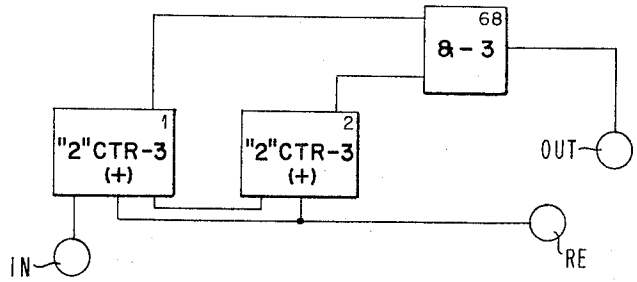
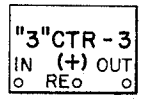


FIG.85



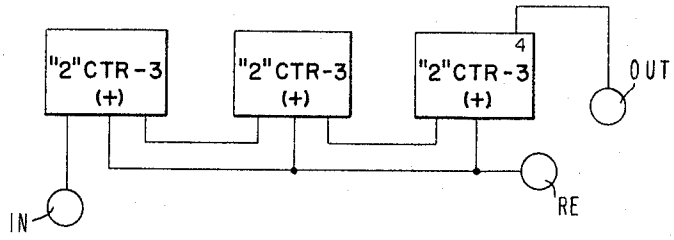
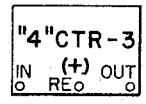


FIG.86



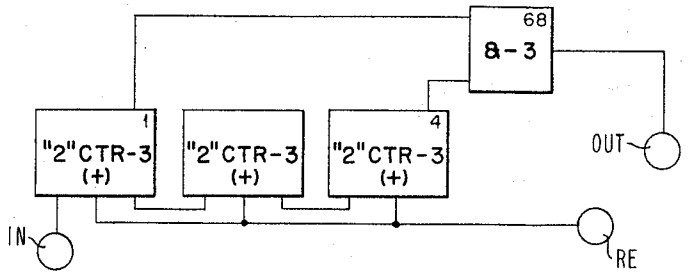
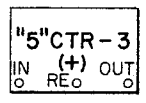


FIG.87



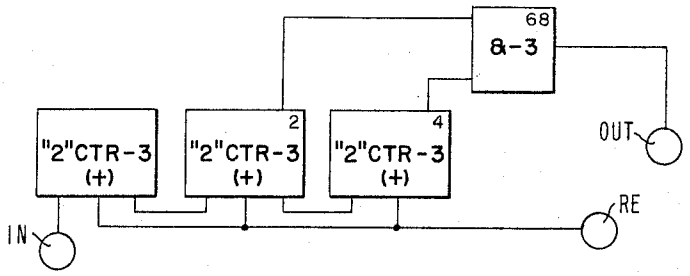
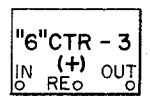


FIG.88



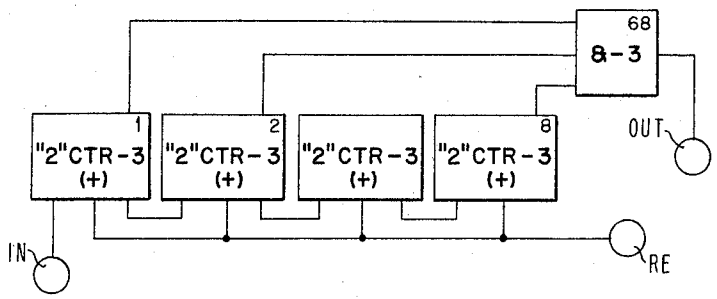
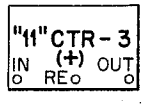


FIG.89



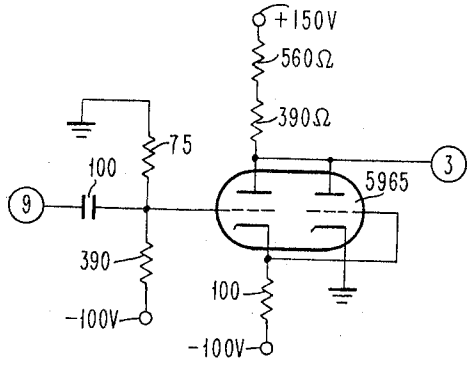


FIG. 90

PKR-1
30
09

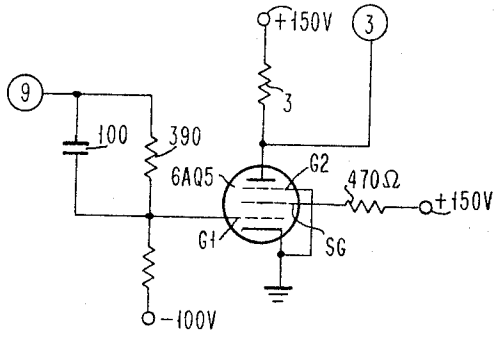


FIG. 91

PW-1
30
09

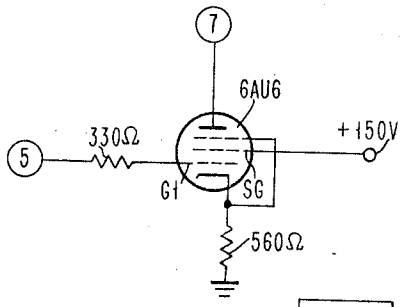


FIG. 92

CD-1
70
05

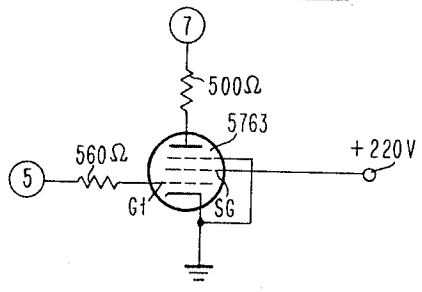


FIG. 93

CD-2
70
05

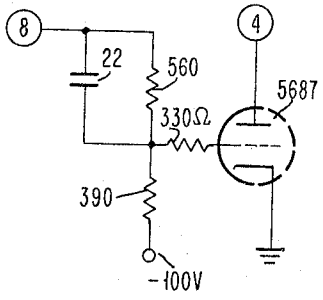


FIG. 94

nRD-1
40
08

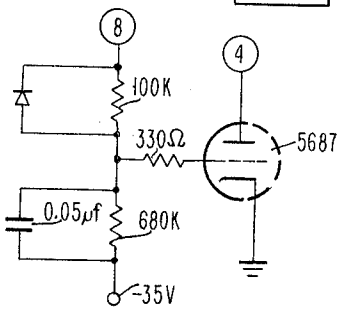


FIG. 95

nRD-2
40
08

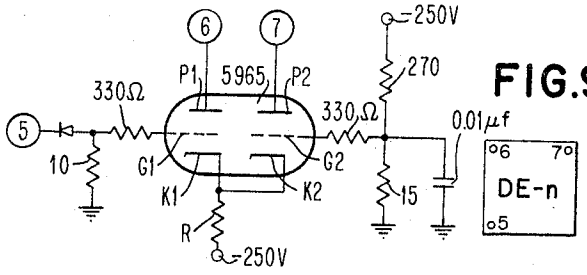


FIG.96

	R-K ohms
DE-1	256
DE-2	127.67
DE-4	63.6
DE-8	31.66
DE-16	15.62

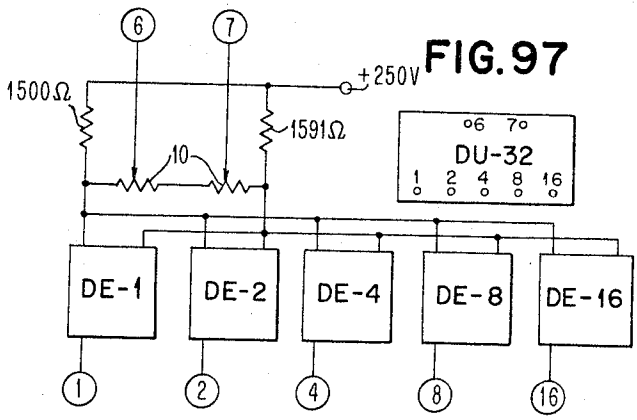


FIG.97

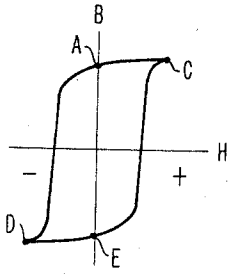


FIG.98

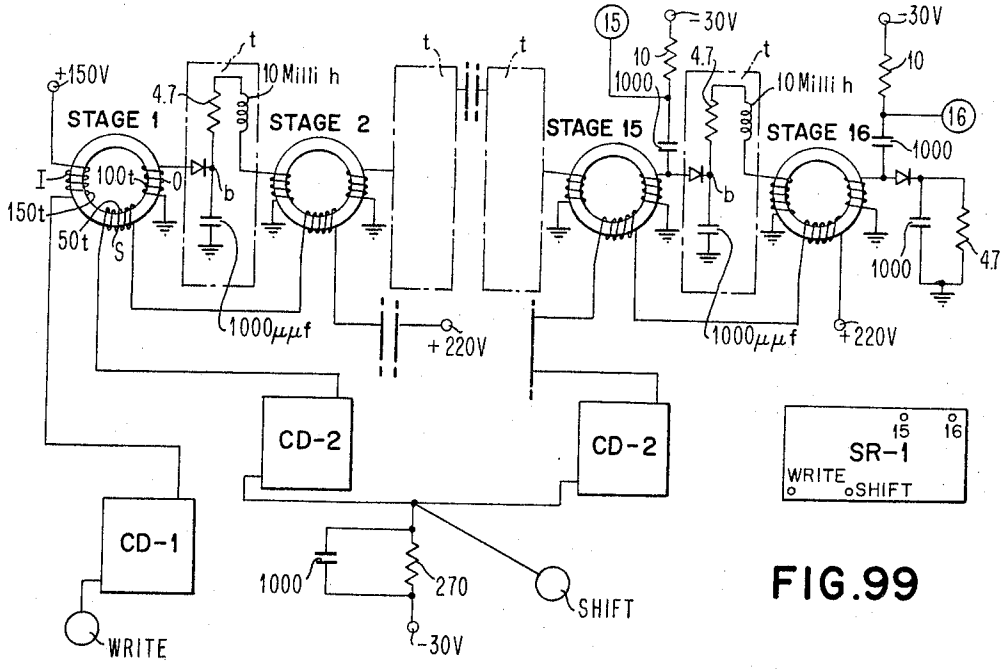


FIG.99

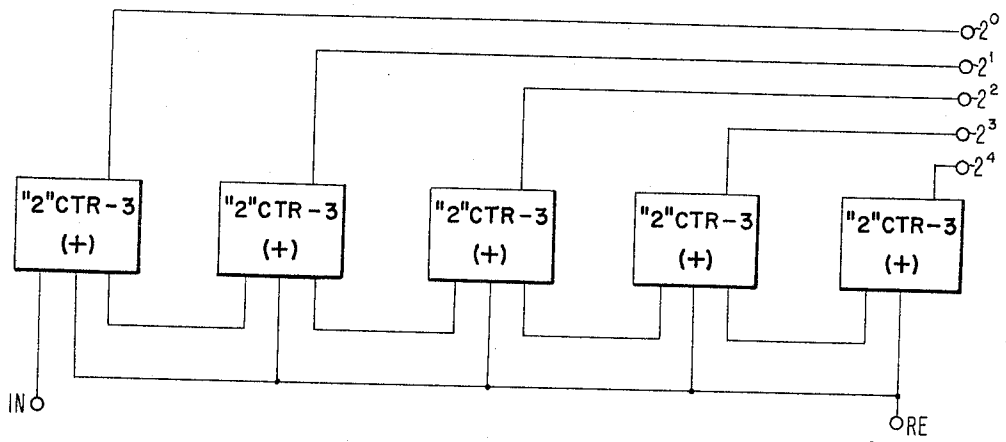
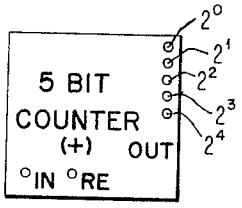


FIG. 100



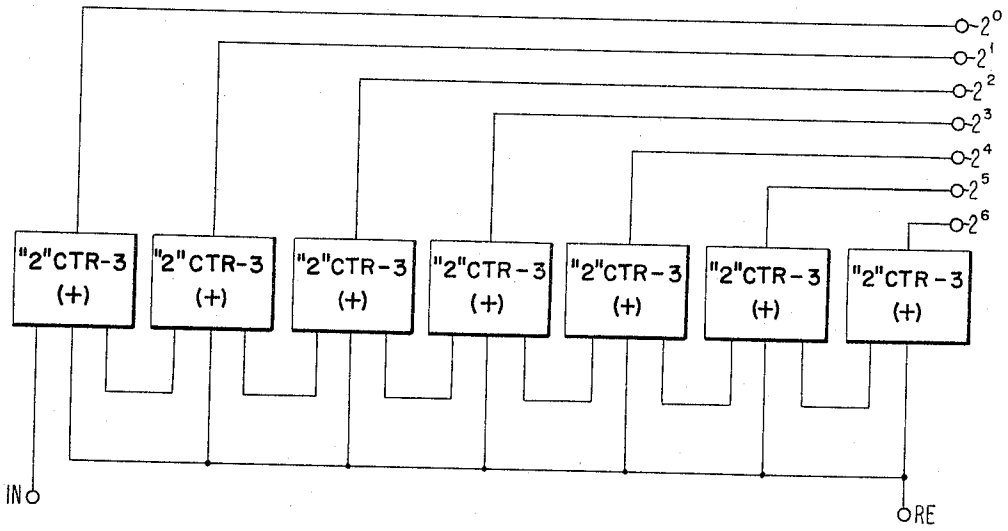
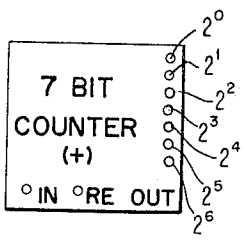


FIG. 101



Sept. 6, 1966 KUANG-CHI HU 3,271,761
CURVATURE AND SHAPE DETECTION
Filed Nov. 29, 1963 69 Sheets-Sheet 69

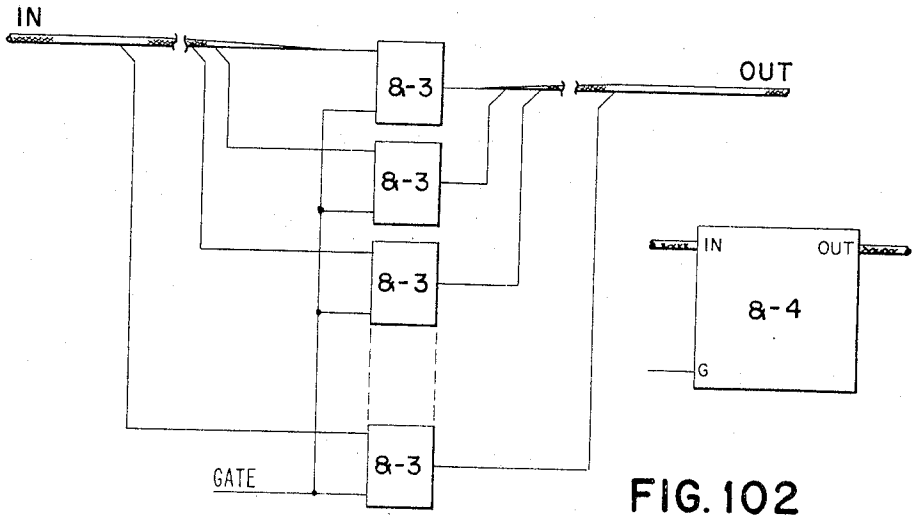


FIG. 102

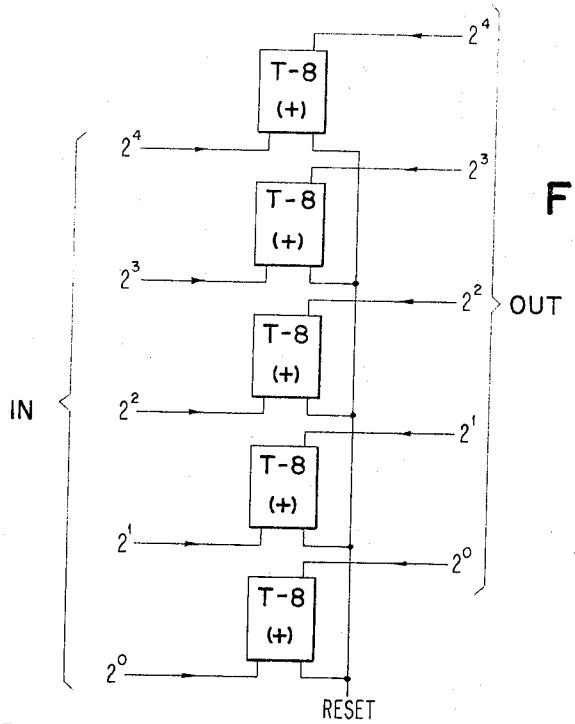
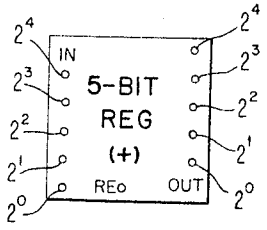


FIG. 103



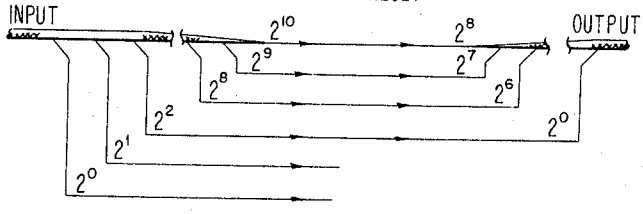
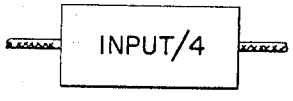


FIG. 104



United States Patent Office 3,271,761 Patented Sept. 6, 1966

3,271,761

CURVATURE AND SHAPE DETECTION

Kuang-Chi Hu, Hartsdale, N.Y., assignor to International Business Machines Corporation, New York, N.Y., a corporation of New York

Filed Nov. 29, 1963, Ser. No. 326,763
12 Claims. (Cl. 340—146.3)

This invention relates to specimen identification techniques and, in particular, the techniques for recognizing printed or written characters and symbols based on an analysis of the properties of the character-defined background areas.

The character-defined background areas that are particularly suitable for accurate recognition are described as "lakes" and "bays," where lakes are background areas that are entirely surrounded by the character (as in "D," "8," etc.), and bays are background areas that are partially surrounded by the character (as in "N," "H," "W," etc.). Recognition techniques based on an analysis of the lakes and bays in printed characters are shown in: U.S. Patent No. 2,889,535 to N. Rochester et al, entitled Recognition of Recorded Intelligence, filed October 20, 1955, issued June 2, 1959; and U.S. Patent No. 3,074,050 to G. L. Shultz, entitled Character Recognition Machine, filed December 31, 1956, issued January 15, 1963. The present invention represents an improvement over the inventions shown and described in these patents. In particular, the present invention provides additional techniques for reliably distinguishing between characters which define background areas that are generally similar. These techniques evaluate the shape of the character-defined background area as an additional measure to enhance the reliability of recognition. The invention is specifically embodied by an apparatus which analyzes background areas to ascertain their relative rectangularity, (whether they are more nearly triangular or rectangular in shape). This particular measure is useful in distinguishing between certain sets of characters, such as "N" and "H," which are similar in structure except for this distinction (both "N" and "H" have a bay at top and bottom and have no lakes). In the present invention, this shape analysis technique is combined with the techniques that are shown and described in the above-noted references to further enhance recognition.

An object of the present invention is to provide enhanced character recognition techniques wherein the shapes of character-defined background areas are interpreted.

Another object of the present invention is to provide enhanced character recognition techniques wherein the relative rectangularity of character-defined background areas is interpreted.

Another object of the invention is to show enhanced character recognition techniques based on an analysis of the relative shapes of character-defined "lakes" and "bays."

A further object is to provide character recognition techniques based on an analysis of the relative rectangularity of character-defined "lakes" and "bays."

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of a preferred embodiment of the invention, as illustrated in the accompanying drawings.

In the drawings:

FIG. 1 is a schematic flow diagram of a character recognition system.

FIG. 2A is a diagram illustrating the operation of the shape detecting techniques for typical character "H."

FIG. 2B is a diagram illustrating the operation of the shape detecting techniques for typical character "N."

FIG. 3A and 3B are diagrams illustrating the relative positions of the basic shapes in a character.

FIG. 4 is a diagram illustrating the nature of the other three basic shapes in a character.

FIG. 5 is a diagram illustrating two of the five special shapes utilized as recognition criteria.

FIG. 6 is a diagram illustrating three of the miscellaneous recognition criteria.

FIG. 7 is a diagram showing the manner in which FIGS. 8A to 8BB are to be arranged to constitute a complete view.

FIGS. 8A to 8BB, when arranged in the order indicated in FIG. 7 comprises a wiring diagram of the electrical circuits of the character recognition system embodying the preferred form of the invention.

FIG. 9 is a diagram showing the manner in which FIGS. 10A to 10B are to be arranged to constitute a complete view.

FIGS. 10A to 10B, when arranged in the order indicated in FIG. 9, comprise a schematic flow diagram of a Christmas tree shape decoder.

FIG. 11 is a diagram indicating the positive regional criteria to be detected for recognition of the different alphanumeric characters.

FIG. 12 is a diagram indicating the black bits in a scan of the numerals 0, 1 and 2, located above the corresponding contents of the marking register during the scan.

FIG. 13 is a diagram similar to FIG. 7 for the scan of the numerals 3 and 4.

FIG. 14 is a diagram similar to FIG. 7 for the scan of the numerals 5 and 6.

FIG. 15 is a diagram similar to FIG. 7 for the scan of the numerals 7 and 8.

FIG. 16 is a diagram similar to FIG. 7 for the scan of the numeral 9 and the letter A.

FIG. 17 through FIG. 31 are diagrams similar to FIG. 7 for the scan of all the rest of the letters of the alphabet.

FIG. 32 is a diagram illustrating the operation of the recognition criteria circuits in assigning the coded numbers 0, 1 and 2 to the marking register.

FIG. 33 is a diagram illustrating the operation of the recognition criteria circuits in assigning the coded number 3 to the marking register.

FIG. 34 is a diagram illustrating the operation of the recognition criteria circuits in assigning the coded numbers 5 and 6 to the marking register.

FIG. 35 is a diagram illustrating the operation of the recognition criteria circuits in assigning the coded numbers 4 and 7 to the marking register.

FIG. 36 is a diagram showing the manner in which FIGS. 37A to 37I are to be arranged to constitute a complete view.

FIGS. 37A to 37I, when arranged in the order indicated in FIG. 36, comprise a timing chart of one horizontal scan by the character recognition circuits.

FIGS. 38 to 46 are detailed circuit diagrams and respective block representations of cathode followers employed in the invention.

FIGS. 47 to 49 are detailed circuit diagrams and respective block representations of multigrid switches employed in the invention.

FIGS. 50 to 52 are detailed circuit diagrams and respective block representations of inverters employed in the invention.

FIGS. 53 to 56 are detailed circuit diagrams and respective block representations of AND circuits employed in the invention.

FIGS. 57 to 59 are detailed circuit diagrams and respective block representations of OR circuits employed in the invention.

FIG. 60 is a detailed circuit diagram and corresponding block representations of an alternating circuit (A.C.) input circuit employed in the invention.

FIG. 61 is a detailed circuit diagram and corresponding block representation of an A.C. AND circuit employed in the invention.

FIG. 62 is a detailed circuit diagram and corresponding block representation of an A.C. OR circuit employed in the invention.

FIGS. 63 and 64 are detailed circuit diagrams and respective block representations of clamp circuits employed in the invention.

FIG. 65 is a detailed circuit diagram and corresponding block representations of a limiter circuit employed in the invention.

FIG. 66 is a detailed circuit diagram and corresponding block representations of an amplifier employed in the invention.

FIG. 67 is a detailed circuit diagram and corresponding block representations of a photo-multiplier employed in the invention.

FIGS. 68 through 76 are detailed diagrams and respective block representations of electronic triggers employed in the invention.

FIG. 77 is a detailed circuit diagram and corresponding block representations of a free running multivibrator employed in the invention.

FIGS. 78 and 79 are detailed circuit diagrams and respective block representations of single shot multivibrators employed in the invention.

FIGS. 80 through 89 are detailed circuit diagrams and respective block representations of counters employed in the invention.

FIG. 90 is a detailed circuit diagram and corresponding block representations of a peaker employed in the invention.

FIG. 91 is a detailed circuit diagram and corresponding block representations of a power unit circuit employed in the invention.

FIGS. 92 and 93 are detailed circuit diagrams and respective block representations of core drivers employed in the invention.

FIGS. 94 and 95 are detailed circuit diagrams and respective block representations of relay drivers employed in the invention.

FIG. 96 is a detailed circuit diagram and corresponding block representations of a deflection stage employed in the invention.

FIG. 97 is a detailed circuit diagram and corresponding block representations of a deflection unit employed in the invention.

FIG. 98 is a curve illustrating a preferred hysteresis characteristic for the material of the cores shown in FIG. 99.

FIG. 99 is a detailed circuit diagram and corresponding block representations of a core shifting register employed in the invention.

FIG. 100 is a detailed circuit diagram and corresponding block representation of a 5 bit counter employed in the invention.

FIG. 101 is a detailed circuit diagram and corresponding block representation of a 7 bit counter employed in the invention.

FIG. 102 is a detailed circuit diagram and corresponding block representation of a multiple AND employed in the invention.

FIG. 103 is a detailed circuit diagram and corresponding block representation of a 5 bit register employed in the invention.

FIG. 104 is a detailed circuit diagram and corresponding block representation of a divider employed in the invention.

GENERAL DESCRIPTION

In the preferred embodiment of the invention, the shape detecting techniques are shown and described in conjunction with a "lakes and bays" recognition system, where the area around printed characters on a sheet is divided into a suitable number of elemental areas. The number of areas is fixed by the degree of resolution required and may be changed as the circumstances dictate. The character is scanned by a moving light source which applies light to one elemental area at a time. The light source is deflected vertically, in steps, and the light reflected from the paper at each elemental area or bit is analyzed as having been or not having been reflected from the black lines of the character. The results of each vertical scan are stored as coded numbers in a marking register which moves in synchronism with the scanning light beam.

A regional criteria rule circuit in the machine provides a means for modifying the coded numbers put into the marking register, dependent upon the apparent white region criteria in the characters being read. As a result of the logical coincidence of certain predetermined events involving the presence of a "now" white or black bit, the condition of the "next" white or black bit, the contents of the marking register positions corresponding to the "now" and "next" scan bit positions, and the state of temporary S triggers in the criteria rule circuit, memory C triggers may be turned On or the contents of the marking register may be further modified. The condition of the memory C triggers are also dependent in certain instances on one another. A novel feature of the invention is that the critia memory C triggers may be both turned On and reset by certain particular conditions at any time during the scan. This action proceeds while the vertical scan progresses across a character, with the result that a unique configuration of the critia memory C trigger states is obtained for each different character to be recognized. Thus, by the time a character has been completely scanned, a decision by a Christmas tree criteria decoder circuit dependent upon the states of the criteria memory C triggers will have been made as to the identity of the character.

Analysis of white regions—Recognition criteria

One of the novel features of this invention is the use of mathematical topology in getting at the crux of the distinctive features. From this point view, little attention is paid to the lines of the character as such, but the lines are only important insofar as they bound white regions. The preferred embodiment of the subject alphanumeric character recognition system utilizes 26 difference recogntion criteria arbitrarily divided into 18 basic shapes, 4 special shapes, and 4 miscellaneous recognition criteria. In addition to these criteria, the inventive shape detection techniques are used to distinguish between sets of characters which are similar with respect to the other criteria.

Recognition criteria—Shape detection

The inventive shape detecting techniques are illustrated in FIG. 2. The result of scanning and sampling a typical "H" and an "N" are shown with sample calculations. A region is considered to be substantially rectangular when its area exceeds a fraction K of the product of its height and width. A region is considered to be substantially triangular when its area is less than this fraction of the product of height and width. The lower bay of the "H" in FIG. 2*a* has a height (H) equal to 6, a width (W) equal to 9, and an area (A) equal to 43. When the predetermined fraction (K) is equal to ⅔, KHW equals 36, which is less than A (43), and the lower bay is determined to be substantially rectangular. The lower bay of the "N" in FIG. 2*b* has a height equal to 8, a width equal to 10, and an area of 45. Thus, KHW equals 53⅓, which is greater than A (45), and the lower

bay is determined to be substantially triangular. The fraction K equals ⅔ in the above calculations as this value is approximately optimum for use in recognizing characters with serifs. The value of K is ordinarily established in the range between 1 and ½, corresponding to a perfect rectangle and a perfect triangle, respectively. A value of ¾ is approximately optimum for characters without serifs, while providing accurate recognition of characters with serifs (the shapes of the south bays in the characters in FIG. 2 are also accurately recognized when K=¾). In order to provide a versatile recognition system, a value of ¾ is used in the preferred embodiment which is described below. The value of K can also be altered to distinguish between smaller degrees of rectangularity. For example, with a larger fraction K, the distinction between "D" and "O" can be made, where a "D" is generally more rectangular than an "O." Similarly, other functions may be substituted for KHW, to ascertain measures other than rectangularity.

Recognition criteria—Basic shapes

The 18 basic shapes include different variations of lakes, bays and peninsulas. A lake in a character is a white region completely surrounded by the black lines of the character. A bay is a white region within a character partially surrounded by the black lines of the character so as to have an opening out of the character. A peninsula is defined generally as a projection of a black line defined white region into a lake or bay of the character.

A bay may be further defined by its relative position in the character and the direction of the opening out of the character. A lake is defined by its relative position in the character, and a peninsula by the direction of the projection and the type of basic shape it projects into.

FIG. 3A shows an arbitrary character to illustrate both the relative positions of nine of the lakes and bay basic shapes and the direction of the opening out of the character of the bay basic shapes. The upper left white region in FIG. 3A is called a northwest bay (NWB) and is defined as a partially enclosed white region opening to the north (i.e., upward) and west (i.e., left). The white region in the lower left corner of FIG. 3A is called a southwest bay (SWB) and is defined as a partially enclosed white region opening to the south (i.e., downward) and west. Similarly, the white regions in the upper right and lower left hand corners of FIG. 3A are known respectively as a northeast bay (NEB) and a southeast bay (SEB).

In between the northwest bay (NWB) and the northeast bay (NEB) in FIG. 3A is a north bay (NB) which is defined as a bay having an opening to the north only and having its east shore line **10** at least substantially as long as its west shore line **12**. In between the southwest bay (SWB) and the southeast bay (SEB) in FIG. 3A is a south bay (SB), which is defined as a bay having an opening to the south only and having its east shore line **14** at least substantially as long as its west shore line **16**.

A middle west bay (MWB) is shown in FIG. 3A having an opening only to the west and thus having a north shore line **18** and a south shore line **20**. By the nature of a middle west bay, it can only exist if there are no other lakes or bays above or below it having both a north and south shore line, as will be more fully described presently. A middle east bay (MEB) is shown having an opening to the east only, and can only exist if there are no other lakes and bays above or below it having both a north and south shore line. The ninth basic shape of FIG. 3A is a middle lake (ML) which is enclosed by black on all four sides and can only exist if there are no other lakes and bays above or below it having both a north and south shoreline.

In FIG. 3B are shown six more of the basic shapes found in characters, which include an upper west bay (UWB), a lower west bay (LWB), upper lake (UL), lower lake (LL), upper east bay (UEB), and lower east bay (LEB). The upper right hand with region is an upper east bay (UEB) and is defined as a bay opening to the east and having a lake or bay below it with both a north and a south shoreline. When the upper east bay (UEB) is detected, the bay or lake below it with a north and south shoreline has its designation changed from a "middle" to a "lower." Thus, in FIG. 3B, a lower east bay (LEB) is shown below the upper east bay (UEB). This lower east bay may have been detected as a potential middle east bay, but since the scan of the character proceeds upward, as will be more fully described hereinafter, when the north shore line **22** is detected, an upper east bay (UEB) is noted and the potential (MEB) below has its designation changed to a potential lower east bay (LEB). Therefore, by definition a lower east bay (LEB) is a bay opening only to the east and having a lake or bay with a north and south shoreline above it. It can now be understood that the reason for requiring a north and south shoreline is so that a middle east bay (MEB) can exist below the northeast bay (NEB) (which has no north shoreline) as shown in FIG. 3A, but cannot exist below an upper east bay (UEB).

Similarly, the upper left hand white region is an upper west bay (UWB), defined as a bay opening to the west and having a lake or bay below it with a north and a south shoreline. An upper lake (UL) is enclosed by black on all four sides and having a lake or bay below it with a north and a south shoreline.

A lower west bay is then defined as a bay open to the west and below either an UWB, UEB or UL. A lower east bay is defined as a bay open to the east and below either an UWB, UEB or UL. An upper lake is a lake below an UWB, UEB or UL.

The remaining three basic shapes are illustrated in FIG. 4. A character W is shown which has a black line defined white region **24** projecting into a north bay to illustrate a north peninsula in a north bay (Pen. in NB) basic shape. Similarly, a character M is shown in FIG. 4 having a black line defined white region **26** projecting into a south bay to illustrate a south peninsula in a south bay (Pen. in SB) basic shape. The character G in FIG. 4 illustrates a partial lower lake basic shape (PLL) which is defined as a white region completely closed at the west and one the lower east, but being below an opening on the upper east.

Recognition criteria—Special shapes

Two of the special shapes are a deep west bay (D–WB) and a deep east bay (D–EB). A deep west bay (D–WB) is defined as a deeper than normal bay that is either a middle west bay (MWB), or upper west bay (UWB) having a predetermined horizontal depth to be more fully described hereinafter. Similarly, a deep east bay (D–EB) is deeper than normal bay that is either a middle east bay (MEB), or upper east bay (UEB) having a predetermined minimum horizontal depth.

A tall south west bay (T–SWB) is a taller than normal south west bay of a predetermined height. The letter D in FIG. 5 has a long black vertical line **30** that is defined as a special shape having a black line of a predetermined length and standing in a vertical position.

Recognition criteria—Miscellaneous

There are a number of miscellaneous recognition criteria, three of which are shown in FIG. 6. The type of W shown in FIG. 6 differs from that in FIG. 4 because it has two north bays (NB's). This is true because, by definition, a north bay (NB) basic shape requires that the east shoreline be at least substantially as high as the west shoreline. Thus, the W of FIG. 4 has only one North bay (NB). Since the projection **32** of the W of FIG. 6 is a tall one, two north bays are detected. This presence of a plurality of the same shape, two north bays (2NB's) in this case, is one miscellaneous recognition criteria.

Similarly, the M of FIG. 6 includes two south bays (2SB's) which is another special shape.

One of the novel features of this machine is that the potential recognition criteria are determined during the scan, and not at fixed times in the scan. As will be more fully described, the scan of characters proceeds upward and to the right. Thus, in the scan of the Q of FIG. 6, the lower basic shape will be detected before the upper lake basic shape. This recognition criteria then requires that a lower lake be detected before an upper lake and is abbreviated at LL:UL.

There are some printed characters that are difficult to differentiate: i.e., the numeral 1 (one) from the letter I. It has been found, in these "difficult to differentiate" situations, that the use of context is helpful. That is, it is much more likely that the letter I would follow another letter, and that the numeral 1 another number. This context miscellaneous recognition criteria will be described more fully hereinafter.

Positive recognition criteria in characters

FIG. 11 illustrates the different printed characters and the positive recognition criteria in the characters utilized in the preferred embodiment. The term positive recognition criteria is used herein to distinguish from negative recognition criteria which means the absence of a particular recognition criterion. It will be shown presently, that characters are recognized not only because of the presence of particular positive recognition criteria but because of the absence of other particular recognition criteria.

It can be observed in FIG. 11 that some of the printed characters are shown as having more than one variation. In some cases the variation is due to an unusually large serif or serifs in the character such as, for instance, the serif **40** in one of the P's of FIG. 11. Wherever serifs will not affect the final recognition criteria, they have been ignored in this description. It is to be understood at this point that most of the printed characters in use today, even though different type fonts, will have the recognition criteria that are shown in FIG. 11.

The inventive shape detection techniques are particularly shown wth respect to the distinction between the "H" and "N," where the "H" contains a rectangle-shaped south bay and the "N" contains a triangle-shaped south bay.

Looking at the character D **42** of FIG. 11, there are two positive recognition criteria listed therewith; a middle lake (ML) and a long black vertical line (LBVL). The character D **44** is shown with serifs **46** that extend so far to the left so as to appear as a middle west bay (MWB) to the recognition machine. It will presently be shown how both types of D characters **42** and **44** are recognized as the same character D.

Similarly, the character F **48** of FIG. 11 is shown as having a middle east bay (MEB) and a south east bay (SEB) while the character F **50** has a serif **52** long enough so that a potential lower east bay appears between serif **52** and the line **54** of the character, which is enough to cause an upper east bay recognition criterion to appear between the line **54** and a line **56**. Later in the scan, it will be determined that the lower east bay (LEB) is really a south east bay (SEB), but this will have no effect on the upper east bay designation. Again, it will be shown presently how both characters **48** and **52** are recognized as the character F.

Characters which may appear differently in different fonts, due to other factors than long serifs are the characters M, Q, W, 3, 4, 7, and 9. Since the two types of M's and W's have been hereinbefore briefly noted in conjunction with the description of FIGS. 4 and 6, they will not be further described at this point.

The 3 character **60** differs from the 3 character **62** because it has an upper east bay (UEB). The differences between the variations in the 3's, 4's and 9's are evident from FIG. 11. The character Q has four basic variations due to the different position and length that the line **64** can take. The different recognition criteria resulting from the four different Q characters are evident from the study of FIG. 11.

Christmas tree block differentiation

In a general alphanumeric recognition system, it is obvious that characters may be distinguished from each other by the fact that no two characters will have the same combination of recognition criteria. FIGS. 10A and 10B illustrate a schematic Christmas tree flow diagram indicating the logical process by which the recognition criteria are utilized to determine the character being read each of the different recognition criteria being shown as a block or part of a block. The recognition criteria are combined in some blocks in order to produce one operable Christmas tree block, but it will be obvious that other Christmas tree blocks could be designed to determine the combination of recognition criteria present in the character being read. In FIGS. 10A and 10B, the lower-right hand exit lead of each recognition criteria block is a "yes" lead which indicates the presence of that particular recognition criteria in the character being analyzed and the upper right-hand exit lead of each recognition criteria block is a "no" lead to indicate the absence of the particular recognition criteria. By the time the end of character is reached, the "yes" or "no" conditions of the different recognition criteria blocks are already set up, and a path can be traced from the furthermost left terminal **70** of FIG. 10A through lead **72**, towards the right through the blocks and the leads, corresponding to the presence or absence of the recognition criteria of the respective blocks, to one of the labeled terminals in order to determine which character has been read. While there may be different paths in the tree for the different versions of the characters and some of the characters with serifs, the outputs will be so connected so that there will be only one output terminal representing each character.

In FIG. 10A, the lead **72** is connected to an ML or UL or LL block **74**. Block **74** represents the presence of either a middle lake, upper lake or lower lake recognition criteria, via a character having any one or more of these recognition criteria present will appear on its "yes" lead **76**. Those characters without any of these three lakes appear on a "no" lead **78** from block **74**. The characters on the "yes" lead **76** are further separated from each other by the detection of a lower lake basic shape. The "yes" lead **76** (FIG. 10A) from the block **74**, is connected to a lower lake regional criteria block **80**. Characters having a lower lake (6, 8, B, and one of the Q's) appear on the "yes" lead **82**, and characters without the lower lake appear on the "no" lead **84**.

To further separate the 6, 8, B and the Q having a lower lake, the presence of an upper east bay regional criteria is detected by connecting the "yes" lead **82** of the lower lake block **80** to an upper east bay block **86**. Since a study of the characters shows that a character 6 is the only one of the four having an upper east bay, the character 6 appears on the "yes" lead **88** and is connected to a terminal representative of a 6. Thus, it has just been shown that a character 6 is recognized as such when a middle lake, upper lake or lower lake, and more specifically a lower lake plus an upper east bay, is detected.

No other character is detected in FIGS. 10A and 10B by only positive recognition criteria. For example, a "no" lead of the upper east bay block **86** represents the characters 8, B and Q having the lower lake. The Q with the lower lake can be further separated from the 8 and B by detecting the presence of the lower lake followed by upper lake (LL:UL) recognition criteria. This is accomplished by connecting the "no" lead **90** to a LL:UL block **92** upon the "yes" lead **94** of which appears a character Q. Lead **94** is also connected to the "yes" output of partial lower lake block **96**, the "yes" output of a middle east bay or lower east bay block **98** (FIG. 10B) and the "no" out-

put of a long black vertical line block **100**, and to a terminal representing the character Q. Thus, if a path is made through the blocks to any one of blocks **92, 96, 98,** or **100** to lead **94**, the character Q is recognized.

It is believed unnecessary to follow through a complete written description of how the rest of the characters of FIG. 11 are recognized. However, it will be a relatively simple matter to trace the selection of the characters which have not been described, through the Christmas tree network of FIG. 10A and FIG. 10B. The actual physical structure for the Christmas tree will be described hereinafter.

The inventive shape detection criteria is used in FIG. 10B where an "N" is indicated when the "triangle shape" requirement is met.

Flow diagram—Scanner

Referring now to FIG. 1, a flow diagram of the preferred embodiment of the invention is shown as basically consisting of scan, control and recognition circuits. The scan circuits include a cathode ray tube **110**. A spot of light on the fluorescent screen of the cathode ray tube **110**, produced by a beam therein, is focused by a lens system **112** onto a document **114** which contains the characters to be identified. The reflected light is collected by phototubes **116** which produces an output signal proportional to the amount of light striking them. Since the light reflected from an inked or black area of the document **114** is less than that reflected from an uninked or white area, a smaller signal will be produced by the black area. The signal is fed via a lead **117** to an amplifier-limiter unit **118** which amplifiies it, but selects only the larger signals, i.e., the white signals for transmissions via a sampled video lead **119** to a black-white "next" circuit **120**. The black-white "next" circuit **120** can then make a determination if a white signal has been transmitted to it, and thus produce a signal on the white "next" lead $\overline{B}_N$, or if there was no white signal, producing a signal on the black "next" lead $\overline{B}_N$. The leads B and $\overline{B}_N$ are connected into a black-white determination cable **122**.

The beam producing the spot of light may be moved stepwise vertically by a suitable vertical deflection generator **125** acting via leads **126** on vertical deflection plates **127**. The beam may be moved stepwise horizontally by a horizontal deflection generator **128** acting via leads **129** on horizontal deflection plates **130**. The vertical deflection generator is controlled via a lead **131** by a clock circuit **132** which is a master timer for the character recognition machine.

The vertical deflection generator **125** causes the beam to move vertically upward on the face of the scope in thirty-two discrete steps. Even though the presence of black or white is determined at each of the thirty-two discrete steps, only sixteen steps, or every other one of the thirty-two steps, is utilized in the recognition scheme because it has been found that the analysis of 16 bits per vertical sweep produces adequate recognition results. It may be understood, however, that more or less bits may be used without materially altering the invention. The beam is not moved continuously because of the problem of phosphor persistance of the spots of light on the cathode ray tube screen **110**. An unblank circuit **133** is controlled by the clock circuit **132**, via lead **131**, and in turn is connected to the control grid of the cathode ray tube **110** via a lead **134** to permit the beam to place the spot of light on the cathode ray tube screen only during a portion of the time that the beam is at rest.

Before the white signal is transmitted via the sampled video lead **119** to the black-white "next" circuit **120**, the black-white "next" determination is shifted via a pair of leads **135** to the black-white "now" circuit **136** producing a signal on a white "now" lead $\overline{B}$ if the determination shifted was white, and producing a signal on a black "now" lead B, if black was shifted. Leads B and $\overline{B}$ are also connected to the black-white determination cable **122**. Then when the sampled video is transmitted over lead **119** to the black-white "next" circuit **120**, cable **122** will contain both a black-white "next" and a black-white "now" determination. For reasons of convenience in detecting a minimum white area, to be described hereinafter, the $\overline{B}$ lead and the $\overline{B}_N$ lead are connected to an AND block **137**, the output of which is a lead $\overline{B}$ & $\overline{B}_N$, which is also connected into black-white determination cable **122**.

The scanning process normally starts with the spot at a lower left home position. Upon reaching the top of the vertical scan, the vertical deflection generator **125** resets the beam to the home position and via a lead **137**α steps the horizontal deflection generator **128** to cause the next scan to begin one horizontal step to the right of the previous vertical scan. The vertical scanning progresses across the characters from left to right until there is a complete absence of black during one complete vertical scan, which indicates the end of the character being scanned.

Marking register coding

During the progress of the scanning and at the end of character, recognition circuits operate to detect the presence of the recognition criteria. These recognition circuits comprise recognition criteria rule circuits **138** (FIG. 1) and storage means. The storage means are shown in FIG. 1 as a marking register **140** and C trigger storage within the recognition criteria rule circuits. The marking register **140** stores binary coded numbers which are determined by the result of each "now" bit and its "next" bit, and the history of previous bits, as modified and controlled by the recognition criteria rule circuits **138**. The C triggers **142** within the recognition criteria rules circuits **138** are utilized to store the finding of the particular criteria of the recognition criteria which are present in the character being scanned.

The marking register **140** has 16 positions of storage corresponding to the 16 utilized bits of the vertical scan. Each position of storage is capable of storing any number from 0 to 7 in binary coded form. The binary coded numbers stored in the marking register **140** are caused to step through the marking register **140** in synchronism with the scanning beam.

These binary coded numbers are assigned by the recognition criteria rules circuits **138** into the marking register **140** for each elemental area or bit according to a predetermined code. At the start of the scanning of a character, white bits are assigned the coded number 0. Whenever a black "now" bit is detected, the coded number 1 is assigned. This is illustrated in FIG. 32 where column (α) illustrates the black-white determinations made in a first vertical scan. All 16 bits are shown as white, column (b) of FIG. 32 which illustrates the different coded numbers assigned to the different stages of the marking register indicates that coded 0's were assigned to all the 16 positions of the marking register to represent the 16 white bits in the vertical scan of column (a).

The recognition machine operates to automatically indicate a white "now" determination at the beginning of each vertical scan, so that when the black-white "next" determination is made of the first or lowest bit in a vertical scan, a coded 0 will remain in the first stage of the marking register to indicate this white "now." In addition, the last coded number in column (b) is the coded 0 in the first stage of the marking register when the sixteenth bit of column (a) is read as a white "next" bit. Thus, the coded numbers assigned in the marking register at any time appear in FIGS. 32 through 35 to be offset one position downward in relation to the bits being sensed.

Column (c) illustrates the black-white determination made, in the same character, in a second vertical scan and the assigned numbers therefore are illustrated in column (d). The first, second and third bits from the bottom, which are indicated as white in column (c),

continue to have the coded number 0 assigned to them. It can be observed that the fourth and fifth bits from the bottom, which are illustrated as black in column (*c*), have each been assigned the coded number 1 thereto in column (*d*) to indicate this fact (i.e., assign a coded 1 for each black "now" bit).

All the coded numbers 2 to 7 are assigned for white bits according to the "vertical white zone" the bits is in, the "past history of black," the presence of a "minimum white height," and certain "particular conditions." The first three of these conditions will now be described briefly and a more detailed description of these three conditions and the particular conditions will be given hereinafter with the description of the recognition criteria rule circuits.

There are three possible "vertical white zones." In any vertical scan, the white bits above the first black bits crossed by the scan are in the first vertical white zone. In column (*c*) of FIG. 32, the white sixth through sixteenth bits are vertically above the black fourth and fifth bits and thus are considered in the first vertical white zone. Column (*e*) of FIG. 33 illustrates the situation where the first vertical white zone is closed above by a black crossing comprising the black ninth and tenth bits. The white eleventh through sixteenth bits above this second black crossing are then considered in the second vertical white zone. In column (*c*) of FIG. 34, the thirteenth and fourteenth black bits are illustrative of a third black crossing in a scan and the white fifteenth and sixteenth bits above the third crossing are therefore in the third vertical white zone.

The "past history of black" refers to an examination as to whether there are any black bits to the left on the horizontal level of the bit being observed. This examination is necessary in the separation of east white regions from west white regions.

The "minimum white height" consists merely of the simultaneous presence of a white "now" and white "next" determination, signifying a region two white bits high.

The coded number 2 is assigned where the following conditions are met: there is no "past history of black" to the left, a "minimum white height" exists, and the bit being examined is in the first "vertical white zone." For example, in FIG. 32, when assigning a coded number to the marking register representative of the sixth bit from the bottom of column (*c*), an indication will be available that the sixth bit is in the first vertical white zone. Not only is a black-white determination available on the sixth white bit of column (*c*) (the "now" determination), but also a black-white determination of the seventh white bit of column (*c*) is made (the "next" determination); the two white bits indicating a minimum white height. In addition, information is available that there is no history of black to the left of the sixth and seventh bits. This information is ascertained by the fact that coded number 0's were assigned in the marking register illustrated in column (*b*) representative of the sixth "now" bit and the seventh "next" bit of the previous vertical scan. Coded 0's to the left always indicate no history to black to the left. These three conditions are perceived by the recognition criteria rules circuit **138** causing a coded number 2 to be assigned in the marking register column (*d*) in place of the "now" bit of column (*b*). All the other bits in the scan of column (*c*) will be assigned to coded number 2 for the same reason as that described for the sixth bit.

The coded number 3 is assigned where there is no past history of black to the left, a minimum white height exists, and the bit being examined is in the second vertical white zone. For example, FIG. 33, column (*e*) shows a later vertical scan of the same character as that of FIG. 32. The eleventh bit, as the "now" determination and the twelfth bit, as the "next" determination are both white, and this fact is recognized as a minimum white height by the recognition criteria rule circuits, which also recognize that these bits are in the second vertical white zone. The fact that there is no history of black to the left is ascertained by the coded 2's assigned in marking register column (*d*) of FIG. 32 representative of the eleventh "now" bit and the twelfth "next" bit of the previous vertical scan. Coded 3's are assigned in column (*f*) of FIG. 33 to the twelfth to fifteenth white bits of column (*e*) for the same reasons described to the assignment of the eleventh bit of column (*e*). It may be stated at this point, that any coded number assigned in a vertical scan to the marking register for a particular horizontal bit position is recirculated in the succeeding vertical scans at the same horizontal position if there are no new coincidences of the conditions previously mentioned for assigning a new coded number. For example, FIG. 33, column (*e*), illustrates the vertical scan immediately succeeding the vertical scan of column (*c*) of FIG. 32. It can be observed that the bits of FIG. 33, column (*e*), up to the eighth bit from the bottom are exactly like those of column (*c*) of FIG. 32. Therefore, the coded numbers in column (*f*) of FIG. 33 up to the eighth bit are exactly like those of column (*d*) of FIG. 32.

One of the features of this invention is that a determination can be made of potential recognition criteria during any of the scans after the first vertical scan of the character. For example, coded number 0's in a particular bit arrangement may be a potential southwest bay. Coded number 3's in a particular arrangement may indicate a potential northwest or upper west bay. Coded number 2's in a certain arrangement may indicate a potential middle west bay, a lower west bay, or northwest bay. Enough information has now been described to understand what the recognition criteria circuits look for in recognizing west bays. In most of the bays and lakes utilized as recognition criteria, a minimum white region, two bits high by two bits wide, is required to produce the indication of the particular bay or lake. This minimum white region will hereinafter be referred to as a 2 x 2 white region. When a 3 "now" and a 3 "next" bit are sensed simultaneously with a white "now" and white "next" determination, a 2 x 2 white region is discerned. Coded 3's will now be assigned in this new scan for the white "now" determination and one bit later for the white "next" determination. For convenience of description, this condition is known as a 2 x 2 region of coded 3's, even though it may be understood such a condition has no physical meaning as such. If the coded numbers of these two vertical scans were placed adjacent to each other, the adjacent minimum white height region of coded 3's would make a 2 x 2 region of coded 3's. Thus the presence of a 2 x 2 region of coded 3's implies no history of black to the left, and a white region of a predetermined minimum dimension in the second vertical white zone. This minimum dimension has been selected after an intensive study of the alphanumeric characters to be recognized. A bay or a lake in the first vertical white zone may be a middle or lower bay or lake while a bay or lake in the second vertical white zone may be an upper bay or lake. To recognize an upper west bay, in addition to the above implications, a requirement exists that the 2 x 2 region of coded 3's is blocked by black above and to the right.

As soon as the existence of these facts are recognized by the recognition criteria rules circuits **138**, and the primer triggers, a C trigger in the recognition criteria rule circuits will be operated to indicate this fact.

If the recognition criteria rules circuit indicates coded number 3's in a 2 high by 4 wide pattern with no black above but black to the right, a northwest bay indication will be made by the C trigger storage indicating a northwest bay. This will be described hereinafter in greater detail.

In the same way, a group of coded number 0's 2 high by 4 wide blocked by black from above and to the right

cause the recognition criteria rules circuit **138** to produce a southwest bay indication in the C trigger storage.

A 2 x 2 region of coded number 2's blocked above by black produces a possible middle west bay indication in the C trigger storage. However, when either an upper west bay, upper lake, or upper east bay is recognized, the possible middle west bay indication is changed to a potential lower west bay indication. Then, if in a later vertical scan it is determined that this region is blocked to the right or east by black, the potential lower west bay indication is recognized as a true lower west bay.

A northwest bay indication will also be obtained if instead of having a region of 2 high by 4 wide coded 3's, a region of 2 high by 4 wide coded 2's is detected along with the no black above and black to the right limitation previously described for the northwest bay.

Assignment of coded numbers for bits with a past history of black to the left

The nature of lakes, north bays, south bays and east bays is such that they require a past history of black to the left, and to aid in recognizing then the coded numbers 4 through 7 are utilized. As hereinbefore described, a coded 0, 2 or 3 in the marking register indicates no past history of black to the left, and coded 1 indicates a black "now" bit. The coded number 5 is assigned where a minimum white height exists, the bit being examined is in the first vertical white zone, and the bit has a past history of black to the left. The coded number 6 has the same requirements except that the bit being examined must be in the second vertical white zone rather than the first vertical white zone. A coded number 7 may be assigned where the conditions that exist are the same as for the assignment of coded 5's and 6's except that the bit examined is in the third vertical white zone.

For example, column (*a*) of FIG. 34 illustrates the bits determined in some vertical scan of a character which may be one other than the one discussed for FIGS. 32 and 33. The first and second bits from the bottom are shown as white and have the number 0 assigned thereto in column (*b*). All the other bits are black and therefore are represented by coded number 1's in column (*b*). In column (*c*), which represents the next vertical scan, the fifth and sixth, the eleventh and twelfth, and the fifteenth and sixteenth bits are white. At the time of the assignment of a coded number for the fifth bit, the information as to the fact that a coded 1 was assigned in the marking register for the fifth and sixth bits of the previous scan, indicates a past history of black to the left. The fact that the fifth "now" determination and the sixth "next" determination are both white indicates a minimum white height. The recognition criteria rule circuits will also be aware of the fact that the bit being examined is in the first vertical white zone. The combination of these factors causes a coded 5 to be written into the marking register as shown in column (*d*) of FIG. 34. Coded 5's will continue to be written in the marking register for this white region until a black bit is recognized. Thus, the fifth and sixth bits will both have the coded number 5 assigned thereto.

In assigning a coded number for the eleventh bit of column (*c*) of FIG. 34, the same factors exist as for the fifth bit except that this bit is in the second vertical white zone. This fact then causes a coded number 6 to be placed in the marking register for the eleventh and twelfth bits. In assigning a coded number for the fifteenth bit of column (*c*) of FIG. 34, the same factors exist except that this bit is in the third vertical white zone and therefore a coded 7 is assigned to the marking register column (*d*).

The presence of a 2 x 2 region of coded 6's implies a history of black to the left, and a white region of predetermined minimum dimensions in the second vertical white zone. To recognize a potential upper east bay, an additional requirement that the 2 x 2 region of coded 6's are blocked by black above is necessary. If a later vertical scan determines that the potential upper east bay is blocked by black to the right, the white region of coded 3's is now closed by black in all four directions and the potential upper east bay indication will be changed to an upper lake indication.

A 2 x 2 region of coded number 5's blocked above by black produces a possible middle east bay indication in the C triggers. When the possible middle east bay is subsequently blocked by black to the right, the indication is changed from a middle east bay to middle lake. However, if either an upper west bay, upper lake, or upper east bay is recognized, the possible east bay indication is changed to a potential lower east bay indication. Then, if in a later vertical scan it is determined that this region is blocked to the right by black, the potential lower east bay indication will be changed to a lower lake indication.

The only other coded number assigned to the marking register is a coded 4, the assignment of which is illustrated in FIG. 35. The coded number 4 is assigned where a minimum white height exists, there is a past history of black to the left, and there are no black bits below the bit being examined, i.e., the vertical scan has not yet entered the first vertical white zone. For example, columns (*a*) and (*b*) of FIG. 35 are similar to columns (*a*) and (*b*) of FIG. 34. In FIG. 35, however, column (*c*), which represents the next vertical scan, contains all white bits except bits 7 through 10. Looking at column (*c*), the following factors are present: both the third "now" bit and the fourth "next" bit are white, both are blocked by black to the left, and there are no black bits below the third bit in column (*c*) (i.e., the first vertical white zone has not been entered). The simultaneous occurrence of all these factors represents a condition known as a single dropout to the south. As an indication of all these conditions coded numbers 4's are assigned for the white bits. These 4's have been assigned in column (*d*) representative of the bits of column (*c*).

If the recognition criteria rule circuits indicate coded number 4's in a 4 high by 2 wide pattern, a potential southeast bay indication is stored in the C trigger storage. The reasons for the southeast bay being 4 high by 2 wide rather than 2 high by 4 wide like the southwest bay, will be described hereinafter. If a 2 x 2 region of coded 4's is blocked to the right by black, the recognition criteria rule circuits **138** produce a south bay indication in the C triggers.

In FIG. 35 the eleventh and twelfth bits are white, and since they have a past history of black to the left and they are in the first white vertical zone, the coded number 5's will be assigned thereto as previously described. Since there are no black bits above the eleventh bit, at the end of the sixteenth bit an indication of a single dropout to the north will be produced in the recognition criteria rule circuits. In column (*e*) a similar situation exists (that is, all white bits above the eleventh bit), and the same numbers are assigned in column (*f*) as were assigned in column (*d*). At the end of the sixteenth bit of column (*e*) an indication of a double north dropout will be produced in the recognition criteria rule circuits. In the scan illustrated in column (g) when assigning a coded number for the eleventh bit, the presence of a minimum white region and a double dropout will cause the recognition criteria rule circuits to assign a coded 7 to the marking register as shown in column (*h*). Coded number 7's therefore may represent potential northeast bay. If a recognition criteria rule circuit indicates coded number 7's in a 4 high by 2 wide pattern with no black to the right, a potential northeast bay indication will be made by the C trigger storage. Since all that is necessary for a potential northeast bay indication is a 4 high by 2 wide white region having black to the left and below but not above and to the right, a northeast bay may also be indicated by 4 high by 2 wide pattern of 5's or 6's when there is a double dropout indication.

Where at least a minimum white region of coded 7's is blocked to the right by black, a north bay indication is produced. A north bay indication may also be minimum white regions of coded 5's or 6's in conjunction with a double dropout and blocked by black to the right.

Just enough of the reasons for the assignment of the coded numbers and the analysis of the recognition criteria represented by the arrangement of the coded numbers has been described so as to allow the general description of the machine to be continued. Other reasons for assignment of coded numbers and the analysis of the coded numbers for the recognition criteria will be described hereinafter.

The end of character determination is made when there is a complete vertical scan having all white bits. At the end of character indication, a Christmas tree criteria decoder **146**, which operates like the previously mentioned Christmas tree of FIGS. 10A and 10B analyzes the C triggers via leads **148**, to determine the alphanumeric character on the document **114**. This alphanumeric character may then be punched out on a punch or used by any other utilization means **150**, as desired.

Flow Diagram—Control and recognition circuits

The method for detecting some of the recognition criteria from the binary coded numbers in the marking register **140** and the status of the memory C triggers, has been briefly described. The means for detecting the other recognition criteria will be described later, but the description of the flow diagram of the recognition and control circuits can now be continued.

In order to get the marking register **140** to move in synchronism with the scanning beam, the clock circuit **132** produces pulses alternately at a fixed frequency on a shift 1 line **152** and a shift 2 line **154**, and feeds these pulses to register control circuits **156**. A pulse appears on the shift 1 line **152** at the same time the vertical sweep generator **125** is pulsed to step the light beam. A pulse fed by the shift 2 line **154** to the register control circuits **156** controls the shifting of the marking register **140** by causing a pulse on a register shift line **158**, which is connected to the marking register **140**, to cause the contents of the marking register **140** to be shifted one position. The contents of the sixteenth stage of the marking register **140** are thereby shifted through three leads **160** to a sixteenth stage register read out trigger circuit **162** where they are temporarily stored, still in binary form. The contents of the fifteenth stage of the marking register are at the same time shifted through three leads **164** to a fifteenth stage register read out trigger circuit **166** for temporary storage. The information in the sixteenth stage register read out trigger circuit **162** is the "now" bit via the coded number in the marking register for the bit in the previous vertical scan at the horizontal level of the bit being analyzed for coded number assignment. The information in the fifteenth stage register read out trigger circuit **166** is the coded number representative of the "next" bit, via the bit above the "now" bit. Right after shifting, the first stage of the marking register will contain a coded zero until a coded number is written therein.

The "now" bits from the sixteenth stage register read out trigger **162** are applied through six leads **168** to a sixteenth stage "now" digit decode circuit **170** and through three of the six leads **168** to a digit encode circuit **172**. The sixteenth stage "now" digit decode circuit **170** converts the binary coded "now" bit to an equivalent one out of eight coded "now" bit indication which is applied via one of eight leads **174** to the input of the recognition criteria rule circuits **138**. In the one out of eight code, eight numbers may be indicated by having each number represented by a different one of eight leads being operative.

The "next" bits from the fifteenth stage register read out triggers **166** are applied through six leads **176** to a fifteenth stage "next" digit decode circuit **178**, which converts a binary coded "next" bit to a one out of eight coded "next" bit which is applied via one of eight "next" leads **180** to the input of the recognition criteria rule circuits **138**.

The five black-white determination leads **122** are also connected to the input of the recognition criteria rule circuits **138**. It is to be noted that the register shift lead **158** is also connected to the black-white "next" block **120** and it is a register shift signal on lead **158** that causes the shifting of the black-white "next" determination via leads **135** to the black-white "now" block **136**.

The recognition criteria rule circuits **138** operates in such a manner that a one out of eight coded indication may appear at its output which is dependent upon the different combination of one out of eight coded "next" bits from the fifteenth stage digit decode **178**, the "now" bits from the sixteenth stage digit decode **170**, the black-white "next" determination and the black-white "now" determination cable **122**, and, internally, the status of memory C triggers. For instance, as previously described, if the one out of eight input from the sixteenth stage digit decode circuit **170** is a coded 1 and the one out of eight coded input from the fifteenth stage digit decode **178** is a coded 1, and there is a white "now" and white "next" indication in the black-white determination cable **122**, a one out of eight coded 5 will appear at the output of the recognition criteria rule circuits **138**. As another example, if the one out of eight input from the sixteenth stage digit decode circuit **170** is a coded 5 and the one of eight coded input from the fifteenth stage digit **178** is a coded 5, and there is a white "now" and white "next" indication in the black-white determination cable **122**, no one out of eight signals will appear at the output of the recognition criteria rule circuits **138**, and the recognition criteria circuit will recognize that this is a minimum white region and also set up an indication in the memory C triggers of a potential middle east bay.

The output one out of eight coded indications are fed through one of seven leads **182** and applied to the digit encode circuits **172**. There are only seven output leads **182** because there is no need for a coded 0 to be written in this manner into the marking register. The output one of eight indication in the digit encode circuits **172** is converted to a binary coded indication and fed via three leads **184** for writing into the first stage of the marking register **140**. This new bit, in effect replaces the "now" bit in the marking register. Writing into the first stage of the marking register does not occur until a pulse appears on a write line **186** which is connected from the register control circuits **156** to the digit encode circuits **172**. The write pulse from the register control circuit **156** is produced by a pulse on the shift 1 line **152** to the register control circuit **156** and therefore occurs between two register shift pulses. At the time of a write pulse, if there is no output one of eight indication on any of the leads **182**, the binary coded "now" bit on the three leads **168** is transmitted through the digit encode circuit **172** through leads **184** to the first stage of the marking register **140**. Immediately after the register write pulse, a register read out trigger reset pulse from register control circuits **156** over a lead TP, resets the register read out triggers **166** and **162**.

The register read out trigger reset pulse is also used as a timing pulse in the recognition criteria rule circuits **138**. Thus, the register read out trigger reset lead TP is connected to the recognition criteria rule circuits **138**, and the timing pulse TP is used to get an instantaneous sampling of input conditions to the recognition criteria rule circuits **138**, once, during the time a particular bit is being examined.

Assume for purposes of illustration, that an all white bit vertical scan has been completed, and that the next vertical scan will sense at least one black bit of the character. At this time, an end of vertical scan pulse is gen-

erated by the vertical sweep generator **125** and fed via a lead **190** to the black-white "next" block **120** where it acts to reset the black-white "next" circuit **120** so as to put it in the white "next" condition. The next register shift pulse on lead **158** causes the white "next" condition of the black-white "next" circuit **120** to be shifted to the black-white "now" circuit **136**. Now when a sampled video pulse indicative of the black-white condition of the first bit in the vertical scan is fed via lead **119** to the black-white "next" block **120**, a decision will be made in the recognition criteria rule circuits **138** based on the first bit in the vertical scan as the black-white "next" bit and a reset white ($\overline{B}$) signal from the black-white "now" block **136**. Since the "now" bit will always be white at the start of a vertical scan, nothing but a zero will be written into the marking register at this time. This will be true because, as will be later more fully described, there is no output from the recognition criteria rule circuits to the digit encode circuits **172** for this input. Therefore, no coded number is transmitted via the digit encode circuit **172** to the first stage of the marking register **140**. This is the reason that FIGS. 32 to 35 indicate that the first coded number in the marking register in each scan is a coded 0.

After the events for this first bit are completed, the beam is moved vertically upward to where the second scanned spot is to be sampled, and the contents of the marking register are shifted so that the second binary coded digit, then in the fifteenth stage, is shifted to the fifteenth stage register read out trigger **166** and the first binary coded digit (then in the sixteenth stage) is shifted to the sixteenth stage register read out trigger **162**. Thus, now the first bit from the bottom is the "now" bit and the second bit from the bottom is the "next" bit. The coded number, if any, to be written into the marking register, is now the coded number shown as the second from the bottom in the coded number columns of FIGS. 32 to 36.

For example, assuming that the first bit is black, the presence of black "now" on line B of the black-white determination cable **122** combined with the presence of a coded zero on the leads **174** and **180**, are indicated on the input of the recognition criteria rule circuits **138**. In this case, the one lead of each of the one out of eight outputs from the recognition criteria rule circuits **138** is effective to write a coded 1 and this coded number 1 is transmitted via the digit encode circuit **172** where it is converted to a binary coded number and written into the first stage of the marking register **140**. It is understood, of course, that the next bit also may determine the number to be written into the marking register. This process continues in the same manner until the beam reaches the top of the scan when it is returned to the bottom, home position. It is to be recalled that the sixteenth bit from the bottom is never utilized as a "now" bit. At this point, the marking register had gone through a complete cycle and the first coded number is again in the sixteenth stage register read out triggers **162** in position to be read out. At this point, too, the vertical sweep generator **125** produces a pulse on an end of vertical scan line **190**. This pulse is fed to a reset and end of character circuit **192**. The reset and end of character circuit **192** contains three reset leads **194**, which are connected to triggers in the recognition criteria rule circuits **138**, for resetting at different times. The vertical scan will continue until a complete vertical scan has taken place without the sensing of a black area, indicating an end of character. An OK to Punch signal then appears at the output of the end of character circuit **192** and is transmitted via an OK to Punch lead **196** to the Christmas tree criteria decoded circuit **46**. The character then represented by the Christmas tree criteria decoded is transmitted through leads **198** to the punch **150** where an indication is made of the character that has been sensed from the document **114**.

One more all white vertical scan takes place during punch time, during which time the marking register is shifted through a complete cycle, but the register write pulse is blocked to prevent anything from being written in the marking register and thereby effecting a reset to coded zero of all the stages of the register. After punch time, a punch done lead **199** then transmits a pulse to the reset and end of character circuit which allows the recognition machine to start scanning the next character.

In order to more fully understand the interrelation between the recognition criteria rule circuit **138**, the marking register **140**, and the memory C triggers, these circuits must be described in more detail and therefore a description will be given of FIGS. 8A through 8BB which comprise the circuits of the preferred embodiment of the invention.

Conventions employed

Referring to FIGS. 8A through 8BB of the drawings, it will be seen that the different elements comprising the invention are represented by blocks, whose contents are illustrated in other figures of the drawings, the inputs and outputs to the blocks only being indicated in FIGS. 8A through 8BB. Before proceeding with a description of the FIGS. 8A through 8BB, a detailed description will be given of the respective elements such as the cathode follower, multigrid switch, inverter, AND circuit, OR circuit, clamping circuit, limited circuit, amplifier, photomultiplier, trigger, A.C. Input circuit, A.C. AND circuit, A.C. OR circuit, free running multivibrator, single shot, multivibrator, counter, peaker, power inverter, core driver, and relay driver The contents of the respective blocks and the respective block representations are shown in FIGS. 38 through 99. The position of terminals in the blocks of wiring diagrams FIGS. 8A to 8BB correspond to the position of the terminals in the blocks of block symbol diagrams FIGS. 38 through 99.

Wherever shown in the drawings, unless otherwise indicated, the values for the various resistors, condensers, and inductances are in thousands of ohms, micromicrofarads, and millihenrys respectively. For example, a resistor labeled 200, indicates a 200K (200,000) ohm resistor; a condenser labeled 100, indicated a 100 micromicrofarad condenser; and an inductance labeled 10 indicates a 10 millihenry inductance. Resistors labeled 100Ω and 1 meg. indicate respectively a 100 ohm and a 1,000,000 ohm resistor. A condenser labeled 0.01 μf. indicates a 0.01 microfarad condenser.

Hereinafter, in this specification where a conductor or circuit terminal, etc. is referred to as being shifted positive or negative in potential, this does not necessarily mean that the point in question is positive or negative in an absolute sense, but only more positive or more negative, relative to its previous state. This principle also applies to any description where positive and negative pulses are mentioned.

A multiplier circuit that is suitable for use in FIG. 8 is shown in a text by R. K. Richards entitled Arithmetic Operations in Digital Computers, published by Van Nostrand in 1955, FIGURE 5–1, page 139.

A subtractor that is suitable for use in FIG. 8 is shown in FIGURE 21 of a copending U.S. patent application by Lawrence P. Horwitz and Glenmore L. Shelten, Jr., Serial Number 45,034 filed on July 25, 1960.

Cathode follower CF

Referring to FIG. 38, there is illustrated a block symbol of a standard cathode follower and also the details of the circuit within the block. A cathode follower functions to produce an output signal having greater power than the input signal, but of the same polarity and substantially the same wave shape and with no appreciable time difference between the input signal and the output signal.

The cathode follower may employ, for example, a triode tube, the plate of which is directly connected to a positive supply voltage and the cathode of which is connected to an output terminal and via cathode circuit resistance to a negative voltage source. A positive signal applied to the grid of the tube causes an increased flow of current through the tube and cathode circuit resistance. Consequently, due to the increased current flow, a positive voltage shift occurs at the cathode. The voltage of the output signal at the output terminal remains substantially the same as that of the input signal, but due to the increased current flow the power of the signal is increased proportionately. Likewise, it is obvious that a negative shift on the grid will cause the voltage at the cathode to shift relatively negative.

The standard cathode follower (FIG. 38) which may comprise one triode of a dual triode 5687 type tube, has its grid connected via a 330Ω resistor to an input terminal "5," and its plate directly connected to a +150 volt supply. The cathode, which is directly connected to an output terminal "4," is connected via a resistance R to a −100 volts supply.

It may be necessary in order to help speed output signal shifts and to permit faster discharging of line capacitance, to operate two or more cathode followers in parallel. This may be accomplished where there are no bleeder resistors in the grid circuit by commonly connecting the input terminals to a new common input terminal "5," and commonly connecting the output terminals to a new common output terminal "4." Where there is a bleeder network, in the grid circuit, all but one of the grid circuits are disconnected from their respective bleeder resistor junctions and then the disconnected ends are commonly connected to the bleeder resistor junction of the remaining connected grid circuit.

The standard cathode follower is hereinafter represented by a block containing the alphabetic character CF followed by a numerical designation 1, i.e., CF–1. Where standard cathode followers are connected in parallel, the number of cathode followers so connected is indicated by the letter *n* preceding the CF in the block diagram, for example, if there are two standard cathode followers connected in parallel, the block is identified by the symbol 2CF–1. Further, the value of the effective cathode resistance R which may vary depending on circuit requirements, is indicated in the upper right-hand corner of the block.

Cathode followers *n*CF–2 through *n*CF–9 are shown in FIGS. 39 through 46 respectively, and operate in basically the same manner as the standard cathode follower *n*CF–1. The changes in the cathode followers CF–2 through CF–9 are obvious from the drawings and are well understood in the art. Consequently, no further description of these cathode followers is believed necessary.

Multigrid switch S

Referring to FIG. 47, there is illustrated a block symbol of a standard multigrid switch and also the details of the circuit within the block.

A multigrid switch functions to produce a negative output signal when there is a coincidence of two positive input signals.

The multigrid switch may employ, for example, a multigrid tube, the plate of which is connected via plate circuit resistance to a positive supply voltage. The plate circuit resistance and positive supply voltage may sometimes be shown as part of another circuit. The input terminals of the switch are connected to two grids G1 and G2, and the output terminal is connected in the plate circuit. No current flows through the tube and plate circuit resistance until there is a coincidence of positive signals at both of the grids G1 and G2. When this occurs, the voltage drop across the plate resistance, due to the current flow, causes the voltage at the plate to shift relatively negative.

The standard multigrid switch which includes a 6BE6 type pentagrid tube has its grid G1 connected through a 330 ohm resistor to the junction of a bleeder network consisting of an 82K ohm resistor connected to a −100 volt source, and a 27K ohm resistor connected to ground. The junction is also connected via a 0.01 microfarad condenser to an input terminal "9." Grid G2 is connected through a 330 ohm resistor to the junction of a bleeder network consisting of a 330K ohm resistor connected to a −100 volt source, and another 330K ohm resistor paralleled by a 15-micromicrofarad condenser connected to an input terminal "7."

The plate is connected directly to an output terminal "3," implying that the plate resistance and plate voltage are in the circuit to which the switch is to be connected. The screen grid SG is connected via a 330 ohm resistor to the junction of a bleeder network consisting of a 22K ohm resistor connected to +150 volts, and a 39K ohm resistor connected to ground. The junction of the bleeder network is also connected through a 0.01 microfarad condenser to ground.

The standard multigrid switch is hereinafter represented by a block containing the alphabetic character S followed by a numerical designation 1, i.e., S–1.

Multigrid switches S–2 and S–3 are shown in FIGS. 48 and 49, respectively, and operate in basically the same manner as the standard multigrid switch S–1. The changes in the multigrid switches S–2 and S–3 are obvious from the drawings and are well understood in the art. Consequently, no further description of these multigrid switches is believed necessary.

Inverter I

Referring to FIG. 50, there is illustrated a block symbol of an inverter and also the details of the circuit within the block.

An inverter functions to produce an output signal having substantially the same wave shape as the input signal but of opposite polarity and with no appreciable time difference between the input signal and the output signal.

The inverter may employ, for example, a triode tube, the plate of which is connected via plate circuit resistance to a positive supply voltage. A positive signal applied to the grid of the tube causes an increased flow of current through the tube and plate circuit resistance. The voltage drop across the plate resistance due to the increased current causes the voltage at the plate to shift relatively negative. Consequently, since the output is taken from the plate circuit of the triode, a negative signal is produced in response to the positive input signal. Likewise, a negative shift on the grid will decrease the current through the plate resistance with a resulting positive potential at the plate. Consequently, a positive output signal is produced in response to the negative input signal.

The standard inverter (FIG. 50) which may comprise one triode of a dual triode 5965 type tube, has its grid connected via a 47 ohm resistor to an input terminal "5," and its cathode connected to ground. The plate is connected to an output terminal "7" and via a 20K ohm resistor to a +150 volt supply.

The standard inverter is hereinafter represented by a block containing the alphabetic character I followed by a numerical designation 1, *i.e.* I–1.

Inverters I–2 and I–3 are shown in FIGS. 51 and 52 and operate in basically the same manner as the standard inverter I–1. It is to be noted that inverter I–3 has its plate connected via a cathode follower CF–5 to the output terminal "7." It can thus be understood that inverter I–3 represents an inverter followed by a cathode follower. Since the cathode follower does not affect the logical operation of a circuit, but only the power of the signal, the combined unit may be used to reduce the size, and make for clearer description of the wiring diagram of FIGS. 8A to 8BB.

AND circuit &

Referring to FIG. 53, there is illustrated a block symbol of a standard diode AND circuit and also the details of the circuit within the block.

A positive diode AND circuit functions to produce a positive output signal only when there is a coincidence of positive signals at all of the input terminals thereof.

The positive diode AND circuit employs at least two diodes, the cathodes of which are connected to input terminals, while the anodes are connected to an output terminal and via a common resistor R to a positive voltage source. The input terminals are normally biased so that the diodes are in conductive states. It will be remembered that during conduction the resistance of a diode is negligible compared to that of the common resistor R. Consequently, the anodes are at potentials more nearly that of their respective cathodes. If a positive signal is applied to any of the input terminals, the diode to which the signal is applied is cut off as the cathode is now at a more positive potential than the corresponding anode. However, the remaining diode or diodes are still in a conductive state or states, so that the same amount of current flows through the common resistor R and the potential at the anode of the diode to which the positive input signal is applied, does not follow the change at the corresponding cathode but remains at relatively the same potential. Therefore, since the output terminal is connected to the anodes of the diodes, no change in potential is effectively passed to the output terminal when a positive signal is applied to any or all but one of the input terminals. If positive signals are coincidently applied to all of the input terminals, all of the diodes are cut off and the potential at the anodes starts to rise toward that of the positive voltage source connected at the other end of the common resistor R. When the potential reaches a value approximately that at the input terminals, all of the diodes start to conduct whereupon the potential at the anodes stops rising and is maintained at approximately that at the input terminals. Therefore, since the output terminal is connected to the anodes of the diodes, the rise in potential at the anodes is effectively passed to the output terminal so that the potential at the output terminal is raised to approximately that existing at all of the input terminals. It should be noted at this point that the positive input signals are not necessarily applied simultaneously to the input terminals of the positive diode AND circuit. Hence, in instances where positive signals are applied to all but one of the input terminals thereof, the circuit is said to be conditioned so that when a positive signal is applied to the remaining input terminal there is a coincidence of positive input signals causing the production of a positive output signal in a manner as previously described.

The standard positive diode AND circuit of FIG. 53 comprises at least two diodes (only two of which are shown), the anodes of which are commonly connected through a resistor R to a source of +150 volts. The cathodes are shown connected to input terminals "1" and "2," and the commonly connected anodes are connected to an output terminal "7."

Referring now to FIG. 56, there is illustrated a block symbol of a standard negative diode AND circuit and also the details of the circuit within the block.

A negative diode AND circuit functions to produce a negative output signal only when there is a coincidence of negative signals at all of the input terminals thereof.

The negative diode AND circuit employs at least two diodes, the anodes of which are connected to input terminals while the cathodes are connected to an output terminal and via a common resistor R to a negative voltage source. The input terminals are normally biased so that the diodes are in conductive states. Consequently, the cathodes are at potentials more nearly that of their respective anodes. If a negative signal is applied to any of the input terminals, the diode to which the signal is applied is cut off as the anode is now at a more negative potential than the corresponding cathode. However, the remaining diode or diodes are still in a conductive state or states so that the same amount of current flows through the common resistor R. Consequently, the potential at the cathode of the diode to which the negative input signal is applied, does not follow the change at the corresponding anode but remains at relatively the same potential and since the output terminal is connected to the cathodes of the diodes, no change in potential is effectively passed to the output terminal when a negative signal is applied to any but not all of the input terminals. If negative signals are coincidently applied to all of the input terminals, all of the diodes are cut off and the potential at the cathodes start to fall toward that of the negative voltage source connected at the other end of the common resistor R. When the potential reaches the value approximately that at the input terminals, all of the diodes start to conduct whereupon the potential at the cathodes stops falling and is maintained at approximately that at the input terminals. Therefore, since the output terminal is connected to the cathodes of the diodes, the fall in potential at the cathodes is effectively passed to the output terminal so that the potential at the output terminal falls to approximately that existing at all of the input terminals. It should be noted at this point that the negative input signals are not necessary applied simultaneously to the input terminals of the negative diode AND circuit. Hence in instances where negative signals are applied to all but one of the input terminals thereof, the circuit is said to be conditioned so that when a negative signal is applied to the remaining input terminal, there is a coincidence of negative input signals causing the production of a negative output signal in a manner as previously described.

The standard negative diode AND circuit of FIG. 56 comprises at least two diodes (only two of which are shown), the cathodes of which are commonly connected through a resistor R to a source of −250 volts. The anodes are connected to input terminals "1" and "2," and the commonly connected cathodes are connected to an output terminal "7."

The standard positive diode AND circuit is hereinafter represented by a block symbol containing an ampersand (&) followed by a numerical designation 1, i.e., &—1, while the standard negative diode AND circuit is hereinafter represented by the designation —&–1. It is to be understood that a positive and negative diode AND circuit may have any number of input terminals so long as a diode is provided between each input terminal and the output terminal. If there are more than two inputs required, leads connected to these inputs are shown in the wiring diagram of FIGS. 8A to 8BB as entering the left side of the block. In both the positive and negative diode AND circuits, the value of the common resistor R, which may vary according to circuit requirements, is indicated in the upper right-hand corner of the block.

Positive diode AND circuits &–2 and &–3 are shown in FIGS. 54 and 55 and operate in basically the same manner as the standard positive AND circuit &–1 of FIG. 53. It is to be noted that positive diode AND circuit &–2 has its common anode connected via a CF–4 type cathode follower to the output terminal "7." It can thus be understood that positive diode AND circuit &–2 represents a positive diode AND circuit followed by a cathode follower. Since the cathode follower does not affect the logical operation of a circuit, but only the power of the signal, the combined unit may be used to reduce the size, and make for clearer description of the wiring diagrams of FIGS. 8A to 8BB.

OR circuit—OR-TOR

Referring to FIG. 57, there is illustrated a block symbol of a standard positive diode OR circuit and also the details of the circuit within the block.

A positive diode OR circuit functions to isolate two or more positive input signals from each other and to produce a positive output signal in response to a positive input signal at any or all of the input terminals thereof.

The positive diode OR circuit employs at least two diodes, the anodes of which are connected to the input terminals thereof, while the cathodes are connected to the output terminal thereof and via a common resistor to a negative voltage source. The input terminals are normally biased so that the diodes are in conductive states. If a positive signal is applied to either or both of the input terminals, the potential at the anode or anodes to which the input signal or signals are applied, become more positive causing an increased flow of current through the common resistor. Consequently, since during conduction the resistance of a diode is negligible in comparison to that of the common resistor, the potential at the cathodes of those diodes to which the positive input signals are applied follows more nearly that of their respective anodes. Also, since the output terminal is connected to the cathodes of the diodes, the rise in potential at the cathodes is effectively applied to the output terminal so that the potential at the output terminal is raised to approximately that existing at any or all of the input terminals to which the positive input signals are applied.

The standard positive diode OR circuit of FIG. 57 comprises at least two diodes (only two of which are shown), the cathodes of which are commonly connected through a resistor R to a source of —250 volts. The cathodes are connected to input terminals "1" and "2," and the commonly connected anodes are connected to an output terminal "7."

The standard positive OR circuit is hereinafter represented by a block containing the alphabetic characters OR, followed by a numeric designation 1, i.e., OR–1. It is to be understood that a positive diode OR circuit may have any number of input terminals so long as a diode is provided between each input terminal and the output terminal. If there are more than two inputs required, leads connected to these inputs are shown in the wiring diagram of FIGS. 8A to 8BB as entering the left side of the block. The value of the common anode register R, which may vary according to circuit requirements, is indicated in the upper right-hand corner of the block.

Positive diode OR circuit OR–2 is shown in FIG. 58 and operates in basically the same manner as the standard positive diode OR circuit OR–1. It is to be noted that positive diode OR circuit OR–2 has its common cathode connected via a CF–4 type cathode follower to the output terminal "7." It can thus be understood that positive diode OR circuit OR–2 represents a positive diode OR circuit followed by a cathode follower. Since the cathode follower does not affect the logical operation of a circuit, but only the power of the signal, the combined unit may be used to reduce the size, and make for clearer description of the wiring diagrams of FIGS. 8A to 8BB. Referring now to FIG. 59, there is illustrated a block symbol of a standard triode OR circuit, and also the details of the circuit within the block.

A triode OR circuit functions to isolate two or more positive input signals from each other, and to produce a negative output signal in response to a positive input signal at any or all of the input terminals thereof.

The triode OR circuit employs at least two triodes, the grids of which are connected through circuitry to input terminals, while the plates are connected to an output terminal and via a common plate resistor to a positive voltage source. The grids are normally biased so that the triodes are in non-conductive states. If a positive signal is applied to either of the grids via the input terminals, the respective tube will conduct through the common plate resistor producing a voltage drop across said resistor which causes the potential at the plates and the output terminal to shift negative.

The standard triode OR circuit of FIG. 59 is hereinafter represented by a block symbol containing the alphabetic characters TOR and a numerical designation 1, i.e., TOR–1.

Clamping circuits CL

Referring to FIG. 63, there is illustrated a block symbol of a positive clamp or clamping circuit, and also the details within the block of the components and their connections.

A positive clamping circuit is a circuit which functions to hold the negative amplitude extreme of input waveform to a fixed reference level of potential. A clamping circuit usually couples two units when it is desired that the signals at the plate circuit of a tube in a first unit be transmitted to the grid of a tube in a second unit, and vary from the fixed reference level.

The positive clamping circuit employs one or more diodes in conjunction with the ordinary resistance-capacitance coupling circuit because in coupling between units, a coupling capacitor almost always must be used to keep the high positive D.C. plate potential of the first unit isolated from the grid of the second unit. The input signal of the positive clamping circuit is connected via the coupling capacitor to the cathode of a diode, the plate of which is connected to a D.C. reference level voltage. The output voltage is taken at the junction of the condenser and cathode. Any portion of the input signal more negative than the reference level will be shorted by the conduction of the diode, but the portions more positive than the reference level will be developed across a resistance shunting the diode. Thus any positive swing in the plate circuit of the previous unit is transmitted as a swing in the positive direction from the reference level.

The standard positive clamping circuit (FIG. 63) includes an input terminal "5" connected via a 0.01 microfarad condenser and a 470K ohm resistor to a supply of V volts. An output terminal "4" is connected to the junction of the 0.01 microfarad condenser and 470K ohm resistor, and the junction is also connected to the cathode of a diode which shunts the 470K ohm resistor.

Referring to FIG. 64, there is illustrated a block symbol of a negative clamping circuit.

A negative clamping circuit is a circuit which functions to hold the positive amplitude extreme of an input waveform to a fixed reference level of potentials. Thus, any negative swing in the plate circuit of a previous unit is transmitted by the negative clamping circuit as a swing in the negative direction from the reference level.

The negative clamping circuit employs the same components as the positive clamping circuit except that the connections to the diode or diodes are reversed.

The standard negative clamping circuit (FIG. 64) is similar to the standard positive clamping circuit (FIG. 63) except that the anode of the diode is connected to output terminal "4" and the cathode is connected to the supply of V volts.

It may be necessary, in order to help output signal shifts, to parallel two or more diodes of the clamp. Where this is done, the rest of the circuit remains unaffected.

The standard positive clamp is hereinafter represented by a block containing the alphabetic character CL followed by a numerical designation 1, i.e., CL–1, hereinafter represented by —CL–1. Where diodes in a clamp are connected in parallel, the number of diodes so connected as indicated by the number *n*, preceding the CL in the block diagram, for example, if there are two diodes connected in parallel in a negative clamp, the block is identified by the symbol —2CL–1. Further, the value of the voltage to which the circuit is clamped, which may vary according to circuit requirements, is indicated in the upper right-hand corner of the block.

Limiter circuits LI

Referring to FIG. 65, there is illustrated a block symbol of a limiter circuit, and also the details, within the block, of the components and their connections.

A limiter or clipper circuit is one which removes one extremity or the other of an input wave. A negative portion of the wave may be removed by cut-off limiting, and a positive portion of the wave may be removed by grid limiting. Both cut-off and grid limiting may be performed by one circuit.

Cut-off limiting makes use of the cut-off characteristics of a triode. With a given plate voltage, if the grid is made sufficiently negative with respect to the cathode, all electrons are repelled by it and are forced back to the cathode. No electrons reach the plate and so the plate current is zero. The smallest negative voltage between the grid and cathode which causes the tube to cease to conduct is called the cut-off bias. By clamping the lower level of an input waveform below the cut-off bias, only signals which are greater than the difference between the reference voltage and the cut-off bias will cause the triode to conduct. In this manner, these signals of larger amplitude are selected for transmission through the circuit.

This particular circuit also acts as a grid limiter circuit because it is adapted to remove the positive extremity of the input waveform and this provides for the pulses that pass through to be of no greater than a predetermined amplitude. When the signal at the grid is of a positive potential greater than the potential at the cathode, the resulting grid current causes a drop across the 330 ohm grid resistor and the 470K ohm resistor of the clamp in a direction which tends to counterbalance the positive swing, and the grid therefore will not go materially above the voltage of the cathode. Therefore, the voltage swings at plate will not go negative by more than a predetermined amount.

Referring now to FIG. 65, there is illustrated a standard limiter comprising a clamp and one triode of a 12AU7 type dual triode. The plate of the triode is connected via an 8.2K ohm resistor and a 10K ohm resistor and a 10K ohm resistor to a source of +330 volts. The junction of the 8.2 ohm resistor and 15K ohm resistor is connected via a 2 micromicrofarad condenser to ground. The plate is also connected directly to an output terminal "7." The cathode is connected via a 560 ohm resistor shunted by a 10 micromicrofarad condenser to ground. The grid is connected via a 330 ohm resistor and a 2CL–1 type positive clamp to an input terminal "5." The positive clamp has its reference voltage fixed at —60 volts. Since the cut-off potential of the triode is approximately —15 volts, a signal of greater than +45 volts is required in order to bring the grid above the cut-off. The signals of less than +45 volts will not be transmitted through the standard limiter.

The standard limiter circuit is hereinafter represented by a block containing the alphabetic characters LI followed by a numerical designation 1, i.e., LI–1.

Amplifier A

Referring to FIG. 66, there is illustrated a block symbol of an amplifier, and also the details of the circuit within the block.

An amplifier is a device consisting of one or more vacuum tubes and associated circuits, employed to increase the magnitude of a signal.

The well known inherent characteristics of certain vacuum tubes cause an input signal, applied to the grid, to produce a signal of greater magnitude (i.e. to be amplified) at the plate. The amplified signal may, when desired, be fed through successive amplifier stages for further amplification.

Referring now to FIG. 66, there is illustrated a standard three stage amplifier. Each stage comprises one triode of a 12AU7 type dual triode. The plate of the first stage triode is connected via an 8.2K ohm resistor and a 15K ohm resistor to a source of +330 volts. The junction of the 8.2K ohm and 15K ohm resistors is connected via a 2 micromicrofarad condenser to ground. The cathode is connected via a 10K ohm gain control potentiometer in series with the parallel connected 560 ohm resistor and 10 micromicrofarad condenser to ground. The grid is connected via a 330 ohm resistor and a —CL–1 type negative clamp to an input terminal "5." A negative signal applied to input terminal "5" will be operated on by the clamp so as to cause it to vary negatively relative to ground. This negative signal is then transmitted via the 330 ohm resistor to the grid of the first stage where it is amplified and appears as a larger positive signal at the plate of the first stage. This positive signal is fed via a CL–1 positive clamp, which causes it to vary positively with respect to ground, to a second stage which is similar in every way to the first stage except that there is no 10K ohm gain potentiometer in the cathode circuit. The positive signal is amplified and inverted, and the now negative signal is fed through a —CL–1 type clamp and a third stage which is exactly the same as the second stage. The output of the standard three stage amplifier is then a positive signal taken off the plate of the third stage at an output terminal "7."

The standard amplifier is hereinafter represented by a block containing the alphabetic character A followed by a numerical designation 1, i.e., A–1.

Photomultiplier PM

Referring to FIG. 67, there is illustrated a circle connected to a square, the combination comprising a block symbol of a photomultiplier. The details within the block of the components and their connections are also shown.

A photomultiplier, which includes a photomultiplier tube and associated circuitry, functions to produce an output signal proportional to the amount of light striking it.

The photomultiplier tube of the standard photomultiplier circuit contains a collector, a plurality of emitters having secondary emission characteristics, and a cathode made of material which emits a number of primary electrons proportional to the amount of light striking its surface. The primary electrons from the cathode are drawn to a first emitter, which is at a higher potential than the cathode and where, due to the secondary emission characteristics, secondary electrons are emitted. The secondary electrons and the reflected primary electrons are drawn to a second emitter where secondary emission also takes place. The process is repeated at successive anodes, each of which is at a higher potential than the preceding one. A collector then collects the electrons from the last emitter and feeds it to an output terminal. Since each electron may knock out five or more secondary electrons, and a large number of emitters are used, very high current amplification is obtainable.

The standard photomultiplier (FIG. 67) which includes a Dumont 6291 type photomultiplier tube has a collector C, a cathode K and nine emitters E. The collector C is directly connected to an output terminal "4" and via a 15K ohm resistor to ground. A source of —1000 volts is connected via a 10K ohm resistor to the cathode K, which is connected via a 0.001 microfarad condenser to ground. The cathode K is also connected via a bleeder network comprising an 82K ohm resistor, eight 100K ohm series connected resistors, and another 82K ohm resistor to ground. The first emitter is connected to the junction of the first 82K ohm resistor and its adjoining 100K ohm resistor, and each succeeding emitter is connected so that there is one 100K ohm resistor between adjacent emitters. Thus, each emitter is at a higher potential than the preceding emitter.

The standard photomultiplier is hereinafter represented by a circle having a curved line cathode and a straight line collector which is connected to a block containing the alphabetic characters PM followed by a numerical designation 1, i.e., PM–1.

Trigger T

Referring now to FIG. 68, there is illustrated a block symbol of a standard trigger and also the details of the circuit within the block.

A trigger, commonly known as the Eccles-Jordan trigger, functions as a storage or control device inasmuch as it is a bistable device, that is, one that remains in either one of two stable states until it is forced or triggered by an input signal to assume the other state, each subsequent input signal being effective to turn the trigger to the opposite state.

The trigger may comprise a cross-coupled dual triode, that is, the plate of the right-hand tube is resistively coupled via a voltage divider network to the grid of the left-hand tube, while the plate of the left-hand tube is resistively coupled via a voltage divider network to the grid of the right-hand tube. Therefore, any changes in potential at the plates of the dual triode are coupled to the grids of the opposite tubes. One stable state of the trigger is termed the Off state and exists when the right-hand tube is in a conductive state while the left-hand tube is in a non-conductive state. In this state, the plate of the right-hand tube is at a relatively negative potential while the plate of the left-hand is at a relatively positive potential. If the right-hand tube is triggered to a non-conductive state a positive shift of potential occurs at the plate thereof which is coupled via the voltage divider cross-coupling to the grid of the left-hand tube so that the left-hand tube is triggered to a conductive state with a resulting negative shift of potential occurring at the plate thereof. This is the other stable state of the trigger and is termed the On state. The trigger may also be set to the On state by triggering the left-hand tube to a conductive state with a resulting negative shift of potential occurring at the plate thereof, which is coupled via the voltage divider cross-coupling to the grid of the conducting right-hand tube so that the right hand tube is triggered to a non-conductive state. In a similar manner, when the trigger is in the On state, it may be reset back to the Off state by triggering the left-hand tube to conduct or the right-hand tube to stop conducting.

The standard trigger (FIG. 68) may comprise a 5965 type dual triode having its right-hand plate connected via a voltage divider network comprising a 150K ohm resistor and a 300K ohm resistor to a −250 volt source. The left-hand plate is connected via a similar voltage divider comprising a 150K ohm resistor and a 300K ohm resistor through normally closed reset cam contacts to a −250 volt source. The junction of the 150K ohm resistor and the 300 K ohm resistor in each voltage divider network is connected via a 300 ohm resistor to the respective grids of the dual triode. Additionally, a 39 micromicrofarad capacitor is connected in parallel with each of the 150K ohm resistors. Also, an input terminal "6" is connected to the left-hand junction while an input terminal "3" is connected to the right-hand junction. Each plate of the dual triode is connected via a 10K ohm resistor to a +150 volt source. Output terminal "7" is connected directly to the left-hand plate and output terminal "8" is connected directly to the right-hand plate.

The standard trigger is hereinafter represented by a block containing the alphabetic character T followed by a numerical designation 1, i.e., T–1. The trigger T–1 is never used directly, but rather is used with different input circuits of the type shown in the triggers T–2, T–3, and T–4 of FIGS. 69, 70, and 71 respectively. Trigger T–2 thus includes input terminals "6" and "3" respectively connected to the anodes of diodes, the cathodes of which are connected to the left and right-hand inputs respectively of a trigger T–1. The diodes are inserted in this manner to conduct when pulses by a positive input, to effect a triggering of T–2 by positive input pulses only. Triggers triggered by positive pulses are hereinafter referred to as positive input triggers and have this fact indicated by a (+) indication in the block under the trigger designation, i.e., trigger T–2 has a (+) indication under the designation T–2. Trigger T–3 is similar to trigger T–2 except that the connections to the input diodes are reversed so that the diodes will conduct when pulsed by a negative input to effect a triggering of T–3 by negative input pulses only. A (−) designation under the designation T–3 indicates that trigger T–3 is a negative input trigger.

Trigger T–4 is similar to trigger T–3 except that its input terminal "6" is connected via a 270-micromicrofarad condenser to the cathode of the input diode, and it has an additional left-hand input terminal "5" connected via a 270 micromicrofarad condenser to the anode of another input diode, the cathode of which is connected to input terminal "6" of a trigger T–1. A negative shift at terminal "5" or "6" is integrated and appears as a negative pulse to turn Off the trigger. A negative shift appearing at input terminal "3" will turn On the trigger even if the negative potential is still applied to terminal "5." However, if input terminal "3" remains negative, a negative shift at input terminal "6" will not turn the trigger Off. It thus becomes apparent that a condenser in the input circuit is provided to permit the trigger to change its state even while the potential which turned it to its present state is still being applied.

In all triggers, the opening of the reset cam contacts disconnects the path between a negative voltage and the right-hand grid causing a positive shift at the right-hand grid which resets the trigger Off. This reset operation is performed when the machine is turned On to place all the triggers in the Off condition.

Triggers T–5 to T–9 are shown in FIGS. 72 to 76 respectively and operate in basically the same manner as the triggers hereinbefore described. The changes in the triggers T–5 to T–9 are obvious from the drawings and are well understood in the art. Consequently, no further description of these triggers is believed necessary.

A.C. Input, A.C. AND, and A.C. OR circuits

Referring to FIG. 60, there is illustrated a block symbol of an A.C. Input circuit, and also the details of the circuit within the the block.

An A.C. Input circuit is used where it is desired to flip a trigger Off by a positive shift and still be able to flip the trigger back On with another puse even though the positive shift is still applied to the A.C. Input circuit.

In a resistance-capacitance differentiating circuit, the resistance and capacitance are connected to act as a voltage divider network, and thus the portion of the applied voltage which does not appear across the capacitor, will appear across the resistor. The time constant of the circuit is made short relative to the duration of the applied pulse in order that the capacitor will become charged in a small fraction of the pulse duration. Thus at the first instant, all the voltage drop is across the resistor, but in a very short time the capacitor is charged up and therefore, the voltage across the resistor and at the output of the A.C. Input circuit fall off very rapidly.

The output of the A.C. Input circuit is thus a very sharp pulse that is usually fed to a trigger to turn it Off. Since the voltage at the output of the A.C. Input circuit does not remain positive, further pulses fed to the input of the trigger can turn it On even though the input pulse to the input circuit remains positive.

Thus, the standard A.C. Input circuit of FIGURE 60 has an input terminal "2" connected via an R.C. differentiating network consisting of a 220-micromicrofarad condenser in series with a 10K ohm resistor to a source of −35 volts. The junction between the resistor and condenser is connected to the anode of a diode, the cathode of which is connected to the output terminal "7."

The A.C. Input circuit is hereinafter represented by a block symbol containing the alphabetic characters A.C. Input.

Referring to FIG. 61, there is illustrated a block symbol of an A.C. AND circuit, and also the details of the cir-

cuit within the block. An A.C. AND circuit is used where it is desired to flip a trigger Off by a coincidence of a plurality of positive shifts and still be able to flip the trigger back On with another pulse even though the plurality of positive shifts is still applied to the A.C. AND circuit. The standard A.C. AND circuit of FIG. 61 is an &–3 type AND circuit feeding an A.C. Input circuit.

The A.C. AND circuit is hereinafter represented by a block symbol containing the characters A.C. &.

Referring to FIG. 62, there is illustrated a block symbol of an A.C. OR circuit, and also the details of the circuit within the block. An A.C. OR circuit is used where it is desired to flip a trigger Off by any one or more of a plurality of positive shifts and still be able to flip the trigger back On with another pulse even though the one or more of the positive shifts is still applied to the A.C. OR circuit. The standard A.C. OR circuit of FIG. 62 is an OR–1 type OR circuit feeding an A.C. Input circuit.

The A.C. OR circuit is hereinafter represented by a block symbol containing the characters A.C. OR.

Free-running multivibrator MV

Referring to FIG. 77, there is illustrated a block symbol of a standard free-running multivibrator, and also the details of the circuit within the block.

A free-running multivibrator functions to produce nearly rectangular pulses of a specified (and sometimes adjustable) duration. The free-running multivibrator resembles a standard trigger in that it has two states, but differs in that it oscillates at one frequency between the two states due to its own internal circuitry.

The free-running multivibrator may comprise a cross-coupled dual triode, that is, the plate of the right-hand tube is capacitively coupled to the grid of the left-hand tube, while the plate of the left-hand tube is capacitively coupled to the grid of the right-hand tube. Resistors connected from the grid of each tube to ground in combination with the coupling condensers comprise an RC network which is used to control the time duration of the trigger in each stage. When the left-hand tube is conducting, the coupling capacity between the left-hand plate and the right-hand grid charges through the right-hand grid resistance causing the potential at the grid of the right-hand tube to rise toward a relatively positive value. At some positive value the right-hand tube begins to conduct and switching action takes places causing the left-hand tube to turn off. The frequency of the multivibrator may be varied by simultaneously varying the grid resistance of each tube.

Thus the standard free-running multivibrator of FIG. 77 may comprise a 5965 type dual triode. Plate P1 of the left-hand triode is coupled via a 39 micromicrofarad condenser, in series with a 470 ohm resistor to the grid G2 of the right-hand triode, while plate P2 of the right-hand triode is coupled via a 39 micromicrofarad condenser, in series with a 470 ohm resistor to a grid G1 of the left-hand triode. Connected between ground and the junction of each 39 micromicrofarad coupling condenser and 470 ohm resistor are a 500K ohm potentiometer in series with a 39K ohm resistor. Each plate is connected through a 10K ohm resistor to a source of +150 volts, and the cathodes K1 and K2 are commonly connected to ground. The plate P2 of the right-hand tube is connected to a right-hand terminal "8." For the purpose of the invention, the frequency of the free-running multivibrator may be set to 100 kc. by varying the two 500K ohm potentiometers.

The free-running multivibrator is hereinafter, represented by a block symbol containing the alphabetic characters MV and a numeric designation 1, i.e., MV–1.

Single shot multivibrator SS

Referring now to FIG. 78, there is illustrated a block symbol of a standard single shot multivibrator, the details of the circuit within the block, and a chart of the different values of resistance and capacitance in an RC network for the different time duration of the signal developed by the multivibrator.

A single shot multivibrator functions to produce positive and/or negative rectangular wave shaped signals of predetermined time duration.

The single shot multivibrator resembles the standard trigger in that it may be triggered to the On state by an input signal, but differs therefrom in that it automatically returns to the Off state after a predetermined period of time without requiring a subsequent input signal.

The single shot multivibrator may comprise a cross coupled dual triode, that is, the plate of the left-hand tube is capacitively coupled via a voltage divider network to the grid of the right-hand tube, while the plate of the right-hand tube is resistively coupled to the grid of the left-hand tube. A capacitor between the left-hand plate and the right-hand grid is connected through a resistor to a source of positive voltage and this resistor and condenser comprise an RC network that is used to control the time duration of the On state of the single shot multivibrator. The grids of the dual triode are so biased that the single shot multivibrator is normally in the Off state, that is, with the left-hand tube in its non-conductive state and the right-hand tube in a conductive state. If a negative shift of potential is applied via the input circuit to the grid of the right-hand tube, switching action occurs, as in the standard trigger, and the single shot multivibrator is set to the On state, with a resulting negative shift of potential occurring at the plate of the left-hand tube, and a positive shift of potential occurring at the plate of the right-hand tube. The single shot multivibrator remains in the On state for a period of time dependent upon the time constant of the RC network associated with the grid of the right-hand tube. The capacitance of the RC network, connected to the grid of the right-hand tube starts to charge through its associated resistance causing the potential at the grid of the right-hand tube to rise toward a relatively positive value. At a certain positive value, the right-hand tube begins to conduct once more and switching action takes place causing the single shot multivibrator to be reset back to the Off state. The time duration of the On state of the single shot multivibrator can be varied by varying the values of the resistance and capacitance in the RC network connected to the grid of the right-hand tube.

The standard single shot multivibrator of FIG. 78 may comprise a 5687 type dual triode. Plate P1 of the left-hand triode is coupled via a condenser C in series with a 470 ohm resistor to the grid G2 of the right-hand triode, while plate P2 of the right-hand triode is coupled via a 100K ohm resistor, shunted by a 22 micromicrofarad condenser, in series with a 470 ohm resistor to a grid G1 of the left-hand triode. Connected between −100 volts and the junction of the 100K ohm resistor and 470 ohm resistor is a 100K ohm resistor. The junction between the condenser C and the 470 ohm resistor is connected via a 22 micromicrofarad condenser to an input terminal "3," and also via a resistor R to a source of +220 volts. Each plate is connected through a 4.7K ohm resistor to a source of +150 volts, and the cathodes K1 and K2 are commonly connected to ground. The plate P2 of the right-hand tube is connected to a right-hand output terminal "8," while the plate P1 is connected to an output terminal "7."

The single shot multivibrator is hereinafter represented by a block symbol containing the alphabetic characters SS and a numeric designation 1, i.e., SS–1. The time duration of the On state of single shot multivibrator SS–1 depends on the values of resistor R and condenser C. FIG. 56 contains a chart indicating the different values of resistor R and condenser C for particular time duration *t*. The time duration *t* is indicated in the drawings at the lower left-hand corner of the single shot multivibrator blocks.

Single shot multivibrator SS–2 is shown in FIG. 79 and operates in basically the same manner as the single shot

multivibrator hereinbefore described. The changes in single multivibrator SS–1 are obvious from the drawings and are well understood in the art. Consequently, no further description of this single shot multivibrator is believed necessary.

Binary counter CTR

Referring now to FIG. 80, there is illustrated in the block symbol of standard binary counters and also the details of the circuit within the block.

The binary counter may comprise one or more trigger stages, each of which have commonly connected inputs, and each of which reverses between its two stable states each time a new input signal is introduced. A single trigger so connected may thus act as a "2" counter, i.e., one that produces a carry pulse after two input pulses. Since the right-hand output of a trigger goes positive when the trigger is On, the presence of a positive potential on the right-hand plate of the trigger, and a negative potential on the left-hand plate of the trigger indicates that one pulse has been applied to the "2" counter. The right-hand plate is therefore labeled 1 to indicate that it is positive after one input pulse, while the left-hand plate is labeled $\bar{1}$ (not one) to indicate that it is negative after one input pulse. At the end of two pulses, the "2" counter returns to its initial state, emitting a carry pulse from its output terminal.

The binary "2" counter of FIG. 80 comprises a T–6 type negative input trigger having its two input terminals commonly connected to an input terminal "IN." The left-hand output terminal of the T–6 trigger is connected to a terminal $\bar{1}$ and the right-hand output terminal of the T–6 trigger is connected to the output terminals 1 and "OUT."

The standard binary "2" counter is hereinafter represented by a block containing the alphabetic characters CTR, preceded by a "2" and followed by a numerical designation 1, i.e., "2"CTR–1. The type of input pulse (+) or (—) necessary to operate the counter is shown in parenthesis under the block label.

Binary "2" counters "2"CTR–2 and "2"CTR–3 are shown in FIGS. 81 and 82 respectively, and operate in basically the same manner as the standard binary "2"CTR–1. The binary "2"CTR–3 which is a counter based on a T–9 type trigger has an additional electronic reset terminal "RE" connected to the input terminal "4" of the trigger.

To obtain counts of greater than two binary "2" counters may be connected in cascade by connecting the output terminal of each stage to the input terminal of the succeeding stage. The counts which may be obtained by the counter can be recognized by the number in quotes preceding the alphabetic characters CTR in the block. At the end of two pulses, when the first stage goes from an On, back to an Off condition, the carry pulses from the first stage will cause the second stage to go On. The right-hand plate of the second stage is labeled 2 to indicate that it is positive after two input pulses to the binary counter and the left-hand plate of the second stage is labeled $\bar{2}$ to indicate that it is negative after two input pulses. On the third input pulse, the first stage is turned On, and both output terminals 1 and 2 are positive. On the fourth input pulse, the first stage is turned Off, which in turn, turns the second stage Off creating a carry pulse. Where there is a third stage, it is turned On, and its righthand terminal 4 will be positive. Now it is clear that a "4" binary counter emits a carry pulse after four input pulses and also indicates the number of input pulses, by the status of the output terminals of each stage. The number designating the right-hand output terminal of each stage may then be considered the weighted value of that stage. The weighted value of each stage in a binary counter is always twice as much as that of the previous stage. Thus, to determine the number of input pulses applied to a counter from the last time it was reset to zero, it is only necessary to add the weighted value of the stages in the On condition.

The counter "4"CTR–1 (FIG. 83) comprises two cascaded "2"CTR–1's to provide weighted value indications up to the count of four and a carry pulse at the count of four. The counter "32"CTR–1 (FIG.84) comprises five cascaded "2"CTR–1's to provide weighted value indications up to the count of thiry-two and a carry pulse at the count of thirty-two.

To obtain a carry pulse at a count other than that of the normal carry pulse from the last counter stage, it is possible to connect the input terminals of an AND circuit to the right-hand output terminals. The AND circuit will then only provide an output when all the triggers to which the AND circuit are connected are On. This output will come at a time which can be determined by the sum of the weighted values of the stages connected to the AND circuit.

The counter "3"CTR–3 (FIG. 85) provides a carry pulse at the end of seven input pulses and comprises two stages of cascaded "2"CTR–3 type counters, the input terminals of the first stage being connected to the counter input terminal "IN." The right-hand output terminals of the two stages having weighted values of 1, 2, are connected to the input terminals of an &–3 type AND circuit, the output terminal of which is connected to the counter output terminal "OUT." The reset terminals of all the stages are commonly connected to the counter electronic reset terminal "RESET."

The counter "4"CTR–3 (FIG. 86) provides a carry pulse at the end of four input pulses and comprises three stages of cascaded "2"CTR–3 type counters. The 4 weighted output lead of the third stage is connected to the counter output terminal "OUT."

FIGS. 87, 88, 89 illustrate respectively a "5"CTR–3, a "6"CTR–3 and an "11"CTR–3. The input connections to the &–3 type AND circuits (the outputs of which are the output terminals "OUT") are similar to that of the "3"CTR–3 of FIG. 85 but are made to the properly weighted outputs of the counter stages. These connections are obvious from the drawings and no further description will be given.

Peaker PKR

Referring to FIG. 90, there is illustrated a block symbol of a peaker, and also the details of the circuit within the block.

A peaker functions to produce an output pulse of very short duration and with an extremely sharp leading edge. The function performed by a peaker may be accomplished by a multitude of circuit arrangements.

One standard type of peaker utilizes a resistance-capacitance differentiator input feeding to what is effectively a power inverter. In a resistance-capacitance differentiator circuit, the resistance and capacitance are connected to act as a voltage divider network, and thus the portion of the applied voltage which does not appear across the capacitor, will appear across the resistor. The time constant of the circuit is made short-relative to the duration of the applied pulse in order that the capacitor will become charged in a small fraction of the pulse duration. Thus at the first instant, all the voltage drop is across the resistor, but in a very short time the capacitor is charged up and therefore, the voltage across the resistor falls off very rapidly. The output at the resistor is thus a very sharp pulse that is fed to the power inverter which inverts the polarity of the pulse and gives it greater power.

The standard peaker (FIG. 90) includes a 5965 type dual triode. The left-hand grid G1 is connected to a junction on a bleeder network comprising a 390K ohm resistor connected to —100 volts, and a 75K ohm resistor connected to ground. The grid G1 is also connected via a 100 micromicrofarad condenser to an input terminal "9." The two plates P1 and P2 are commonly connected to an output terminal "3" and also via a 390 ohm resistor in series with a 560 ohm resistor to a +150 volt supply.

The left-hand cathode K1 is connected via a 100K ohm resistor, a −100 volt supply, and also to the right-hand grid G2. The right-hand cathode K1 is connected directly to ground. Due to the bleeder network, the grid of the left-hand tube is kept at approximately −17 volts which is enough to keep the left-hand tube cut off. The cathode of the left-hand tube will therefore be at a negative potential because it is tied via the 100K ohm resistor to −100 volts. Since the cathode of the left-hand tube is connected to the grid of the right-hand tube, the right-hand grid is negative too, and the right-hand triode is cut off. The capacitance of the resistance-capacitance differentiator is the 100 micromicrofarad input capacitor, and the resistance includes the two cathode to grid resistances in series in the path from ground through the cathode K2, cathode K1, and grid G1. A positive going input pulse applied via the 100 micromicrofarad capacitor to the grid G1 will cause the left-hand tube to conduct. The cathode K1 follows the grid G1 and goes positive causing the grid G2, to which it is tied, to go positive. The right-hand tube then conducts and since the only external resistance in the circuit of the right-hand tube are the two low plate resistors, the right-hand tube conducts heavily. The 100 micromicrofarad condenser charges through a path from ground via the cathode K2 to grid G2, and via cathode K1 to grid G1. Since this is a low resistance path, the 100 micromicrofarad capacitance charges very rapidly until −17 volts appear at the right-hand plate at which point the tube has been cut off, as previously indicated. The effect is a very short pulse of high power in the plate circuit.

The standard peaker is hereinafter represented by a block containing the alphabetic characters PKR followed by a numerical designation 1, i.e. PKR–1.

Power inverter PW

Referring to FIG. 91, there is illustrated a block symbol of a power inverter, and also the details of the circuit within the block.

A power inverter functions to produce an output signal having greater power than the input signal. The power inverter is no more than a special inverter inasmuch as the output signal is of opposite polarity and has substantially the same waveshape as the input signal.

A power inverter however, generally employs a pentode tube, and circuitry which provides a greater current flow than is normally obtained in an inverter with consequent increase in power.

The standard power inverter (FIG. 91), which includes a 6AQ5 type pentode tube, has a grounded cathode and a suppressor grid directly connected to the cathode. The screen grid SG is connected via a 470 ohm resistor to a source of +150 volts. The plate, which is directly connected to an output terminal "3," is connected via a 3K ohm resistor to +150 volts. The grid G1 is connected through a 47K resistor, in series with a 330K resistor to a −100 volt negative bias supply. Grid G1 is coupled through the same 47K resistor, in series with a 390K ohm resistor shunted by a 100 micromicrofarad condenser to an input terminal "9."

The standard power unit circuit is hereinafter represented by a block containing the alphabetic characters PW followed by a numerical designation 1, i.e., PW–1.

Core driver CD

Referring now to FIG. 92, there is illustrated a block symbol of a standard core driver, and also the details of the circuit within the block.

A core driver is a circuit which provides current to a core winding of sufficient magnitude to cause the core to assume a predetermined state, more fully described presently.

A standard core driver may comprise a pentode having its plate connected to an output terminal which is externally connected through a core winding or windings to a positive D.C. voltage source. The application of a positive pulse to the grid will cause the core driver tube to conduct through the external core winding.

The standard core driver (FIG. 92) which comprises a pentode 6AU6 type tube, has its cathode and suppressor grid commonly connected through a 560 ohm resistor to ground, its screen grid SG connected to a source of +150 volts, and its grid G1 connected via a 330 ohm resistor to an input terminal "5." The plate is directly connected to an output terminal "7."

The standard core driver is hereinafter represented by a block containing the alphabetic characters CD followed by a numerical designation 1, i.e., CD–1.

Core driver CD–2 is shown in FIG. 93 and operates in basically the same manner as the standard core driver CD–1. The changes in the core driver CD–2 are obvious from the drawings and are well understood in the art. Consequently, no further description of this core is believed necessary.

Relay driver RD

Referring now to FIG. 94, there is illustrated a block symbol of a standard relay driver and also the details of the circuit within the block.

A relay driver is a circuit which provides the current required for energizing a relay upon the application of a positive input pulse.

A standard relay driver may comprise a triode having its cathode connected to ground and its plate connected to an output terminal which is externally connected through a relay to a positive D.C. voltage source. The application of a positive pulse to the grid will cause the relay driver tube to conduct through the external relay causing the energization thereof.

The standard relay driver (FIG. 94), which comprises one triode of a dual triode 5687 type tube, has its cathode connected to ground and its plate directly connected to an output terminal "4." The grid is connected via a 330 ohm grid resistor to a junction on a divider network comprising a 390K ohm resistor connected to a −100 volt supply and a 560K ohm resistor, shunted by a 22 micromicrofarad condenser, connected to an input terminal "8."

It may be necessary for current carrying reasons to operate two or more relay drivers in parallel. This may be accomplished by commonly connecting the plates and commonly connecting the cathodes. Each grid is then connected via its own 330 ohm grid resistor to a common point, and where there is a bleeder network input in the single relay driver, the common point is connected to the junction of the resistor in the bleeder network.

The standard relay driver is hereinafter represented by a block containing the alphabetic characters RD followed by a numerical designation 1, i.e., RD–1. Where relay drivers are connected in parallel, the number of relay drivers so connected is indicated by the number *n* preceding the RD in the block diagram, for example, if there are two standard relay drivers connected in parallel, the block is identified by the symbol 2RD–1.

Relay driver *n*RD–2 is shown in FIG. 95 and operates in basically the same manner as the standard relay driver *n*RD–1. The changes in the relay driver *n*RD–2 are obvious from the drawings and are well understood in the art. Consequently, no further description of this relay driver is believed necessary.

Deflection unit DU and deflection stage DE

Referring now to FIG. 97, there is illustrated a block diagram of a deflection unit containing deflection stage blocks and associated circuitry. FIG. 96 illustrates the standard deflection stage block, the details of the components and connections within the block, and a chart of the number of tubes and the value of cathode resistance for the different variations of the standard block.

A deflection unit is a circuit which may be utilized for deflecting the beam of a cathode ray tube, and functions

to provide a control of the voltages at its two output terminals for use by a pair of cathode ray tube deflection plates.

The deflection unit consists of a series of deflection stages, each of which comprises at least one dual triode. The left-hand triode of a deflection stages is normally conducting and the right-hand triode is normally not conducting. The deflection stage can be energized so as to start the left-hand triode conducting and cut off the right-hand triode.

A deflection unit is comprised of a plurality of deflection stages, each of which can provide twice as much current as its previous stage. This permits the input of each stage to be connected to respective right-hand output terminals of a binary counter, which, as has been previously described, have stages the outputs of which go positive according to their weighted values. Thus, as the counter is stepped by input pulses and produces voltage conditions at its outputs representative of the number of input pulses, the respective inputs of the deflection stages are energized so that an amount of current flows through the left-hand triode of the deflection stages proportional to the number of pulses applied to the counter. Thus, when the first counter stage produces an output, the first stage of the deflection unit provides a unit amount of current through the left-hand triode to cause a deflection of one unit. Then when the second counter stage is On, the second stage of the deflection unit provides two units of current to cause a deflection of two units, etc.

The standard deflection stage (FIG. 96) which comprises a dual triode 5965 type tube, has its cathodes commonly connected via a cathode resistance R to a source of —250 volts. The left-hand grid G1 is connected via a 330 ohm resistor to the anode of a diode, the cathode of which is connected to an input terminal "5." The junction of the 330 ohm resistor and the diode is connected via a 10K ohm resistor to ground. The right-hand grid G2 is connected via a 330 ohm resistor to the junction of the resistors of a bleeder network comprising a source of —250 volts connected via a 270K ohm resistor and a 15K ohm resistor shunted by a 0.01 microfarad to ground. The left-hand plate P1 is directly connected to an output terminal "6" and the right-hand plate P2 is directly connected to an output terminal "7."

The standard deflection stage is hereinafter represented by a block containing the alphabetic characters DE followed by a numerical designation *n*, i.e., DE–*n*. The value of *n* is the weighted value of the deflection stage. The value of the cathode resistance R for the different deflection stages are shown in the chart of FIG. 96. It is to be noted that as the weighted value *n* of the deflection stage doubles the cathode resistance R approximately halves, providing double the current carrying capacity.

The standard deflection unit (FIG. 97), comprises five deflection stages with commonly connected left-hand output terminals and commonly connected right-hand output terminals. The commonly connected left-hand output of the deflection stages are connected through a 1500 ohm resistor to +250 volts, and the right-hand output of the deflection stages are commonly connected via a 1591 ohm resistor to the +250 volt source. The commonly connected left-hand outputs are also connected via two 10K ohm resistors in series to the commonly connected right-hand outputs. An output terminal "6" is connected to a tap on the 10K ohm resistor that is connected to the commonly connected left-hand terminals, and an output terminal "7" is connected to a tap on the 10K ohm resistor connected to the commonly connected right-hand output terminals. Initially, since all the right-hand triodes are conducting, and the left-hand triodes are not conducting, the right-hand plates are at a negative potential with respect to the left-hand plates and therefore, output terminal "7" of the deflection unit is negative with respect to the output terminal "6." As the left-hand triodes are caused to conduct by the operation of the counter stage, more and more current is caused to flow through the 1500 ohm resistor lowering the voltage at the commonly connected left-hand plates and the output terminal "6," and raising the voltage at the output terminal "7." Due to the nature of the binary counter action, it is obvious that the voltage at terminal "6" goes down in step-wise fashion while the voltage at output terminal "7" goes up in synchronism in step-wise fashion.

The standard deflection unit is hereinafter represented by a block containing the alphabetic characters DU followed by a numerical designation 32. This deflection unit is capable of producing a 32 step deflection of the cathode ray ray tube.

Magnetic core shifting register SR

Referring to FIG. 99, there is illustrated a block symbol of a standard core shifting register and also the details of the circuit within the block.

A magnetic core shifting register functions to store a bit of binary information in each stage thereof and is provided with means for shifting the binary information from each stage to its succeeding stage when externally pulsed.

The magnetic core shifting register may employ a plurality of magnetic cores, each of which has a shift winding, an input winding, and an output winding. The cores, magnetizable to either of two stable states, have remanent flux either clockwise or counterclockwise within the cores. Ordinarily, the value of remanent flux in either direction, referred to as retentivity, is substantially equal. Remanent flux is established in one direction to represent a binary one and in the opposite direction to represent a binary zero. For the purposes of the present invention, a current pulse applied to a shift winding changes the core if in the One state to the Zero state; whereas a current pulse through the input winding, if sufficient in magnitude, changes the core if in the Zero state to the One state. The magnetic state of a core is transferred to the succeeding core by a transfer circuit which is energized when a core changes its magnetic state from One to Zero in response to a shift pulse. If a core is in the One state when a shift pulse is applied, the output winding serves to energize the transfer circuit which establishes the One state in the succeeeding magnetic core; if a core is in the Zero state when a shift pulse is applied, the transfer circuit is not energized and the succeeding magnetic core remains in the Zero state.

Before describing a standard core shifting register, a description will be given of FIG. 98 which illustrates an idealized hysteresis loop of commercially obtainable magnetic core material. Points A and E are stable remanent states further adapted for representing binary information, and a core may be driven to either of these states by the application of a positive or negative magnetomotive force respectivly. If the state or remanence of a core of such material is that indicated by the point A, application of a positive magnetomotive force greater than the coercive force causes it to traverse the hysteresis curve to point C, and upon relaxation of this positive force, revert to point A. Application of a negative magnetomotive force greater than the coercive force causes curve to be traversed to point D, and when the force is terminated, traversed to point E. Similarly, when the remanence state of the core stands at point E, the application of a negative magnetomotive force causes the curve to be traversed to point D and returned to point E when the negative force is relaxed; while a positive force greater than the coercive force causes the traversal of the curve from point E to point C and return to point A when the positive force is terminated.

The standard magnetic core shift register of FIG. 99 may comprise sixteen magnetic core stages, only the first two and last two of which are shown. A write terminal is connected to the input of a CF–1 type core

driver unit, the output of which is connected through an input winding I to a +150 volt source. A shift terminal is connected through the parallel combination of a 270K ohm resistor and a 1000 micromicrofarad condenser to a source of −30 volts. The shift terminal is also connected to the input of two CD–2 type core drivers, one of which is connected through the series connected shift windings S of the first eight core stages to +220 volts and the other of which is connected through series connected shift windings S of the last eight core stages to +220 volts. A circuit in each core stage is completed from ground through the output winding O to a transfer circuit *t*. The contents of transfer circuit *t* is shown between the first and second core stages. The output winding O is connected to the anode of a diode D1, in the transfer circuit *t*, the cathode of which is connected to a junction point *b*, and through a 1000 micromicrofarad condenser to ground. The junction point *b* is also connected through a 4.7K ohm resistor and a 10 milihenry inductance out of the transfer circuit to the input winding I of the succeeding stage to ground. There is a transfer circuit *t* between each of the core stages.

The output winding O the fifteenth stage is also connected via a 1000 micromicrofarad condenser and a 10K ohm resistor to a source of −30 volts. An output terminal "15" is connected to the junction of the 1000 micromicrofarad condenser and 10K ohm resistor.

The output winding O of the last stage is connected to the anode of a diode, the cathode of which is connected to the parallel combination of a 4.7K ohm resistor and a 100 micromicrofarad condenser to ground. The anode of the diode is also connected through a 1000 micromicrofarad condenser and a 10K ohm resistor to a source of −30 volts. An output terminal "16" is connected to the junction of the 1000 micromicrofarad condenser and the 10K ohm resistor.

With the state of remanence indicated at point A on the curve in FIG. 98 arbitrarily selected as representing a binary One and the state or remanence indicated at point E as a binary Zero application of a negative magnetomotive force, by pulsing a shifting winding S on the Stage 1 magnetic core, simultaneously causes a voltage to be induced on the output windings O of the Stage 1 core if it previously was in the One state; while a negligible voltage is induced in these output windings if the core was in the Zero state. If the Stage 1 core is in the One state when a negative magnetomotive force is applied, the resulting voltage induced on the output winding O establishes current flow through the diode D1 to charge the 1000 micromicrofarad condenser in the transfer circuit *t* between Stage 1 and Stage 2. Simultaneously, the voltage on each of the output windings O establishes current flow through their respective diodes to charge the 1000 micromicrofarad condensers. As soon as the shift pulse terminates, the charge on the upper plate of the 1000 micromicrofarad condenser discharges through the 4.7K ohm resistor, the 10 millihenry inductance and the input winding I of the Stage 2 core to ground. This positive magnetomotive force established in the Stage 2 core by the discharge current through the Stage 2 input winding I changes the magnetic state of this core from that indicated at point E on the curve in FIG. 98 to that state indicated at point A. Thus, the binary One previously stored in the Stage 1 magnetic core is transferred to the Stage 2 magnetic core in response to the first shift pulse. Thus, it can be understood that each shift pulse applied to the shift terminal will shift all the bits of information to its succeeding stage, leaving the Stage 1 core in a Zero state and providing an output at terminals "15" and "16" which are representative of what the states of Stage 15 and Stage 16, respectively, had been. Write pulse may be applied to the write terminal between shift pulses and thus provide the information for the Stage 1 magnetic core.

The standard magnetic core shift register is hereinafter represented by a block containing the alphabetic characters SR followed by a numerical designation 1, i.e., SR–1.

5 bit counter

A block representation of a conventional 5 bit counter is shown in FIG. 100. This circuit accepts a sequence of input pulses at the IN terminal and provides a binary-coded sum indication at output terminals 2^0, 2^1, 2^2, 2^3, and 2^4. The circuit is thus capable of counting 11111 (decimal 31).

The 5 bit counter comprises five counters of the

"2"CTR–3(+)

type which have been described with respect to FIG. 82. The counter is reset to "0" by a signal at the RE terminal. Input signals are applied to the left-most counter and every second signal restores the stage to its initial (reset) status and produces an input signal which is applied to the next adjacent counter. In the same manner, the successively higher-order counters are controlled and their output signals represent a count of the applied input signals.

7 bit counter

A conventional 7 bit counter is shown in FIG. 101. This circuit operates in the same manner as the 5 bit counter described above with respect to FIG. 100, except that two additional stages are provided to extend the counting range to 1111111 (decimal 127).

Multiple AND—&4

The circuit shown in FIG. 102 contains a group of AND gates of the &–3 type which are under the simultaneous control of a single gate signal. Data is applied on separate leads in the IN cable to the separate AND gates. This data is supplied on separate leads in the OUT cable during the time that a conditioning signal is present on the GATE lead.

5 bit register

FIG. 103 shows a conventional buffer register comprising triggers of the T–8(+) type. The register is reset by a signal on the RESET lead. The data to be stored is momentarily applied on the IN leads to control the status of the triggers which store the data, making it available on the OUT leads until the circuit is again reset or over-riding data is applied.

Divider—input/4

The circuit shown in FIG. 104 provides output data which has a value equal to one quarter of the value of the input data. This is accomplished by simply relabelling the leads with indicia that are lower by two binary orders of magnitude (e.g., since $2^9/4=2^7$, the 2^9 lead is relabelled 2^7). The two lowest order input leads are not used.

Scanner

A description will now be given of the preferred embodiment of the invention, the block circuitry being shown in FIGS. 8A to 8BB, and the timing of the electronic signals in the block circuitry being shown in FIGS. 37A to 37I. A multivibrator **200** (FIG. 8B) is used as a parent source of square waves having a ten microsecond period. These square waves are transmitted through a Space multi-grid switch **202** and a Punch multi-grid switch **204** to the input of a "4" counter **206**. Waveform (*a*) of FIGS. 37A to 37I shows the square waves at the input to "4" counter **206**. The operation of the Space multi-grid switch **202** and the Punch multi-grid switch **204** will be described hereinafter.

Every fourth pulse into the "4" counter **206** produces a negative output shift, i.e., one every forty microseconds at its output. The output which is shown as waveform (*b*) of FIGS. 37A to 37I is fed via a lead **208**, a cathode

follower 210, and a lead 211 to a "32" counter 212. The 1, 2, 4, 8 and 16 terminals of the "32" counter are each connected via cathode followers 214, 215, 216, 217, and 218, respectively, to the terminals 1, 2, 4, 8, and 16, respectively, of a DU–32 type vertical deflection unit 220. The two outputs of the vertical deflection unit 220 are connected via leads 222 and 224 to the upper and lower vertical deflection plates. The vertical carry pulse from 225 (FIG. 8A). As has been previously described, the combination of a "32" counter and a DU–32 type deflection unit acts to produce a "32" step waveform at the vertical deflection plates. The vertical carry pulse form the "32" counter 212 (FIG. 8B) is transmitted via a lead 226, a cathode follower 228, and a vertical carry lead 229 to a "32" counter 230. The "32" counter 230 is connected in a manner similar to the "32" counter 212 to a horizontal deflection unit 232, the two outputs of which are connected via leads 234 and 236 to the left and right horizontal deflection plates respectively of cathode ray tube 225 (FIG. 8A). The combination of the "32" counter 230 and the horizontal deflection unit 232 acts to produce a "32" step waveform to the horizontal deflection plates of the cathode ray tube 225. The height of the total vertical deflection is controlled by varying the 10K ohm taps (see FIG. 97) in the deflection unit 220 and the width of the total horizontal deflection is controlled by varying the 10K ohm taps in deflection unit 232.

The waveforms in FIGS. 37A to 37I are plotted against time from the start of the first vertical scan at the first bit from the bottom to the end of the thirty-second vertical scan at the last bit from the bottom. The bits have been identified by two numbers and a letter, the first number representing the horizontal position and the second number, the vertical position. Since there are thirty-two vertical bits, and only every other one, i.e., sixteen bits, have been found necessary for adequate recognition, the vertical bits have been numbered up to 16 and have been suffixed alternately by a letter *a* or *b*. The suffix *a* bits are the ones used in the recognition system, while the suffix *b* bits are ignored, as will be presently described. For example, the 18 in the notation 18–16*a* represents the eighteenth vertical column to the right of the first scan and the 16*a* represents the thirty-first bit from the bottom, but the sixteenth bit used.

The cathode ray tube 225 (FIG. 8A) which is used as a source of the moving light spot, has its cathode 238 directly connected to a source of —2300 volts. The accelerating anodes 240 and 242 are connected to a source of +330 volts, and the focusing anode 244 is connected to a 10 megohm potentiometer, which in turn is connected between —2300 volts and ground. The control grid 246 is ordinarily at a more negative potential than the cathode 238. When the control grid 246 goes positive, however, the cathode ray tube 225 is unblanked to produce a light spot on its fluorescent screen. The negative output shift of the "4" counter 206 (FIG. 8B), is fed through the output lead 208 and the cathode follower 210 and lead 211 to the right-hand input of an unblank trigger 250. A positive shift appears on the right-hand output of trigger 250 (waveform (*d*) of FIG. 37) and is applied via lead 252 to the input of a power inverter 254 (FIG. 8A). The output of the power inverter is connected through a 0.015 microfarad condenser through an unblank lead 256 to the control grid 246. Lead 256 is connected to the cathode of a diode 258, the anode of which is connected to a source of —2400 volts. A 1 megohm resistor is shunted across the diode 258. Ordinarily, —2400 volts is applied via the 1 megohm resistor directly to the conrtol grid 246 to prevent the conduction of the cathode ray tube 225. However, when the output of the power inverter 254 goes positive, this positive pulse is applied via the 0.015 microfarad condenser and lead 256 to the control grid 246 to unblank the electron beam and cause a spot of light to fall on the fluorescent screen of the cathode ray tube 225. The discharge time of the 0.015 microfarad condenser and the 1 megohm resistor is relatively slow and so the 0.015 microfarad condenser does not discharge before the positive potential at the output of the power inverter 254 is removed. The same pulse from the "4" counter 206 (FIG. 8B) which turned on trigger 250 via lead 211 is applied to a single shot 260 having a 10 microsecond duration. The waveform (*e*) of FIG. 37 appears at the output of single shot 260 and the negative shift at the end of 10 microseconds is applied to a single shot multivibrator 262 having a 5 microsecond duration positive output (i.e., waveform (*f*) of FIG. 37). Five microseconds after the input pulse, the output of single shot 262 goes negative (a total of 15 microseconds after the unblank trigger 250 is turned On) and the negative pulse is fed via a lead 263 to turn Off unblank trigger 250 and end the unblank pulse (waveform *d*). The five microsecond positive pulse is also applied via lead 263 and a cathode follower 264 to a sample lead 265. The use of the 5 microsecond sample pulse on lead 265 will be described hereinafter.

The unblank pulse permits a spot of light to appear on the surface of the cathode ray tube 225. The spot of light is focused by a suitable lens 266 on to a document 268 upon which are shown a plurality of characters to be recognized. The particular embodiment shown in FIGS. 8A to 8BB contemplate the use of a carriage 270 of a standard electric typewriter 272 to move the document. The carriage 270 is stationary for a period of thirty-two vertical sweeps at which time it is caused to space in a well known manner. The height of the total sweep on the document may be adjusted in a manner previously described, so as to sweep an area as high as the height of the tallest character. (Where all the characters to be read are of the same height, the height is adjusted so that the character is thirteen bits high in the sixteen bit scan.) The width of the total sweep is adjusted so that the first vertical sweep after spacing will occur one horizontal position to the right of the last vertical sweep before the spacing, thus providing for a continuous series of vertical sweeps across the entire line. As will be shown presently, the determination of end of character and beginning of new character takes place independently of the spacing. Thus, it is obvious that the same results could be obtained by moving the document continuously and vertically sweeping in the same horizontal position over the moving document.

At the end of the thirty-second vertical sweep, a negative horizontal carry (waveform *g* of FIGS. 37A to 37I) from the horizontal sweep counter 230 (FIG. 8B) is applied via a lead 274 to a 30,000 microsecond (30 millisecond) single shot 276 (FIG. 8A). For 30 milliseconds a positive pulse (waveform *h*) is applied via a lead 278 to energize a relay driver 280 which causes current to flow through a lead 282 and Space relay 284 to actuate a standard space bar 286 to space the carriage 270 in any well known manner. Simultaneously, the negative shift on the lead 274 is applied to a half second single shot multivibrator 288 which goes On to apply a positive shift (waveform *i*) via lead 290 to the Space multi-grid switch 202 via an OR circuit 292 and its output lead 294. The positive shift at the grid of the Space multi-grid switch prevents any multivibrator pulses from passing through. FIG. 37I (waveform *i*) indicates that at the end of the 32 vertical sweep there is a one half second delay to allow time for spacing during which time the multivibrator pulses (waveform *a*) are not permitted to pass through to counter 206.

When the carriage has reached it extreme left position, a member 296 (FIG. 8A) moving with the carriage, closes stationary contacts 298 to complete a circuit from +150 volts to the input of an inverter 300. The negative resulting output is applied via a lead 302 to a single shot multivibrator 304 which remains On for 30 milliseconds to apply a positive potential via a lead 306 to a relay

driver **308**. Relay driver **308** conducts through lead **310** and relay **312** to energize said relay which actuates a carriage return key CR to move the carriage to the beginning of the next line in any well known manner. Simultaneously, the negative output voltage from inverter **300** is applied via lead **302** to a single shot multivibrator **314** which remains On for one second to apply a positive potential to the positive OR circuit **292** which prevents the multivibrator pulses from passing through to counter **206** during a carriage return operation.

As has been previously described, it is necessary to shift the marking register, make a black-white determination, and then write the results of the determination into the first stage of the marking register. To get the proper timing to perform these three functions in sequence, the outputs of the second stage of the "4" counter **206** is utilized. The output of terminal 2 of counter **206** (waveform *b* of FIGS. 37) is fed via a lead **314** and a cathode follower **316** to a peaker **318**. The positive shift, every forty microseconds, causes a negative peaked output every forty microseconds as shown in waveform *j* of FIGS. 37A to 37I. This negative peaked output is fed via a cathode follower **320** to a shift 1 line **322**. The output of terminal "2" of counter **206** (waveform *c* of FIGS. 37) is fed via a cathode follower **324** to a peaker **326** where its positive shift causes a negative peaked output every forty microseconds (waveform *k*) which is fed via a cathode follower **328** to a shift 2 line **330**. Since every time the output of terminal "2" of counter **206** goes positive, the output of terminal "$\bar{2}$" goes negative and vice versa, the pulses will appear on the shift 1 and shift 2 lines **322** and **330** alternately.

The light spot reflected off the document **268** (FIG. 8A) is collected by a pair of photomultiplier tubes **332** and **334** where it is converted to an electrical video pulse and fed via lead **336** to an amplifier **338**. The amplified video signal is fed to an LI–1 type limiter **340** which, as previously described, will only allow signals of magnitude of greater than +45 volts to pass through as a negative pulse. Since a white area will reflect more light than a black area, only white indications will cause a signal of over +45 volts to be applied to the limiter **340**. The discrimination level need not be fixed at +45 volts but may be adjusted by means of a potentiometer dependent upon the particular document's black to white ratio. The negative pulse representing a white area is then applied via a negative clamp **342** and a cathode follower **344** to an inverter **346**, the output of which is a positive video pulse which is applied via a cathode follower **348** and a lead **350** to a multi-grid switch **352**. The positive video pulse representing white on lead **350** is shown in waveform *l* (FIGS. 37A to 37I) as a pulse of 15 microseconds which is the length of the unblank pulse. The other input to multi-grid switch **352** is the sample lead **265** carrying the 5 microsecond positive sample pulse (waveform *f*) starting 10 microseconds after the start of the video pulse on lead **350**. The resulting output of multi-grid switch **352** is a negative pulse, shown in waveform *m*, which is fed to the left-hand input of a trigger **354**, turning it Off. Trigger **354** is turned On by the shift 1 pulse on the shift 1 lead **322** which is connected to the right-hand input of trigger **354**. Since the shift 1 pulse appears 10 microseconds after the turning Off of the trigger **354**, a 10 microsecond negative pulse appears at the right-hand output of trigger **354** (waveform *n*) and this negative pulse representation of white is fed via a cathode follower **356** to sampled video lead **358**.

The negative shift of the vertical carry on lead **229** (FIG. 8B) (waveform *o*), previously described, is fed to a single shot multivibrator **360**, the output of which is then a negative end of vertical scan pulse of 5 microseconds (waveform *p*) which is fed via a cathode follower **362** to an end of vertical scan lead **364**.

Control circuits

The control circuit, shown in FIG. 8C, includes marking register control, reset, and black-white determination circuits. The marking register control circuits include circuits for developing a register shift signal, a register write signal, and register read out triggers reset signal.

To develop the register shift signal, the shift 1 lead **322** (FIG. 8B) is fed to a negative AND circuit **366** (FIG. 8C), the other input of which is an OK to Punch lead **368**. The OK to Punch lead **368** is negative at all times except at the end of character when the result of the recognition process is fed to a punch output unit, as will be more fully described hereinafter (see waveform *q*, FIGS. 37A to 37I). This negative output is fed to a "2" counter **370** which acts as a frequency divider. The output wave of terminal "1" of counter **370**, which is shown in waveform *s*, is fed via a lead **372**, cathode follower **374** and a lead **376** to one input of a negative AND circuit **378**. The other input of negative AND circuit **378** is the shift 2 lead **330**. Since lead **376** from the terminal "1" of the "2" counter **370** will be negative only during every other negative shift 2 pulse, a negative output will be obtained from negative AND circuit **378** every 80 microseconds which is half the frequency of the shift 2 pulses. The output of the negative AND circuit **378** is fed to a single shot multivibrator **380** which then feeds a 2 microsecond positive pulse via a cathode follower **382** to a register shift lead **384** (waveform *t*). Since only every other shift 2 pulse causes a pulse on the register shift lead **384**, only 16 register shift pulses will occur for every 32 shifts of the beam in a vertical scan.

The register write signal is designated to occur between the register shift signals. The output pulse from terminal "$\bar{1}$" of the "2" counter **370** (waveform *r*) is fed via a lead **386**, the cathode follower **388** and a lead **390** to a negative AND circuit **392**. The other input of the negative AND circuit **392** is the shift 2 lead **330**. A negative output will be obtained from negative AND circuit **392** every 80 microseconds which is at half the frequency of the shift 2 pulses and will occur between the register shift pulses because the terminal "1" output of "2" counter **370** is negative when the terminal "$\bar{1}$" output is positive. This negative pulse is fed to a single shot multivibrator **394** which emits a two microsecond positive pulse that is fed via a cathode follower **396** to a register write lead **398** (waveform *u*).

The register write lead **398** is connected to the input of a single shot multivibrator **404**. The output of single shot multivibrator **404** is one microsecond positive pulse (waveform *v*) which is fed via a cathode follower **406** to a register read out trigger reset lead TP, and is utilized to reset the register read out triggers immediately following a write pulse, and to initiate the operation of the recognition criteria rules circuit.

As has been previously described, the bit sensed by the photocells is considered the "next" black-white determination. Thus, a pulse will appear on sampled video lead **358** when a white bit is sensed by the photocells. Once again, in order to utilize only every other sampled video bit, lead **376**, upon which appears waveforms from the "2" counter **370**, is fed to one input of a negative AND circuit **410**, the other input of which is the sampled video lead **358**. A negative pulse on the sampled video lead **358** will be passed through the output of negative AND circuit **410** to indicate a white bit and the pulse is fed via a lead **412** to the left-hand terminal of a negative black-white "next" trigger **414**. Thus, a white bit sensed will cause the black-white "next" trigger **414** to turn Off. This trigger is cam reset Off before the start of operation and in the Off position it indicates a white "next" bit. The register shift lead **384** is connected to the right-hand input of black-white "next" trigger **414**, and the negative trailing edge of the register shift pulse

(waveform *t*) thereon causes the black-white "next" trigger **414** to be set On. If the sampled video pulse (waveform *n*) indicates white, the black-white "next" trigger will be turned Off to signify white when interrogated by a timing pulse, but if there is no white sampled video pulse, the black-white "next" trigger will remain black when interrogated by the timing pulse. The output terminal "$\overline{1}$" of black-white "next" trigger **414** (waveform *x*) connected via a cathode follower **416** and a lead **418** to one input of a positive AND circuit **420**. The output terminal "1" of trigger **414** (waveform *w*) is connected via a cathode follower **422** and a lead **424** to one input of a positive AND circuit **428**. The other inputs of AND circuits **420** and **428** are connected to lead **376** which carries waveform *s*. When the lead **376** goes positive it acts as a timing pulse to transmit a positive shift through only one of the two AND circuits **420** or **428**. If the black-white "next" trigger **414** is Off, the lead **418** is positive, and a positive shift is transmitted via AND circuit **420** and a cathode follower **430** to a white "next" lead $\overline{B}_N$ (waveform *y*). However, if the black-white "next" trigger **414** is On, the lead **424** is positive, and a positive shift is fed via AND circuit **428** and a cathode follower **434** to a black "next" lead B_N (waveform *z*). The black "next" lead B_N is fed to a black-white determination cable **438** which feeds to the recognition criteria rules circuits in a manner to be more fully described hereinafter.

Since it is obvious that the black-white "next" determination becomes the black-white "now" determination when a new determination is made, means for shifting the "next" determination from the black-white "next" trigger **414** to a black-white "now" trigger will now be described. The output terminal "$\overline{1}$" of black-white "next" trigger **414**, which is positive when black-white "next" trigger **414** is in the white condition, is connected via the cathode follower **416** and the lead **418** to one input of a positive AND circuit **440**. The output terminal "1" of black-white "next" trigger **414**, which is positive when black-white "next" trigger **414** has sensed black, is connected via the cathode follower **422**, and the lead **424** to one input of a positive AND circuit **442**. The other inputs of AND circuits **440** and **442** are connected to the register shift lead **384**. When register shift lead **384** goes positive, it will transmit a positive shift through only one of the two AND circuits **440** and **442**. If the black-white "next" trigger **414** is in the white "next" condition, the lead **418** is positive and a positive shift is transmitted via AND circuit **440** to the right-hand input of a black-white "now" trigger **444**. Thus, a white "next" bit will be transmitted by the positive shift of the register shift pulse to cause the black-white "now" trigger **444** to turn Off. This trigger is cam reset off before the start of operation and in the Off position it indicates a white "now" bit. When the black-white "next" trigger **414** is in the black "next" condition, the register, shift pulse on lead **384** will pass through AND circuit **442** to the left-hand input of black-white "now" trigger **444** turning it On if it is Off. The output terminal "1" of black-white "now" trigger **444** (waveform *bb*) is connected via a cathode follower **450** to one input of an AND circuit **452**. The output terminal "1" of black-white "now" trigger **444** (waveform *aa*) is connected via a cathode follower **446** to one input of an AND circuit **448**. The other inputs of AND circuits **448** and **452** are connected to lead **376** which carries waveform *s*. When lead **376** goes positive, it will transmit a positive shift through only one of the two AND circuits **448** and **452**. If the black-white "now" trigger **444** is Off, the output of cathode follower **446** is positive, and a positive shift is transmitted via AND circuit **448** and a cathode follower **454** to a white "now" lead $\overline{B}$ (waveform *cc*). However, if the black-white "now" trigger **444** is On, the output of cathode follower **450** is positive and a positive shift is fed via AND circuit **452** and a cathode follower **456** to a black-white "now" lead B (waveform *dd*). Both black "now" lead B and white "now" lead $\overline{B}$ are fed to the black-white determination cable **438** to feed the recognition criteria rule circuits. Leads $\overline{B}$ and $\overline{B}_N$ are also connected to the inputs of an AND circuit **458**, where they are "anded" and the output is connected via cathode follower **459** to a lead $\overline{B}.\overline{B}_N$ (waveform *ee*) which is also connected into the black-white determination cable **438**. This lead $\overline{B}\overline{B}_N$ is fed to the recognition criteria rule circuits for convenience in detecting a minimum white area, as will be described hereinafter.

It is to be noted that in FIG. 37A at the beginning of operation the black-white "next" trigger **414** and the black-white "now" trigger **444** are reset off so that each of their terminals "$\overline{1}$" are positive. When the register shift lead **384** (waveform *t*) goes positive, the white condition in the black-white "next" trigger **414** is shifted to the black-white "now" trigger **444**, but since trigger **444** is in the white condition, it is not effected. Then, when the register shift lead **384** goes negative, the black-white "next" trigger **414** is turned On, making its terminal "1" positive.

It is to be noted in FIG. 37A that at 1–1*a* and 1–1*b* time, waveform *l* on video lead **350** goes positive indicating a white area was sensed by the photocells. The white "next" indication of 1–1*a* time will cause the white "next" lead $\overline{B}_N$ (waveform *y*) to go positive while the white "next" indication of 1–1*b* time is ignored. This can be more readily observed by noting that at 1–3*a* time, waveform *l* on video lead **350** goes positive while at 1–3*b* time waveform *l* remains negative indicating a black area was sensed by the photocells. The white indication of 1–3*a* time causes the white "next" lead $\overline{B}_N$ to go positive and the black indication at 1–3*b* time is ignored. At 1–4*a* time, waveform *l* indicates a black area and at 1–4*b* time, a white area. This time the black "next" indication of 1–4*a* time causes the black "next" lead B_N to go positive and the white "next" indication of 1–4*b* time is ignored. Black-white "next" trigger **414** may also be turned On by the register shift pulse on the register shift lead **384** Off and by a pulse on the end of vertical scan lead **364**. Thus, at the beginning of each 80 microsecond bit period, the register shift pulse turns On the black-white "next" trigger **414**. The trigger **414** will then indicate black "next" unless turned Off by a white sampled video pulse on lead **358**.

At the end of the vertical scan, certain triggers in the recognition criteria rule circuits must be reset. To develop the reset pulses, the end of vertical scan lead **364** is connected to one input of a negative AND circuit **460**, the other input of which is the OK to Punch lead **368**. As previously described, the OK to Punch lead **368** is negative at all times except at the end of character. The negative shift on lead **364** (waveform *p*) at the end of vertical scan is fed via negative AND circuit **460** to turn on single shot multivibrator **462** for five microseconds. The output of single shot multivibrator **462** is a five microsecond positive pulse which is fed via a cathode follower **464** to a reset lead X_s of a reset cable **465** where it appears as waveform *ff*.

At the end of five microseconds, the lead X_s goes negative and this negative pulse if fed to a single shot multivibrator **468** which is turned On for five microseconds. The resulting five microsecond positive pulse is fed from the output of single shot multivibrator **468** via a cathode follower **470** to a reset lead X_{sd} (waveform *gg*). Both leads X_s and X_{sd} are fed via a reset cable which is fed to the program rule circuits.

To determine an end of character, there must be one complete vertical scan without the presence of a black bit. A positive trigger **474** is reset Off at the end of every vertical scan by the X_{sd} reset pulse on reset lead X_{sd} which is connected to its right-hand input. The left-hand input is connected to black "next" B_N from black-white determination cable **438**, and if at any time during a vertical scan black "next" lead B_N goes positive, trigger **474** will be

set On. The left-hand output of trigger **474** is connected via a lead **475** to one input of a positive AND circuit **476**, the other input of which is reset lead X_{sd}. The output of positive AND circuit **476** is connected to the left-hand input of an End of Character trigger **478**. In order for a positive X_{sd} pulse to pass through AND circuit **476** to turn On the End of Character trigger **478**, trigger **474** must be in the Off condition so that **475** is positive. Thus, if during a vertical scan a black "next" bit is sensed, trigger **474** will be turned On and prevent the X_{sd} pulse from turning On the End of Character trigger **478**. After an all white bit vertical scan, End of Character trigger **478** is turned On, and a positive shift is fed from its output via a cathode follower **480** to the OK to Punch lead **368**. The positive OK to Punch shift on lead **368** is fed to a relay driver **482** (FIG. 8Z) causing it to conduct through an OK to Punch relay R30 to +150 volts. This energizes OK to Punch relay R30 closing its contact R30–1 to complete a circuit from a punch line terminal **484** (FIG. 8BB) of a Punch **486**, a lead **487**, closed contact R30–1, the selected Christmas tree shape decoder contacts to one of the alphabetic or numeric character terminals of the Punch (FIG. 8BB). This Punch may be of the type shown in the patent to Gardinor, 2,647,581, or of any well known type where the completion of the circuit to one of the terminals causes the characters selected to be punched and/or printed on a card. Any other output medium may be used. When the punching operation is over, a positive Punch Done pulse is fed via a Punch Done lead **488** to the right-hand input of End of Character trigger **478** (FIG. 8C), turning it Off. The Punch Done pulse may be obtained by the closing of contacts by a cam in a well known manner. A negative shift appears on the output of End of Character trigger **478** and is transmitted via the cathode follower **480**, causing the OK to Punch positive pulse on lead **368** to end. The lead **368** is also connected to the input of single shot multivibrator **490** which is turned On transmitting a positive pulse via a cathode follower **492** to an End of Character reset lead X_c. The X_c is connected to the Reset Cable **465**.

The vertical carry lead **229** (FIG. 8B) is connected to the right-hand input of a Punch negative trigger **496** lead X_{sd} is connected to the input of an inverter **498** (FIG. 8B), the output of which is connected to the left-hand input of Punch trigger **496**. At the end of each vertical scan, Punch trigger **496** is turned on by the negative shift of the vertical carry (see FIGS. 37A to 37I, waveform *o*) and turned Off 10 microseconds later by the reset pulse X_{sd} which causes a negative shift (waveform *gg*) at the output of inverter **498** and left-hand input of punch trigger **496** (waveform *ll*). After the first all white vertical scan, further reset pulses are blocked by the OK to Punch pulse on lead **368**. This is accomplished because OK to Punch lead **368** is connected to the input of negative AND circuit **460** (FIG. 8C) and remains postiive to block the end of vertical scan pulse on leads **364** from creating reset pulses. The OK to Punch lead **368** is also connected to negative AND circuit **366**, where it prevents negative shift 1 pulse on lead **322** stepping the "2" counter **370**. Counter **370** remains in the condition where its terminal "1" output is negative until a Punch Done pulse is received. This permits normal register shift pulses on lead **384** as previously described. However, the terminal "$\overline{1}$" remains positive and prevents the shift 2 pulses on lead **330** from generating register write pulses on lead **398** and register read out trigger reset pulses on lead TP. This has the effect of shifting the marking register through a complete vertical scan cycle without writing therein which effectively causes the marking register to be reset during the vertical scan following the all white bit scan.

Marking register, code and decode circuits

The marking register **500** (FIG. 8D) comprises three 16 position shift registers **502**, **504** and **506**. The shift terminal of each of the shift registers is connected to the register shift lead **384** and each shift register is thus shifted in synchronism by the register shift pulse (waveform *t*). Each of the shift registers is given a weighted value; shift registers **502**, **504** and **506** having weighted values 1, 2 and 4 respectively. The same numbered stage of each of the three shift registers, taken together, may thus represent any number from zero to seven according to a binary 1–2–4 code. In order to illustrate the binary code, numbers from zero to seven are shown with their binary coded representations in Table 1 below. The binary coded representations for each number is shown in terms of the presence or absence of the three weighted digits 1, 2 and 4, and X indicating the presence, and no X indicating the absence of the weighted digit.

TABLE 1

	Binary Coded		
	1	2	4
Zero			
One	X		
Two		X	
Three	X	X	
Four			X
Five	X		X
Six		X	X
Seven	X	X	X

The One state of a core in each shifting register may indicate the presence of the weighted digit and the Zero state may indicate the absence thereof.

For example, in the sixteenth stage of the marking register a five may be represented by the One state in the sixteenth stage of the 1 weighted shift register **502**, a Zero state in the sixteenth stage of the 2 weighted shift register **504**, and a One state in the sixteenth stage of the 4 weighted shift register **506**. In order to utilize the information in the sixteenth stage, the sixteenth stage outputs of shift registers **502**, **504** and **506** are connected respectively to the left-hand inputs of the sixteenth stage register read out triggers **508**, **510** and **512**, weighted 1, 2 and 4 in that order.

To utilize the information in the fifteenth stage, the fifteenth stage outputs of shift registers **502**, **504** and **506** are connected respectively to the left-hand inputs of the fifteenth stage register read out triggers **514**, **516** and **518**. The right-hand inputs of the triggers in both the fifteenth and sixteenth register stage read out triggers are commonly connected to the register read out trigger reset lead TP. A register read out trigger reset pulse on lead TP resets all the register read out triggers Off. Thirty-eight microseconds later (see FIG. 37A) the register shift pulse on lead **384** causes a shift of the bits to the next stage. Assuming again that there is a five being shifted in to the sixteenth stage, the sixteenth stage of the weighted 1 and the weighted 4 shift registers **502**, and **506**, respectively are placed in the One state turning the weighted 1 and weighted 4 sixteenth stage register triggers **508** and **512** On, and leaving the 2 weighted trigger **510** Off.

The output of the sixteenth stage register read out triggers **508**, **510** and **512** are leads which represent the presence or absence of a weighted one, two and four. The right-hand output lead of sixteenth stage register read out triggers **508**, **510** and **512** represent the present of 1, 2 and 4 respectively, and are labeled leads Read 1, 2, and 4 respectively. The left-hand output leads represent the absence of 1, 2 and 4 respectively and are labeled leads Read $\overline{1}$, $\overline{2}$ and $\overline{4}$ respectively. These six register trigger output leads are fed into a "now" Read cable **524** and thence to a "now" Decode circuit **526**. The "now" Decode circuit **526** is provided to convert the binary coded output on the Read leads into the one out of eight code. The one out of eight code, used in the recognition criteria rule circuits, is just the use of one lead for each of the eight numbers; the presence of the number being represented by a positive potential on that lead. The

"now" Decode circuit **526** comprises a plurality of AND circuits **527** to **534** inclusive, each of which has three inputs, one from each of the sixteenth stage register read out triggers **508**, **510** and **512**. AND circuits **527** to **534** inclusive are respectively connected via cathode follower **535** to **542** inclusive respectively, to one out of eight coded leads IN0 to IN7 inclusive. The one out of eight coded leads IN0 to IN7 inclusive, are fed into a rule circuit "now" input cable **550**. Only one of the AND circuits **527** to **534** will have all its inputs positive at any one time and therefore, only one of the one out of eight coded leads IN0 to IN7 will be positive. For example, a five in the sixteenth stage register read out triggers causes the Read 1, $\overline{2}$, and 4 output leads to go positive. And circuit **529** is the only one which has all three inputs positive. A positive shift results at the output of AND circuits **529** which is applied via cathode follower **537** to the IN5 lead in the rule circuit "now" input cable **550**.

The output of the fifteenth stage register read out triggers **514**, **516** and **518** have their right-hand leads representing the presence of 1, 2 and 4 respectively and are labeled leads Read 1_N, 2_N, and 4_N respectively. The left-hand output leads represent the absence of the 1, 2 and 4 respectively and are labeled leads Read $\overline{1}_N$, $\overline{2}_N$ and $\overline{4}_N$ respectively. The six fifteenth stage register trigger output leads are fed into a next read cable **552** and thence to a next decode circuit **54**. The next decode circuit **554** is provided to convert the binary coded outputs in the next read cable **552** into a one out of eight code, and operates in a manner similar to that described for the now decode circuit **526** (FIG. 8D). The one out of eight coded leads $IN0_N$ through $IN7_N$ inclusive are fed into a rule circuit next input cable **556**.

A rule circuit output cable **558** (FIG. 8E) coming from the recognition criteria rule circuits contains seven leads OUT 1 to OUT 7, inclusive, which are connected to the different inputs of an Encode circuit **564**. The leads OUT 1 to OUT 7 inclusive in the Rule Circuit Output Cable **558** contain one out of eight coded information which is converted by the Encode circuit **564** into binary coded information which is to be fed into the first stage of the marking register **500** (FIG. 8D). Coming out of the right-hand side of the Encode circuit **564** (FIG. 8E) are three leads **565**, **566** and **567**, weighted 1, 2 and 4 respectively, which are respectively fed to one of the input terminals of AND circuits **568**, **569** and **570** respectively.

The three leads **565**, **566** and **567** can contain binary coded information because the presence of a positive potential on any lead of the leads **565**, **566** and **567** indicate the presence of its weighted value, while presence of a negative potential indicate the absence of the weighted value. A five would thus be represented by a positive voltage on weighted 1 lead **565**, a negative voltage on weighted 2 lead **566**, and a positive voltage on weighted 4 lead **567**. The other inputs of AND circuits **568**, **569** and **570** are commonly connected to the register write lead **398**. The outputs of AND circuits **568**, **569** and **570** are leads Write 1, 2 and 4 respectively which are connected via write cable **572** to the write inputs of shift registers **502**, **504** and **506** respectively. Forty microseconds after the register shift pulse, a register write pulse is applied to register write lead **398** and if any of the leads **565** to **567** inclusive are positive, a positive pulse will appear on the respective output lead Write 1, Write 2 and Write 4 and cause the writing of a 1, 2 and 4 respectively into the first stage of the respective shift registers. Thus, in the case of the coded five, a positive on the 1 and 4 weighted leads **565** and **567** and a negative on 2 weighted lead **566** would put the first stage of shifting registers **502** and **506** in a One state, and leave the first stage of shifting register **504** in a Zero state.

In the Encode circuit **564**, OUT 1 lead in the Rule Circuit Output Cable **558** (FIG. 8E) is conencted via an OR circuit **574**, a lead **576**, a cathode follower **578**, an OR circuit **580**, and a cathode follower **582** to the 1 weighted lead **565**. The OUT 2 lead in the Rule Circuit Output Cable **558** is connected via an OR circuit **584**, a lead **586**, a cathode follower **588**, an OR circuit **590**, and a cathode follower **592** to the 2 weighted lead **566**. The OUT lead 4 in the Rule Circuit Output Cable **558** is connected via an OR circuit **594**, a lead **596**, a cathode follower **598**, an OR circuit **600**, and a cathode follower **602** to the 4 weighted lead **567**. Since the OUT 1 lead from the Rule Circuit Output Cable **558** is connected only to OR circuit **574** of the three OR circuits **574**, **584** and **594**, a positive potential on the OUT 1 lead from the Rule Circuit Output Cable **558** will cause only the 1 weighted lead **565** to go positive, similarly, the OUT 2 lead from the Rule Circuit Output Cable **558** will cause only the 2 weighted lead **566** to go positive, and the OUT 4 lead from the Rule Circuit Output Cable **558** will cause only the 4 weighted lead **567** to go positive. The OUT 3 lead from the Rule Circuit Output Cable **558** is connected to both OR circuits **574** and **584** to cause positive outputs on both the 1 and 2 weighted leads **565** and **566** in accord with the code indicated in Table 1. The OUT 5 lead from the Rule Circuit Output Cable **558** is connected to OR circuits **574** and **594** to cause positive outputs on both the 1 and 4 weighted leads. The OUT 6 lead from the Rule Circuit Output Cable **558** is connected to OR circuits **584** and **594** to cause positive outputs on both the 2 and 4 weighted leads, and the OUT 7 lead is connected to OR circuits **574**, **584** and **594** to cause positive outputs on the weighted 1, 2 and 4 weighted leads.

If none of the leads in the Rule Circuit Output Cable **558** is positive, then the number in the sixteenth stage of the marking register **500** will be automatically written into the first stage. The leads **576**, **586** and **596** are all connected to the input of an OR circuit **604**. If any of the leads OUT 1 to OUT 7 inclusive from the Rule Circuit Output Cable **558** go positive, then at least one of the leads **576**, **586** and **596** will be positive. Thus, if any of the leads OUT 1 to OUT 7 inclusive from the Rule Circuit Output Cable **558** go positive, a positive shift will be applied to the inverter **606** and cause the lead **608** connected to the output of inverter **606** to go positive. Lead **608** is connected to one of the inputs of each of the AND circuits **610**, **611** and **612**. The other input of AND circuit **610** is connected to the lead Read 1 from the sixteenth stage register read out triggers and the output is connected via OR circuit **580** and cathode follower **582** to the 1 weighted lead **565**. The other inputs of AND circuits **611** and **612** are connected to the leads Read 2 and Read 4 respectively from the sixteenth stage register read out triggers and the respective outputs are connected to the 2 and 4 weighted leads **566** and **567**, respectively. Thus, if any of the leads OUT 1 to OUT 7 from the Rule Circuit Output Cable **558** are positive, lead **608** is negative and all the AND circuits **610**, **611** and **612** are deconditioned. If none of the leads OUT 1 to OUT 7 are positive, then lead **608** is positive and positive potential on leads Read 1, Read 2 and Read 4 representative of the "now" bits in the sixteenth stage triggers, are transmitted through the Encode circuit **564** to leads **565**, **566** and **567**, respectively, for application to the leads Write 1, Write 2 and Write 4 into the first stage of the marking register **500**.

Recognition criteria rule circuits and examples

FIGS. 12 through 31 show examples of the recognition of different imperfect alphabetic and numeric characters as performed by the subject machine. FIG. 12 represents the numeric character 0 within a rectangle **614**, followed by the numeric characters 1 and 2 within rectangles **615** and **616** respectively. Each vertical scan is numbered, for ease of description, by numbers 1 through 32, placed above the rectangles **614**, **615** and **616**, and the horizontal bit positions of each scan is indicated by the numbers 1 through 16. Each cross, in the rectangle **614**, making

up the numeric character 0, being representative of a black bit sensed by the scanner at the indicated location of the vertical scan. The absence of a cross at a particular location indicates a white bit thereat. A rectangle **617** in FIG. 12 contains the indications of each coded number written into the different stages of the marking register during each vertical scan of the black-white indications of rectangles **614**, each coded number being placed within rectangle **617** at the horizontal bit position, corresponding to the time at which it is written into the marking register. For example, on the first vertical scan of the character 0, black bits are detected at horizontal positions 5 through 11 in rectangle **614**, and since coded number 1's are written into the marking register when the black bits become "now" bits, coded 1's are shown in rectangle **617** at the horizontal bit positions 5 through 11. Since, as hereinbefore described, the black-white "now" determination is always reset to white "now" at the beginning of each vertical scan, and since a coincidence of a 0 "now" and a white "now" always cause a coded 0 to be placed in the marking register (by just not writing any number into the marking register), a "phantom" horizontal bit position under the first horizontal bit position always appears with all coded 0's therein, as shown within rectangle **617**. Similarly, it is to be noted that the top bit of each vertical scan in rectangle **617** is a coded number written into the marking register at the time that the fifteenth bit of the rectangle **614** is the "now" bit and the sixteenth bit is the "next" bit. Since the machine never utilizes the sixteenth bit as the "now" bit, there is no sixteenth horizontal bit position shown in rectangle **617**.

The recognition criteria rule circuits are shown in FIGS. 8F through 8BB. The inputs to the recognition criteria rule circuits are the black-white determination cable **438**, the rules circuit "now" input cable **550**, the rules circuit "next" input cable **556**, the register read out trigger reset lead TP and the reset cable **465**. The outputs from the recognition criteria rule circuits are the rules circuit output cable **558** and a cable from memory C triggers to be described hereinafter. The recognition criteria rule circuits recognize the black-white "now" determination and the black-white "next" determination from the black-white determination cable **438** and also the coded "now" bit and the coded "next" bit in the rules circuit input cables **550** and **556** respectively, and thereby operate both to assign the arbitrary coded numbers, previously described, to the first stage of the marking register, and to turn On the memory triggers which act to set up relays in the Christmas tree circuit.

For ease of description, the recognition criteria rule circuits have been divided into ninety-one labeled rules circuit, separated from each other, in FIGS. 8F to 8BB by dashed lines.

A cursory study of the recognition criteria rule circuits show that there are some triggers labeled with an S and others labeled with a C. The S triggers are those known as the temporary triggers and are reset at the end of each vertical scan by either the X_s or X_{sd} pulse from the reset cable **465**. The triggers labeled with a C are known as the memory triggers and are reset at the end of character by an X_c reset pulse from the reset cable **465**. The resetting of the S and C labeled triggers will not be described any further in the description of the rule circuits unless they operate differently from the description just given.

Generally, the S and C triggers are turned On if there are a certain number of predetermined conditions. Since these predetermined conditions may be effected by the other S and C triggers being turned On, it is necessary to have a timing pule for testing the presence of all the predetermined conditions at one particular time. For this, the register read out trigger reset pulse on lead TP is utilized. The input circuitry for turning On the S and C triggers usually include an AND circuit, one of the input leads of which may be the register read out trigger lead TP. Due to the nature of the trigger circuitry the trigger outputs will not rise sufficiently fast to effect the inputs during a single register read out trigger reset pulse. In the description of the AND circuits, which are the inputs to the S and C triggers and to certain counters in the rule circuits, the register read out trigger lead TP will not be further described because it will be henceforth understood that it is used only for timing reasons.

Rule circuits—Vertical white zones

Before describing the Write rule circuits which perform the assignment of the coded numbers into the marking register, a description will be given of other rule circuits which detect vertical white zones and other incidentals, preferably to be first understood, to facilitate the understanding of the Write rule circuits. As has been previously described, the recognition criteria rule circuits are able to detect a first, second and third vertical white zone. Rule 1 circuit (FIG. 8F) through Rule 4 circuit are used for detecting the vertical white zones, the positions of which are shown in FIGS. 32 through 34. In Rule 2 circuit (FIG. 8F), a trigger S_1 is turned On to signify entrance into the first vertical white zone. The black lead B and the white "next" lead $\overline{B}_N$ from the black-white determination cable **438** (and the register read out trigger reset lead TP for timing) are connected in the Rule 2 circuit to an AND circuit **620**, the output of which is connected to the left-hand input of a first vertical white zone entrance trigger S_1. Trigger S_1 has its left-hand output connected to a lead "$\overline{S}_1$" and its right-hand output connected to a lead "S_1," both of which are connected into an S trigger cable **621**. All of the leads from both outputs of all the S triggers are fed into and out of S trigger cable **621**. A positive potential on both leads B and $\overline{B}_N$ will turn ON trigger S_1, causing lead "S_1" to go positive and lead "$\overline{S}_1$" to go negative. The presence of both a B and a $\overline{B}_N$ indicates that in a particular vertical scan there is a black "now" bit and a white "next" bit above it. Referring to FIG. 32, column (*c*) indicates a black fifth bit and a white sixth bit. At the time that the black fifth bit is looked at as the black "now" bit, and the white sixth bit is looked at as the white "next" bit, it is an indication that the scan is passing from a first black crossing into the first vertical white zone. When the register read out trigger reset pulse TP comes along, somewhere in time between the "now" and "next" bits, the trigger S_1 gets turned On, to indicate the entrance into the first vertical white zone.

It will be shown that trigger S_2 of Rule 3 circuit is turned On, making its output lead "S_2" positive, in order to indicate an entrance into the second vertical white zone, and that trigger S_3 of Rule 4 circuit is turned On to indicate an entrance into the third vertical white zone. In the Write rule circuits, the fact that the bits being examined are in the first vertical white zone is detected by the fact that not only is first vertical white zone entrance trigger S_1 On, but that second vertical white zone entrance trigger S_2 is Off, indicating the second vertical white zone has not been entered. Similarly, the second vertical white zone is detected by second vertical white zone entrance trigger S_2 being On and third vertical white zone entrance trigger S_3 Off. The fact that trigger S_3 is On, without any other information, is enough to indicate that the bit being examined is in the third vertical white zone.

If any of the vertical white zones contain a minimum white height it is known as a bona fide vertical white zone. It is necessary that a vertical white zone be identified as a bona fide vertical white zone before the next vertical white zone can be indicated. A minimum white height zone (MWH zone) trigger S in Rule 1 circuit is utilized to indicate if a vertical white zone is bona fide. In Rule 1 circuit, the white "now" and white "next" lead $\overline{B}$ & $\overline{B}_N$ indicative of a minimum white height is connected

to one input of an AND circuit **622**, the other input of which is fed from an OR circuit **624**. One of the inputs of OR circuit **624** is the first vertical white zone entrance lead "S_1" from S trigger cable **621**. A simultaneous positive condition of the lead $\overline{B}$ & $\overline{B}_N$ and the lead "S_1" via OR circuit **624** and at TP time, will turn On the MWH zone trigger S_0 making its lead "S_0" positive. Thus, in the first vertical white zone, the fact that both first vertical white zone entrance lead "S_1" and MWH zone lead "S_0" are positive indicates a bona fide vertical white zone.

MWH zone trigger S_0 is used to indicate a bona fide zone for all three vertical zones, and therefore it must be reset as soon as there is an indication of the entrance into a new zone. Then, if the succeeding "now" determination is white, the lead $\overline{B}$ & $\overline{B}_N$ will go positive, and since once first vertical white zone entrance trigger S_1 is turned On, it remains On until the end of vertical scan, the positive condition of lead $\overline{B}$ & $\overline{B}_N$ will then permit the TP pulse to turn On MWH zone trigger S_0 via AND circuit **622**.

As soon as a new vertical white zone is indicated it is desirable to reset MWH zone trigger S_0 to again test the new zone for a minimum white height to insure a bona fide zone. The resetting of MWH zone trigger S_0 is accomplished by connecting the three vertical white zone entrance leads "S_1," "S_2," and "S_3" to the input of an A.C. OR circuit **626**, the output of which is connected to the right-hand A.C. input of MWH zone trigger S_0. As soon as one of the these triggers gones On, the pulse is transmitted via A.C. OR circuit **626** to reset MWH zone trigger "S_0."

It is to be noted that OR circuit **624** of Rule 1 circuit has as its other input the lead $\overline{O}_N$, which is "anded" at AND circuit **622** with lead $\overline{B}$ & $\overline{B}_N$ for turning On the MWH zone trigger S_0 in a special case which is described in more detail hereinafter with the description of the assignment of coded 4's. The reset lead X_s is connected via an OR circuit **628** and the lead **630** to the right-hand input of MWH zone trigger S_0, for resetting it at the end of scan at X_s time. The circuitry associated with the other input of OR circuit **628** will also be described hereinafter in conjunction with the assignment of coded 4's.

As a prerequisite to the turning On of second vertical white zone entrance trigger S_2, in addition to the leads B and $\overline{B}_N$ being positive as an indication of the scan going from black into white, the first vertical white zone entrance lead "S_1" and MWH zone lead "S_0" must be positive as an indication that the first vertical white zone was bona fide, and so leads B, $\overline{B}_N$, "S_1" and "S_0" are fed to the input of an AND circuit circuit **632** in Rule 3 circuit, the output of which goes positive at TP time upon a coincidence of positive conditions on the input leads to effect the turning On of second vertical white zone entrance trigger S_2.

To indicate the entrance to the third vertical white zone, in addition to the leads B and $\overline{B}_N$ being positive as an indication of the scan going from black into white, the leads "S_2" and "S_0" must be positive as an indication that the second vertical white zone was bona fide, and so leads B, $\overline{B}_N$, "S_2" and "S_0" are fed to the input of an AND circuit **634** in Rule 4 circuit, the output of which goes positive at TP time upon a coincidence of positive conditions on the input leads to effect the turning On of third vertical white zone entrance trigger S_3.

The vertical white zone entrance triggers S_1, S_2 and S_3 are all reset at the end of a vertical scan by an X_{sd} pulse which comes later than the X_s pulse, because the X_s determination of the presence of a dropout to the north is made at X_s time. Since the vertical white zone information is used for determining a north dropout, it would not be desirable to reset the vertical white zone triggers S_1, S_2 and S_3 until after this determination is made.

Rule circuits—Dropouts

Rule 5 through Rule 11 circuits inclusive (FIGS. 8F and 8G), are used for detecting "dropouts" which signify that an included white region extends upward or downward out of a character. A south dropout, which is utilized in detecting a south bay or a southeast bay, extends downward out of the character and thus has the additional requirement of a hitsory of black to the left of the dropout. A north dropout, which also requires a history of black to the left, extends upward out of a character and is utilized in detecting a north bay or a northeast bay.

Rule 5 circuit (FIG. 8F) is used for detecting a double south dropout which implies included white regions dropping out the bottom of the character in two successive vertical scans, and is indicated by turning on the double south dropout trigger C_0. A single south dropout is thus ignored to avoid an incorrect recognition of a poor printed character that has, for example a one bit break in its lower horizontal line that might otherwise appear to be a south bay.

For example, FIG. 16 illustrates the alphabetic character A which contains a double south dropout. In the twenty-fifth labeled vertical scan of FIG. 16, the fourth and fifth bits **636** are white, and the marking register at this time indicates coded 1's **638** for the fourth and fifth bits of the twenty-fourth vertical scan representative of a history of black to the left. Since there are no black bits below the fourth bit of the twenty-fifth vertical scan, the first vertical zone has not yet been entered and the first vertical white zone entrance trigger S_1 of Rule 2 circuit is not yet On, this is effectively a single south dropout. Coded 4's **640** are also inserted in the marking register for this set of facts as will be more fully described hereinafter in the description of assignment of coded 4's.

In the twenty-sixth vertical scan, the fourth and fifth bits **642** are white and first vertical white zone entrance trigger S_1 is not yet On, and this indicates a second south dropout. Thus, it is obvious that the requirements for a double south dropout are that the marking register indicates coded 4's as the "now" and "next" bit (leads IN4 and $IN4_N$ positive), that there be a minimum white height, and that the first vertical white zone entrance trigger S_1 be Off. Thus, for a double south dropout, in addition to the leads IN4 and $IN4_N$ being positive as an indication of a single south dropout of a minimum white height, the leads $\overline{B}$ & $\overline{B}_N$ must be positive as an indication of a minimum white height, and the lead "$\overline{S}_1$" must be positive as an indication that the first vertical white zone has not been entered. Therefore, in Rule 5 circuit, the leads IN4, $IN4_N$, $\overline{B}$ & $\overline{B}_N$ and $\overline{S}_1$ are fed to the input of an AND circuit **644** and and a coincidence of these conditions at TP time causes the output of AND circuit **644** to go positive to turn on double south dropout trigger C_0. The right-hand and left-hand outputs of trigger C_0 are the lead "C_0" and "$\overline{C}_0$" which are connected to a C trigger cable **646**, along with all other output leads from the C memory triggers, from which it may be connected to any other of the rule circuits as needed. Lead "C_0" goes positive to indicate that a south double dropout is present. As previously described, memory triggers labeled C are reset at the end of the character by an X_c pulse because once a double south dropout is detected, that information is required until the end of the character. Trigger C_0 may also be reset by a lead from the output of an A.C. OR circuit **648**, the inputs of which are leads "C_{18}" and "C_{19}" which, as will be hereinafter described, are positive after the detection of the presence of a south bay and after the detection of the presence of two south bays, for reasons to be more fully described hereinafter.

Rule 6 circuit, Rule 7 circuit and Rule 8 circuit (FIG. 8B) cooperate to detect a double north dropout from the first vertical white zone and this condition is indicated by the turning On of double north dropout

from zone 1 trigger C_1 of Rule 8 circuit. Rule 9 circuit, Rule 10 circuit and Rule 11 circuit are utilized for detecting a double north dropout from the second vertical white zone, a condition indicated by the turning On of double north dropout from zone 2 trigger C_2 of Rule 11 circuit. The reason for distinguishing between a dropout from the first vertical white zone and the second vertical white zone is hereinafter described in the section describing the Write rules circuits relating to the assignment of coded 5's, 6's and 7's.

The numeric character 1 of FIG. 12 illustrates a double north dropout from the first vertical white zone. In the twenty-first vertical scan of FIG. 12 the marking register indicates coded 1's **650** for the fourth and fifth bits representative of a history of black to the left, and the fourth and fifth bits **652** of the twenty-second vertical scan are white. It is obvious that the white bits **652** of the twenty-second vertical scan are in the first vertical white zone because there is only one black crossing of bits below them. This condition will turn On the trigger S_{23} as an indication of a possible single north dropout of the white bits **652** from the first vertical white zone. Thus, for the trigger S_{23} to be turned On as indicative of a possible single dropout to the north from the first vertical white zone, the leads "S_1" and "$\overline{S}_2$" must be positive as an indication of the first vertical white zone, the lead $\overline{B}$ & $\overline{B}_N$ must be positive as an indication of a minimum white height and the leads IN1 and $IN1_N$ must be positive as an indication of black to the left. Therefore, the leads "S_1," "$\overline{S}_2$," $\overline{B}$ & B_N, IN1 and $IN1_N$ of Rule 6 circuit FIG. 8G, are fed to the input of an AND circuit **654**, and a coincidence of these conditions at TP time causes the output of AND circuit **654** to go positive to turn ON trigger S_{23} via an OR circuit **656**. Any black bit in this twenty-second vertical scan will reset trigger S_{23} as a sign of no dropout and so that lead B is connected via an AND circuit **657** for timing and an OR circuit **658** to the right-hand input of trigger S_{23} to reset it on the sensing of a black bit. The actual single dropout to the north is detected at the end of the vertical scan as can be seen in Rule 7 circuit where the leads X_s and S_{23} are connected as the inputs of an AND Circuit **658**. If trigger S_{23} is still On at the end of the vertical scan, a true single dropout to the north has been sensed and a positive output from AND circuit **660** will turn On single north dropout trigger C_3 as an indication thereof. A little later at X_{sd} time, trigger S_{23} is reset so that a new possible dropuot condition from vertical white zone 1 can be examined anew in each vertical scan.

Referring again to FIG. 12, coded 5's **662** will have been written at the fourth and fifth positions of the marking register indicative of a minimum white height in a first vertical white zone with a history of black to the left as will be hereinafter described. In the twenty-third vertical scan, the fourth and fifth bits **664** are again white and so there is another possible dropout to the north. Thus, for a second possible dropout to the north, the leads IN5 and $IN5_N$ must be positive as an indication of a first vertical white zone in the previous scan and the lead $\overline{B}$ & $\overline{B}_N$ must be positive as an indication of a minimum white height. The leads IN5, $IN5_N$ and $\overline{B}$ & $\overline{B}_N$ are thus fed to an input of an AND circuit **666**, the output of which goes positive at TP time on coincidence of the input conditions, and the positive pulse is fed via OR circuit **656** to turn On trigger S_{23}. This time if both single north dropout trigger C_3 and trigger S_{23} are On at the end of the twenty-third vertical scan, it will be an indication of a double dropout to the north from vertical white zone 1. The leads S_{23} and C_3 and X_s in Rule 8 circuit, are thus fed to the input of an AND circuit **668**, the output of which goes positive to turn On double north dropout from zone 1 trigger C_1. In Rule 7 circuit the leads X_s and $\overline{S}_{23}$ are connected to the input of an AND circuit **670**. If at the end of the vertical scan, trigger S_{23} is not On because it was reset by a black bit above, a positive output will be produced to reset single north dropout trigger C_3 via an OR circuit **672**. Thus, a double dropout to the north can be indicated only if a single dropout to the north occurs in two successive vertical scans. Double north dropout from zone 1 trigger C_1 is ordinarily reset at the end of the character by lead X_c connected to its right-hand input but may be reset in another manner as is described hereinafter in the description of the Write rules circuits relating to the assignment of coded 5's, 6's and 7's.

A possible north dropout from the first vertical white zone in the alphabetic character U in FIG. 28 is detected in a slightly different manner. This is due to the long serif **674**, which blocks by black above, the minimum white height **676**, in the seventh vertical scan, when the fact that the coded 1's **687** in the marking register indicate a history of black to the left. In the ninth vertical scan, wherein the minimum white height **680** does dropout to the north, there is no condition of a coded 1 and 1_N in the marking register after the sixth bit, to allow AND circuit **654** of Rule 6 circuit to turn On trigger S_{23}. In this situation, however, AND circuit **666** of Rule 6 circuit (FIG. 8G) actually turns On trigger S_{23} to detect the first single north dropout, because during the ninth vertical scan, when the fifth and sixth bits **680** (FIG. 28) are white ($\overline{B}$ & $\overline{B}_N$), the coded 5's **682** in the marking register (5 and 5_N) are representative of the fact that there was a history of black to the left and that they are in the first vertical white zone. In this case, AND circuit **666** (Rule 6 circuit, FIG. 8G) also detects the second possible dropout to the north in the usual manner.

The operation of the Rule 9, Rule 10 and Rule 11 circuits are similar to that of the Rule 6, Rule 7 and Rule 8 circuits except that the leads "S_2" and "$\overline{S}_3$" are used instead of the leads "S_1" and "$\overline{S}_2$" and the lead IN6 and $IN6_N$ instead of IN5 and $IN5_N$ so that the former will apply to the second vertical white zone, and the latter to the first vertical white zone. Thus, the triggers S_{24}, C_2 and C_4 for north dropouts from the second vertical white zone are exactly analogous to the triggers S_{23}, C_3 and C_1, respectively for the first vertical white zone and therefore the operation of the Rule 9, Rule 10, and Rule 11 circuits will not be further described.

Rule circuits—Assignment of coded 1's, 2's, 3's and 4's

Rule 19 circuits to Rule 25 circuit, inclusive, relate to the assignment of writing of numbers in the marking register and are therefore referred to occasionally in this specification as the Write rule circuits. Rule 12 circuit to Rule 18 circuit, inclusive, are Write auxiliary rule circuits for modifying the Write rule circuits, and will be described simultaneously therewith.

As previously described, there are no specific circuits for assigning coded 0's. Coded 0's are in the marking register only because when the marking register is shifted, no coded number is shifted into the first stage, and if no coded number is assigned to the first stage before the next shift, the coded 0 in the first stage will effectively be shifted to the second stage.

Rule 19 circuit of FIG. 8I indicates that the lead B representative of the black "now" is connected directly to the lead OUT 1 which is the lead that is connected into the rule circuit output cable **558** and causes the writing of coded 1's into the marking register. Thus, every time a black "now" determination is made, a coded 1 is written into the marking register. It is not necessary to have a special timing pulse in the rule circuits, for writing because the register write pulse on lead **398** of FIG. 8E acts as a timing pulse.

The assignment of the other coded numbers usually depends on the three general conditions previously described, the vertical white zone, the minimum white condition, and the past history of black. In addition, cer-

tain particular conditions may cause the assignment of the coded numbers. This may be illustrated in Rule 20 circuit.

In Rule 20 circuit, the leads "S_1" and "$\overline{S}_2$" from the S trigger cable **621** are connected to the input of an AND circuit **700**, the output of which is the lead OUT 2 which is utilized for writing coded 2's. The leads "S_1" and "$\overline{S}_2$" signify the first vertical white zone as previously described. The NWH lead $\overline{B}$ & $\overline{B}_N$ is connected to the input of an OR circuit **702**, the other input of which is the output lead of an AND circuit **712**, the input leads of which are the white "now" lead $\overline{B}$ and the MWH zone lead "S_0." The lead $\overline{B}$ & $\overline{B}_N$ geing positive represents a minimum white height and causes a positive output from OR circuit **702**, the output lead of which is labeled MWC representative of a minimum white condition. The minimum white condition means either a minimum white height, or the top bit in any vertical white zone. For example, in FIG. 14 when the white bit **706** is a "now" determination, "next" determination is the black bit **708** and therefore there is no minimum white height associated with this white "now" bit. However, it is necessary to assign a coded 2 **710** for the white "now" determination because it is the top white of a definite included white region, and to take care of the fact that the top white bit of an included white region is a member of that white region, if the MWH zone trigger S_0 is On from a previous bit of that scan and there is a white "now" determination, a minimum white condition will be indicated which should be at least equivalent to a minimum white height.

This is accomplished by requiring that if a minimum white height has been determined (by turning On of MWH zone trigger S_0) when a white "now" condition $\overline{B}$ exists leads MWC is made positive. The leads "S_0" and $\overline{B}$ of Rule 20 circuit (FIG. 8I) produces an output from AND circuit **712** which is fed via OR circuit **702** to the minimum white condition lead MWC. The lead IN0 from "now" cable **550** goes positive to represent the fact that there was no history of black to the left. The leads IN0 and MWC are "anded" at an AND circuit **714**, the output of which is fed via an OR circuit **716** to AND circuit **700**. Thus, the output of AND circuit **700** will go positive to cause the OUT 2 lead to go positive and write coded 2's when these three general conditions are present; a first vertical white zone, a minimum white condition, and no past history of black to the left.

The rest of Rule 20 circuit is utilized for the expanding of coded 2's both northward and southward. The importance of the expanding of the coded 2's can be observed in the character S of FIG. 25. Due to the upward curvature of the black **718** between the sixth to the ninth bit of the character, it would appear that the coded numbers assigned to the right of black bits **718** should be 5's representative of a history of black to the left. The machine would then mistakenly detect a lower lake, and recognize a character 6, instead of detecting a lower west bay in a character S. If the coded 2 **720** assigned for the tenth bit of the twenty-sixth vertical scan can be caused to effectively move southward along the inside black of the lower west bay **722**, it will then be possible to recognize the pattern of the resulting coded 2's representative of no history of black to the left and therefore, as inside a lower west bay.

A southward expansion of 2's is accomplished by Rule 20 circuit (FIG. 8I) by noting a simultaneous occurrence of a minimum white height and a coded 2 "next" condition, causing the writing of a coded 2. Thus, AND circuit **724** has as its inputs the MWH lead $\overline{B}$ & $\overline{B}_N$ and the lead $IN2_N$ which produce an output that is fed via OR circuit **716** and AND circuit **700** to the OUT 2 lead. Since normally in this case the "now" bit is coded 1 representative of black to the left of the "now" bit, the coded 5 would be written normally. However, it will be shown hereinafter that Rule 23 circuit operates to inhibit the writing of coded 5's where coded 2's are expanded southward. Thus, in FIG. 25, in the twenty-seventh labeled vertical scan, when the bit **720** is a 2 "next" bit, the bits **726** are white "now" and white "next," and therefore, the coded 2 **728** will be written into the marking register. The coded 2 **728** is thus a southward expansion of the coded 2 **720**. The coded 2's **730** are illustrations of a further southward expansion of coded 2's by Rule 20 circuit of FIG. 8I in a similar manner.

Rule 12 circuit is used as a write auxiliary circuit which in conjunction with part of Rule 20 circuit operates to produce a northward expansion of coded 2's. Rule 12 circuit indicates that wherever a coded 2 is examined as a "now" bit and a coded 5 as the "next" bit, if there is a minimum white height, a trigger S_4 in Rule 12 circuit representative of this fact will be turned On. Thus, the trigger S_4 On indicates that a possible expansion of coded 2's to the northward replacing coded 5's should occur since there exists an opening to the west in this white region as signified by the 2 "now" bit.

Thus, in Rule 12 circuit the leads IN2, $IN5_N$ and $\overline{B}$ & $\overline{B}_N$ are connected to the input of an AND circuit **732**, which produces an output at TP time for turning On Trigger S_4. In Rule 20 circuit AND circuit **700** is then utilized to write 2's in place of all the 5's in this scan. Thus, an AND circuit **734** has as inputs the lead "S_4" representative of this possible northward expansion and the leads IN5 and $\overline{B}$ indicative of a white to the right of a coded 5. An output from AND circuit **734** is fed through OR circuit **716** to AND circuit **700** to produce a signal on lead OUT 2, if the leads "S_1" and "$\overline{S}_2$" representative of the first vertical white zone are positive.

An illustration of this northward expansion of coded 2's is the character Z in FIG. 15. It is to be noted that the coded 5 **736** and the coded 5 **738** have been written on the twenty-ninth vertical scan as indications of a history of the black bits **740** to the left. On the thirtieth vertical scan, when the determinations **742** and **743** are white "now" and white "next" respectively, a coded 2 **744** is the "now" bit and coded 5 **736** is the "next" bit, the conditions are met for turning On trigger S_4 of Rule 12 circuit (FIG. 8H). Then when the next bit is examined, the coded 5 **736** becomes the "now" bit, the determination **743** becomes the white "now" determination, and since trigger "S_4" is On, the input conditions of AND circuit **734** are met and a coded 2 **746** replaces the coded 5 **736**. Similarly, coded 2 **748** replaces the coded 5 **738** to complete the northward expansion of coded 2's.

Rule 21 circuit operates to write coded 3's in the marking register. Normally, the coded 3's are written in the marking register when there is a minimum white condition, and a coded 0 "now" bit in the second vertical white zone. Thus, the MWC lead representative of the minimum white condition from the Rule 20 circuit is "anded" at AND circuit **750** with the IN0 lead and the output is fed via an OR circuit **752** to the input of an AND circuit **754**, the other two inputs of which are leads "S_2" and "$\overline{S}_3$" representative of the second vertical white zone. The coincidence of these conditions produces a positive pulse at the output of AND circuit **754** on the lead OUT 3 to cause the writing of 3's in the marking register.

Where coded 2's have been written because of the detection of a first vertical white zone, and in a later vertical scan it is determined that the bits being examined are in the second vertical white zone, coded 2's must be replaced by coded 3's as previously described. This is accomplished by Rule 21 circuit where the lead IN2 is connected as an input of an OR circuit **756**, the output of which is "anded" with $\overline{B}$ at AND circuit **758**. Thus,

any time there is a coded 2 "now" and a white, an output is produced from AND circuit **758** which is fed via OR circuit **752** to AND circuit **754**. AND circuit **754** will then have an output if the coded 2 and white are detected in a second vertical white zone because of the other leads "S_2" and "$\overline{S_3}$" at its input. An illustration of 3's replacing 2's was described hereinbefore in conjunction with the description of FIGS. 32 and 33.

Due to the nature of the characters to be read in the preferred embodiment, coded 3's may be expanded northward but it is not necessary to expand them southward for reliable recognition. Northward expansion of code 3's is illustrated in the character 3 of FIG. 13 and is accomplished by Rule 21 circuit and the Rule 13 circuit (FIG. 8H). Basically, Rule 13 circuit operates to recognize that whenever a coded 3 is a "now" bit and a coded 6 is the "next" bit, if there is also a minimum white height present, a trigger S_5 representative of this fact will be turned On.

Thus, in the fifth vertical scan of FIG. 13, when determinations **756** and **758** are white "now" and white "next" respectively, bits **760** and **762** are coded 3 "now" and coded 6 "next" respectively and coincidence of these conditions produce the On condition of trigger S_5 of Rule 13 circuit. The lead $IN6_N$ of Rule 13 circuit is connected via an OR circuit **764** to one of the inputs of an AND circuit **766**, the other two inputs of which are the lead $\overline{B}$ & $\overline{B}_N$, and IN3, a coincidence of which at TP time produces a pulse for turning On trigger S_5. It is understood that the coded 6's **762** and **768** are written because of the history of black to the left. Then, when determination **758** is examined as the "now" determination, the fact that trigger S_5 is On will permit coded 3's to replace coded 6's. That is in FIG. 13, the coded 3's **770** and **772** will replace the coded 6's **762** and **768** respectively. This is accomplished by Rule 21 circuit wherein the AND circuit **758** has as its input the lead $\overline{B}$ and a lead from OR circuit **756**, one of the inputs of which is an AND circuit **774**. The input of AND circuit **774** are the lead "S_5" and the output of an OR circuit **776**, one of the inputs of which is the lead IN6. A coincidence of a coded 6 and the possible northward expansion of coded 3's lead "S_5" produces an output from AND circuit **774** which is fed via OR circuit **756** to AND circuit **758** where it is "anded" with the lead $\overline{B}$ to produce a pulse which is fed via OR circuit **752** to AND circuit **754**. There it is "anded" with the leads representative of the second vertical white zone to write a coded 3. Thus the white "now" determination **758** of FIG. 13 and the 6 "now" bit **762** will cause the writing of coded 3 **770** when the trigger S_5 is On. The coded 3 **772** is an example of the further northward expansion up to the black above.

It may be possible that coded 5's are written because the area appears to be a first vertical white zone, and then in the succeeding vertical scan coded 3's are written because it is determined that this zone is actually a second vertical white zone. At that time, if it is necessary to expand 3's northward, the 3's will expand northward in place of the 5's. Therefore in Rule 13 the lead IN_{5N} is also connected to the other input of OR circuit **764**, the other input of which is lead $IN6_N$, and in Rule 21 circuit lead IN5 is "ored" at OR circuit **776** with the lead IN6.

Normally a coded 4 is written when a minimum white condition MWC is detected simultaneously with a coded 1 "now" before the first vertical white zone has been entered. Thus, in Rule 22 circuit (FIG. 8J) the lead MWC from Rule 20 circuit and the lead IN1 are "anded" at an AND circuit **778**, the output of which is connected via an OR circuit **780** to one input of an AND circuit **782**, the other input of which is the lead "$\overline{S_1}$" representative of the fact that the first vertical white zone had not yet been entered. A coincidence of the input signals produces an output from AND circuit **782** which is the lead OUT 4 to write a coded 4 into the marking register.

The character F of FIG. 19 will illustrate two conditions where 4's are written in place of other coded numbers. Due to the long lower serif in the character F of FIG. 19, a potential lower east bay is detected due to the coded 5's which are assigned to this area. In order to indicate that this is also a potential southeast bay so as to be able to distinguish the characters E from F, coded 4's must replace the coded 5's. Thus, in Rule 22 circuit of FIG. 8I, the lead IN5 is fed via an OR circuit **784** to one input of an AND circuit **786**, the other input of which is the white "now" lead $\overline{B}$. A coincidence of the two input signals produces an output which is fed via OR circuit **780** where it is "anded" with the lead "S_1" to produce a coded 4. Thus, in FIG. 19 the presence of the coded 5 **788** and the white "now" bit **790** will cause a coded 4 **792** in the thirteenth vertical scan to be written because the lead "$\overline{S_1}$" representative of entrance into the first vertical white zone has not yet been turned On.

To prevent the coded 6's assigned to the upper east of the character F in FIG. 19, from appearing to be blocked to the right by the serif **794**, and therefore appearing to be an upper lake, it has been found expedient to replace the coded 6's by coded 4's rather than expand the coded 6's downward. This is permissible, because if by the time the coded 6's are replaced by coded 4's, a potential upper east bay indication has been detected, the fact that the coded 6's themselves will not be blocked by coded 1's to the right will prevent this potential upper east bay indication from turning into an upper lake indication. The coded 4's **796** and **798** in the sixteenth vertical scan have replaced the coded 6's **800** and **802** as an illustration of this.

The operation for performing this is accomplished by the write auxiliary Rule 16 circuit (FIG. 8H) in conjunction with Rule 22 circuit. Rule 16 circuit indicates that if there is a 4 "now" and a 6 "next" when there is a minimum white height, and the south double dropout trigger C_0 and a potential upper east bay trigger C_{10} and On, and AND circuit **804** will have an output and turn On trigger S_7. Then in Rule 22 circuit the lead "S_7" is "anded" at AND circuit **806** with the lead IN6 to produce an output which is fed via OR circuit **784** where it is in turn "anded" with the white "now" lead $\overline{B}$. If the trigger S_7 is On when a 6 "now" bit is detected, and a white "now" bit is being examined an output is produced from AND circuit **786** which is fed via OR circuit **780** where it is "anded" with a "S_1" lead to write a coded 4.

Rule circuits—Assignment of coded 5's, 6's and 7's

The Rule 23 circuit is utilized for assigning coded 5's into the marking register. Basically, coded 5's are written when a minimum white height exists within the first vertical white zone, coincidently with a coded 1. Rule 23 circuit is complicated, however, by the fact that the writing of coded 5's may be inhibited by certain other coded numbers expanding southward. As previously described, when a coded 2's expand southward into areas of coded 5's, the writing of coded 5's is inhibited. Similarly, it will be shown that when coded 6's and coded 7's expand southward, the writing of coded 5's is also inhibited.

In the Rule 23 circuit, lead MWC and IN1 are fed to an AND circuit **808** which has three other leads that are used for inhibiting the writing of coded 5's. If there is no inhibiting necessary, a coincidence of a minimum white condition and a coded 1 "now" bit produces an output from AND circuit **808**, which is fed via OR circuit **810** to AND circuit **812**. AND circuit **812** also has an inhibiting lead "$\overline{C_1}$," which will be described hereinafter. If this inhibitory lead "$\overline{C_1}$" is positive, the coincidence of pulses on the MWC and IN1 leads from OR circuit **810** and the leads "S_1" and "$\overline{S_2}$" representative of the first ver-

tical white zone, produces an output from AND circuit **812** to cause the lead OUT 5 to go positive, to thereby assign a coded 5 to the marking register. The assignment of coded 5's has been illustrated and described hereinbefore in conjunction with the description of FIG. 35.

Thus coded 5's will normally be written where there is a coded 1 "now" bit and a white "now" and white "next" except where there is a coded 2 "next," or 6 "next" or 7 "next's" bit, at which time the coded 2 or 6 or 7 will expand southward by being written into the marking register.

Coded 5's are written when a coded 1 "now" bit and coded 3 "next" bit are detected only because, due to the nature of the characters, it is not necessary to expand coded 3's southward. However, if it were necessary to expand coded 3's southward, it would only be necessary to put an inhibitor $\overline{3}_N$ lead in Rule 23 circuit to prevent the writing of coded 5's when it was desired to expand 3's southward.

It can be seen that the simultaneous condition of a minimum white height and a 1 "now" and a 5 "next" permits an effective southward expansion of coded 5's. Thus, in the character 6 of FIG. 14, when examining determinations **814** and **816** as the "now" and "next" determinations respectively, the presence of the 1 "now" bit **818** and the 5 "next" bit **820** in the marking register will cause a coded 5 to be assigned as an effective southward expansion of coded 5 **820**.

The inhibiting of the writing of coded 5's when coded 2's must be expanded southward will now be described. The lead $IN2_N$ of Rule 23 circuit of FIG. 8J is fed to an inverter **824**, the output of which is a lead $\overline{2}_N$ which is fed via an OR circuit **826** to AND circuit **808**. As long as there is no 2_N, lead $\overline{2}_N$ will be positive and therefore the output of OR circuit **826** will be positive to condition AND circuit **808**. However, if there is a 2 "next" bit present, the lead "$\overline{2}_N$" will be negative deconditioning AND circuit **808** and inhibiting coded 5's from being written as has previously been described. However, at certain times it may be undesirable to expand coded 2's southward. This is illustrated in the character 4 of FIG. 13. In the nineteenth vertical scan, when the determination **828** is made as white "now," the "now" bit in the marking register is the coded 1 **830** and the "next" bit is the coded 2 **832**, it is undesirable to have coded 2, **832** expand southward through the black diagonal **834** of the character 4. In the writing of coded 2's in Rule 20 circuit, it was necessary to have both a white "next" input to AND circuit **724** to get an expansion of coded 2's to the south. If a black "next" bit **836** exists, the conditions of the character 4 of FIG. 13, are met as to the undesirability to expand coded 2 **832** southward. To allow the coded 5 **838** of FIG. 13 to be written, when the lead $\overline{2}_N$ of Rule 23 circuit is negative, AND circuit **808** must be conditioned by the black "next" lead B_N via OR circuit **826**. Thus, if a B_N exists when there is a 2_N in the marking register, coded 5's will not be inhibited. Any attempt by the lead "2_N" to inhibit the writing of coded 5's will overcome by the lead "B_N" going positive and thereby conditioning AND circuit **808**.

The lead $\overline{7}_N$ connected to AND circuit **808** will be discussed with the description of the southward expansion of coded 7's and the lead from an OR circuit **840** connected to AND circuit **808** will be described hereinafter with the description of the southward expansion of coded 6's.

There is a special case, where coded 5's are written in place of coded 6's, that is best illustrated in the character E of FIG. 18.

Just as in the character F of FIG. 19 where the coded 6's would appear to be blocked by the serif **794** to the right to cause the detection of an upper lake which does not in fact exist, the serif **842** of the character E of FIG. 18 appears to block the coded 6's in the upper east bay. In addition, the coded 5's in the lower east bay of the E appear to be blocked to the right by the serif **844** to give the appearance of a lower lake. To avoid this, and insure that at least either the coded 5's, assigned in the lower east bay, or the coded 6's, assigned to the upper east bay, both do not appear to be blocked by black to the right, the coded 6's are replaced by coded 5's, giving the coded 5's a better chance to appear not to be blocked to the right by either the upper serif **842** or lower serif **844**. This is accomplished by the use of the Rule 15 circuit (FIG. 8H) and the Rule 23 circuit (FIG. 8J). In Rule 15 circuit, a lead IN5 and $IN6_N$ being positive simultaneous with lead $\overline{B}$ and $\overline{B}_N$, representative of a minimum white height, and the potential upper east bay lead "C_{10}," and a potential lower east bay lead "C_{11}" are "anded" to an AND circuit **846** and a coincidence of these leads will turn On the trigger S_6. Thus, when determinations **848** and **850** of the character E of FIG. 18 are examined as white "now," white "next" respectively, bit **852** is a coded 5 "now" and bit **854** is a coded 6 "next." It is obvious from the drawing that a potential upper east bay and lower east bay are present at that time, and so the trigger S_6 will be turned On to signify the presence of all these conditions. In Rule 23 circuit FIG. 8J, the lead "S_6" is "anded" at AND circuit **856** with the lead IN6. Thus, if trigger S_6 is On, all coded 6's examined as "now" bits thereafter in this vertical scan will cause coded 5's to replace the coded 6's. This is accomplished by having the output of AND circuit **856** fed through OR circuit **858** to and AND circuit **860** where it is "anded" with the lead $\overline{B}$ representative of a white "now" bit. An output from AND circuit **860** is fed via OR circuit **810** to AND circuit **812** to cause the writing of 5's if this occurs in the first vertical white zone. Thus, when determination **850**, FIG. 18, is being examined as the white "now" determination coded 6 bit **854** will be the "now" bit and coded 5 **862** will be written into the marking register to replace coded 6 **854**. The other coded 6's in the sixth labelled vertical scan of character E will be replaced by coded 5's in the seventh labelled vertical scan.

It is possible that coded 6's may be erroneously found in the first vertical white zone due to imperfections in the black. This is illustrated best in the character D of FIG. 18.

The presence of the black bit **869** causes coded 6's **866** and **868** to be written, even though it is later determined that the area is not a true second vertical white zone. In this next vertical scan, the coded 6's **866** and **868** are replaced by coded 5's **870** and **872**, since there is no indication that these coded 6's are in a potential upper east bay. This replacement is accomplished by Rule 23 circuit of FIG. 8J by having the lead IN6 and the no potential upper east bay lead "$\overline{C}_{10}$" "anded" at AND circuit **874**. Thus, if there is a coded 6 when there is no potential upper east bay, the Rule 23 circuit will operate to write 5's. AND circuit **874** will produce an output which is fed via OR circuit **858**, the output of which is "anded" with the lead $\overline{B}$ at AND circuit **860** to write the coded 5 as previously described.

It is desirable to replace coded 4's by coded 5's in a condition which is best illustrated in the character G of FIG. 19. It is noted that there is a single south dropout **878** which causes the writing of coded 4's **878** in the third labelled vertical scan of the character G. In the fourth labelled vertical scan the coded 4's will be replaced by coded 5's **880** because no double south dropout has been detected. Thus, in Rule 23 circuit, the lead IN4 is "anded" at AND circuit **882** with the no double south dropout lead "$\overline{C}_0$" to produce an output from AND circuit **882** which is fed to OR circuit **858** which will eventually cause the writing of coded 5's if a lead $\overline{B}$ is present, and the coded 5's are in the first vertical white zone.

The Rule 24 circuit is utilized for assigning coded 6's into the marking register. Basically, coded 6's are written when a minimum white condition exists within the second vertical white zone simultaneous with a coded 1. Just as in Rule 23 circuit, when coded 7's expand southward

the writing of coded 6's must be inhibited. In Rule 24 circuit, lead MWC and IN1 are fed to an AND circuit 884 which has an output that is fed via an OR circuit **886** to an AND circuit **888**. AND circuit **888** has as its other inputs the leads "S_2" and "$\overline{S_3}$" representative of the second vertical white zone. It also has as its inputs the leads "$\overline{C_2}$" and "$\overline{7}_N$ which are inhibitory leads used during the southward expansion of coded 7's which will be described hereinafter. Where there is no inhibiting of coded 7's, the coincidence of the MWC and the coded 1 in the second vertical white zone will produce an output from AND circuit **888** that is fed via an OR circuit **890** to the OUT 6 lead for writing coded 6's in to the marking register.

The presence of a 6 "next" bit with a coded 7 "now" bit permits an effective southward expansion of coded 6's. Thus, in the character S of FIG. 24, when examining determination **892** and **894** as the "now" and "next" determination respectively, the presence of the 1 "now" bit **896** and the 6 "next" bit **898** in the marking register will cause a coded 6 **900** to be assigned as an effective southward expansion of coded 6 **898**.

Now in a special case, it is possible that coded 5's may be erroneously found in the second vertical white zone due to imperfections in the black. This is illustrated best in the character B of FIG. 17 where, because of the white bit **902**, coded 5's **904** are written up into the zone which is later determined to be a second vertical white zone. In the next vertical scan, the coded 5's **904** are replaced by coded 6's **906**, since they are in the second vertical white zone.

This is accomplished by having the lead IN5 and the white "now" lead $\overline{B}$ "anded" at AND circuit **908**, the output of which is connected via OR circuit **886** to AND circuit **888**. At AND circuit **888**, a coincidence with the leads representative of the second vertical white zone, if there is no inhibiting due to southward expansion of coded 7's, causes the coded 6 **906** to be written.

Similarly, it may be that coded 7's are erroneously found in a second vertical white zone due to imperfections in black. This condition is very much like the condition illustrated in the character D of FIG. 18 where the coded 5's replace coded 6's in the first vertical white zone. In a similar manner, coded 6's would replace coded 7's if this type of black imperfection were found in the vertical white zone. This is accomplished in Rule 24 circuit by having the white "now" lead $\overline{B}$ "anded" with the lead IN7 and the not condition of the possible north bay lead "$\overline{C_{15}}$" at AND circuit **910**. Thus, if there is no possible north bay present when the coded 7 and white "now" bit are found in the second vertical white zone, the coded 7's will be replaced by coded 6's because the output of AND circuit **910** is connected via OR circuit **886** to AND circuit **888** where it is "anded" with the lead "S_2" and "$\overline{S_3}$" representative of the second vertical white zone.

In the circuitry described for Rule 24 circuit, where coded 6's expand southward, one of the necessary conditions was that these coded 6's be in the second vertical white zone. The character 5 of FIG. 14 illustrates a special case where it is desirable to expand coded 6's southward in other than the second vertical white zone. An examination of the ninth bit **912** of the tenth vertical scan indicates that this is the first vertical white zone but since there are coded 6's **914** generally to the left which are representative of a potential upper east bay it is undesirable to write coded 5's which may give a lower east bay indication. Therefore, these coded 6's must be expanded southward even though they are in the first vertical white zone and coded 6 **916** is assigned for bit **912**. Thus, if there is a 1 and 6 "next," a potential upper east bay, but no potential lower east bay, and at least an entry into the first vertical white zone, coded 6's will be expanded southward, if there is a white and white "next." In FIG. 8K, the leads IN1, $IN6_N$," "C_{10}," "$\overline{C_{11}}$" and "S_1" representing the required conditions are connected to the input of the AND circuit **918**, as is the lead $\overline{B}_N$. The white "now" requirement is fulfilled by having the output of AND circuit **918** connected via an OR circuit **920** to the input of an AND circuit **922**, the other input of which is the lead $\overline{B}$. The output of AND circuit **922** is connected via OR circuit **890** to the lead OUT 6 for the writing of coded 6's.

Due to imperfections in the black of vertical characters, coded 5's might be found above coded 6's in a particular vertical scan. This condition is indicated in FIG. 14 by a box **924** and in FIG. 25 by a box **926**. Actually, what is desired is that coded 6's replace the coded 5's erroneously found in a previously determined second vertical white zone due to the imperfections in the black. This is accomplished by the Rule 14 circuit (FIG. 8H) and Rule 24 circuit (FIG. 8K). In Rule 14 circuit leads representative of a 6 and 5 "next" and a minimum white height will produce an output from AND circuit **928** to turn On trigger S_{25} at TP time. Thus, in the character S of FIG. 25 when the determinations **930** and **932** are being examined as the white "now" and "next" determinations respectively, the coded 6 and 5 of box **926** are the "now" and "next" bits respectively, and the trigger S_{25} will be On to indicate this condition. Then, when determination **932** is being examined as the white "now" determination, the fact that trigger S_{25} is On will cause a coded 6 **934** to replace the coded 5 of box **926**. This is accomplished by Rule 24 circuit where lead "S_{25}" is connected to an AND circuit **938** where it is "anded" with lead IN5. Thus, when what was the 5 "next" bit is examined, as the 5 "now" bit, if trigger S_{25} is On, an output will be produced from AND circuit **938** which is fed via OR circuit **920** to be "anded" with the white "now" lead $\overline{B}$ at AND circuit **922**, the output of which is fed via OR circuit **890** to lead OUT 6 to write a coded 6 into marking register.

Referring to the character G of FIG. 19, the horizontal black line in the seventh horizontal row between the eighth vertical scan and the thirteenth vertical scan appears to divide the potential middle east bay of the character in half to produce both a potential lower east bay and a potential upper east bay. Then, if the optential lower east bay closes an indication of a partial lower lake is produced, which will be fully described hereinafter. The seventh bit **938** of vertical scan labelled 8 is part of the horizontal black dividing line and when it is detected as a black "next" bit in a potential middle east bay, this is noted. When examining the determinations **940** and **938** as the white "now" and black "next" determinations respectively, 5 "now" and 5 "next" bits **942** and **944** respectively, are present, and so are the determinations of a middle east bay and a minimum white height zone. These conditions are met and a trigger $S_{7.1}$ in Rule 17 circuit (FIG. 8H) is turned On by the inputs IN5, $IN5_N$, $\overline{B}$, B_N, "C_9" (middle east bay) and "S_0" (minimum white height zone) at AND circuit **945**. Leads "$S_{7.1}$" in a positive condition then represents the fact that the middle east bay might be divided and a determination must then be made as to whether there is white above the black to indicate that the black line does actually divide the middle east bay. Therefore, later in the vertical scan, if a minimum white height is examined in the form of white "now" determination **946** and white "next" determination **948**, when 5 "now" and 5 "next" bits **950** and **952** respectively are present, a possible partial lower lake indication is produced. A trigger C_5 of Rule 18 circuit (FIG. 8I) is turned On to signify the presence of all these conditions by an AND circuit **954** which has as input leads IN5, $IN5_N$, $\overline{B}$ & $\overline{B}_N$ and "$S_{7.1}$." To determine if the upper east bay closes, a coded 6 **956** must then be written to replace the coded 5 **950** because this is the second vertical white zone. This is accomplished by the AND circuit **908** of Rule 24 circuit which requires a 5 "now" and white "now" indication to write a coded 6 in the second vertical white zone, as hereinbefore described. Further descrip-

tion of the partial lower lake will be described hereinafter.

Rule 25 circuit (FIG. 8L) is utilized for assigning coded 7's. Coded 7's are generally used for indicating north bays and they are generally written in the third vertical white zone if there is a history of black to the left. The only characters of the generally utilized characters of FIG. 11 that has a third vertical white zone with black to the left is the character X **958** which has a third vertical white zone **960** having black to the left. Since the zone **960** in the character X is a north bay, it is permissible to write coded 7's as soon as this zone is detected, so that coded 5's and 6's can be utilized for detecting other zones in the character. Thus, in Rule 25 circuit a minimum white condition, MWC, and 1 "now" bit in the third vertical white zone represented by lead "S_3" will produce an output from an AND circuit **962** which is fed via an OR circuit **964** to the lead OUT 7 which causes coded 7's to be written into the marking register. As hereinbefore described, the more usual the case in which coded 7's are written takes place when there is a double dropout to the north, in which case coded 7's would replace coded 5's or 6's. The coded 7's are an indication of this double dropout and are written so that other coded 5's and 6's can then be put into use for indications of such things as east bays. This is illustrated in the character X of FIG. 30, where the coded 7's **966** are shown in the north bay replacing coded 5's **968**. In the sixteenth vertical scan when the north bay closes to the right, the fact that coded 5's **970** exist would prevent an indication of the fact that the north bay in closing. Later, the coded 5's **970** are used for detecting the middle east bay. To accomplish the replacing of coded 5's by coded 7's, the lead IN5 is fed (in Rule 25 circuit) via an OR circuit **972** to one input of an AND circuit **974**, the other input of which comes from an OR circuit **976**. The inputs of OR circuits **976** are the double dropout to the north from the first vertical white zone lead "C_1" and a possible north bay lead "C_{15}," either of which produces an output from OR circuit **976**. A coincidence at the input of AND circuit **974** produces a signal which is fed via an OR circuit **978**, the output of which is "anded" with the white "now" lead $\overline{B}$ at AND circuit **980** to produce an output which is fed to OR circuit **964** to write a coded 7 in the marking register. An illustration of coded 7's replacing coded 5's was described hereinbefore in relation to the description of FIG. 35. The character H of FIG. 20 illustrates that there is a possibility that coded 6's may be in the first vertical white zone. The coded 6's **982** in the first vertical white zone of tenth labelled vertical scan are shown being replaced by the coded 7's **984**, in the eleventh vertical scan. Thus, the lead IN6 is "ored" at OR circuit **972** with the lead IN5 to produce the writing of coded 7's, as described.

To take care of the possibility of coded 7's replacing coded 6's in the second vertical white zone such as in the example of the character Y of FIG. 31 where the coded 7's **986** replace the coded 6's **988**, the lead IN6 in Rule 25 circuit is fed via an OR circuit **990** to an AND circuit **992** where it is "anded" with the condition of a double north dropout from the second vertical white zone lead "C_2" or a possible north bay lead "C_{15}" from an OR circuit **994**. The output of AND circuit **992** is fed via OR circuit **978** to the input of AND circuit **980** where it is "anded" with the lead $\overline{B}$ to produce an output which will write coded 7's in the marking register.

As has been described hereinbefore, coded 7's may expand southward as illustrated by the coded 7's **996** of FIG. 23. This southward expansion of coded 7's is performed in Rule 25 circuit by the lead IN1 and lead $IN7_N$ being "anded" at an AND circuit **998** to be fed to OR circuit **972**. Therefore, a coded 7 will be expanded southward if a white "now" bit ($\overline{B}$ at AND circuit **980**) and a possibility of a double dropout to the north or possible north bay (leads "C_1" and "C_{15}" at OR circuit **976**) has been detected as previously described. The southward expansions of coded 7's in the second vertical white zone is acomplished by the leads IN1 and IN7 being "anded" at an AND circuit **1000** and being fed to OR circuit **990**.

It is not necessary to expand coded 7's southward in the third vertical white zone because a minimum white height found in a third vertical white zone to the right of a coded 1 will automatically be written as a coded 7 by the circuitry at the top of Rule 25 circuit as hereinbefore described.

Rule circuits—West bays

Rule 26 circuit to Rule 35 circuit inclusive (FIGS. 8L to 8N) relate to the recognition of the three west bays, MWB, UWB and LWB. In detecting west bays, the rule circuits first look for west inlets. A west inlet differs from a west bay only in that a bay is definitely closed to the right by black. It is obvious, that in the characters of FIG. 11 if there is a west inlet indication, the west inlet will be closed by black to the right before the end of character due to the fact that there are no discontinuous characters, and therefore it is not actually necessary to look for the closing to the right. However, if the described teachings were applied to recognition of lower case letters and other discontinuous symbols such as i and =, etc., and inlet might be considered as a recognition criteria distinct from a bay. In the rule circuits shown in the drawings, the west inlet indications are utilized only as a step in the detection of a west bay. Generally then, Rule 26 circuit to Rule 35 circuit inclusive, first look for a 2 x 2 bit white area, in the first vertical white zone, and blocked above by black. This then, becomes a possible middle west inlet indication, and when this inlet is closed to the right by black, a middle west bay is indicated. If during any vertical scan in which a possible middle west inlet is detected, an upper west inlet UW1 or a potential upper east bay UEB is detected, the middle west inlet indication is reset, and a lower west inlet indication is also produced. If the upper west inlet or the lower west inlet is closed to the right, an upper west bay UWB or lower west bay LWB, respectively, is indicated.

Rule 26 circuit contains a trigger S_8 which is utilized for indicating a 2 x 2 bit white area in the first vertical white zone and with no history of black to the left. Trigger S_8 is turned On by a positive signal from an AND circuit **1002** produced by a coincidence of positive signals on its six input leads. The two input leads IN2 and $IN2_N$ are representative of the fact that there was a minimum white height in the previous vertical scan, and that this minimum white height had no history of black to the left and was in the first vertical white zone. Three other input leads $\overline{B}$ & $\overline{B}_N$, "S_1" and "$\overline{S}_2$" are representative of a minimum white height in the first vertical white zone, and a coincidence of signals on the five input leads with the sixth TP lead input turns On trigger S_8 to represent the 2 x 2 bit white area.

Rule 27 circuit is utilized for detecting a possible middle west inlet representative of the fact that the 2 x 2 white bit area of Rule 26 circuit is blocked by black to the north. Thus, the lead "S_8" representative of the 2 x 2 bit white area of Rule 26 circuit is connected to one of the inputs of an AND circuit **1004**, another input of which is the lead "$\overline{C}_8$" representative of no lower west inlet indication. The other two inputs of AND circuit **1004** will both be positive only if both the present scan and the previous scan are blocked by black to the north. Thus, one of these input leads is from an OR circuit **1006** having in turn as its inputs the leads IN1 and $IN1_N$, and the other input is connected to an OR circuit **1008** having as its input the leads B and B_N. Thus, if a coded 1 and a B, or a coded 1 and a B_N, or a coded 1_N and a B_N, or a coded 1_N and a B are present, it is an indication that the 2 x 2 bit of Rule 26 circuit is blocked to the north. The different possible arrangements of blocking by black to the north are illustrated in the character 9 of FIG. 16. The detecting of the black bit **1010** in the fourth vertical

scan produces a 1 bit **1012**. In the fifth vertical scan, when examining black bit **1014** as the "now" bit (B), the marking register contains bit **1010** as the "next" bit (I_N), and it is thus obvious that the coded 2's of the fourth and fifth vertical scan are blocked by black to the north by this arrangement of 1_N and B. Similarly, 1_N and B_N produces in the illustration of FIG. 16 a blocking by black **1016**, and the 1 and B_N produces a blocking by black **1018**. At the coincidence of input signals, a positive signal will appear at the output of AND circuit **1004** or Rule 27 circuit to turn On triggers S_{30} and C_6. Trigger C_6 in the On condition is representative of a possible middle west inlet which will become a bona fide middle west bay if it is blocked to the right by black. The trigger S_{30} which is reset at the end of each scan, is used as the indication of a potential middle west inlet determined during each vertical scan.

Rule 28 circuit and Rule 29 circuit of FIG. 8M are utilized for indicating a closure of the middle west inlet to the right, to thus signify a middle west bay MWB. In Rule 28 circuit, leads B and B_N are fed via an OR circuit **1020** to an AND circuit **1022**, the other two leads of which are IN2 and "$\overline{S}_0$." The 2 and (B or B_N) signifies that there is some black generally to the right of the coded 2, and the "$\overline{S}_0$" lead represents the fact that a minimum white height has not yet been detected in the vertical white zone containing the coded 2 in the present vertical scan. A coincidence of the three input signals on AND circuit **1022** at TP time will turn On a trigger S_{20} to signify a possible closure to the right. If a minimum white height is detected thereafter during the present vertical scan, the MWH zone trigger S_0 going On will cause the A.C. reset of trigger S_{20} via A.C. Input circuit **1024** and end the possibility of a closure to the right indication for this zone in the scan.

Thereafter, in this vertical scan, if a coded $\overline{2}$ and $\overline{2}_N$ are detected, it is indicative of the scan closure by black to the north because in order to change from a coded 2 to a coded $\overline{2}$ during a vertical scan, a black bit must appear. If when the $\overline{2}$ and $\overline{2}_N$ are detected, the possible closure to the right trigger S_{20} and the MWI trigger C_6 have not been reset, a trigger $C_{6.1}$ in Rule 29 circuit will be turned On to signify a bona fide middle west bay. This is accomplished by having the leads IN2 and $IN2_N$ fed via inverters **1026** and **1028** respectively, to leads $\overline{2}$ and $\overline{2}_N$ respectively which are two of the input leads of an AND circuit **1030**. Leads "S_{20}" and "C_6" are also connected as inputs to AND circuit **1030** which will produce a signal at a coincidence of its inputs at TP time to turn On MWB trigger $C_{6.1}$.

The character J of FIG. 21 illustrates a closure to the right of a middle west inlet, to produce the middle west bay indication. In the twenty-first vertical scan, when the black bit **1032**, is being examined as a "now" bit, a coded 2 **1034** will be the "now" bit and the trigger "S_0" will be Off to indicate no minimum white height zone. From the examination of the black bit **1032** until the examination of the thirteenth bit **1036**, there is no minimum white height zone detected, and so MWH zone trigger "S_0" is not turned On to reset trigger S_{20}. Also, there has been nothing detected to cause a change from the middle west inlet indication to a lower west inlet and so trigger C_6 is still On. Then when the black bit **1038** is being examined as a "now" determination, the bit **1040** are $\overline{2}$ and $\overline{2}_N$ (actually 1 and 3_N) and since triggers C_6 and S_{20} are On, Rule circuit 29 acts to turn On trigger $C_{6.1}$ to indicate a middle west bay.

The character X of FIG. 30 also illustrates the detection of a middle west bay. In the eighth vertical scan, the examination of the seventh black bit **1042** as a "now" bit when the coded 2 **1044** is detected turns On the possible closure of the right trigger S_{20}. Since the eighth and ninth bits **1046** are white, MWH zone trigger S_0 will go on to reset possible closure to the right trigger S_{20}. Thus, when the eleventh and twelfth bits **1048** are examined, and the $\overline{2}$ and $\overline{2}_N$ **1050** are MWB trigger $C_{6.1}$ will not be turned On because possible closure to the right trigger S_{20} is Off. However, in the next vertical scan, when the ninth bits **1052** is being examined, the possible closure to the right trigger S_{20} will turn On because of the coded 2 **1054**. Now when the eleventh and twelfth bits **1056** are examined, bits **1058** are $\overline{2}$ and $\overline{2}_N$ since there was no minimum white height to turn On trigger S_0, the MWB trigger $C_{6.1}$ will turn On to indicate a middle west bay. Thus, it is evident, that a single white bit like **1052** is not enough to prevent a closure to the right, and so imperfections in the character of one bit will be ignored. Rule 30 circuit and Rule 31 circuit detect an upper west inlet UWI by recognizing a 2 x 2 bit white area of coded 3's blocked by black to the north by similar circuitry as that utilized by Rule 26 circuit and Rule 27 circuit for detecting a middle west inlet MWI. The upper west inlet UWI is therefore indicated by the turning On of trigger C_7 of Rule 31 circuit. It is to be noted that trigger C_7 is reset only by lead X_c at the end of character. Rule 32 circuit then turns On a trigger S_{21} as an indication of black to the right of coded 3 in the same manner that Rule 28 circuit detects black to the right of a coded 2.

The actual closure to the right by black of an UWI to indicate an UWB is performed in a slightly different manner by Rule 33 circuit than that described for the indication of a MWB by Rule 29 circuit. The difficulty is that coded 3's may exist in both the second and third vertical white zones, and therefore, if in the vertical scan before the closure by black to the right, the black to the north is only one bit high, there may never exist a $\overline{3}$ and $\overline{3}_N$, and therefore there would be no UWB indicated. This is illustrated in the character 3 of FIG. 13, where in the ninth vertical scan, during the examination of the thirteenth black bit **1058** as the "now" bit a 3_N bit **1060** exists. Therefore, Rule 33 circuit (FIG. 8N) requires a 3 and $\overline{3}_N$ and B_N in addition to S_{21} and C_7 to turn On a trigger $C_{7.1}$ as an indication of an UWB. The 3 and $\overline{3}_N$ **1062** of FIG. 3, plus the black bit **1058** as the "next" bit to insure that there is no sneaking of coded 3's diagonally upward, is enough to indicate the blocking to the right.

Rule 34 circuit detects a lower west inlet LWI by recognizing the presence of either an upper west inlet or a potential upper east bay during a vertical scan in which a middle west inlet has been found. This is an indication that the middle west inlet is actually a lower west inlet and so the middle west indication must be reset. Thus, in Rule 34 circuit, either the lead "C_7" representative of an upper west inlet UWI, or the lead "C_{10}" representative of a potential upper east bay as will be described hereinafter, will produce an output signal from an OR circuit **1064**. This output signal is "anded" at AND circuit **1066** with the lead "S_9" representative of a middle west inlet during the present vertical scan to produce an output signal which turns On a trigger C_8 as an indication of a lower west inlet. The lead "C_8" from trigger C_8 is utilized in Rule 27 circuit (FIG. 8L) to A.C. reset (via A.C. input circuit **1068**) the triggers C_6 and S_9 which are representative of the possible middle west inlet. Triggers C_6 and S_9 are also reset by other circuitry which is described hereinafter in the section on east bays and lakes.

If there is a closure to the right, the lower west inlet becomes a lower west bay. This is accomplished by Rule 35 circuit which operates to turn On a trigger $C_{8.1}$ indicative of a lower west bay. Trigger $C_{8.1}$ is turned On by a coincidence of leads $\overline{2}$, $\overline{2}_N$, "S_{20}" and "C_8" to indicate the closure for the same reasons described in the closure of the middle west inlet in the Rule 29 circuit and therefore needs no further explanation.

Rule circuits—East bays and lakes

Rule 36 circuit to Rule 46 circuit inclusive (FIGS. 8N through 8P) relate to the recognition of the three east

bays, MEB, UEB, and LEB, and the lakes ML, UL, LL and the partial power lake PLL. The circuitry for recognizing the east bays and lakes are analogous to those for recognizing west inlets and west bays, in that first potential east bays are detected and if these east bays are blocked by black to the right, a lake is then indicated. However, after an indication of a lake is made, the particular east bay which closed to the right to produce the like indication acts to remove the respective east bay indication. Rule 36 circuit is utilized to indicate a 2 x 2 bit white area in the first vertical white zone and with a history of black to the left. Rule 36 circuit therefore, looks for a coded 5 and 5_N as an indication of a history of black to the left in the first vertical white zone, as hereinbefore described. It also takes into account the special case where a character A might have a long enough lower left serif to produce a coded 6 and 6_N in the lake of the character A. Since the lake in the character A might be fairly small, if the next vertical scan examines the 6 and 6_N along with a $\overline{B}$ and $\overline{B}_N$ while in the first vertical white zone. A legitimate 2 x 2 bit white area is indicated by Rule 36 circuit. A trigger S_{11} of Rule 36 circuit, indicative of this 2 x 2 bit white area, is turned On by a positive signal from an AND circuit **1070** produced by a coincidence of positive signals on its input leads. One of the input leads of AND circuit **1070** is from an OR circuit **1072**. Leads IN5 and $IN5_N$ representative of the existence of a minimum white height in the previous vertical scan and that this minimum white height had a history of black to the left, are connected to an AND circuit **1074**, the output of which feeds OR circuit **1072**. Leads IN6 and $IN6_N$ for reasons just described are also connected to an AND circuit **1076**, the output of which also feeds OR circuit **1070**. The input leads, of AND circuit **1070**, $\overline{B}$ & $\overline{B}_N$, "S_1" and "$\overline{S}_2$" are representative of a minimum white height in the first vertical white zone of the present vertical scan. The one other necessary condition to make AND circuit **1070** produce a positive signal is a lead "$\overline{C}_{10}$" representative of an absence of a potential upper east bay. The lead "$\overline{C}_{10}$" is necessary to prevent a possible middle east bay indication, especially in a character 6 where the upper east bay of the character extends out beyond the lake portion, a condition which might cause an erroneous middle east bay indication.

Rule 37 circuit is utilized for detecting a possible middle east bay, indicative of the fact that the 2 x 2 white bit arear of Rule 36 circuit is blocked by black to the north. The triggers S_{32} and C_9 are turned On to indicate a blocking to the north in a manner similar to that described for Rule 27 circuit and need not be further described except to note that the lead "S_{11}" to an AND circuit **1078**, which turns On triggers C_9 and S_{32} represents the 2 x 2 bits white area of Rule 36 circuit, and lead "$\overline{C}_{11}$" represents an absence of a potential lower east bay.

The possible MEB triggers C_9 and S_{32} are reset by a number of different conditions which will be described in detail after a description of the turning On of the triggers that indicate the other east bays and lakes.

To detect a potential upper east bay, Rule 38 circuit is utilized for indicating a 2 x 2 bit white area in the second vertical white zone having a history of black to the left. The leads "S_2," "$\overline{S}_3$," IN6, $IN6_N$, and $\overline{B}$ & $\overline{B}_N$ are thus connected via an AND circuit **1080** to turn On a trigger S_{26} indicative of this 2 x 2 white bit area. In Rule 39 circuit, a closure to the north of this 2 x 2 white bit area of Rule 38 circuit produces a potential UEB indication. This is accomplished by "anding" at an AND circuit **1082**, the lead "S_{26}" with the output from a pair of OR circuits **1084** and **1086**. OR circuit **1084** has as its inputs the leads IN1 and $IN1_N$, and OR circuit **1086** has as its inputs the leads B and B_N. This combination of circuitry indicates a closure to the north, in the same manner as the equivalent circuitry of Rule 31 circuitry, by producing an output from AND circuit **1082** which is fed via an OR circuit **1088** and an AND circuit **1090** for proper timing to the potential UEB triggers C_{10} and S_{33}.

Similarly, Rule 40 circuit operates to indicate a potential lower east bay in a manner similar to the lower west inlet indication of Rule 34 circuit. It recognizes the presence of either an upper west inlet or a potential east bay during a vertical scan in which a possible middle east inlet has been found. Thus, in Rule 40 circuit, either the lead "C_7" representative of an upper west inlet UWI, or the lead "C_{10}" representative of a potential upper east bay, will produce an output signal from an OR circuit **1092**. This output signal is "anded" at AND circuit **1094** with the lead "S_{32}," representative of a middle east bay during the present vertical scan, to produce an output signal which feeds through an OR circuit **1096**, the output of which is "anded" with timing lead TP at AND circuit **1098** to turn On trigger C_{11} as an indication of a potential lower east bay.

When a possible partial lower lake is detected, it is desirable to turn On triggers indicative of a potential upper east bay and potential lower east bay, and if the lower east bay is closed by black to the right while the upper east bay remains open, a bona fide partial lower lake is indicated. Therefore, lead "C_5" and "$S_{7.1}$" from Rule 17 circuit and Rule 18 circuit indicative of a possible partial lower lake are "anded" in Rule 39 circuit at an AND circuit **1100**, the output of which is applied through OR circuit **1088** and AND circuit **1090** to turn On the trigger C_{10}, representative of a potential upper east bay. Lead "C_5" and "$S_{7.1}$" are also "anded" in Rule 40 circuit at an AND circuit **1102**, the output of which is applied through OR circuit **1096**, and AND circuit **1098** to turn On the trigger C_{11}, representative of a potential lower east bay.

Rule 41 circuit and Rule 42 circuit are utilized for indicating a closure of the possible middle east bay to the right to thus signify a bona fide middle lake, ML. These two circuits operate to detect a blocking of coded 5's to the right in a manner similar to that described for a blocking to the right in Rule 28 circuit and Rule 29 circuit. In Rule 41 circuit, leads B and B_N are fed via an OR circuit **1104** to an AND circuit **1106**, the other two leads of which are leads IN5 and "$\overline{S}_0$." The coded 5 and (B or B_N) signifies that there is some black to the right of the coded 5, and the "S_0" lead represents the fact that a minimum white height has not yet been detected in the vertical white zone of the present vertical scan. A coincidence of the three input signals on AND circuit **1106**, at TP time, will turn On a trigger S_{13} to signify a possible closure to the right. If a minimum white height is detected thereafter during the present vertical scan, the MWH zone trigger S_0 going On will cause the A.C. reset of trigger S_{13} via an A.C. reset circuit **1108**. Thereafter, in this vertical scan if a $\overline{5}$ and $\overline{5}_N$ are detected representative of the scan closure by black to the north and the triggers S_{13} and C_9 (representative of a possible MEB) have not yet been reset, a trigger C_{12}, in Rule 42 circuit, will be turned On to signify a closure to the right and therefore a bona fide middle lake. This is accomplished by feeding leads IN5 and $IN5_N$ via inverters **1110** and **1112** respectively, to an AND circuit **1114** where they are "anded" with the lead "S_{13}" and "C_9" for producing a signal at TP time for turning On ML trigger C_{12}. The actual closure to the right by black of a potential upper east bay to indicate a bona fide upper like is accomplished by Rule 43 and Rule 44 circuit, which operates in a manner similar to that of Rule 41 circuit and Rule 42 circuit except that a closure to the right of coded 6's instead of coded 5's is indicated. Rule 43 circuit operates to turn On a trigger S_{15} indicative of a possible closure by black, and Rule 44 circuit is turned On by a coincidence of signals on leads $\overline{6}$, $\overline{6}_N$, "S_{15}" and "C_{10}" applied to an AND cir-

cuit **1116** in Rule 44 circuit for turning On trigger C_{13} indicative of the bona fide upper lake. Lead "C_{10}" is representative of a potential upper east bay. Thus, in the vertical scan in which trigger S_{15} is turned On, if a $\overline{6}$ and $\overline{6}_N$ are detected representative of the scan closure by black to the north, and the triggers S_{15} and C_{10} (potential UEB) have not been reset, the trigger C_{13} in Rule 44 circuit will be turned On to signify the bona fide upper lake.

If a potential lower east bay as indicated by lead "C_{11}" is closed to the right and there is no potential partial lower lake indication ($\overline{C}_5$), a bona fide lower lake indication is produced. This is accomplished by Rule 45 circuit which operates to turn On a trigger C_{14}, indicative of the bona fide lower lake. Lower lake trigger C_{14} is turned On by a coincidence of signals on leads $\overline{5}$, $\overline{5}_N$, "S_{13}" and "C_{11}" at an AND circuit **1118** (to indicate the closure for the same reasons described in the closure of the middle east bay in the Rule 42 circuit) plus a signal on lead "$\overline{C}_5$" (no potential PLL). Where, however, there is a possible partial lower lake indication and all the other conditions of Rule 45 circuit, a bona fide partial lower lake will be indicated. Therefore, AND circuit **1120** of Rule 46 circuit has all the same input conditions as AND circuit **1118** of Rule 45 circuit, except the lead "C_5" instead of the lead "$\overline{C}_5$" and a coincidence of all the input signals turns On a trigger $C_{14.1}$ indicative of a bona fide partial lower lake.

In addition to the means for changing west inlets to west bays, and east bays to lakes, means are provided for changing "middle" criteria indications to "upper" and "lower." In the character 3 of FIG. 13, in the fifth vertical scan, an MWI indication will be produced when the eighth bit **1122** is being examined as the "next" bit. Then, when the thirteenth bit **1124** is being examined as the "next" bit, an UWI indication is produced. This means that the MWI indication must be changed to an LWI indication. This is accomplished by having the UWI indication turn On the LWI trigger which in going On causes the resetting of MWI trigger. Thus, in Rule 34 circuit of FIG. 8N, the UWI lead "C_7" and the MWI in that vertical scan lead "S_{30}" turn On LWI trigger C_8. Lead "C_8" then is fed to Rule 27 circuit for resetting the possible MWI triggers C_6 and S_{30} via the A.C. Input **1068**.

Similarly, a possible MEB indication may be changed, as illustrated in character F of FIG. 19. In the ninth vertical scan a possible MEB indication will be produced when the eighth bit **1126** is being examined at the "next" bit. Then when the thirteenth bit **1128** is being examined as the "next" bit, a potential UEB indication is produced. In this case, the potential MEB indication must be changed to a potential LEB indication, and this is accomplished by having the potential UEB indication turn On the potential LEB trigger which, in going On, causes the resetting of the possible MEB trigger. Thus, in Rule 40 circuit of FIG. 80, the UWI lead "C_7" and the "possible MEB in that vertical scan" lead "S_{32}" turn On potential LEB trigger C_{11}. Potential LEB lead "C_{11}" then is fed to Rule 37 circuit of FIG. 8N and via an A.C. OR circuit **1129**, for resetting the possible MEB triggers C_9 and S_{32}.

In a character such as the character 5 of FIG. 11, it is possible to have an MWI indication followed by a UEB indication. In this case, the UEB indication must turn On the LWI trigger which in turn rests the MWI trigger. Thus, in Rule 34 circuit the UEB lead "C_{10}" and the "MWI in that vertical scan" lead "S_{30}" turn On LWI trigger C_6 and S_{30} in Rule 27 circuit. In the same way, in the character 2 of FIG. 11, it is possible to have an MEB indication followed by a UWI indication. The UWI indication must turn On the LEB trigger which, in turn, must reset the MEB trigger. Thus, in Rule 40 circuit the UWI lead "C_7" and the "MEB in this vertical scan" lead "S_{32}" turn On the potential LEB trigger C_{11}. Lead "C_{11}" is then fed to Rule 37 circuit for resetting the possible MEB triggers C_9 and S_{32}.

A character 2 of FIG. 12 illustrates a special case where a MWI is detected first followed by the detection in a latter scan of an MEB. Thus, in the twenty-ninth vertical scan when the thirteenth bit **1130** is being examined as the "next" bit, an MWI indication is produced. In the thirteenth vertical scan when bit **1131** is being examined as the "now" determination of coded 2 **1132** is detected in the second vertical white zone before the MEB in that vertical scan lead S_{32} is turned On. This indicates that there is a zone below the MWI and the detection of this condition will cause the resetting of the MWI. Thus, in Rule 27 circuit of FIG. 8L, the 2 "now" lead IN2, the second vertical white zone leads "S_2" and "$\overline{S}_3$," and the no MWI in this vertical scan lead "$\overline{S}_{30}$" are "anded" at an AND circuit **1134**. A coincidence of input signals at TP time produces an output signal from AND circuit **1134** which is fed via an OR circuit **1136** to reset the possible MWI trigger C_6. Then in the next vertical scan an MEB followed by a UWI are detected, and the LEB trigger is turned On and the MEB trigger is reset in the same manner in the character 2 in which an MEB is detected before a UWI as described hereinbefore.

Similarly, in the character 5 of FIG. 11, if the lower black border of the LWB is a short one, coded 5's will be written in the UEB and an MEB indication will be produced first. Some vertical scans later when the lower black border is detected during a vertical scan the coded 5's of the MEB will be in the second vertical white zone. This causes the reset of the possible MEB trigger C_9 of Rule 37 circuit, by a coincidence of input signals and the 5 "now" lead IN5, the second vertical white zone leads "S_2" and "$\overline{S}_3$" and no MEB in this vertical scan lead "S_{32}" at an AND circuit **1138**. At TP time the output signal is fed via an OR circuit **1140** to reset the possible MEB trigger C_9. Then the "next" vertical scan an MWI followed by a UEB are detected and the LWI trigger is turned On and the MWI trigger is reset in the character 5 in which an MWI is detected before a UEB, as described hereinbefore in this section.

As previously described, it is not necessary in the preferred embodiment to reset the west inlets when it is determined that they are closed by black to the right to form this respective west bays. However, in certain characters, in the embodiment shown, it is important in distinguishing between these characteristics to determine whether they contain an east bay or a lake. Therefore, it is necessary to rest the east bay when its respective lake is detected. In Rule 39 circuit, the upper lake lead "C_{13}" is fed via an A.C. OR circuit **1142** to the potential UEB trigger C_{10} and S_{33} to provide an A.C. reset. In Rule 40 circuit the lower lake lead "C_{14}" and the partial lower lake lead "$C_{14.1}$" are fed via an A.C. OR circuit **1144** to the potential LEB trigger C_{11} to accomplish the A.C. reset. The middle lake, lower lake and possible partial lower lake reset the possible MEB in Rule 37 circuit by having the ML lead "C_{12}," the LL lead "C_{14}," and the possible PLL lead "$C_{14.1}$" (not shown) fed via A.C. OR circuit **1129** to the MEB triggers C_9 and S_{32}.

Since a study of FIGS. 10A and 10B will show that east bays must be distinguished from south bays and north bays, it is necessary that wherever serifs in a character cause indications of east bays which are later determined to be north or south bays, that the east bay be reset. This condition is well illustrated in the character H of FIG. 20 where the white regions **1146** and **1148** produce indications of lower east bay and upper east bay respectively. After a south bay **1150** is detected, the lower east bay **1146** indication must be reset, and after a north bay **1152** is detected, the upper east bay **1148** indication is reset. Actually, the LEB trigger C_{11} of Rule 40 circuit is reset by both a south bay lead "C_{18}" and a 2 south bay or peninsula in a south bay lead "C_{19}"

fed via A.C. OR circuit **1144** to LEB trigger C_{11}. The UEB trigger C_{10} of Rule 39 circuit is reset by both a north bay lead "C_{16}" and a 2 north bays or peninsula in a north bay lead "C_{17}" fed via A.C. OR circuit **1142** to UEB trigger C_{10}. Since it is possible that a middle east bay may drop out to the north or south, not only the north bay lead "C_{16}" and "C_{17}" are fed via A.C. OR circuit **1129** of Rule 37 circuit to reset MEB triggers C_9 and S_{32}. An illustration of a MEB becoming a north bay is in the character U of FIG. 28 where the MEB **1154** becomes a north bay **1156**. An illustration of a MEB becoming a south bay is in the character K of FIG. 22 where the MEB **1158** becomes a south bay **1160**.

Since expanding coded 2's southward is relatively slow compared to a northward expansion, it might be possible in a character 3, for example, for a serif to protrude upward far enough so as to cause some coded 5's to be written in what should actually be a LWB, and yet not far enough upward to close the LWB to the left. Then, in the next vertical scan a minimum white area of coded 5's in the first vertical white zone will appear before the coded 5's can be replaced by the southward expansion of the coded 2's, and when black is detected blocking the 2 x 2 coded 5's, the possible MEB trigger C_9 would be turned On. To prevent this, if a minimum white area of coded 2's is found in the first vertical white zone (turning On trigger S_8), it will reset the trigger S_{11} representing the minimum white area of coded 5's in the first vertical white zone. Thus, trigger S_{11} will not be On when the black blocking the subject minimum white areas to the north is detected and no possible MEB indication is produced. This is accomplised in Rule 36 circuit by feeding lead "S_8" via an A.C. Input circuit **1161** to the A.C. reset input of trigger S_{11}.

Rule circuits—North bays, south bays and peninsulas

Rule 47 circuit to Rule 55 circuit inclusive (FIGS. 8P through 8S) relate to the recognition of the recognition criteria, north bay, two north bays or a peninsula in a north bay, south bay, two south bays or a peninsula in a south bay.

There are a number of different methods for detecting a north bay, and these methods will now be described in conjunction with Rule 47 circuit to Rule 49 circuit inclusive. Firstly, since coded 7's of necessity, indicate an opening to the north if a 2 x 2 bit area of coded 7's is closed to the right, it is an indication of a north bay. Thus, Rule 47 circuit indicates a 2 x 2 white bit area of coded 7's by lead IN7 and $IN7_N$, and $\overline{B}$ & $\overline{B}_N$ connected to AND circuit **1162**. A coincidence of input signals at TP time produces an output signal at TP time which is fed via an OR circuit **1164** to turn On a trigger C_{15}. Then, Rule 48 circuit indicates a possible closure of coded 7's to the right by the leads B or B_N from an OR circuit **1166**, the output of which is "anded" at the input of AND circuit **1168** with the leads IN7 and "$\overline{S}_0$." This possible closure circuit operates in the same way as possible closures to the right circuits (such as Rule 28 circuit and Rule 32 circuit, etc.) previously described. The output of AND circuit **1168** therefore, turns On trigger S_{17} as an indication of the possible closure to the right. Thus, later in this same scan , when coded $\overline{7}$ "now" and $\overline{7}_N$ "next" are detected, if the triggers S_{17} and C_{15} are still On, this will indicate a closure to the right and therefore, a bona fide north bay. The leads $\overline{7}$ and $\overline{7}_N$ are connected to the input of an AND circuit **1170** and fed at TP time via an OR circuit **1172** to an AND circuit **1174** where they are "anded" with the leads "S_{17}" and "C_{15}". The output of AND circuit **1174** is connected via an OR circuit **1176** to the bona fide north bay trigger C_{16}. Since this indication of a north bay may be fairly high up in the vertical scan, it may be that the 2 x 2 bit white area of 7's will not have enough room at the top of the scan for both a $\overline{7}$ and $\overline{7}_N$. Therefore, if at the end of the vertical scan, both the triggers S_{17} and C_{15} are On, that will also be an indication of a bona fide north bay. Thus, the end of vertical scan lead X_s is "ored" at OR circuit **1172** with the lead $\overline{7}$ and $\overline{7}_N$ in Rule 49 circuit to provide this indication.

A north bay may also be indicated by 2 x 2 bits of coded 6's or 5's where there is a double dropout of these coded numbers to the north and a closure to the right. Thus, the lead "S_{11}" from Rule 36 circuit which indicates 2 x 2 bit coded 5's or 2 x 2 bit coded 6's in a first vertical white zone, as previously described is "anded" at an AND circuit **1178** at Rule 47 circuit with the leads X_s, "S_{23}," and "C_3." The three leads X_s "S_{23}" and "C_3" are also shown "anded" in Rule 8 circuit to indicate a double dropout to the north from zone 1. Thus, AND circuit **1178** will produce an output signal if there is a 2 x 2 bit coded 5's and a double dropout to the north from zone 1, or a 2 x 2 bit coded 6's and a double dropout to the north from zone 1. This output signal will turn On trigger C_{15}. In this case to indicate closure to the right and therefore a north bay, somewhat different circuitry is utilized. To detect the closure of the coded 5's to the right, the possible closure to the right of coded 5's lead "S_{13}" from Rule 41 circuit is utilized in Rule 49 circuit. In Rule 49 circuit, then, the leads "C_{15}" and "S_{13}" are "anded" at an AND circuit **1180** with the double north dropout from zone 1 lead "C_1" and the output of an OR circuit **1182**. OR circuit **1182** has one of its inputs connected to an AND circuit **1184** which produces an output for $\overline{5}$ and $\overline{5}_N$. Therefore, when the $\overline{5}$ and $\overline{5}_N$ is detected if the possible closure lead "S_{13}" is positive and the other conditions are met an output signal will be produced from AND circuit **1180** which is fed via OR circuit **1176** to turn On NB trigger C_{16}.

If at the end of a vertical scan lead "S_{13}" is still positive and all the other conditions at AND circuit **1180** are met, this is an indication of a closure to the right and therefore a north bay. Thus, the end of a vertical scan lead X_s is "ored" at OR circuit **1182** with the lead $\overline{5}$ and $\overline{5}_N$ to provide this indication.

To detect the closure of the coded 6's to the right, a possible closure to the right of coded 6's lead "S_{15}" from Rule 43 circuit is utilized in Rule 49 circuit. For this, the leads "C_{15}" and "S_{15}" are "anded" at an AND circuit **1186** with a double north dropout from zone one lead "C_1" (via an OR circuit **1188**), and the output of an OR circuit **1190** has one of its inputs connected to an AND circuit **1182** which produces an output signal for $\overline{6}$ and $\overline{6}_N$. Therefore, when the $\overline{6}$ and $\overline{6}_N$ is detected, if the possible closure lead "S_{15}" is positive and the other conditions are met, an output signal will be produced from AND circuit **1186** which is fed via OR circuit **1176** to turn On NB trigger C_{16}.

If at the end of a vertical scan lead "S_{15}" is still positive and all the other conditions at AND circuit **1186** are met, this is an indication of a closure to the right and therefore a north bay. Thus, the end of vertical scan lead X_s is "ored" at OR circuit **1190** with the lead $\overline{6}$ and $\overline{6}_N$ to provide this indication.

A third method for indicating a north bay is by 2 x 2 bits of coded 6's in a second vertical white zone and a double dropout to the north from zone 2. The lead "S_{26}" from Rule 38 circuit, which indicates 2 x 2 bit coded 6's in a second vertical white zone, as hereinbefore described, is "anded" at an AND circuit **1194** at Rule 47 circuit with the leads X_s, "S_{24}" and "C_4." The three leads X_s, "S_{24}" and "C_4" are also shown "anded" in Rule 11 circuit to indicate a double dropout to the north from zone 2. AND circuit **1194** will produce an output signal if there is a 2 x 2 bit coded 6's and a double dropout to the north from zone 2, and turn On trigger C_{15}.

In this case, to indicate closure to the right and therefore a north bay, the same circuitry just described for closure of coded 6's in the first vertical white zone is

used except that in Rule 49 circuit the double north dropout from zone **2** lead "C_2," which is connected to OR circuit **1188**, is utilized to cause AND circuit **1186** to turn On NB trigger C_{16}.

In certain characters like the W of FIG. 29, there is a north peninsula within the north bay. In these characters, the north bay is usually wide enough so that coded 7's are written. Then, if there is a slope by the black shore towards the northeast, at least three bits wide, followed by a slope to the southeast three bits wide, it is an indication of a north peninsula. If the north bay is then closed to the right by black, an indication of a peninsula in a north bay is produced. Rule 70 circuit and Rule 71 circuit (FIG. 8V) are utilized for detecting this short slope three bits wide, to the northeast. Thus, if a coded 7 and 7_N are detected at the same time that a black "now" bit and a white "next" bit are detected, an output signal will be produced from an AND circuit **1202** in Rule 70 circuit to step a three counter K_4. Since the coded 7 and 7 "next" are indications of white in the previous vertical scan, and the lead $\overline{B}_N$ is an indication of a white "next" bit, the fact that the "now" bit is black, indicates a slope to the northeast. This is illustrated in the charatcer W of FIG. 29. When black bit **1204** is being examined as the "now" determination, white bit **1206** is the "next" determination and coded 7's **1208** and **1210** are the "now" and "next" bits respectively. Since the coded 7's **1208** and **1210** were written for the white bits **1212** and **1219**, respectively, the pattern of the fours bits **1204, 1206, 1212** and **1219** is such that a line **1216** separating the white bits **1206, 1212** and **1219** from the black bit **1204** is sloped to the northeast. This condition will normally occur only once per vertical scan. If it occurs in three successive vertical scans, it is an indication of a slope to the northeast three vertical scans wide. Thus, each time AND circuit **1202** of Rule 70 circuit has an output signal, the three counter K_4 is stepped. After the third step, an output signal will be fed from the OUT terminal to the trigger C_{82} of Rule 71 circuit, the output lead "$\overline{C}_{82}$" of which is fed back to decondition AND circuit **1202** and prevent further stepping of counter K_4.

To get an indication of a slope to the southeast, the black of the shore must be in the lower left-hand corner of a 2 x 2 bit area. This result may be obtained by looking for a coded one "now" bit in coincidence with a 7 "next" and a minimum white height. When white bit **1220** is being examined as the "now" determination and white bit **1222** as the "next" determination, a coded 1 **1224** is the "now" bit and a coded 7 **1226** is the "next" bit. Since the coded 1 **1224** and the coded 7 **1226** were assigned for a black bit **1228** and white bit **1230**, respectively, the pattern of the four bits **1220, 1222, 1228** and **1230** is such that a line **1232** separating the black bit **1228** from the white bits **1220, 1222** and **1230** is sloped to the southeast. In Rule 72 circuit the lead IN7, $IN7_N$, $\overline{B}$ and $\overline{B}_N$ are fed to an AND circuit **1232** and a coincidence thereat produces an output at TP time which steps a three counter K_5. Three pulses to three counter K_5 produces an output indicative of this southeast slope over three vertical scans. This output signal is sent to Rule 73 circuit to turn On a trigger C_{83}. Thus, when both triggers C_{82} and C_{83} are On, it is indicative of the fact that there has been a sloped shore to the northeast followed by a sloped shore to the southeast to produce an indication of a north peninsula. The leads "C_{82}" and "C_{83}" are fed to an AND circuit **1234** of Rule 50 circuit, the output of which at TP time effects the turning On of a peninsula trigger $C_{16.1}$ which is indicative of the north peninsula.

To insure that the slope to the southeast follows the slope to the northeast and not vice versa, the slope to the southeast trigger "C_{83}" is constantly reset during a northeast slope, so that it is not possible for both leads "C_{82}" and "C_{83}" to be positive unless the southeast slope is recognized after the northeast slope. Therefore, in Rule 72 circuit, an AND circuit **1236** has as its inputs the leads $\overline{1}$, $\overline{1}_N$, B and $\overline{B}_N$, and its output is connected via an R circuit **1238** to the reset terminal of 3 counter K_5. These inputs represent a northeast slope for the same reasons described for the inputs to AND circuit **1202** of Rule 70 circuit.

Rule 51 circuit illustrates means for indicating either two north bays or a north peninsula in a north bay. If the north bay trigger C_{16} is On and the same indications as produced north bay trigger C_{16} of Rule 49 circuit are again produced, it is an indication of a second north bay. Similarly, if north peninsula trigger $C_{16.1}$ is On and there is then an indication of a north bay by circuitry similar to Rule 49 circuit, it is an indication of a peninsula in a north bay. To indicate these two conditions, a trigger C_{17} of Rule 51 circuit is turned On. A comparative study of Rule 49 circuit and Rule 51 circuit indicates that they are both alike except that AND circuits **1240, 1242** and **1244** of Rule 51 circuit have one more input lead than the equivalent AND circuit **1172, 1176** and **1180**, respectively, of Rule 49 circuit. This one input lead to AND circuit **1240** is from an OR circuit **1246**, the inputs to which are the north bay lead "C_{16}" and the north peninsula lead "$C_{16.1}$." The OR circuit **1248** and **1250** to AND circuits **1242** and **1244** respectively are connected in the same manner. Thus, if either a north bay represented by lead "C_{16}" or a north peninsula represented by lead "$C_{16.1}$" are present at the respective OR circuit **1246, 1248** or **1250**, and all the other necessary conditions of Rule 51 circuit are met so as to produce a north bay such as was produced by Rule 49 circuit, the trigger C_{17} will be turned On, and thus indicate either two north bays or a peninsula in a north bay. However, since lead "C_{15}" from Rule 47 circuit is needed to indicate a new 2 x 2 bit area for a new north bay indication, the north bay lead "C_{16}" and the north peninsula lead "$C_{16.1}$" are connected via an A.C. OR circuit **1252** (Rule 47 circuit) to reset trigger C_{15} so that if the new 2 x 2 bit area of coded 5's, 6's or 7's is sensed with the proper north dropout requirements, trigger C_{15} will again be turned On, and the different possible closure to the right circuits plus the Rule 51 circuit detect the actual new north bay to produce the 2NB's or peninsula in NB indication.

A south bay may be detected by a 2 x 2 bit area of coded 4's with a double dropout to the south and a closure to the right. Since the trigger C_0 of Rule 5 circuit is turned On when there is a 2 x 2 bit area of 4's as an inherent indication of a double dropout to the south, it is only necessary that there be a simultaneous condition of the trigger C_0 being On and a closure to the right in order to indicate a south bay. The possible closure to the right of coded 4's is indicated by the Rule 52 circuit which has an AND circuit **1254**, the inputs of which are the lead "$\overline{S}_0$" and IN4 and the lead (B or B_N) from an OR circuit **1256**. Rule 52 circuit operates to indicate a possible closure to the right of the coded 4's, as previously described for other coded numbers to turn On a trigger $\overline{S}_{19}$ as an indication thereof. Then, when a coded $\overline{4}$ and 4_N is indicated along with a double south dropout, a south bay by trigger C_{18} in Rule 53 circuit will be turned On. The double south drop out lead "C_0" the possible closure to the right lead "S_{19}" and leads 4 and 4_N are conected to an AND circuit **1258**, the output of which is connected to the bona fide south bay trigger C_{18}.

Rule 54 circuit, in conjunction with Rule 66, 67, 68 and 69 circuits, are utilized for detecting a south peninsula. A south peninsula is one in which the shore of a south bay would first be sloped in a southeasterly direction followed by a slope in a northeasterly direction in a region of coded 4's.

Rule 66 and Rule 67 circuits are utilized for detecting the short slope three bits wide, to the southeast. Thus, if a coded 4 and 4_N are detected at the same time that a white "now" bit and a black "next" bit are detected,

an output signal will be produced from an AND circuit **1260** in Rule 66 circuit to step a three counter K_2. Since the coded 4 and 4 "next" are indications of white in the previous vertical scan and the lead $\overline{B}$ is an indication of a white "now" bit, the fact that the next bit is black indicates a slope to the southeast. This is illustrated in the character M of FIG. 23. When the white bit **1262** is being examined as the "now" determination, black bit **1264** is the "next" determination and coded 4's **1266** and **1268** are the "now" and "next" bits, respectively. Since the coded 4's **1226** and **1268** were written for the white bits **1270** and **1272**, respectively, a pattern of the four bits **1262, 1264, 1270** and **1272** is such that a line **1274** separating the white bits **1262, 1270** and **1272** from the black bits **1264** is sloped to the southeast. When this condition occurs in three vertical scans, a signal is produced from the counter K_2 and transmitted to turn On the trigger C_{80} of Rule 67 circuit.

To indicate a slope to the northeast in a south bay, the black of the shore must be in the upper right-hand corner of a 2 x 2 bit area. This result may be obtained by looking for a coded 4 "now" bit in coincidence with a 1 "next" and a minimum white height. In FIG. 23 when white bit **1276**, is being examined as a "now" determination, a white bit **1278** as the "next" determination, a coded 4 **1280** is the "now" bit and a coded 1 **1282** is the "next" bit. Since the coded 4 **1280** and the coded 1 **1282** were assigned for white bit **1284** and black bit **1286** respectively, a patttrn of the 4 bits **1276, 1278, 1284** and **1286** is such that a line **1288** separating the black bit **1286** from the white bits **1276, 1278** and **1284** is sloped to the northeast. In Rule 68 circuit, the leads IN4, $IN1_N$ and $\overline{B}$ & $\overline{B}_N$ are fed to an AND circuit **1290** and a coincidence thereat produces an output at TP time which steps a three counter K_3. Three pulses to three counter K_3 produces an output indicative of this northeast slope over three vertical scans. This output signal is sent to Rule 69 circuit to turn On a trigger C_{81}. Thus, when both triggers C_{80} and C_{81} are On it is indicative of the fact that there has been a slope shore to the southeast followed by a slope shore to the northeast to produce an indication of a south peninsula. The leads "C_{80}" and "C_{81}" are fed to an AND circuit **1292** of Rule 54 circuit, the output of which at TP time effects the turning On of a south peninsula trigger $C_{18.1}$. To insure that the slope to the northeast follows the slope to the southeast and not vice versa, the slope to the northeast trigger C_{81} is constantly reset during a southeast slope so that it is not possible for both leads "C_{80}" and "C_{81}" to be positive unless the northeast slope is recognized after the southeast slope. Therefore, in Rule 68 circuit, an AND circuit **1294** has as its inputs the lead $\overline{1}$, $\overline{1}_N$, $\overline{B}$ and B_N, and its output is connected via an OR circuit **1296** to the reset terminal of three counter K_3. These inputs represent a southeast slope for the same reasons described for the inputs to AND circuit **1260** of Rule 66 circuit.

Rule circuits—Northwest, southwest, northeast and southeast bays

Rule 56 circuit, Rule 57 circuit, and Rule 62 circuit through Rule 65 circuit, inclusive (FIGS. 8T and 8U) are utilized in the recognition of northwest and southwest bays.

A southwest bay has been described as a region of coded 0's, two high by four wide, blocked above and to the right by black. The southwest bay is recognized by counting four vertical scans from the extreme left of the character and then looking for a minimum white height of coded 0's blocked by black to the right.

Thus, in Rule 56 circuit, a four counter K_0 operates to detect the first four vertical scans of a character, and produces an output on the lead "K_0=4" to turn on the trigger C_{20} of Rule 57 circuit as indicative of this condition. At the end of each vertical scan when an X_s pulse comes along, if the trigger S_1 (indicative of an entrance into the first vertical white zone) is On and trigger C_{20} has not yet been turned On, the AND circuit **1300** of Rule 56 circuit goes positive to step the four counter K_0. The significance of the lead "S_1" is that it gets turned On for the first time in the first vertical scan in which black is sensed at the extreme left of the character and also gets turned On anew in each vertical scan thereafter in which a black is sensed. When trigger C_{20} goes On, the lead "$\overline{C}_{20}$" goes negative to prevent any further stepping of the four counter K_0.

In Rule 62 circuit, when coded 0 and 0_N are detected after the fourth vertical scan trigger C_{20} is On, since no coded 0 would be written to the right of any other coded number, it is indicative of a 2 high by 4 wide area of coded 0's. If a black and black "next" determination is also made at this time, it indicates that the 2 x 4 white area is blocked by black to the right. Thus, the leads B and B_N are "anded" at AND circuit **1302**, the output signal of which passes via an OR circuit **1304** to a fifth input of an AND circuit **1306**, the other inputs of which are leads C_{20}, IN0 and $IN0_N$. The fact that there is black above the 2 x 4 white area is implied by the fact that trigger S_1 was On at the end of the four vertical scans.

If one single black bit (i.e. not a simultaneous black "now" and black "next" bit) is sensed, it is sufficient to produce an indication of a first vertical white zone which will disturb the coded 0's and prevent the detection of a SWB. This is indicated in the character T of FIG. 27, where the coded 0's are shown as being assigned for the white bits of the first four vertical scans into the character. In the fifth vertical scan (vertical scan 30 of FIG. 27), the black bit **1308** is sensed. In this fifth vertical scan, there does not exist a condition of a simultaneous occurrence of a black ("now") and black ("next") bit to indicate a closing of the 2 high by 4 wide white area to the right. However, if the lead "S_1" goes positive it is an indication that the scanning is into the character, that is, that there is black of the character somewhere to the right of the 2 high by 4 wide white area, and if the leads "IN0," "$IN0_N$" and "C_{20}" are also positive, SWB trigger C_{23} will be turned On. This is accomplished by connecting the lead "S_1" to the OR circuit **1304**, the other input of which represents B and B_N.

A northwest bay has been described as a region of coded 2's or 3's, two high by four wide, open to the north and blocked to the right by black. The northwest bay may be recognized by counting four vertical scans from the extreme left of the character and then looking for a minimum white height of coded 2's or coded 3's blocked by black to the right.

In Rule 63 circuit, when coded 2 and 2_N are detected, and the fourth vertical scan count trigger C_{20} is On, it means that there is a 2 high by 4 wide area of coded 2's. To insure that the 2 x 4 bit area is not closed to the north by black, there is a requirement that there be no middle west inlet lead "$\overline{C}_6$" at an AND circuit **1310**, the output a black and black "next" determination is also made at this time, it indicates that the 2 x 4 bit area of 2's is closed by black to the right. Thus, in Rule 63 circuit the leads IN2 and $IN2_N$ are "anded" with the no middle west inlet lead "$\overline{C}_6$" at an AND circuit **1310**, the output of which is fed via an OR circuit **1312** to the input of an AND circuit **1314**, the other inputs of which are the leads B and B_N and the fourth vertical scan count lead "C_{20}." A simultaneous occurrence of positive signals at the input of AND circuit **1314** produces an output signal which is fed via OR circuit **1316** to turn On a northwest bay (NWB) trigger C_{24}.

The 2 x 4 bit area of coded 3's will also effect a turning On of the NWB trigger C_{24} in much the same manner as described for the 2 x 4 bit area of coded 2's except that to insure no closure by black to the north there is a requirement of no upper west inlet rather than no middle west inlet. Thus, the leads IN3, $IN3_N$ and the UWI lead

"$\overline{C}_7$" are "anded" at an AND circuit **1318**, the output of which is also fed via OR circuit **1312** to the input of the AND circuit **1314**.

The rest of Rule 63 circuit functions to produce a NWB indication in the two cases where due to a serif the 2 x 4 bit area of coded white is not blocked to the right by a black "now" and black "next" until there is an indication of a MWI, even though there is a legitimate NWB. One of these cases is illustrated in the character J of FIG. 21. In the character J the black bit **1320** is in the fifth vertical scan into the character and there is no simultaneous black "now" and black "next" determination at the time 2 "now" and 2 "next" bits are produced by the marking register output. If the white region of coded 2's in the character J are not determined at that time to be a NWB, then during the following vertical scan when a MWI indication is produced, it will be too late for a NWB indication. Therefore, if in any scan after the fourth vertical scan into the character (trigger C_{20} On), a minimum white region of coded 2's is found in the first vertical white zone (turning On trigger S_8), and then a black bit is detected which when white is later detected in that scan produces an indication of a second vertical white zone (trigger S_2 On), then at the end of vertical scan, an X_s pulse will produce a NWB indication, if there is a $\overline{MWI}$ indication along with these indications triggers C_{20}, S_8 and S_2 On. The black bit **1320** which resulted in the turning On of trigger S_2, then indicates that there is a black in the character somewhere to the right of the two high by four wide white area of coded 2's. An AND circuit **1322** has as its input, the leads "S_2," "S_8" and "$\overline{C}_6$" and feeds via an OR circuit **1324** to an AND circuit **1326** where it is "anded" with the leads "C_{20}" and X_s. The output of AND circuit **1326** feeds via OR circuit **1316** to turn on NWB trigger C_{24}.

An AND circuit **1328** in Rule 63 circuit is provided having as inputs the leads "S_3," "S_{10}" and "$\overline{C}_7$" to provide for the indication of a NWB when a 2 high by 4 wide area of coded 3's is blocked to the right by a single black bit. The operation of AND circuit **1328** in Rule 63 circuit proceeds in much the same manner as that described for the AND circuit **1322**, except that it relates to a NWB one vertical white zone higher in the character.

A southeast bay is a region of coded 4's two wide by four high. Rule 58 circuit and Rule 59 circuit operate to recognize the potential southeast bay and indicate this condition by the turning On of the potential SEB trigger C_{21} in Rule 59 circuit. Each time there is a simultaneous appearance of a coded 4 and a white "now," the TP pulse will cause a 4 counter K_9 to step one, if the lead "$\overline{C}_{21}$" is still positive. This is accomplished by having the leads TP, IN4, $\overline{B}$ and "$\overline{C}_{21}$" "anded" at an AND circuit **1330**, the output of which steps counter K_9. At the end of four pulses, an output is produced on the lead "$K_9=4$," which is fed to potential SEB trigger C_{21} of Rule 59 circuit. Since the coded 4 and $\overline{B}$ conditions must be four bits high, if a black bit is sensed before this condition is detected four times it is desirable to reset the counter K_9. This is accomplished by having the leads B and TP connected via an AND circuit **1332** and an OR circuit **1334** to the reset terminal of counter K_9. Similarly, at the end of each vertical scan the counter K_9 is reset by feeding the X_s pulse via OR circuit **1334** to the reset terminal of counter K_9. If now either a south bay or the two south bays condition are detected, the potential SEB trigger C_{21} is reset, because the detecting of a south bay implies a closure of this white area by black to the right. Thus, the SB lead "C_{18}" and the 2SB's lead "C_{19}" are fed via an A.C. OR circuit **1336** to the A.C. reset side of trigger C_{21}.

A northeast bay which is detected by Rule 60 and Rule 61 circuit, is a region of coded 5's in the first vertical white zone at least 2 wide by 4 high and open to the north and east; or of coded 6's in the second vertical white zone at least 2 wide by 4 high and open to the north and east; or of coded 7's in the third vertical white zone 2 wide by 4 high and open to the north and east. If a double dropout to the north is present when a coded 5 "now" and white "now" is detected, the four counter K_{10} of Rule 60 circuit will be stepped. At the end of four steps, to indicate the "four high," the lead "$K_{10}=4$" goes positive to turn On a potential NEB trigger C_{22} of Rule 61 circuit. In Rule 60 circuit, the lead IN5 is "anded" with the double dropout to the north from the first vertical white zone lead "C_1" at AND circuit **1338**, the output of which is connected via an OR circuit **1340** to an input of an AND circuit **1342**, the other inputs of which are leads TP, "$\overline{C}_{22}$" and $\overline{B}$. If lead "$\overline{C}_{22}$" is positive, each TP pulse steps the counter K_{10}. After four pulses, potential NEB trigger C_{22} goes On. If there is a black bit sensed before this condition is detected four times, the counter K_{10} is reset. This is accomplished by "anding" lead TP and B at an AND circuit **1344**, the output of which is fed via an OR circuit **1346** to the reset terminal of counter K_{10}. Similarly, at the end of each vertical scan, the counter K_{10} is reset by the lead X_s fed via OR circuit **1346** to counter K_{10}. If a north bay is thereafter detected, it is an indication of a closure to the right and so the potential northeast bay indication must be reset. This is accomplished in Rule 61 circuit by the lead "C_{16}" being connected via A.C. OR circuit **1348** to the A.C. input of trigger C_{22}.

In Rule 60 circuit, the lead IN6 and the double dropout to the north from the second vertical white zone lead "C_2" are "anded" at an AND circuit **1350**, the output of which is connected to OR circuit **1340**. Thus, AND circuit **1350** is connected via OR circuit **1340** to AND circuit **1342** for producing a NEB indication for coded 6's in the second vertical white zone, in a manner similar to that described for AND circuit **1338** for coded 5's in the first vertical white zone.

Lead IN7, in Rule 60 circuit, is also connected to OR circuit **1340** for producing a NWB indication for coded 7's. It is to be noted that since coded 7's are written in place of coded 5's and coded 6's only when the latter are two wide, the only time that the NWB indication is made effective by the lead IN7 is when the coded 7's are written in the third vertical white zone.

Long black vertical lines

The recognition of a long black vertical line (LBVL) criteria is performed by the Rule 64 circuit and Rule 65 circuit which look for a black area 2 wide by 11 high. Since a coded 1 "now" and a black "now" represent black area two bits wide, it is only necessary to count eleven different times that this condition appears before the end of a vertical scan. At the count of eleven, an 11 counter K_1, in Rule 64 circuit, produces an output on its lead "$K_1=11$" to turn On the LBVL trigger C_{79} in Rule 65 circuit. Counter K_1 is stepped by pulses from an AND circuit **1352**, the input of which are the leads IN1 and B, and also the timing pulse lead TP and the LBVL lead "$\overline{C}_{79}$." At the end of the count of eleven, lead "$\overline{C}_{79}$" goes positive to prevent any further stepping. The 11 counter K_1 is reset if there is a break in the long black vertical line as indicated by a simultaneous $\overline{1}$ "now" bit and a white "now" determination. Thus, the lead IN1 is fed to an inverter **1354**, the output of which is the lead $\overline{1}$ which is "anded" with the lead $\overline{B}$ and TP at an AND circuit **1356**. The output of AND circuit **1356** is fed via an OR circuit **1358** to the reset terminal of counter K_1. In addition, at the end of each scan, the lead X_s resets counter K_1 via OR circuit **1358**.

Triangle shape

The inventive shape-responsive techniques are particularly described with respect to the circuits shown for Rules 74 and 75 to determine whether a south bay is relatively

triangular in shape (corresponding to "N") or relatively rectangular in shape (corresponding to "H").

As described above with respect to FIG. 2, the area (A) of the region is compared to a fraction (K) of the product of the height (H) and width (W) of the region. When the area exceeds this measure (when A>KHW), the region is deemed to be relatively rectangular. When this measure exceeds the area (when A>KHW), the region is deemed to be relatively triangular. The fraction (K) that is used in the preferred embodiment equals ¾.

Referring to Rule 74 in FIG. 8W, signals are applied on the IN4 lead to the input of a 5 bit counter **1501**. These signals are present during the scanning of a south bay. The number of IN4 signals that occur during a vertical scan of the character represents the height of the south bay in the vertical region being scanned. The maximum height of the south bay is established in a 5 bit register **1503** by comparing the height of the bay during each scan with the largest height derived from previous scans. This comparison is accomplished by a subtractor **1505** which provides an output signal at the "sign" terminal when a negative difference is obtained by subtracting the output of the height counter **1501** from the maximum height register **1503**. Thus, when the height of the south bay in a scan exceeds the maximum height derived from earlier scans, the subtractor **1505** provides a signal which indicates that a new "maximum height" has been detected. The subtractor output is applied through an AND circuit **1507**, which is conditioned by the end of scan signal, X_s and through an OR circuit **1509** to reset the maximum height register **1503**. The signal supplied by AND circuit **1507** is applied to an SS–2 circuit **1511** which generates a delayed one-microsecond signal to condition an AND circuit **1513**. This AND circuit passes the output of the height counter **1501** to the maximum height register **1503** to replace the previous-stored data. The height counter is then reset by a signal derived by delaying the signal from single-shot **1511** in another single-shot **1514**. The maximum height register is also reset by the end of character signal X_C.

The width of the south bay is determined by counting the number of vertical scans that contain an IN4 indication. When a scan traverses a south bay, one or more IN4 signals are generated and the first of these signals sets a trigger **1515**. At the end of each scan, the trigger output is sampled by an AND circuit **1517** and a signal is applied to a width counter **1519** when the scan contains an IN4 signal. The AND circuit **1517** is conditioned by the end of scan signal X_S. At the same time, this signal initiates the reset operation of the trigger **1515**. Since the AND circuit has a faster response than the trigger, the AND circuit is sampled before the trigger data is lost by the rest operation. A delay circuit may be used to avoid relying on the transient operating time of these circuits. Thus, the width counter **1519** eventually stores a value equal to the number of scans contained in a south bay. The outputs of the maximum height register **1503** and the width counter **1519** are continuously applied to a multiplier **1521** which, in turn, continuously generates the product of these quantities at the OUT terminal.

As described above, with respect to FIG. 2, the product of the height (H) and width (W) is multiplied by a fraction. A fraction of ⅔ is used for the calculations described with respect to FIG. 2 because this fraction is approximately optimum for characters with serifs. However, the fraction ¾ is used in the preferred embodiment as it is approximately optimum for use with characters that do not contain serifs, while providing accurate recognition of characters with serifs. Obviously, this operation could be embodied such that the fraction were adjustable by using a divider circuit but, for economy and simplicity of operation, a non-adjustable circuit is shown. The operation is accomplished by subtracting ¼ HW from HW in a subtractor **1523**. The subtrahend (¼HW) is obtained by applying the value HW (from multiplier **1521**) to the subtractor **1523** through a divider **1525**.

The value ¾HW provided at the DI# terminal of subtractor **1523** is compared to the area (A) of the south bay in a subtractor **1527**. The area corresponds to the number of IN4 signals that are obtained during the scanning of the south bay of the character and are accumulated in an area counter **1529**. This counter is reset by the end of character signal X_C. When the area (A) exceeds the value ¾HW (indicating a rectangular south bay), the subtractor **1527** provides a signal at the SIGN terminal which is applied through an AND circuit **1530** to control a trigger circuit **1531** which supplies a $\overline{C}_{87}$ signal. When the south bay is triangular in shape, no signal is supplied by the subtractor **1527** and a C_{87} signal is provided because of the previous-supplied end of character signal X_C to the trigger **1531**. Thus the trigger output indicates a "triangle shape" (C_{87}) south bay unless rectangularity is indicated by a signal from subtractor **1527**. In order to insure that only the IN4 signals that are present in the south bay of the character are considered, AND circuit **1530** is conditioned only after the termination of the south bay. Referring to FIGS. 20 and 24, it can be seen that IN4 signals (labelled "4") are also present at the extreme right side of the characters. These signals do not affect the operation of the shape-sensitive circuits in FIG. 8W because AND circuit **1530** is conditioned to sense the sign output of subtractor **1527** before these additional signals are obtained. A trigger circuit **1533** is set by each delayed end of scan signal X_{sd} and reset during the next scan only if an IN4 signal is present. When no IN4 signal is present during a scan, the trigger conditions an AND circuit **1535** to pass the end of scan signal X_s to an AND circuit **1537**. Another trigger circuit **1539** is set when the first IN4 signal is sensed and is reset by the end of character signal X_C. The output of this trigger circuit conditions AND circuit **1537** such that a signal is provided at the output of this AND circuit at the termination of each scan which (1) contains no IN4 signals and (2) follows a scan or scans which contain one or more IN4 signal. Thus, the signal at the output of AND circuit **1537** indicates the termination of a south bay. This signal sets a trigger **1541** which provides a negative-going signal to a delay single-shot circuit **1543**. The trigger is reset by the end of character signal X_C. The delay single-short **1543** generates a 1-microsecond pulse to condition AND circuit **1530**. In this manner, the output of subtractor 1527 is sampled once after the scanning of a south bay (before scanning the extreme right portion of character). Note that some characters, such as "M" (FIG. 23) contain two south bays and hence, the output of subtractor **1527** would be sampled twice. However, the shape-sensitive signal C_{87} is only used in distinguishing between the characters "H" and "N" in the preferred embodiment and these characters contain only one south bay. Obviously, the circuits of FIG. 8W could be readily extended to sense the shape of either or both of two south bays, if desired. Furthermore, these circuits could be modified to sense the shape of other lakes or bays.

Deep and tall bays and inlets

A deep west inlet in an inlet 6 white bits wide and is detected by Rule 76 circuit and Rule 77 circuit. The deep west inlet designation (D–WI) is utilized mainly to distinguish between a character K with a west bay formed by serifs and a character X having a deep west bay. In the preferred embodiment of the invention it has been deemed unnecessary to detect the closure to the right by black which causes an inlet to become a bay. It has just been assumed that the inlet, of necessity, for the type of character being identified, is actually a bay. The D–WI may be recognized by the On condition of the

MWI trigger S_{30} at the end of vertical scan in five different vertical scans. Since the MWI trigger S_{30} goes On, for the first time, upon recognition of a 2 x 2 bit white area, at the end of the fifth turning On of MWI trigger S_{30}, the white region inlet is 6 bits wide. Thus, in Rule 76 circuit, the lead "S_{30}" is connected via an OR circuit **1360** to the input of an AND circuit **1362**, the other inputs of which are leads X_s and "$\overline{C}_{84}$." The lead "$\overline{C}_{84}$" comes from a D–WI indicating trigger C_{84} in Rule 77 circuit and is positive until a D–WI indication. At the end of each vertical scan therefore, until the D–WI indication, if there is a MWI indication (lead "S_{30}" positive), a pulse from AND circuit **1362** will step a five counter K_6, until at the end of five pulses, the D–WI trigger C_{84} of Rule 77 circuit goes On. Since it is also possible to have an upper west inlet in the character X if the lower left serif of the character X extends for a considerable distance to the right, the UWI lead "S_{31}" will also cause the 5 counter K_6 to step. However, to insure that there be no stepping of two during any one vertical scan, the UWI lead "S_{31}" will cause the stepping only if the no $\overline{\text{MWI}}$ lead "S_{30}" is positive, as indicated in Rule 76 circuit by the leads "$\overline{S}_{31}$" being "anded" at an AND circuit **1364**, the output of which is connected to OR circuit **1360**.

The potential D–EB which is also 6 white bits wide is detected in Rule 78 circuit and Rule 79 circuit by the use of the potential MEB lead "S_{33}," the potential UEB lead "S_{23}" and the no potential MEB lead "$\overline{S}_{32}$," in the same manner described for the detection of the D–WI of Rule 76 circuit and Rule 77 circuit. Thus, after a count of five, a five counter K_7 of Rule 78 circuit produces an output on lead "K_7=5" which turns On a potential D–EB trigger C_{85}. Since, however, the potential D–EB may be later closed to the right, both the counter K_7 and the trigger C_{85} are reset by the detection of recognition criteria that indicate a closing to the right such as the detection of lakes, north bays and south bays. Thus, the ML lead "C_{12}," the UL lead "C_{13}," the LL lead "C_{14}," the NB lead "C_{16}," the 2NB's lead "C_{17}," the SB lead "C_{18}," and the 2SB's lead "C_{19}" cause the reset of counter K_7 and trigger C_{85} via an A.C. OR circuit **1366**.

A tall southwest bay (T–SWB) is a 4 x 4 white region of coded 0's blocked by black to the right, and its recognition is accomplished by Rule 80 circuit and Rule 81 circuit. A trigger C_{86}, in Rule 81 circuit, indicative of the tall southwest bay is turned On by a lead "K_8=4" from a four counter K_8 in Rule 80 circuit. After the trigger C_{20} is On to indicate the end of the fourth vertical scan of the character, if a coded 0 is in the marking register, it is an indication of coded 0's four wide, because there can be no other coded number to the west of a coded 0. If the coded 0 is sensed four times, it is an indication of coded 0's at lead four bits high, and if for each coded 0 a black "now" bit is sensed, it is an indication of black blocking, to the right, the 4 x 4 white region of coded 0's. Thus, the lead B is fed via an OR circuit **1368** to the input of an AND circuit **1370** where it is "anded" with the leads IN0 and the end of fourth vertical scan lead "C_{20}" to produce an output for stepping the four counter K_8. Four steps of counter K_8 turns On trigger C_{86} to indicate a tall southwest bay, and makes lead "C_{86}" positive to prevent any further stepping of the counter K_8.

In case there is a serif, there would be no blocking by black to the right, and so if the "entering first vertical white zone" lead "S_1" is On, it indicates a serif has been sensed for reasons previously described and the lead "S_1" and IN0 at four different times in a vertical scan will then produce a T–SWB indication. This is accomplished by connecting lead "S_1" to the input of the OR circuit **1368**, the other input of which is the lead B.

Miscellaneous recognition criteria and Christmas tree shape decoder

The miscellaneous recognition criteria (LL:UL) (lower lake followed by upper lake) is detected in Rule 82 circuit to Rule 84 circuit inclusive (FIG. 8Y). Since the vertical scanning is from bottom to top, if the lower lake LL and upper lake UL were detected in the same vertical scan, the lower lake would be followed by the upper lake. However, the miscellaneous recognition criteria (LL:UL) requires that the UL be detected at least two vertical scans after the LL. Thus, in Rule 82 circuit, a two counter K_{14} will be stepped at the end of vertical scan, if an LL is detected, but only if there is no UL present. At the end of two vertical scans, with this condition, counter K_{14} will produce an output signal on its "K_{14}=2" lead to turn On trigger C_{48} of Rule 83 circuit. To step the two counter K_{14}, the LL lead "C_{14}" and the $\overline{\text{UL}}$ lead "$\overline{C}_{13}$" are "anded" at an AND circuit **1372** with lead X_s. The lead "C_{48}" is then "anded" at AND circuit **1374** of Rule 84 circuit with the UL lead "C_{13}" and timing lead TP to produce a pulse for turning On the LL:UL trigger C_{46}.

The manner in which most of the C triggers are turned On to signify the numerous recognition criteria has been described. The states of the C triggers control the Christmas tree networks of FIGS. 8Z, 8AA and 8BB. Each C trigger has its "C" lead connected to the input of relay drivers **1375** the outputs of which in turn are connected via relays to +15 volts. Each of the relays is labeled with the letter R followed by a number that is the same as the subscript of the "C" lead which is connected to its respective relay driver. Thus, the positive condition on a "C" lead causes its respective relay driver **1375** to conduct through its respective R relay causing the energization thereof. The energization of the relays causes the closing of their respective contacts to set up a path of the type discussed hereinbefore in conjunction with FIGS. 10A and 10B, i.e., the closing of the contacts of the relays are the same as the yes condition of the blocks of FIGS. 10A and 10B. For example, the C_{87} signal generated by the Rule 74 and 75 circuits in FIG. 8W causes relay R87 to be activated when a south bay is relatively triangular-shaped. The contacts of this relay are operated to indicate that the scanned character is an "N" in this case (presuming that other circuits have determined that the scanned character is either an "H" or an "N"). A the end of character, an OK to Punch signal on lead **368** energizes relay R30, as previously described, and causes a path to be completed from the punch line **487** through closed contacts R30–1 through the closed contacts of the different relays to one of the terminals of the punch **486**, to cause the punch to punch and/or print the character recognized. It is obvious that devices other than a punch may be utilized as an output unit. Incidentally, the relay R30 is made slower acting than the other relays, a insure that the latter operate their contacts before the contacts R30–1 close to complete the circuit to the punch.

It is to be noted that the Christmas tree requires an "oring" of certain of the recognition criteria in the preferred embodiment of the invention. Thus, Rule 85 circuit through Rule 90 circuit inclusive (FIG. 8Y), each consists of an A.C. OR circuit and a trigger which is turned On if one or more of the particular recognition criteria exists. Thus, in Rule 85 circuit the ML lead "C_{12}," the UL lead "C_{13}" and the LL lead C_{14} are connected to the input of an A.C. OR circuit **1376**, which provides an output signal for turning On a (ML or UL or LL) trigger C_{40}. The (UEB or LEB) trigger C_{41}, the (LWB or SWB) trigger C_{42}, the MWB or LBVL) trigger C_{43}, the (MEB or LEB) trigger C_{44} and the (NWB or MWB) trigger C_{45} are turned On in a similar manner by A.C. OR circuits in Rule 86 circuit through Rule 90 circuit and it is not necessary to further describe them.

The last rule circuit, Rule 91 circuit, is the circuit for detecting context. This is used for distinguishing, for example, a numeral 1 from a letter I by determining whether the previous character was a number or letter and assuming that the character being studied is probably the same. Thus, if the previous character recognized was a letter L, then a context trigger C_{47} will be turned On and the next character studied will be assumed to be the letter I rather than the number 1. Thus, all letters should turn On the trigger C_{47} and all numbers turn it Off, except that, if one of the four cases where context is necessary, is recognized, that recognition will have no effect on the context trigger. Thus, all letters except I, Z, S and O turn On context trigger C_{47} and all numbers except 1, 2, 5 and 0 turn Off trigger C_{47}. The letter terminals of punch **486** are connected in FIG. 8BB to a letters cable **1378**, which is then fed to an A.C. OR circuit **1380** (FIG. 8Y), the output of which turns On context trigger C_{47}. The number terminals of the punch **486** is similarly connected via a figures cable **1382** to an A.C. OR circuit **1384**, the output of which turns Off context trigger C_{47}.

In FIG. 12, the numeric character 0 is thirteen vertical scans wide, i.e., no black bits appear during the fourteenth vertical scan and an end of character is indicated after the fourteenth scan. At the end of this fourteenth vertical scan, the OK to Punch signal starts the punch, but one more cycle of the marking register is permitted in order to reset it. This resetting takes place automatically during the "next" or fifteenth scan by shifting the marking register without writing anything into it, as previously described. After the fifteenth vertical scan the marking register is not stepped again until the punching is over, at which time the punch will send a punch done signal which may be generated in a punch of the type shown in Gardinor 2,647,581 by the closing of contacts by a cam therein to complete a circuit to a positive potential. This punch done signal starts the sixteenth vertical scan by turning Off the end of character trigger **478** (FIG. 8C), which ends the positive OK to Punch signal on lead **368**. The OK to Punch signal going negative, causes an output from AND circuit **460** to turn On signal shot multivibrator **462** and create the reset pulse X_s, which in turn creates reset pulse X_{sd}, which is applied via inverter **498** (FIG. 8B) to turn Off the punch trigger **496** and allow for the multivibrator pulses to pass through punch switch **204** and start the sixteenth vertical scan as illustrated in FIG. 37H.

In FIG. 12, the sixteenth vertical scan is all white but during the seventeenth vertical scan, black bits of numeric character 1 are detected and the vertical scans continue. At the end of the 32nd vertical scan, the typewriter must be spaced in a manner previously described. The horizontal carry on lead **274** (FIG. 8B) causes single shot multivibrator **288** (FIG. 8A) to go On for one-half second during which time the carriage is spaced. None of the circuits are effected during the time for carriage spacing because the marking register is not shifted and all temporary and memory triggers S and C in the rule circuits remain in status quo. Single shot multivibrator **288** goes negative to end the one-half second space time and start thirty-two more vertical scans.

It is apparent at this point, that additional marking registers could be utilized and also that more than two stages of each marking register can have outputs, so that a plurality of slices and bits in the slices could be sensed, to produce a minimum white region of a different size.

An inventive shape-responsive recognition technique has been shown and described.

Although many shapes are obviously ascertainable using the inverted technique, it is particularly shown and described with respect to determining relative triangularity and octangularity. An example of the use of this technique is shown wherein the character "N" is distinguished from the character "H" by the triangle-shaped south bay in the "N" and the rectangle-shaped south bay in the "H."

While there have been shown and described and pointed out the fundamental novel features of the invention as applied to a preferred embodiment, it will be understood that various omissions and substitutions and changes in the form and details of the device illustrated and in its operation may be made by those skilled in the art without departing from the spirit of the invention. It is the intention therefore, to be limited only as indicated by the scope of the following claims.

What is claimed is:

1. An apparatus for determining the shape of a two-dimensional pattern comprising, in combination:
- means for providing an indication of the size of the pattern along a first direction;
- means for providing an indication of the size of the pattern along a second direction;
- means for providing an indication of the area of the pattern;
- and means for comparing the area indication with a predetermined fraction of the product of the first two indications to determine the shape of the pattern.

2. The apparatus described in claim **1**, wherein the first two indications correspond to distances along directions that are essentially perpendicular.

3. The apparatus described in claim **2**, wherein the predetermined fraction is greater than one-half and less than one, whereby the pattern is determined to be relatively rectangular when the area indication exceeds the fraction of the product and, whereby the pattern determined to be relatively triangular when the fraction of the product exceeds the area indication.

4. The apparatus described in claim **1**, wherein the first two indications correspond to the height and width of the pattern.

5. The apparatus described in claim **4**, wherein the predetermined fraction is greater than one-half and less than one, whereby the pattern is determined to be relatively rectangular when the area indication exceeds the fraction of the product of the height and width indications, and whereby the pattern is determined to be relatively triangular when the fraction of the product of the height and width indications exceed the area indication.

6. In a system for recognizing two-dimensional patterns, an apparatus for determining the shape of a pattern-defined background region comprising, in combination:
- means for providing an indication of the maximum height of the region;
- means for providing an indication of the maximum width of the region;
- means responsive to the maximum height and maximum width indications for providing an indication of the product of the maximum height and maximum width;
- means responsive to the product indication for providing an indication of a predetermined fraction of the product, where the fraction exceeds one-half and is less than one;
- means for providing an indication of the area of the region;
- and means responsive to the area indication and the indication of the predetermined fraction of the product, for providing an indication of the larger of these indications, whereby the region is determined to be relatively rectangular when the area indication exceeds the indication of the fraction of the product, and whereby the region is determined to be relatively triangular when the indication of the fraction of the product exceeds the area indication.

7. In a pattern recognition system wherein the pattern is scanned along a sequence of adjacent columns, an apparatus for determining the shape of a pattern-defined background region comprising, in combination:
- means for providing an indication of the height of the region along each scanned column;

means responsive to the height indications to provide an indication of the maximum height of the region;

means for providing an indication of the maximum width of the region;

means responsive to the maximum height and maximum width indications for providing an indication of the product of the maximum height and maximum width;

means responsive to the product indication for providing an indication of a predetermined fraction of the product, where the fraction exceeds one-half and is less than one;

means for providing an indication of the area of the region;

and means responsive to the area indication and the indication of the predetermined fraction of the product, for providing an indication of the larger of these indications, whereby the region is determined to be relatively rectangular when the area indication exceeds the indication of the fraction of the product, and whereby the region is determined to be relatively triangular when the indication of the fraction of the product exceeds the area indication.

8. In a system for recognizing two-dimensional patterns, an apparatus for determining the shape of a pattern-defined background region comprising, in combination:

means for providing an indication of the size of the region along a first direction;

means for providing an indication of the size of the region along a second direction;

means for providing an indication of the area of the region;

and means for comparing the area indication with a predetermined fraction of the product of the first two indications to determine the shape of the region.

9. The apparatus described in claim **8**, wherein the first two indications correspond to distances along directions that are essentially perpendicular.

10. The apparatus described in claim **9**, wherein the predetermined fraction is greater than one-half and less than one, whereby the region is determined to be relatively rectangular when the area indicated exceeds the fraction of the product and, whereby the region is determined to be relatively triangular when the fraction of the product exceeds the area indication.

11. The apparatus described in claim **8**, wherein the first two indications correspond to the height and width of the region.

12. The apparatus described in claim **11**, wherein the predetermined fraction is greater than one-half and less than one, whereby the region is determined to be relatively rectangular when the area indication exceeds the fraction of the product of the height and width indications, and whereby the region is determined to be relatively triangular when the fraction of the product of the height and width indications exceed the area indication.

References Cited by the Examiner

UNITED STATES PATENTS

1,782,445	11/1930	Rieber	181—0.5
1,909,205	5/1933	McCollum	181—0.5
1,923,107	8/1933	McCollum	181—0.5
2,021,943	11/1935	McCollum	181—0.5
2,231,575	2/1941	Gardner	181—0.5
2,865,104	12/1958	Gensoldt	33—121
3,075,289	1/1963	Schreuder et al.	33—121

MAYARD R. WILBUR, *Primary Examiner.*

DARYL W. COOK, *Examiner.*

J. E. SMITH, *Assistant Examiner.*