



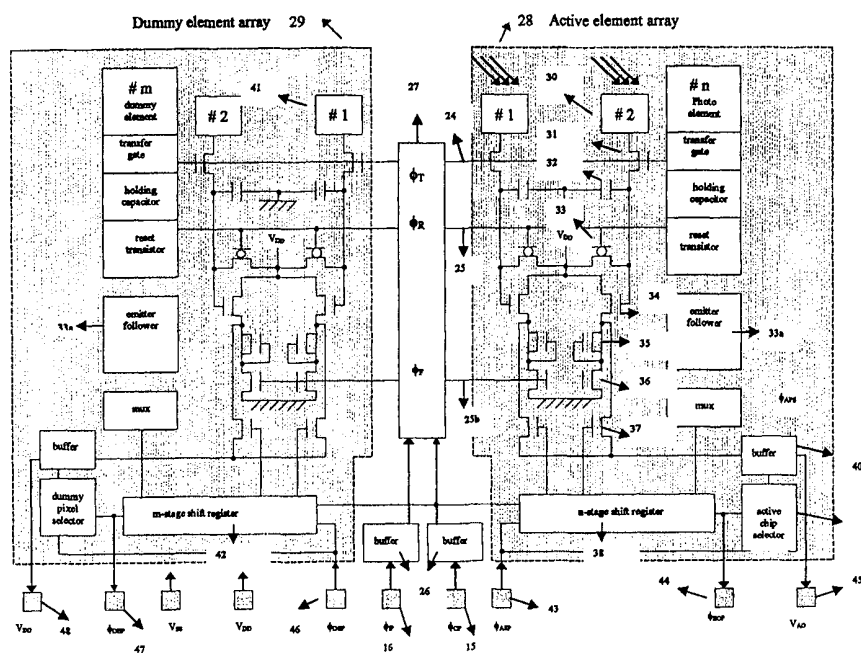
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(54) Title: SILICON BUTTING CONTACT IMAGE SENSOR CHIP WITH LINE TRANSFER AND PIXEL READOUT (LTPR) STRUCTURE

(57) Abstract

A contact image sensor (CIS) chip uses a line transfer and pixel readout structure. Integration and signal readout are separated. The device provides more accurate data while avoiding distortion, vertical resolution reduction, and reduction of scan speed. Operational amplifiers combine signals from active photoelements and dummy elements to remove any dark fixed pattern noise or DC offset voltage from the output signal. The dummy elements are identical to the active photoelements except that they are shielded so that they receive no light. The linearity of the photoresponse is greatly assisted by this optical black level reference, strongly promoting accurate color reconstruction. One preferred embodiment entails the use as photoelements of photodiode Passive Pixel Sensors, while a second preferred embodiment uses phototransistor Active Pixel Sensors. A small holding capacitor capacitance increases the devices's sensitivity, reduces reset noise, and further improves signal-to-noise ratio. The chips may be butted together end-to-end on a single substrate in one line with approximately equal space between adjacent detectors. Thus, CIS module offering higher sensitivity, low reset noise, and high signal-to-noise ratio may be built using this device. All necessary clock pulses and operational amplifiers can be built on a single chip, reducing the necessary peripheral circuitry. Because the dummy element array operates independently from the active photoelement array, design flexibility for different CIS module configurations is promoted.



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SILICON BUTTING CONTACT IMAGE SENSOR CHIP WITH LINE TRANSFER AND PIXEL READOUT (LTPR) STRUCTURE

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FIELD OF THE INVENTION

The invention relates generally to the field of contact type image sensing systems for scanning and digitizing documents. More particularly, the invention relates to a contact image sensor chip with a line transfer and pixel readout (LTPR) structure.

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BACKGROUND OF THE INVENTION

The technology required to scan and digitize documents has existed for approximately twenty years. Earlier scanning devices consisted of charge-coupled devices or self-scanned photodiode arrays (or MOS). Contact image sensor (CIS) systems improved on these devices by replacing their optical system with a rod lens system. This arrangement permitted the distance between the image sensor and the document being scanned to be reduced to approximately 2 cm. A schematic diagram of a typical CIS system is shown in FIG. 1. The system contains three principal components: (1) an LED light source array 1, (2) a rod lens array 3, and (3) a long image sensor array 4. LED light source array 1 illuminates a document 2, reflecting light off it through a cover glass 7 to the rod lens array 3. The rod lens array 3 is composed of a line of individual glass rods, each of which will cover approximately 16 photodetectors 4.6. The rod lens array 3 focuses the reflected image to the image sensor array 4. Image sensor array 4 is composed of a plurality of individual image sensing photoelements 4a, each composed of a number of photodetectors 4b. Image sensor array 4 is typically mounted on a hybrid image sensor board 5 capable of converting the image to an electronic signal.

All of the components and the optical path are integrated into a compact module called the CIS module 6, which is shown in cross section in FIG. 2. In addition to the components mentioned above, the CIS module 6 includes an output line 8, and a plastic case 9. The output line 8 transmits the signal generated by the hybrid image sensor board 5 to the outside circuitry. The plastic case 9 houses all of the above components in a compact module.

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One well known embodiment of this system involves a paper feed image scanning system such as a facsimile machine. The CIS module 6, including the cover glass 7, is fixed in place relative to the roller 10. The document 2 is sandwiched between the roller

10 and cover glass 7 and is held in place by its contact with both the roller 10 and the cover glass 7. When a stepping motor 10a causes roller 10 to rotate, the roller 10 advances the document 2 until the first line of the document 2 comes into position to be read by the CIS module 6. The light source array 1 is turned on. The optical signal of the reflected document is then focused on a series of photoelements 4a. This series of photoelements 4a converts the optical signal into an electronic signal in either charge or voltage form and stores that signal in its associated holding capacitors.

The CIS module 6 then integrates the first line of the document. After the CIS module 6 has read out the first line of the document 2, the CIS module 6 sends a signal to the stepping motor 10a. In response to the signal, the stepping motor 10a starts driving roller 10, continuing until the second line of document 2 comes into position to be read by the CIS module 6. The CIS module 6 then reads the second line of the document. This process is repeated until each line of the document has been read. The stepping motor 10a then advances document 2 one final time to eject it from its position sandwiches between the roller 10 and the cover glass 7.

FIG. 3 shows the prior art circuit diagram of the hybrid image sensor board 5. The hybrid image sensor board 5 is a long printed circuit board containing a plurality of identical individual silicon contact image sensor chips 11 butted together end-to-end on a single substrate in one line with approximately equal space between adjacent detectors. The board 5 also includes with peripheral circuitry including signal processing means 12 to serially activate the individual chips and an operational amplifier 13 capable of combining and then amplifying all of the analog signals generated by said CIS chips. The number of individual image sensor chips 11 chosen depends on the desired width of scanning. If twenty-seven individual chips are selected, the resulting width will be roughly equivalent to standard paper width, which is about 8.5 inches for A4 size paper.

The hybrid image sensor board 5 generates an analog video signal output. Two input pulses generated by the signal processing means 12 trigger the operation of the CIS module 6. These two triggering input pulses are a start pulse ϕ_{SP} 14 and a clock pulse ϕ_{CP} 15. As shown in FIG. 3, the start pulse ϕ_{SP} 14 triggers the generation of an input pulse ϕ_{IP} 16 by a first chip 11. The first chip 11 also generates an end pulse ϕ_{EP} 17 that triggers the generation of an input pulse ϕ_{IP} 16 by the second chip. The process repeats itself until all chips 11 have fired. On all of the chips 11, the input sites for the

clock pulses ϕ_{CP} 15 are wired together and therefore all clock pulses ϕ_{CP} 15 occur simultaneously. All of the analog signals generated by the image sensor board 5 are combined and then amplified by the operational amplifier 13.

5 The timing diagram of the prior art hybrid image sensor board 5 is shown in FIG. 4, illustrating the temporal relationship between the activation of stepping motor 10a to advance the document 2 to the next line which is to be read out, the transmission of clock pulse ϕ_{CP} 15, the transmission of start pulse ϕ_{SP} 14, the time required for each chip 11 to read a given line of the document 2, the readout time required for one line of the
10 document to be read, and the integration time, which is the time between two consecutive readouts for a given photodiode.

A block diagram illustrating the function of the prior art CIS module 5 using phototransistor sensing elements 4a is shown in FIG. 5. (The structure and function of
15 this chip is described in detail in U.S. Pat. No. 5,299,013, issued Mar. 29, 1994.) The image sensor chip 11 comprises an array of phototransistor sensing elements 111, an array of multiplexing switches 112, an n-stage digital scanning shift register 113 comprising n identical stages 113b, a built-in buffer 113a, and an active chip selector 114.

20 In operation, the image sensor chip 11 is triggered by a start pulse to the first in sequence active individual photoelement 111 which serially activates the photodetectors 4b on the first photoelement 111. After the signal from the last phototransistor sensing element 111 of the first image sensor chip 11 is read, an end of
25 scan pulse is generated so that the next image sensor chip in sequence is triggered. Each of the multiplexing switches is coupled between one of the photoelements and the output line.

The input pulse ϕ_{IP} 16 triggers the reading of the current line of the document 2 by each
30 phototransistor sensing element 111 in sequence. The input pulse ϕ_{IP} 16 also triggers the generation of the clock pulse ϕ_{CP} 15. The input pulse ϕ_{IP} 16 is transmitted to the first stage 113b of the shift register 113, which then activates the active chip selector 114. Each stage 113b of the shift register 113 is then turned on one by one in sequence. The output of each shift register stage 113b is connected to a control input of one of the
35 multiplexing switches 112. When one of the multiplexing switches 112 is activated, it

then transmits the signal to a video line 115. After all of the shift register stages 113b have been scanned, the shift register 113 generates the end pulse ϕ_{EP} 17. This end pulse ϕ_{EP} 17 disables the active chip selector 114 and indicates that the scanning by that chip is completed. In this device, the readout mechanism is transmitted by the current flowing into video line 115. The phototransistor 111 transfers an electronic signal to video line 115 and video line 115 simultaneously reads out an electronic signal from phototransistor 111. This transfer and readout scheme is known as a pixel transfer and pixel readout (PTPR) structure.

FIG. 6 shows a block diagram of the prior art image sensor chip 4 utilizing a photodiode sensing element 4a and a differential voltage pickoff. (The structure and function of this chip is described in detail in U.S. Pat. No. 5,724,094 issued Mar. 3, 1998.) The output of the nth stage 113b of the shift register 113 is transmitted to a corresponding nth multiplexing switch 117 and to an (n-1)th reset transistor 118. Turning on multiplexing switch 117 initiates the readout mechanism. Turning on a reset transistor 118 initiates the reset mechanism. The device simultaneously reads out the nth pixel signal and resets the (n-1)th pixel signal. The charge readout and charge transfer is thus separated by one clock cycle. This transfer and readout scheme constitutes another example of a PTPR structure.

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One difficulty of the prior art has involved distortion which arises during pixel readout in the video signal output of a CIS module 6 employing a PTPR image sensor board 5 and a constant light source (as is used, for example, with a facsimile machine). The distortion arises due to different integration times for each pixel in the scanned document.

25 After readout, each pixel of the video signal combines data from the present and immediately previous lines. In addition to this undesirable distortion, this effect also reduces the vertical resolution to approximately half of its optimum value.

Consider the simplified, digitized document as shown in Fig. 7(a) in which four rows of the original digitized document are shown. When the first row of the document is located on the glass surface of the CIS module, the first sensing element reads a first pixel on the document. At this time, no signal for the first pixel 18 is detected because the light source did not illuminate the first pixel 18 yet. After the first pixel 18 is readout, a first sensing element integrates the first pixel 18. During this time, a second sensing element reads a second pixel 19 on the document. The output of the second sensing element reads out 10% of the second pixel 19 on the document. After readout, the second

sensing element integrates the second pixel 19. This process is repeated again until end of the row. The CIS module is then moved to second row and reads the image signal on second row of document. The CIS module read first pixel 20 out from second row. In this condition, the first sensing element on the CIS module carries about 100% of first pixel 18 signal on first row and 0% of first pixel 20 signal on second row. Similarly, the second sensing element on CIS module carries about 90% of the second pixel 19 signal on the first row and about 10% of the second pixel 21 signal on the second row. The video signal output of the CIS module is distorted because the integration time of each pixel is different, varying from 0% to 100% of the integration time. The sensing element on the CIS module already carries a lot of the information from previous row. After readout, each pixel of the video signal consists in part of the present row and in part of the previous row. FIG. 7b shows the image data read out from an image sensor chip having a PTPR structure. The image data comprises part of the image signal on the nth row and part of the image data on the (n-1)the row.

While strobe light illumination of the CIS module 6 is known in the prior art to prevent this problem, as with a color scanner, it does reduce the scan speed to half of what it would otherwise be. FIG. 8 shows a prior art timing diagram using strobe light illumination. The strobe is timed to turn on and off at a frequency which enables the CIS module 6 to avoid the distortion discussed above by only illuminating the pixels it is desired to sample within a given line. However, the scan time to read one line is now the sum of the integration time 22 during which the light source array 1 is turned on plus the pixel readout time 23 during which the light source array 1 is turned off. In this case, the image data is not distorted, but the scan speed is reduced by half.

Thus a need exists for an accurate, sensitive CIS chip with high signal-to-noise ratio capable of avoiding distortion, vertical resolution reduction, and reduction of scan speed. It is desirable to create a device in which all necessary clock pulses and operational amplifiers can be built on a single chip, reducing necessary peripheral circuitry.

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SUMMARY OF THE INVENTION

The invention provides an image sensor chip for a CIS module capable of accurate scanning a document at optimal speed while avoiding distortion effects and maintaining optimal vertical resolution. The circuit comprises a plurality of sensing photoelements and a like number of dummy elements capable of providing a baseline signal. The

signal from the dummy elements is combined with the signal from the active photoelements by an operational amplifier which then outputs a signal scrubbed of all dark fixed pattern noise and all direct current (DC) offset voltage.

- 5 The invention uses a line transfer and pixel readout (LTPR) structure. A series of photodetectors scan each line of a document and generate a signal. One by one, each line of data is isolated and then parallel transferred via a line of transfer gates to holding capacitors associated with the corresponding photodetectors. A digital scanning shift register then reads out a line of the video signal. In this case, the integration and readout
10 are therefore separated. This structure not only provides more accurate data and higher vertical resolution but also increases scan speed. To build a CIS board, the chips may be butted together end-to-end on a single substrate in one line with approximately equal space between adjacent detectors. Such a CIS module offers higher sensitivity, low reset noise, and high signal-to-noise ratio.

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- The dummy elements function in the same manner as the active photoelements. However, they are shielded by some blocking means so that they receive no light. The output of the dummy sensors will therefore not vary with the images on the subject document. The dummy sensors therefore provide a baseline signal that is used to
20 cancel any dark fixed pattern noise or DC offset voltage from the signal from the sensors. This scrubbing of the output signal is accomplished in the operational amplifiers. The optical black level reference also significantly assists the process of color reconstruction. The image sensor chip internally generates the two external input clock pulses needed to drive its operation, clock pulse ϕ_{CP} 15 and input pulse ϕ_{IP} 16.

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- One advantage of the invention is that the transfer gates permit the separation of the sensing element from the holding capacitor, so that the sensing element can integrate a line of signal and the previous signal on the holding capacitor can be simultaneously read out by the shift register. Because all of the charge is parallel transferred, the accuracy and
30 vertical resolution are both excellent. This structure improves the scan speed.

A further advantage of this invention is that a small value for the capacitance C_H of the holding capacitor increases the device's sensitivity, reduce reset noise, and improves signal-to-noise ratio.

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A further advantage of this invention is that all necessary clock pulses and operational amplifiers can be built on a single chip, reducing the necessary peripheral circuitry.

5 A still further advantage of this invention is that the linearity of the photoresponse is greatly assisted by the optical black level reference, strongly promoting accurate color reconstruction.

10 A still further advantage of this invention is that the dummy element array is operated independently from the active photoelement array, promoting design flexibility for different configurations of the CIS modules.

Other and further advantages, embodiments, variations and the like will be apparent to those skilled in the art from the present specification taken with the accompanying drawings and appended Claims.

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BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of a prior art contact image sensor (CIS) system;

20 FIG. 2 shows a cross section view of a prior art CIS module;

FIG. 3 shows a prior art circuit diagram of a hybrid image sensor board;

FIG. 4 is a timing diagram for the prior art hybrid image sensor board;

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FIG. 5 is a block diagram of the prior art silicon butting CIS module with phototransistor sensing elements;

30 FIG. 6 is a block diagram of the prior art silicon butting CIS module with photodiode sensing elements;

FIGS. 7a and 7b provide a schematic representation of a simplified, digitized original document (FIG. 7a) and a detected range signal using a prior art, silicon butting image sensor chip having a pixel transfer and pixel readout (PTPR) structure (FIG. 7b);

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FIG. 8 is a prior art timing diagram with strobe light illumination;

FIG. 9 is a timing diagram for a silicon butting CIS chip with line transfer and pixel readout (LTPR) structure;

- 5 FIGS. 10a and 10b provide a schematic representation of a simplified, digitized original document (FIG. 10a), and a detected range signal according to the invention (FIG. 10b);

FIG. 11 is a block diagram of the silicon butting CIS chip with LTPR structure;

- 10 FIG. 12(a) shows a cross section view of the image sensing photoelement, transfer gate, and holding capacitors for the image sensor chip with LTPR structure;

FIG. 12(b) is a potential diagram during one integration period for the image sensor chip with LTPR structure;

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FIG. 12(c) is a potential diagram during one transfer period for the silicon butting CIS chip with LTPR structure;

- FIG. 12(d) is a potential diagram following a transfer for the silicon butting CIS chip with
20 LTPR structure;

FIG. 13 is a timing diagram for the CIS chip with LTPR structure;

FIG. 14 is a chip layout plan for the silicon butting CIS chip with LTPR structure;

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FIG. 15 is a block diagram of a hybrid, silicon butting CIS board with LTPR structure;

FIG. 16 is a timing diagram for a hybrid, silicon butting CIS board with LTPR structure;

- FIG. 17 is a simplified schematic diagram of a phototransistor APS image-sensing
30 photoelement;

FIG. 18 is a block diagram of the image sensor chip and an Active Pixel Sensor (APS) for an image sensing photoelement;

- 35 FIG. 19 is a block diagram of the CIS chip with LTPR structure, an APS image sensing photoelement and Correlated Double Sampling (CDS) circuitry; and

FIG. 20 is a timing diagram for the CIS chip with LTPR structure, an APS image sensing photoelement and CDS circuitry.

5 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

One advantage of the silicon butting contact image sensor (CIS) chip with line transfer and pixel readout (LTPR) structure are that it has the capability to scan a document accurately and quickly while avoiding distortion and while maintaining optimum vertical
10 resolution.

Referring first to FIG. 9, there is shown a timing diagram for a silicon butting CIS board 5 with LTPR structure. A series of photodetectors 4b scan the first line of the document 2 and generate an electronic signal. This electronic signal is isolated and then parallel
15 transferred to the holding capacitors associated with the photodetectors 4b when a transfer gate is turned on, triggering the transmission of a transfer pulse ϕ_T 24. After the transfer, all of the photodetectors 4b are reset to the reset voltage by a reset pulse ϕ_R 25. The input pulse ϕ_{IP} 16 triggers the shift register to read out a line of the video signal. The input pulse ϕ_{IP} 16 also turns on the stepping motor 10a which activates the roller 10
20 to advance the document 2 to the next line. The CIS board 5 then begins to read out the next line of document 2. As can be seen, integration times for all pixels are identical. The invention thus avoids the distortion problem experienced in the prior art due to different integration times for each pixel in the scanned document. Optimum vertical resolution is attained, providing accuracy which is superior to prior art conventional PTPR
25 image sensors. The scan period for one line equals readout time 23. Unlike the case with the prior art system which used strobe light illumination to eliminate distortion, no additional integration time 22 is necessary to complete a scan period (See FIGS 10a and 10b). Relative to the prior art, the scan speed is improved significantly.

30 FIG. 11 shows a simplified block diagram of the silicon butting CIS board 5 with LTPR structure. Its principal components are (1) buffer 26, (2) a timing generator 27, (3) an active photoelement array 28, and (4) a dummy element array 29. The buffer 26 is used to isolate the device from outside circuitry and to provide enough power to drive the timing generator 27, the active photoelement array 128, and the dummy element
35 array 29. Upon receipt of two pulses, clock pulse ϕ_{CP} 15 and input pulse ϕ_{IP} 16, the

timing generator 27 generates the transfer pulse ϕ_T 24, reset pulse ϕ_R 25, and frame pulse 25b.

The active photoelement array 28 consists of several components: (1) a plurality of active photoelements 30, (2) a plurality of transfer gates 31, (3) a plurality of holding capacitors 32, (4) a plurality of reset transistors 33, (5) a plurality of emitter-followers 33a, (6) the plurality of multiplexing switches 37, (7) the n-stage digital scanning shift register 38, (8) the active chip selector 39, and (9) a video buffer 40. Each emitter-follower 33a is in turn composed of one MOS transistor 134, one depletion transistor 35 and one energy-saving transistor 36.

The dummy element array 29 contains a lesser number of the same components as the active photoelement array 28, replacing the plurality of active photoelements 30 by a plurality of dummy elements 41. The dummy elements 41 have the same size as the active photoelements 30. Each dummy element 41 is placed in close proximity to a corresponding said active photoelement 30 but is shielded by some blocking means, generally aluminum, to block out the light. Only dark fixed pattern noise is generated on the dummy elements 41. The dark fixed pattern noise associated with the photoelements 30 is the same as those associated with the dummy elements 41. Comparison of the outputs from the active photoelements 30 and the dummy elements 41 permits the scrubbing from the output signal of dark fixed pattern noise and DC offset voltage. Use of dummy elements 41 cancels out the dark fixed pattern noise of the photoelements 30.

The active element array may be operated either before or after the dummy element array. The active element array and the dummy element array may each be either operated or disabled without reference to whether the other array is being operated or is disabled.

FIG. 12(a) shows a cross section view of an image sensing photoelement 30, transfer gate 31, and holding capacitor 32. The photoelements 30 are composed of a photodiode 301 and a V_{OG} gate 302. Voltage of the V_{OG} gate 302 is adjusted between the high and low levels of the transfer pulse ϕ_T 24, setting a threshold level for said photodiode. The V_{OG} gate 302 is used to set threshold levels for the photodiode 301. In one preferred embodiment, the V_{OG} gate 302 will be made of polysilicon. The

V_{OG} gate 302 also can be made by implantation of an ion with a potential voltage equal to the V_{OG} gate potential.

As depicted in potential diagrams FIGS. 12(b), 12(c), and 12(d), the transfer gate 31 is used to transfer a photocharge 303 from the photoelement 301 to the holding capacitor 32. As shown in FIG. 12(b), a potential diagram during one integration period, within an integration period the transfer gate 31 is turned off and the document 2 is illuminated by the LED light source array 1. The photocharge 303 is generated from photoelement 301 and stored in photoelement 301. As shown in FIG. 12(c), a potential diagram during one transfer period, within a transfer period the transfer gate 31 is turned on and the LED light source array 1 is shut off. The stored charge 303 on photoelement 301 is transferred to the holding capacitor 32.

As shown in FIG. 12(d), a potential diagram following a transfer, after all of the charge 303 is transferred to the holding capacitor 32, the transfer gate 31 is turned off again. At this point, all of the photocharge 303 from photoelement 301 has been transferred to the holding capacitor 32. The photoelement 301 is then ready to integrate the next line of the document 2. Because the photoelement 301 is separated from the holding capacitor 32 by the transfer gate 31, the charge on the photoelement 301 differs from that on the holding capacitor 32. The charge on the holding capacitor 32 represents the signal from the previous or (n-1)th line. The charge on photoelement 301 represents the signal from the current or nth line. Therefore, one can read the signal from the holding capacitor 32 and integrate the signal on the photoelement 301 simultaneously. The period of time to read a line of the document 2 equals either the integration time 22, or the readout time 23, significantly increasing the line scan speed. The use of holding capacitor 32 increases not only the line scan speed but also the device's sensitivity and also reduces the reset noise, significantly improving the signal-to-noise ratio. The voltage across the holding capacitor 32 equals the photocharge 303 divided by the capacitance. If the photocharge 303 generated by the photoelement 301 is ΔQ , and the capacitance of the holding capacitor 32 is C_H , then the signal $\Delta V_H = \Delta Q / C_D$. Normally, the capacitance of the photoelement 301 is large due to its large size (in a preferred embodiment, approximately $125\ \mu\text{m}$ by $125\ \mu\text{m}$ for 200 dpi). The voltage across the photoelement 301 is $\Delta V_D = \Delta Q / C_H$. Because the video signal is increased from ΔV_D across the photoelement 301 to ΔV_H across the holding capacitor 32, the device amplifies the signal by a factor of G.

$$G = C_D / C_H \quad \text{Eq. (1)}$$

where C_D is the capacitance of the photoelement 301, and
 C_H is again the capacitance of the holding capacitor 32.

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As shown in Eq. (1), a small value for the capacitance C_H of the holding capacitor 32 will increase the device's sensitivity G .

The other advantage of a small holding capacitor 32 is the reduction of reset noise.
 10 Because the charge on the holding capacitor 32 must be reset after readout, the reset mechanism generates a reset noise when resetting the holding capacitor 32 to DC level. The reset noise is proportional to the square root of the capacitance of the holding capacitor 32. Reduction of the capacitance of the holding capacitor reduces reset noise by a factor of K .

15

$$K = (C_D / C_H)^{1/2} \quad \text{Eq. (2)}$$

For a given holding capacitor 32 capacitance C_H , the reset noise N_R is given by:

$$\begin{aligned} N_R &= [(k \times T) / q] \times (C_H)^{1/2} \\ 20 \quad &= 400 (C_H)^{1/2} \text{ electrons @ } 25^\circ\text{C} \end{aligned} \quad \text{Eq. (3)}$$

If C_H equals 0.1 pF, the reset noise is 126 electrons at room temperature. This reset noise is negligible compared to a photocharge of one million electrons on the photoelement 301. The signal-to-noise (S/N) ratio is therefore significantly improved.

25 The charge on the holding capacitor 32 is converted to a voltage signal by the emitter-follower 33a. As mentioned above, the emitter-follower 33a is composed of an MOS transistor 34, a depletion transistor 35, and an energy-saving transistor 36. The depletion transistor 35 acts like a load resistor, stabilizing the signal by providing a constant current while voltage varies. The gate of the energy-saving transistor 36
 30 triggers a frame pulse ϕ_F from the timing generator 27. The emitter-follower 33a comes on only when this frame pulse is activated and is turned off during the holding period, significantly reducing power dissipation. This function reduced the power dissipation on the emitter-follower 33a. The voltage signal ΔV output by the emitter-follower 33a

equals the gain A of the emitter-follower 33a times the voltage across the holding capacitor 32.

$$\Delta V = (\Delta Q / C_D) \times A \quad \text{Eq. (4)}$$

5 where A is the gain of the emitter-follower 33a.

This signal is then read by the multiplexing switch 37 that is controlled by the n-stage shift register 38. After the signal is read by the n-stage shift register 38, the holding capacitor 32 is then reset to the reset voltage by turning on the reset transistor 33. The
10 holding capacitor 32 is then ready to receive the signal from the second line of the active photoelement 30.

As mentioned above, upon receipt of two pulses, clock pulse ϕ_{CP} 15 and input pulse ϕ_{IP} 16, the timing generator 27 generates the transfer pulse ϕ_T 24, the reset pulse ϕ_R 25,
15 and frame pulse ϕ_F 25b. Both the n-stage shift register 38 and an m-stage digital scanning shift register 42 associated with the dummy element array 29 operate in response to the same clock pulse ϕ_{CP} 15. Because the start pulses of these two shift registers are designed separately, one can read the active pixels and dummy pixels independently. An active start pulse ϕ_{ASP} 43 is used to activate the n-stage shift
20 register 38, whereas dummy start pulse ϕ_{DSP} 46 is used to trigger the m-stage shift register 42. The number of stages in the m-stage shift register 42 is smaller than the number of stages in the n-stage shift register 38. The time interval between successive activations of the m-stage shift register 42 will be longer than the time interval required to generate transfer pulse ϕ_T 24 and reset pulse ϕ_R 25, and frame pulse ϕ_T 25b.

25

FIG. 13 shows a timing diagram of an individual image sensor chip with LTPR structure. The dummy start pulse ϕ_{DSP} 46 on the dummy element array 29 connects to the input pulse ϕ_{IP} 16, which activates the m-stage shift register 42. After m clock cycles, the dummy element array 29 generates the dummy end pulse ϕ_{DEP} 47. The segment of
30 the dummy output signal V_{DO} 48 between the input pulse ϕ_{IP} 16 and the transfer pulse ϕ_T 24 is distorted by the reset and transfer process and cannot be used for black level reference. The segment of the dummy output signal V_{DO} 48 starting with the falling edge of the transfer pulse ϕ_T 24 and ending with the dummy end pulse ϕ_{DEP} 47

represents dark fixed pattern noise from the dummy element array 29. This dummy output signal V_{DO} 48 is used to provide a black level reference that cancels out the dark fixed pattern noise from the active photoelement array 28. The dummy end pulse ϕ_{DEP} 47 of the dummy element array 29 connects to the active start pulse ϕ_{ASP} 43 of the active photoelement array 28, inducing the active photoelement array 28 to activate the active photoelement 30 and read the active video signals one by one in sequence.

The use of the dummy element 41 to cancel out the dark fixed pattern noise from the photoelement 30 can be explained as follows. During the integration time 22, the charge on the capacitor associated with each active photoelement 30 is gradually removed by reverse current flowing across the associated active photoelement 30. The reverse current consists of two components: photocurrent and dark fixed pattern noise. The photocurrent equals the product of photodetector responsiveness and light intensity. During a line scan, the charge integrated from each photodetector is the product of the sum of photocurrent and dark fixed pattern noise ("dark leakage current") times the integration time 22. This charge is stored on the active photoelement 30, which builds up a potential voltage. Equation 5 describes the charge built up on photoelement site:

$$\Delta Q_A = (I_L + I_D) \times T_{int} \quad \text{Eq. (5)}$$

where I_L is light current,

I_D is dark leakage current, and

T_{int} is the integration time 22 of the image sensor.

Assuming the size of the dummy element 41 is the same as that of the active photoelement 30, the charge built up on the dummy element 41 equals the product of dark leakage current times the integration time T_{int} 22.

$$\Delta Q_D = I_D \times T_{int} \quad \text{Eq. (6)}$$

The emitter-follower 33a converts charge on the holding capacitor 32 to its associated voltage level as explained above. The active output voltage ΔV_{AO} of active photo element array is linear proportional to charge on the active photoelement 30.

$$\Delta V_{AO} = (\Delta Q_A / C_H) \times A \quad \text{Eq. (7)}$$

where C_H is the capacitance of the holding capacitor 132, and
 A is the gain of the emitter-follower 33a.

The dummy output voltage ΔV_{DO} of the dummy element array 29 is linearly
 5 proportional to the charge on the dummy element array 29.

$$\Delta V_{DO} = (\Delta Q_D / C_H) \times A \quad \text{Eq. (8)}$$

The capacitances of the holding capacitors 32 in the active photoelement array 28 and
 10 dummy holding capacitors in the dummy element array 29 are the same, as are the
 gains of the emitter-followers 33a in the two arrays. In order to cancel out the dark fixed
 pattern noise, the system is designed so that the net output signal ΔV equals the active
 output signal 45 from the active photoelement array 28 minus the dummy output signal
 48 from the dummy element array 29.

15

$$\Delta V = \Delta V_{AO} - \Delta V_{DO} = [(I_L + I_D) - I_D] \times T_{int} = I_L \times T_{int} \quad \text{Eq. (9)}$$

The integration time T_{int} 22 is constant for all of the active photoelements 30 and dummy
 elements 41. Therefore, the net output signal ΔV is linearly proportional to the
 20 photocurrent as shown in equation 9. The photocurrent is the product of the
 photoresponse R times the light intensity λ_l . The photoresponse R of the active
 photoelement 41 is the same for each of the active photoelements 30 and dummy
 elements 41. Therefore, the net output signal ΔV is linearly proportional to the light
 intensity λ_l from the reflected image of the document 2.

25

$$\Delta V \propto \lambda_l \quad \text{Eq. (10)}$$

The photoresponse linearity, defined as the net output signal ΔV divided by the light
 intensity λ_l , is thus constant. While the linearity of the photoresponse is a desirable
 30 aspect for embodiments of the invention using CIS modules 6 designed to scan black
 and white documents 2, this feature is particularly important for embodiments involving
 color CIS modules 6. In the case of applications using color CIS modules 6, each pixel
 of the digitized representation of the color document 2 is composed of a combination of
 three colors: red, green and blue. A conventional color scanner offers at least 8 bits for

each color or $2^8 = 256$ total options for each color. Therefore, considering that each pixel is composed of combinations of these three colors, a grand total of $2^{24} = 16,777,216$ different colors may be reconstructed. The color C of a given pixel is determined according to the formula:

5

$$C = A\% \times R + B\% \times G + C\% \times B \quad \text{Eq.}$$

(11)

where

10

A% is the percentage representation of the red color under the three-color description of the pixel,

B% is the percentage representation of the green color,

C% is the percentage representation of the blue color,

15

R denotes the red color,

G denotes the green color, and

B denotes the blue color.

20

Note that $A + B + C = 100$. The above demonstrated constancy of the photoresponse linearity strongly promotes accurate reconstruction of the color image of the document 2.

25

FIG. 14 shows a chip layout plan for the silicon butting CIS chip with LTPR structure. As pictured, the active photoelement array 28 is arranged on the upper half of the image sensor chip 11, while the dummy element array 29 is located on the lower half of the chip 11. A total of n active photoelements 30 are set in a single line at equal distances from each other. A very long active photoelement 30 or series of photoelements 30 which may, for example, be A4 size, can easily be butted on the chip 11.

30

FIG. 15 is a block diagram of the silicon butting CIS board with LTPR structure, comprised of (1) a plurality of silicon butting CIS chips 11; (2) a flip-flop circuit 67; and (3) an operational amplifier 68a. In response to the start pulse ϕ_{SP} 14, the dummy element array 29 on a first chip 49 emits a dummy start pulse ϕ_{DSP} 52 which triggers the input pulse ϕ_{IP} 16. A dummy end pulse ϕ_{DEP} 53 is emitted by the dummy element array 29. The dummy end pulse ϕ_{DEP} 53 is coupled to an active start pulse ϕ_{ASP} 54.

35

This design allows for great flexibility in that further connections to the dummy element array 29 may be arranged prior to the connection to the active photoelement array 28 in order to provide a longer time for determination of the black level reference. The dummy element array 29 produces a dummy output signal V_{DO} 55 which is combined

5 with an active output signal V_{AO} 56 generated by the active photoelement array 28. The active photoelement array 28 of the first chip 49 emits an active end pulse ϕ_{AEP} 58, which connects to a second chip active start pulse ϕ_{ASP} 59 on a second chip 51, and so on. The last chip 50 connects a last chip active start pulse ϕ_{ASP} to the active end pulse of previous chip and outputs 60 to a last-but-one chip active end pulse ϕ_{AEP} 161 on a

10 last-but-one chip 50. The active photoelement array 28 triggers a last chip active end pulse ϕ_{AEP} 62 from the last chip 50 which in turn connects to a dummy start pulse ϕ_{DSP} 63 on the dummy element array 29. A dummy output signal V_{DO} 64 from the dummy element array 29 is combined with an active output signal V_{AO} 65 generated by the active photoelement array 28. Three bonding pads exist for the active photoelement

15 array 28, corresponding to the active start pulse ϕ_{ASP} 54, the active end pulse ϕ_{AEP} 58, and the active output signal, V_{AO} 65. Three bonding pads exist for the dummy element array 29, corresponding to the dummy start pulse ϕ_{DSP} 52, the dummy end pulse ϕ_{DEP} 53, and the dummy output signal V_{DO} 55. The dummy end pulse ϕ_{DEP} 53 and the start pulse ϕ_{SP} 14 are connected to alternate sides of the flip-flop circuit 67. The flip-flop

20 circuit 67 generates an LED output pulse ϕ_{LED} 68. This pulse causes the automatic illumination of the document 2. The dummy element arrays 29 of all chips 51 other than the first chip 49 and the last chip 50 are disabled by disabling the dummy start pulse ϕ_{DSP} 52a, the dummy end pulse ϕ_{DEP} 53a and the dummy output signal V_{DO} 55a. All of the analog signals generated by the chips 11 are combined and then amplified by the

25 operational amplifier 68a.

FIG. 16 is a timing diagram for the hybrid, silicon butting CIS board with LTPR structure. A number m_1 of preceding dummy pixels 69 from dummy signal precede active pixels 70, which carry the video signal, while a number m_2 of following dummy pixels 71 follow

30 the active pixels 70. As discussed above, the preceding and following dummy pixels 69 and 71 enable the cancelling out of the dark fixed pattern noise. In operation, upon receipt by the CIS module 6 of a start pulse ϕ_{SP} , the timing generator 27 simultaneously generates the reset pulse ϕ_R 25, the frame pulse ϕ_F , and the transfer pulse ϕ_T 24. The

capacitance of the holding capacitor 32 is reset to the reset voltage by the reset pulse ϕ_R 25. The transfer pulse ϕ_T 24 triggers the operation of a series of active photoelements 30. This electronic signal is isolated and then parallel transferred to the holding capacitors 32 associated with the active photoelements 30.

5

The series of active photoelements 30 integrates the next line of the document 2. The charge on the active holding capacitor 32 is converted to a voltage signal by the emitter-follower 33a as described by equation (4). This signal is then read by the multiplexing switch 37 that is controlled by the n-stage shift register 38. After the signal
10 is read by the n-stage shift register 38, the holding capacitor 32 is then reset to the reset voltage by turning on the reset transistor 33. The holding capacitor 32 is then ready to receive the signal from the second line of the photoelement 30. This mechanism is repeated again to read the next line of the document 2.

15 In one embodiment, a passive pixel sensor (PPS) can be used to make an active photoelement.

FIG. 12 shows the active photodiode PPS comprises a photodiode 301 and a V_{OG} gate. The voltage level of the V_{OG} gate is adjusted between the high and low levels of
20 the transfer pulse ϕ_T in order to set a threshold level for the photodiode. The photodiode accumulates charge and then converts a charge signal to a voltage signal. In one embodiment, the active photodiode is an active pn junction photodiode capable of converting a charge signal to a voltage signal. In an alternative embodiment, the diode is a p-i-n photodiode, which has ten times lower dark fixed pattern noise than does a
25 conventional pn junction photodiode. In one embodiment, the V_{OG} gate is an gate made by ion implantation. In this case, a single polysilicon wafer process can be used.

In an embodiment having a photodiode with an image sensor chip principally comprises: (1) a buffer, (2) a timing generator, (3) an active photoelement array, and (4)
30 a dummy element array. The active photoelement array itself comprises several components: (1) a plurality of active PPS's, (2) a plurality of active holding capacitors, (3) a plurality of reset transistors; (4) a plurality of emitter-followers, (5) a plurality of multiplexing switches, (6) the n-stage shift register, (7) the active chip selector, (8) the video buffer, and (9) a plurality of transfer gates capable of separating the charges on
35 the active PPS's from the charges on the active holding capacitors and capable of

transferring the charges on the active PPS's to the active holding capacitors. This arrangement permits the simultaneous reading of the charge on the active holding capacitor and integration of the charge on the photoelement.

- 5 A dummy element array contains a lesser number of the same components as the active photoelement array, replacing the plurality of active PPS's by a plurality of dummy PPS's. Again, the dummy element array may be simplified by separating out selected components from the rest of the dummy array. For example, if the m-stage shift register 42 is separated out, a dummy output signal V_{DO} of constant voltage results.

10

Each emitter-follower is composed of one MOS transistor 34, one depletion transistor 35 and one energy-saving transistor 36. The depletion transistor acts like a load resistor, stabilizing the signal by providing a constant current while voltage varies. The gate of the energy-saving transistor triggers a sample pulse. The emitter-follower
15 comes on only during the sampling period and is turned off during the holding period, significantly reducing power dissipation. During the integration period, photocharges are generated by the photodiode and stored by its associated holding capacitor. The photocharge on the holding capacitor is converted to a voltage signal by the emitter-follower.

20

In another embodiment, an active pixel sensor (APS) can be used to make a CIS chip 11. The chip principally comprises: (1) a buffer, (2) a timing generator, (3) an active photoelement array, and (4) a dummy element array. The active photoelement array
128 itself comprises several components: (1) a plurality of active APS's, (2) a plurality
25 of sample/hold switches, (3) a plurality of holding capacitors, (4) a plurality of multiplexing switches, (5) the n-stage shift register, (6) the active chip selector, and (7) the video buffer. The dummy element array again contains a lesser number of the same components as the active photoelement array, replacing the plurality of APS's by a plurality of dummy APS's. The dummy elements have the same size as the active
30 photoelements but are covered with aluminum to block out the light. Again, the dummy element array may be simplified by separating out selected components from the rest of the dummy array. For example, if the m-stage shift register is separated out, a dummy output signal V_{DO} 64 of constant voltage will result.

- 35 FIG. 17 shows a simplified schematic diagram of a phototransistor APS. The phototransistor APS comprises: (1) a phototransistor 85, (2) a pn junction photodiode

86, (3) a base reset transistor 87, (4) a APS capacitor 88, and (5) an emitter-reset transistor 89. The phototransistor 85 converts an optical signal to an electronic signal. The phototransistor 85 switches on when the base voltage exceeds a fixed non-zero emitter voltage such as 0.7 V. In order to prevent problems in low lighting levels, the
5 pn junction photodiode 86 is inserted between the base of the phototransistor 85 and the base reset transistor 87. The base voltage resets to a fixed non-zero voltage such as 0.7 V instead of to ground as with a conventional phototransistor structure. The other advantage of the pn junction diode 86 is it allows for rapid temperature equalization between the photodiode 86 and the base-emitter of the phototransistor. During reset,
10 the emitter-reset transistor 89 resets the emitter to ground, whereas the base reset transistor 87 resets the voltage across the base of the phototransistor to a fixed non-zero value such as 0.7 V. Both the base and the emitter of the phototransistor are reset to the reset voltage at the same time. The APS capacitor 88 stores the charge corresponding to the converted signal. The combination of the phototransistor 85 and
15 the APS capacitor 88 effectively acts as an emitter-follower. This design follows a simple schematic, lowering the cost of the board.

FIG. 18 shows a block diagram of the image sensor chip 11 with an active photodiode APS 74 as an active image sensing photoelement 30. Each photodiode APS 74
20 comprised of one photodiode 301, one reset transistor 33, and one emitter-follower 33a. The photodiode 301 converts a charge signal to a voltage signal on every pixel. Each emitter-follower 33a is in turn composed of one MOS transistor 34, one depletion transistor 35 and one energy-saving transistor 36. The depletion transistor 35 acts like a load resistor, stabilizing the signal by providing a constant current while voltage varies.
25 The gate of the energy-saving transistor 36 triggers a sample pulse. The APS 74 comes on only during the sampling period in response to the chip selector pulse and is turned off during the holding period, significantly reducing power dissipation. During the integration period, photocharges are generated by the photodiode and stored by its associated capacitor 32. The photocharge is converted to a voltage signal by the
30 emitter-follower 33a. In one embodiment, the active photodiode is an active pn junction photodiode capable of converting a charge signal to a voltage signal on every pixel. In an alternative embodiment, the diode is a p-i-n photodiode, which has ten times lower dark fixed pattern noise than does a conventional pn junction photodiode.

35 For both the PPS and APS embodiments, the voltage signal ΔV generated by the emitter-follower 33a is given by the equation:

$$\Delta V = (\Delta Q / C_D) \times A \quad \text{Eq. (12)}$$

where ΔQ is the photocharge,

C_D is the photodiode capacitance, and

5 A is the gain of the emitter-follower 33a.

For the APS system, during the transfer period, the sample/hold switch 75 generates a sample/hold pulse $\phi_{S/H}$ which triggers the sampling of the voltage signal ΔV and then the holding of the signal on the holding capacitor 32. After the sampling and holding has
 10 taken place, the reset transistor 33 resets the charge on the photodiode 301, causing the voltage signal ΔV to be reset. The photodiode 301 is then ready to integrate the charge from the next line of the document 2. The voltage ΔV_C across the holding capacitor 32 thus represents the video signal from the previous line of the document 2. The discharge of the voltage $\Delta V_C(t)$ across the holding capacitor 32 as a function of time t
 15 is described by:

$$\Delta V_C(t) = \Delta V \times \exp(-t/RC_H) \quad \text{Eq. (13)}$$

where R is the effective resistance of the system, and

20 C_H is again the capacitance of the holding capacitor 32.

Therefore, the capacitance C_H of the holding capacitor 32 must be large enough that the voltage signal ΔV can be retained for one transfer period. The voltage signals across the holding capacitors 32 are then read one by one in sequence by the multiplexing
 25 switch 37 that is controlled by the n -stage shift register 138.

After a signal has been read by the n -stage shift register 38, the reset transistor 33 resets the voltage signal ΔV . Reset noise in the form of kTC noise results and may be significant given the large surface area of the active photoelement 30. Therefore a
 30 preferred embodiment incorporates correlated double sampling (CDS) circuitry to cancel the reset noise. This is achieved by creating more than one row of active sample/hold switches, active holding capacitors, and active multiplexing switches as well as more than one row of dummy sample/hold switches, dummy holding capacitors, and dummy multiplexing switches. Again, the dummy element array may be simplified by

separating out selected components from the rest of the dummy array. FIG. 19 shows a block diagram of the CIS chip with LTPR structure, an APS image sensing photoelement and Correlated Double Sampling (CDS) circuitry.

- 5 FIG. 20 is a timing diagram for the same chip. Instead of using one sample/hold pulse as in the previous embodiment, this embodiment uses two sample/hold pulses $\phi_{S/H1}$ 93 and $\phi_{S/H2}$ 94 to cancel reset noise.

The above disclosure is not intended as limiting. Those skilled in the art will readily
10 observe that numerous modifications and variations of the present invention are possible while retaining the teachings of the invention. Accordingly, the invention may be practiced otherwise than as specifically described herein.

CLAIMS

1. A silicon butting contact image sensor (CIS) chip with line transfer and pixel readout (LTPR) structure, comprising:
 - 5 a timing generator capable of generating pulses required to operate the chip including a transfer pulse ϕ_T , a reset pulse ϕ_R , and a frame pulse ϕ_F .
 an active photoelement array capable of responding to pulses from said timing generator, said active photoelement array containing a plurality of active photoelements, said active photoelement array having the capability of converting an optical signal into
 - 10 an electronic signal;
 a dummy element array containing a plurality of dummy elements, each said dummy element being placed in close proximity to a corresponding active sensing element, said dummy element array having the capability of providing an optical black level reference;
 - 15 a shielding means to ensure that said dummy elements receive no light exposure so that each dummy elements generates a reference output signal;
 an output line capable of transmitting the signal generated by the CIS chip to outside circuitry; and
 a buffer capable of isolating said chip from outside circuitry and of driving the
 - 20 video line capacitance of said chip.
 2. The CIS chip of Claim 1, wherein:
 said active element array comprises an active clock pulse bonding pad for a clock pulse ϕ_{CP} ;
 - 25 said dummy element array comprises a dummy clock pulse bonding pad for said clock pulse ϕ_{CP} ; and
 said dummy clock pulse bonding pad may be said active clock pulse bonding pad or may be a distinct bonding pad.
 - 30 3. The CIS chip of Claim 1, wherein:
 said active element array comprises one active start pulse bonding pad for an active start pulse ϕ_{ASP} , one active end pulse bonding pad for an active end pulse ϕ_{AEP} , and one active output signal bonding pad for an active output signal V_{AO} ; and

said dummy element array comprises one dummy start pulse bonding pad for a dummy start pulse ϕ_{DSP} , one dummy end pulse bonding pad for a dummy end pulse ϕ_{DEP} , and one dummy output signal bonding pad for a dummy output signal V_{DO} .

5 4. The CIS chip of Claim 1, wherein:

said active element array may be either operated or disabled without reference to whether said dummy element array is being operated or is disabled; and

said dummy element array may be either operated or disabled without reference to whether said active element array is being operated or is disabled.

10

5. A hybrid silicon butting CIS board, comprising:

a plurality of the silicon CIS chips of Claim 1, butted together end to end on a substrate in one line with approximately equal space between adjacent detectors.

15 6. The CIS board of Claim 5, further comprising:

a flip-flop circuit capable of generating an LED output pulse ϕ_{LED} , said output pulse ϕ_{LED} causing the automatic illumination of said document; and

an operational amplifier capable of combining and then amplifying all of the analog signals generated by said CIS chips.

20

7. The CIS board of Claim 6, in which said plurality of silicon CIS chips comprise:

a first chip dummy start pulse ϕ_{DSP} on a first chip of said dummy element array, said first chip dummy start pulse ϕ_{DSP} being triggered by a start pulse ϕ_{SP} from an external circuit, said dummy start pulse ϕ_{DSP} in turn triggering an input pulse ϕ_{IP} to said
25 external circuit;

a dummy end pulse ϕ_{DEP} for each said chip;

an active start pulse ϕ_{ASP} for each said chip, each said active start pulse being connected to each said dummy end pulse bonding pad, except in the case of said active start pulse for a last chip;

30 said bonding pads for said active start pulse ϕ_{ASP} of all said chips other than said last chip being connected to said bonding pad for said active end pulse ϕ_{AEP} of immediately previous said chip; and

said active start pulse ϕ_{ASP} bonding pad of said last chip being connected to an active end pulse ϕ_{AEP} bonding pad of a last-but-one chip; and

said bonding pad for said active end pulse ϕ_{AEP} of said active element array being connected to said bonding pad for said dummy start pulse ϕ_{DSP} on said dummy element array.

5 8. The hybrid silicon butting CIS board of Claim 7, wherein one or more said active element arrays and one or more said dummy element arrays may be flexibly configured on said silicon butting contact image sensor board.

9. The hybrid silicon butting CIS board of Claim 6, in which said board comprises a
10 strobe light generator capable of generating output pulses of LED strobe light to illuminate said document.

10. The hybrid silicon butting CIS board of Claim 6, in which said operational amplifier is capable of amplifying said signals to achieve a voltage reference.

15

11. The board of Claim 10, in which said operational amplifier is built on said chip, and said operational amplifier comprises a gain and offset adjustment to facilitate the achievement of a reference voltage.

20 12. The board of Claim 10, in which said operational amplifier is built on said CIS board;

said operational amplifier maintains constant gain; and

said operational amplifier achieves said voltage reference by adjusting LED current or by varying integration time.

25

13. The CIS chip of Claim 1 wherein said active element array comprises:

a plurality of active photoelement Passive Pixel Sensors (PPS's) capable of gathering a charge and converting it into a voltage on every pixel;

a plurality of active holding capacitors capable of accepting and storing the charge
30 gathered by said active photoelement PPS's;

a plurality of active reset transistors capable of resetting said active holding capacitors to a fixed reset voltage;

a plurality of active emitter-followers capable of converting said charge on said active holding capacitors into voltage signals;

35 a plurality of active multiplexing switches, each said switch being coupled between one of said active photoelements and said output line;

an n-stage digital scanning shift register having a plurality of outputs, each of said outputs being coupled to a control input of one of said active multiplexing switches;

an active chip selector capable of emitting an active chip selector pulse which activates said emitter-follower;

5 an active video buffer; and

a plurality of active transfer gates capable of separating said charges on said active PPS's from said charges on said active holding capacitors and capable of transferring said charges on said active PPS's to said active holding capacitors,

10 said n-stage shift register activating each said active photoelement PPS in sequence, each said photoelement PPS thereby generating an active output signal that is received by said active video buffer, as said n-stage shift register activates each succeeding active photoelement PPS in sequence, said n-stage shift register resetting each preceding active photoelement PPS in sequence to a dark level.

15 14. The CIS chip of Claim 13, wherein said dummy element array comprises:

a plurality of dummy Passive Pixel Sensors (PPS's) capable of gathering a charge and converting it into a voltage on every pixel;

a plurality of dummy holding capacitors capable of accepting and storing the charge gathered by said dummy PPS's;

20 a plurality of dummy reset transistors capable of resetting said dummy holding capacitors to a fixed reset voltage;

a plurality of dummy emitter-followers capable of converting said charge on said dummy holding capacitors into voltage signals;

25 a plurality of dummy multiplexing switches, each switch being coupled between one of said dummy elements and said output line;

an m-stage digital scanning shift register having a plurality of outputs, each of said outputs being coupled to a control input of one of said dummy multiplexing switches;

a dummy chip selector capable of emitting a dummy chip selector pulse which activates said emitter-follower;

30 a dummy video buffer; and

a plurality of dummy transfer gates capable of separating said charges on said dummy PPS's from said charges on said dummy holding capacitors and capable of transferring said charges on said dummy PPS's to said dummy holding capacitors,

35 said m-stage shift register activating each said dummy PPS in sequence, each said dummy PPS thereby generating a dummy output signal that is received by said dummy video buffer, as said m-stage shift register activates each succeeding dummy

PPS in sequence, said m-stage shift register resetting each preceding dummy PPS in sequence to a dark level;

said active output signals from said active photoelements being compared to said dummy output signals from said dummy elements to scrub said active output signals of dark fixed pattern noise and DC offset voltage, thereby generating a resultant video output signal.

15. The CIS chip of Claim 1, wherein said active element array comprises:

a plurality of active Active Pixel Sensor (APS's) capable of gathering a charge and converting it into a voltage signal on every pixel;

a plurality of active holding capacitors capable of accepting and storing the charge gathered by said active photoelement APS's;

a plurality of active sample/hold switches, each capable of generating a sample/hold pulse $\phi_{S/H}$ which triggers a sampling of the voltage signal ΔV and then a holding of said voltage signal on said active holding capacitor;

a plurality of active multiplexing switches, each switch being coupled between one of said active photoelements and said output line;

an n-stage digital scanning shift register having a plurality of outputs, each of said outputs being coupled to a control input of one of said active multiplexing switches;

an active chip selector capable of emitting an active chip selector pulse which activates said active APS; and

at least one active video buffer.

16. The CIS chip of Claim 15, wherein said dummy element array comprises:

a plurality of dummy APS's capable of gathering a charge and converting it into a voltage signal on every pixel;

a plurality of dummy sample/hold switches, each capable of generating a sample/hold pulse $\phi_{S/H}$ which triggers a sampling of the voltage signal ΔV and then a holding of said voltage signal on said dummy holding capacitor;

a plurality of dummy holding capacitors capable of and storing the charge gathered by said dummy APS's;

a plurality of dummy multiplexing switches, each switch being coupled between one of said dummy elements and said output line;

an m-stage digital scanning shift register having a plurality of outputs, each of said outputs being coupled to a control input of one of said dummy multiplexing switches;

a dummy chip selector capable of emitting a dummy chip selector pulse which activates said dummy APS; and
at least one dummy video buffer.

- 5 17. The CIS chip of Claim 13, wherein:
each of said active PPS's comprises an active photodiode capable of accumulating photocharge and an active V_{OG} gate;
said active V_{OG} gate having a voltage level which is adjusted between the high and low levels of said transfer pulse ϕ_T , setting a threshold level for said active
10 photodiode.
18. The CIS chip of Claim 14, wherein:
each of said dummy PPS's comprise a pn junction diode capable of accumulating photocharge and a dummy V_{OG} gate;
15 said pn junction diode having the capability to convert a charge signal to a voltage signal and provide a black level reference;
said dummy V_{OG} gate having a voltage level which is adjusted between the high and low levels of said transfer pulse ϕ_T , setting a threshold level for said photodiode.
- 20 19. The CIS chip of Claim 14, wherein said dummy emitter-follower comprises:
a self-scanned photodiode array (MOS) transistor;
a depletion transistor capable of functioning as a load resistor by stabilizing the signal by providing a constant current while the voltage varies; and
an energy-saving transistor capable of triggering a frame pulse,
25 said dummy emitter-follower being turned on in response to said frame pulse.
20. The CIS chip of Claim 15, wherein each said active APS is an active phototransistor APS comprising:
an active phototransistor capable of converting an optical signal to an electronic
30 signal;
an active pn junction photodiode capable of preventing low light problems with said active phototransistor;
an active base reset transistor capable of resetting voltage across base of said active phototransistor to a fixed non-zero value;

an active capacitor capable of storing the charge corresponding to said converted signal; and

an active emitter-reset transistor capable of resetting the emitter of said phototransistor to ground.

5

21. The CIS chip of Claim 15 wherein each said active APS is a photodiode APS comprising:

an active photodiode having the capability of converting a charge signal to a voltage signal on every pixel;

10 an active reset transistor capable of resetting said active holding capacitor to a fixed reset voltage; and

an active emitter-follower capable of converting said charge on said active holding capacitors into voltage signals.

15 22. The CIS chip of Claim 16, wherein each said dummy APS comprises:

a dummy diode having the same size as said active photoelements, said dummy diode being covered with aluminum to block out the light, said dummy diode having the capability of converting a charge signal to a voltage signal on every pixel;

20 a dummy reset transistor capable of resetting said dummy holding capacitor to a fixed reset voltage; and

a dummy emitter-follower capable of converting said charge on said active holding capacitors into voltage signals.

23. The CIS chip of Claim 16, wherein each said dummy APS is a dummy transistor
25 APS comprising:

a dummy transistor capable of converting an optical signal to an electronic signal;

a dummy pn junction diode capable of preventing low light problems with said dummy transistor;

30 a dummy base reset transistor capable of resetting voltage across base of said dummy transistor to a fixed non-zero value;

a dummy capacitor capable of storing the charge corresponding to said converted signal; and

a dummy emitter-reset transistor capable of resetting the emitter of said dummy transistor to ground.

35

24 The CIS chip of Claim 6, wherein:

said plurality of active APS's comprises at least two active rows of said active sample/hold switches, said active holding capacitors, and said active multiplexing switches;

5 said plurality of dummy APS's comprises at least two dummy rows of said dummy sample/hold switches, said dummy holding capacitors, and said dummy multiplexing switches; and

said at least two active rows and said at least two dummy rows operating as a Correlated Double Sampling (CDS) circuit and cancelling out reset noise from the active photodiode.

10

25 The CIS chip of Claim 21, wherein said active emitter-follower comprises:
an active MOS transistor;

an active depletion transistor capable of functioning as a load resistor by stabilizing the signal by providing a constant current while the voltage varies; and

15

an active energy-saving transistor capable of triggering a frame pulse,
said active emitter-follower being turned on in response to said frame pulse.

26. The CIS chip of Claim 1, wherein said shielding means is aluminum.

20

27. The CIS chip of Claim 13, wherein said active transfer gates are polysilicon gates.

28. The CIS chip of Claim 13, wherein said active holding capacitors are diffusion capacitors.

25

29. The CIS chip of Claim 13, wherein said active holding capacitors are polysilicon capacitors.

30. The CIS chip of Claim 13, wherein said active photodiode is a pn junction photodiode.

30

31. The CIS chip of Claim 13, wherein said active photodiode is a p-i-n photodiode.

32. The CIS chip of Claim 14, wherein said dummy holding capacitors are diffusion capacitors.

35

33. The CIS chip of Claim 14, wherein said dummy transfer gates are polysilicon gates.

34. The CIS chip of Claim 17, wherein said active V_{OG} gate is an ion implant gate.

5

35. The CIS chip of Claim 17, wherein said active photodiode is a pn junction photodiode.

36. The CIS chip of Claim 17, wherein said active photodiode is a p-i-n photodiode.

10

37. The CIS chip of Claim 18, wherein said dummy V_{OG} gate is an ion implant gate.

38. The CIS chip of Claim 21, wherein said active photodiode is a pn junction photodiode.

15

39. The CIS chip of Claim 21, wherein said active photodiode is a p-i-n photodiode.

40. The CIS chip of Claim 22, wherein said dummy diode is a pn junction diode.

20 41. The CIS chip of Claim 22 wherein said dummy diode is a p-i-n diode.

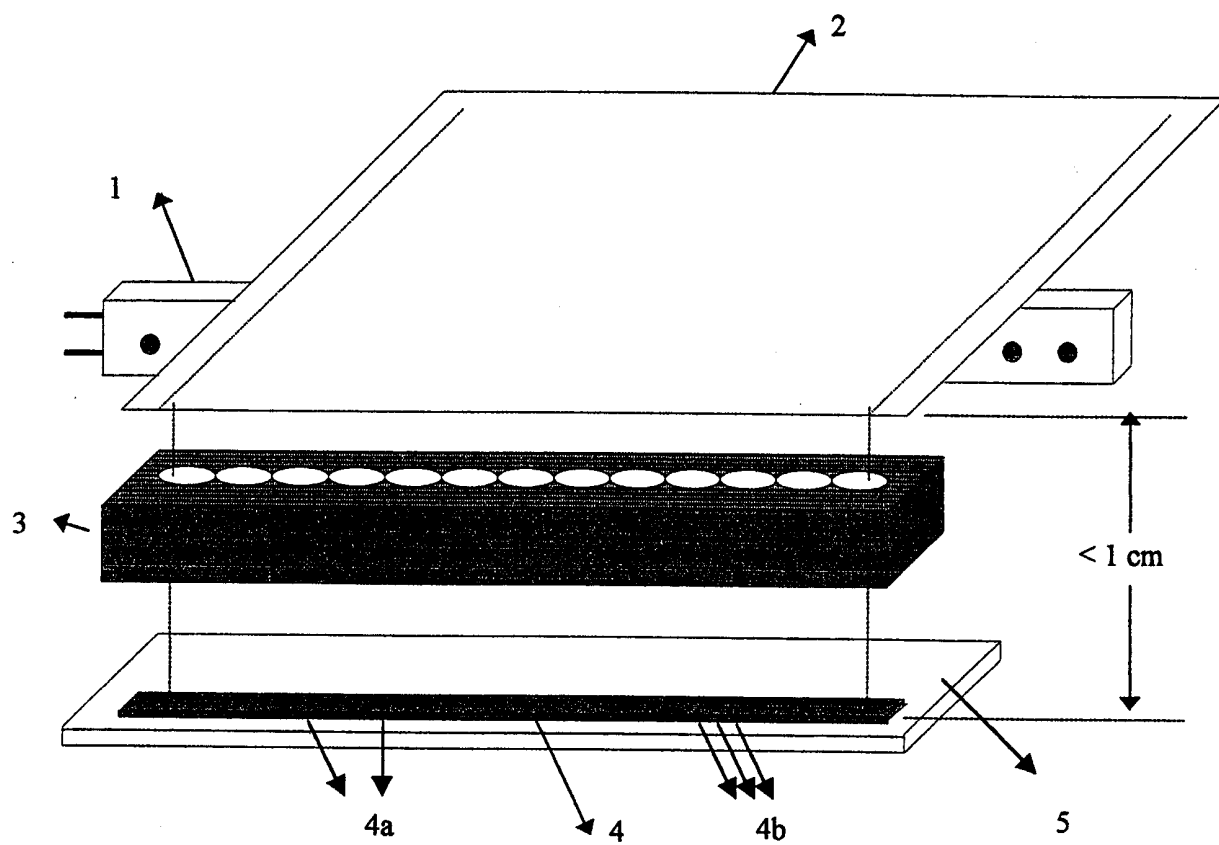


Figure 1 (prior art)

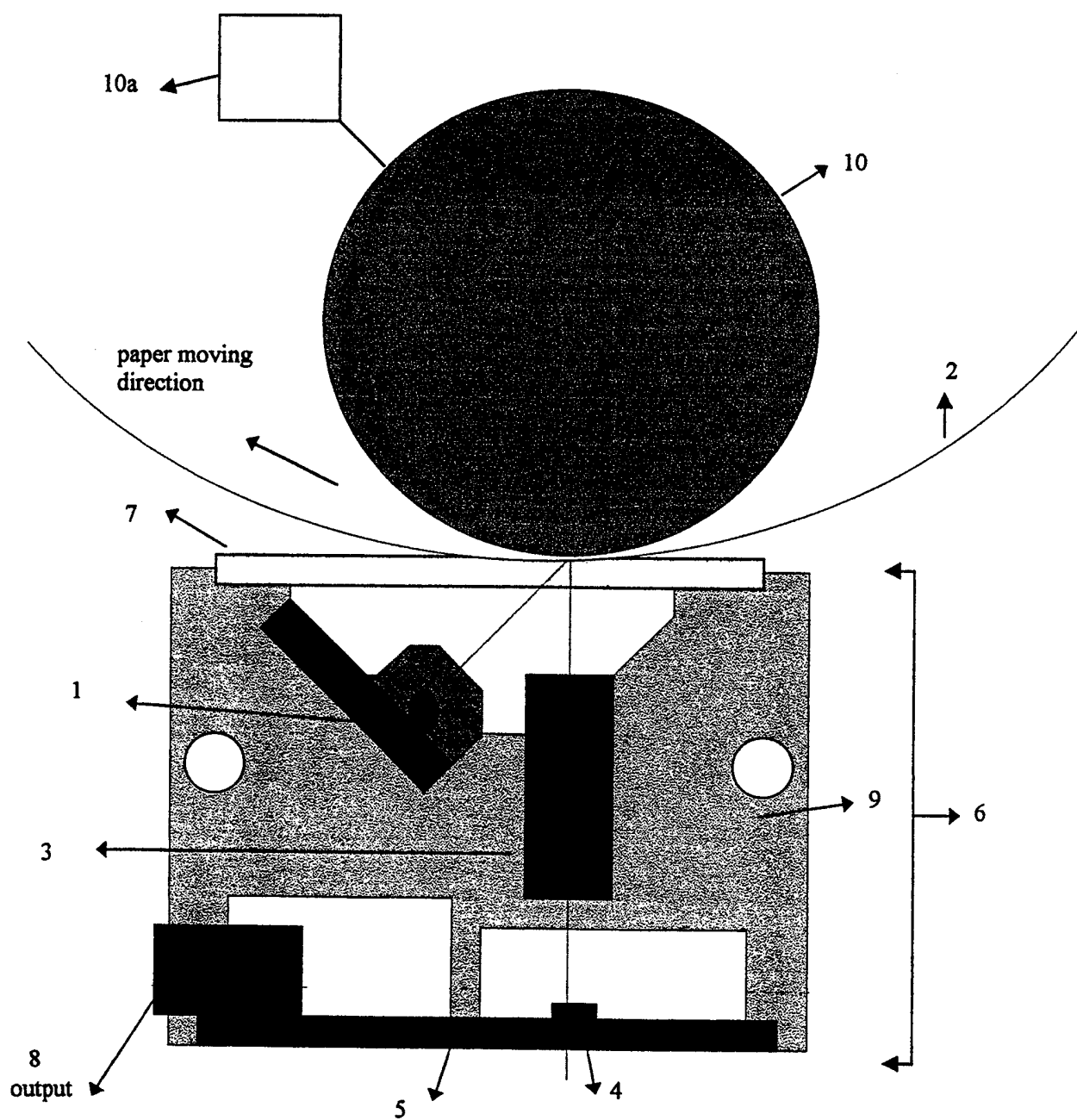


Figure 2. (prior art)

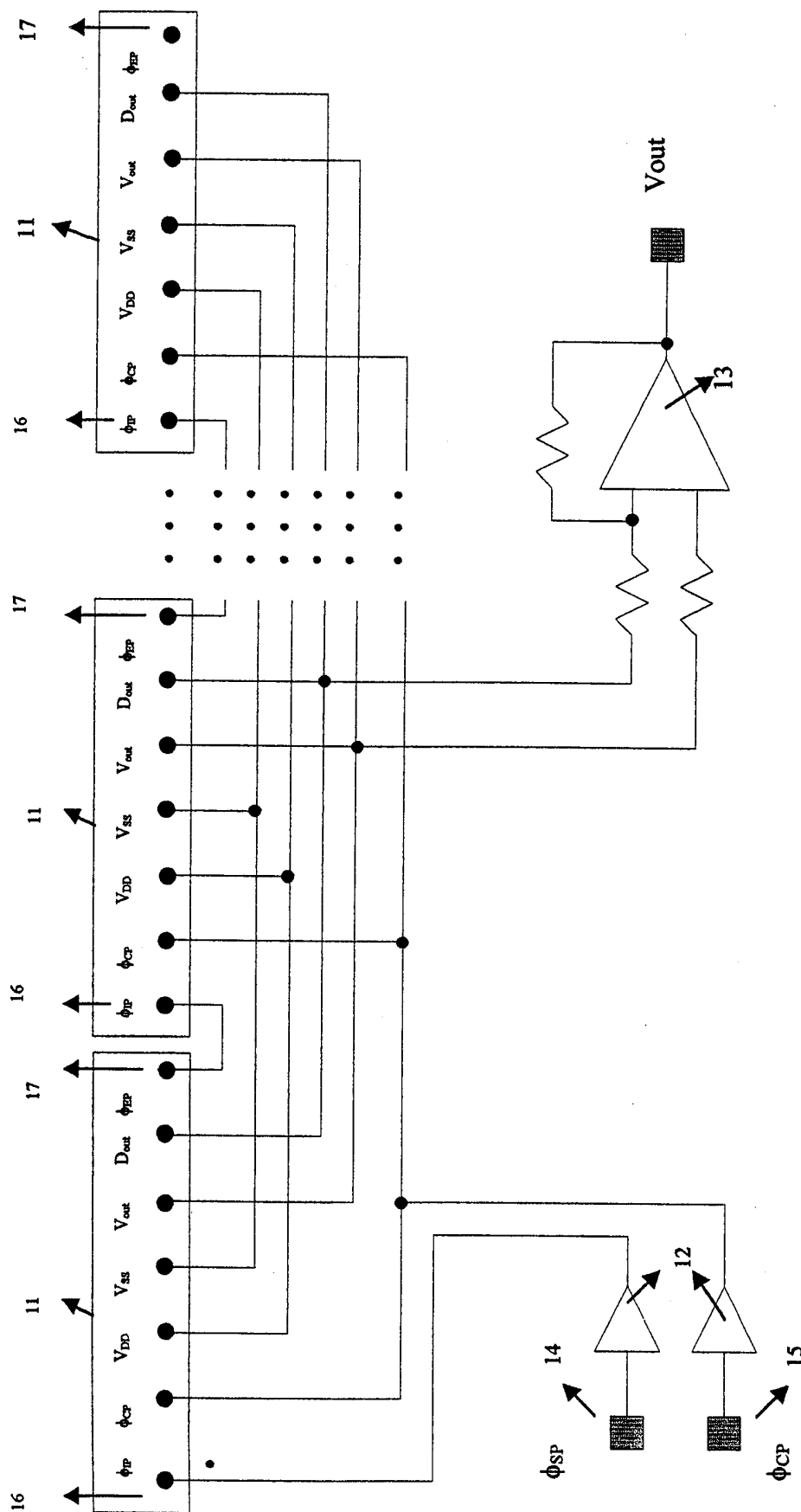


Figure 3. (prior art)

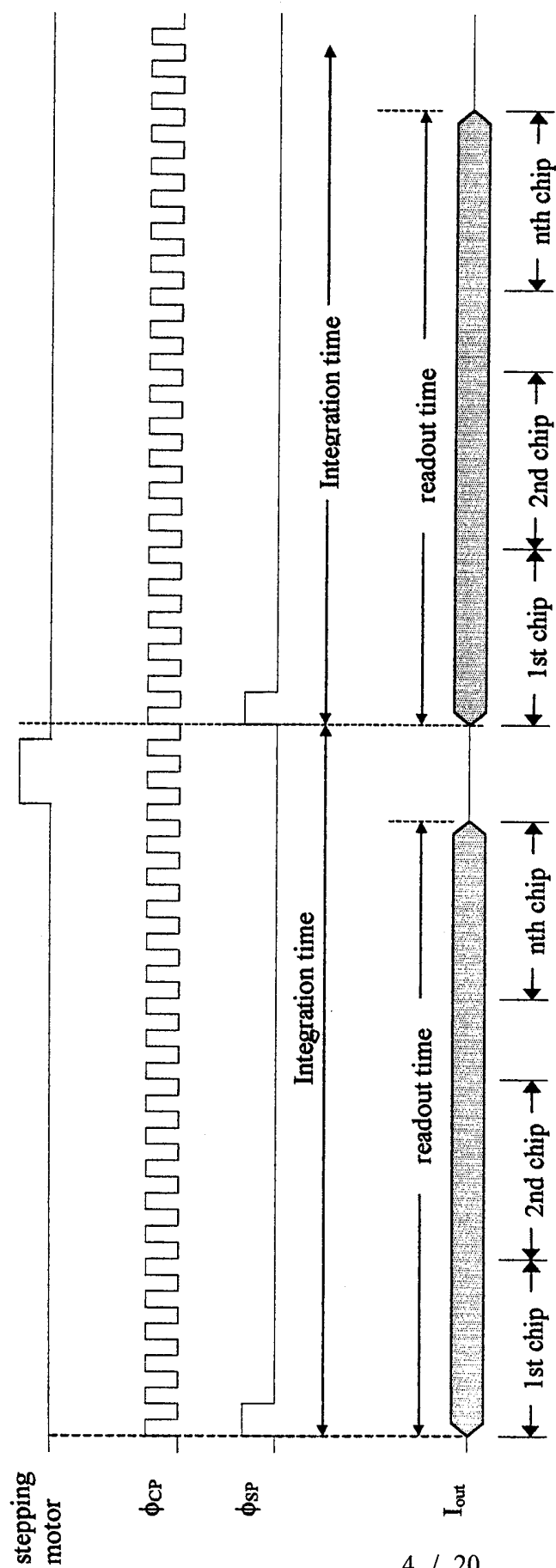


Figure 4 (prior art)

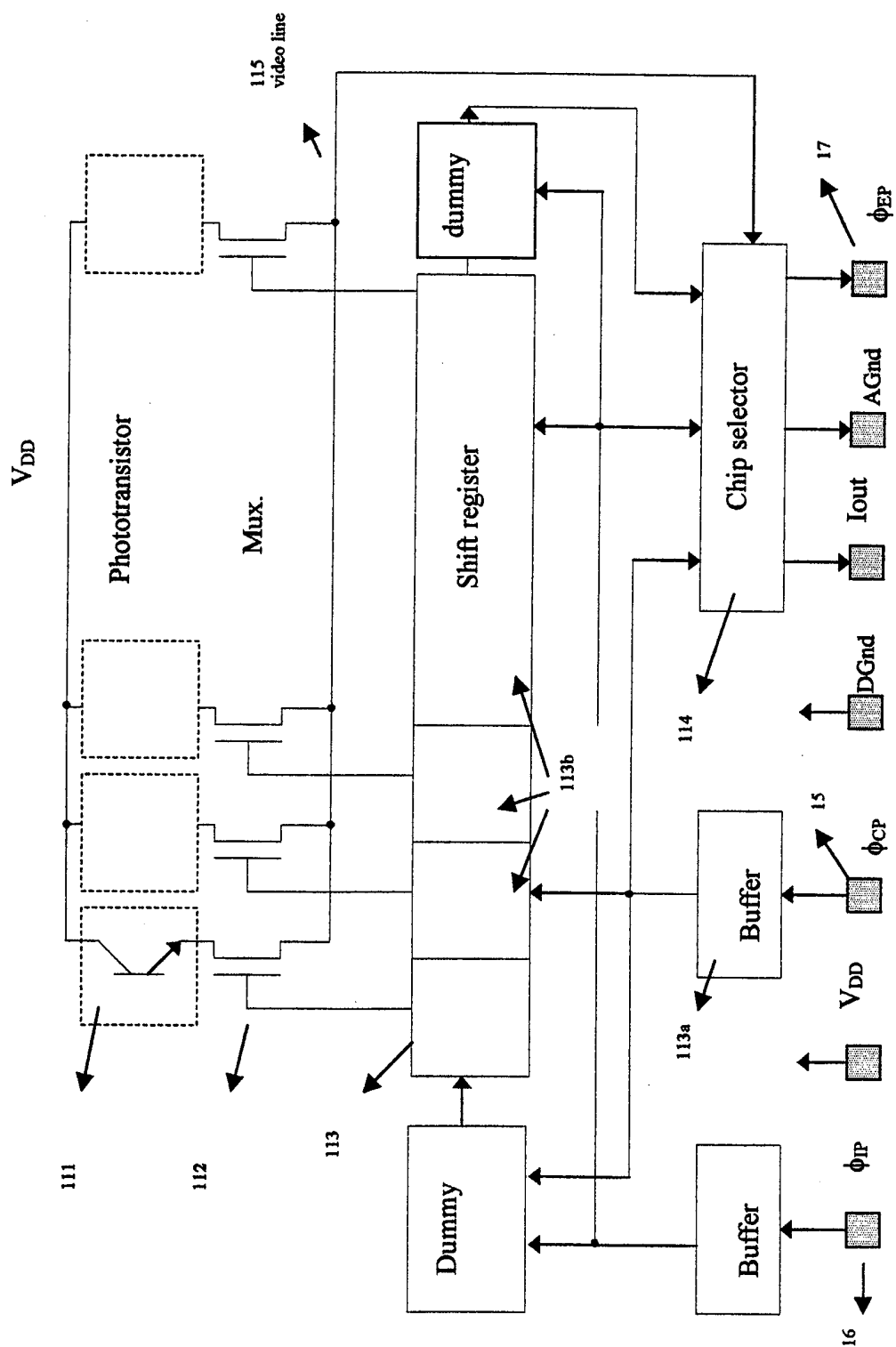


Figure 5. (prior art)

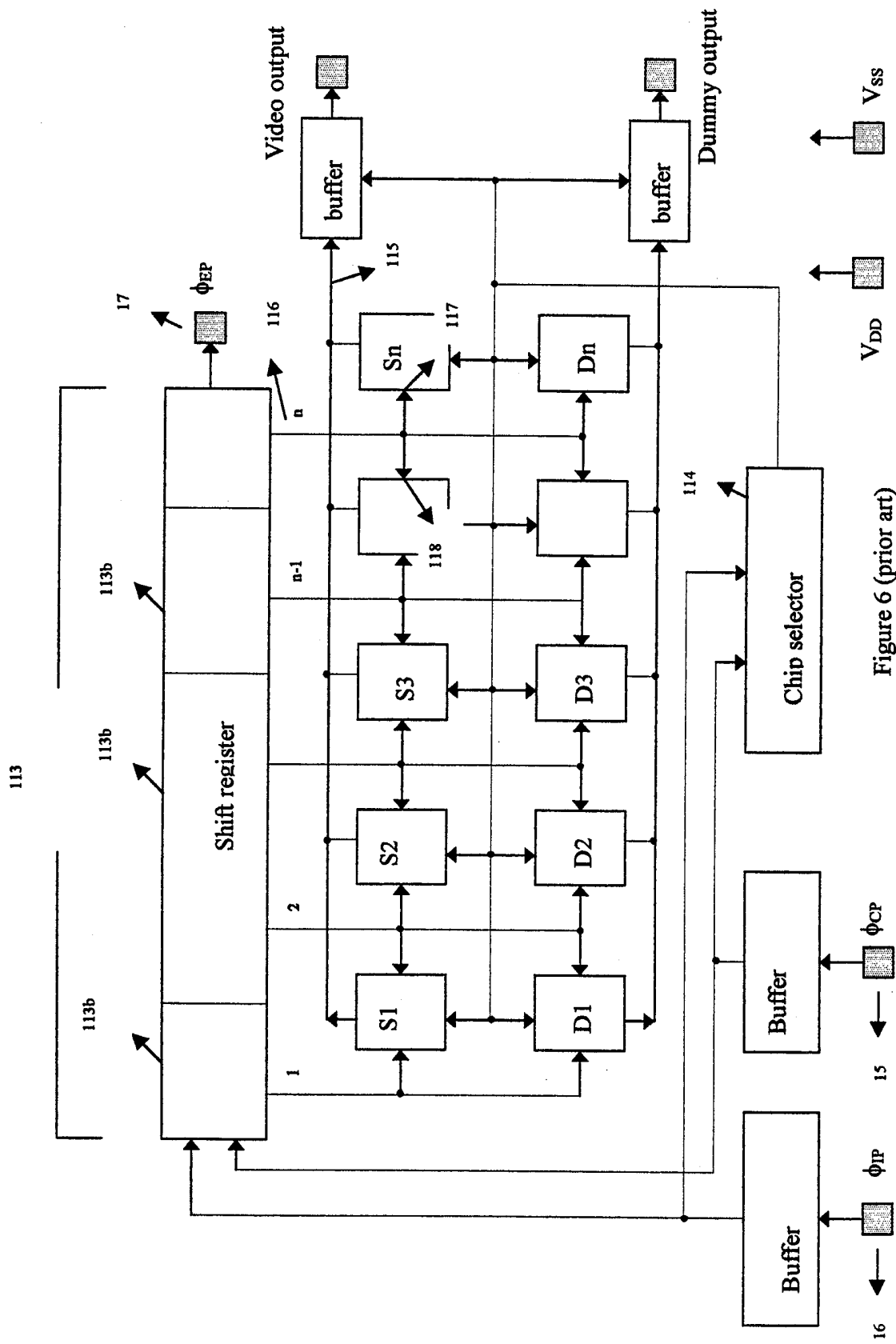


Figure 6 (prior art)

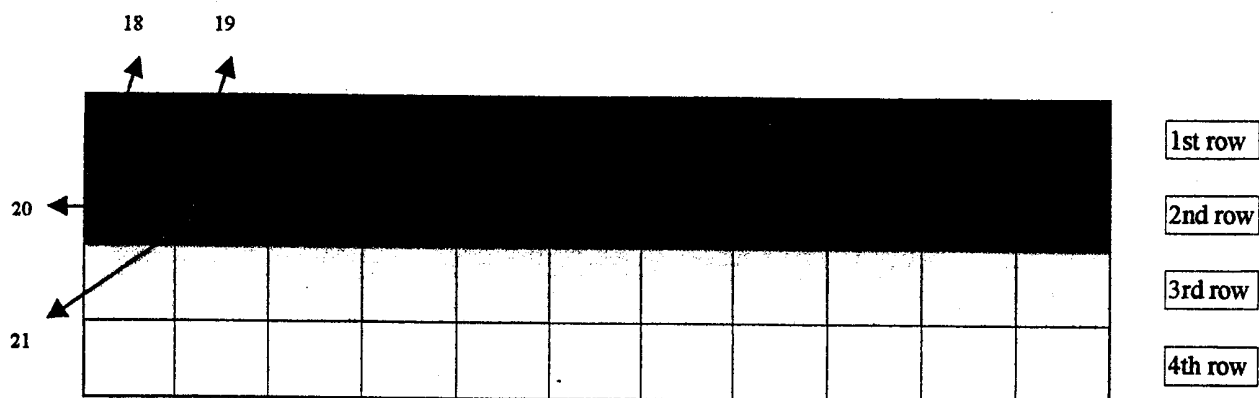


Figure 7(a) (prior art)

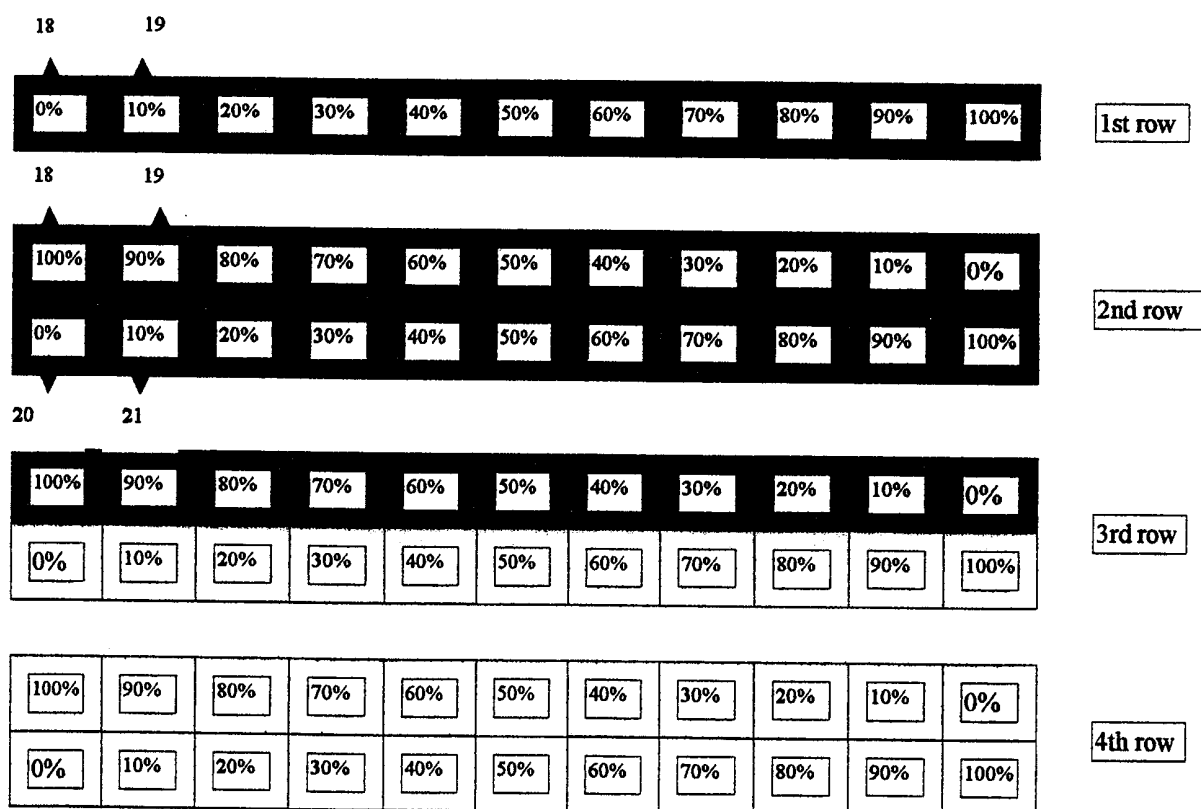


Figure 7(b) (prior art)

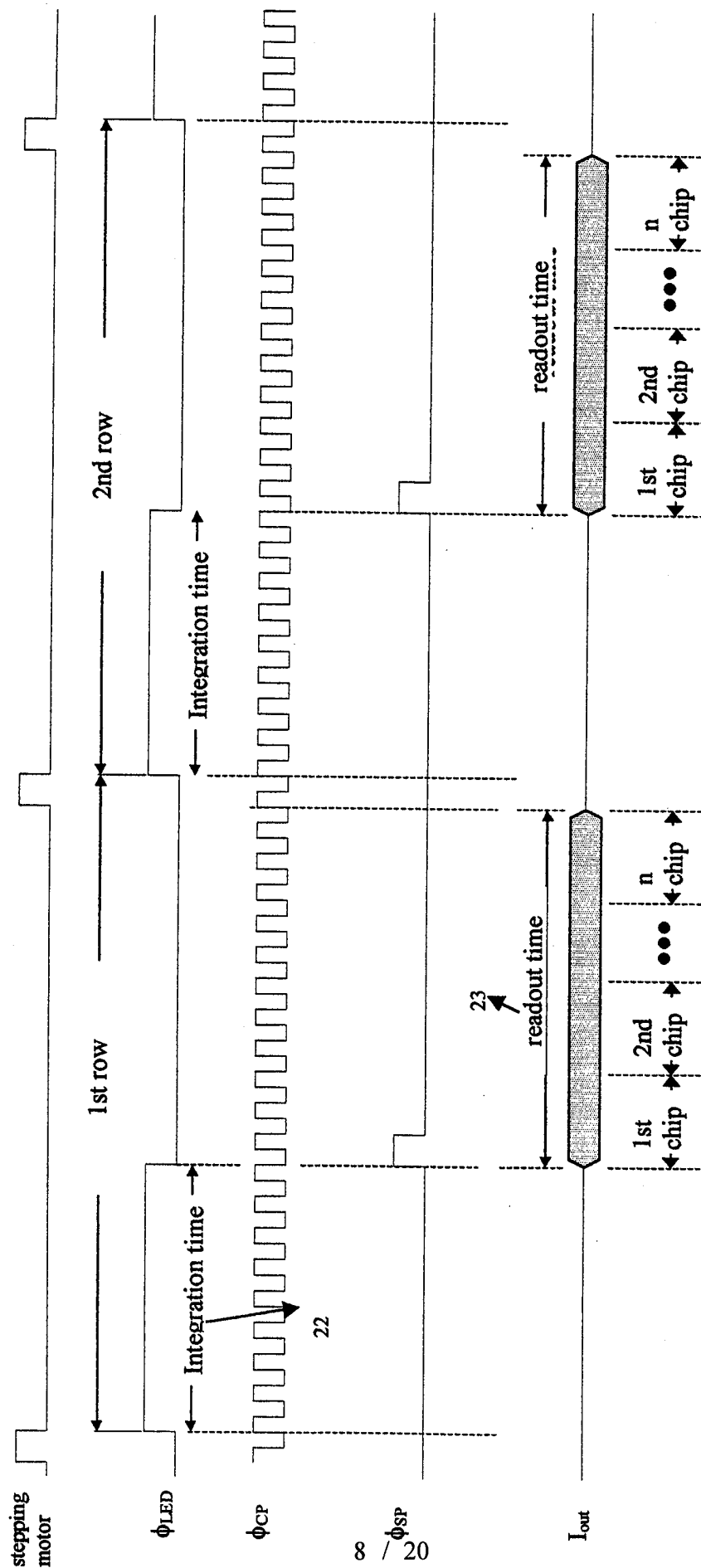


Figure 8 . (prior art)

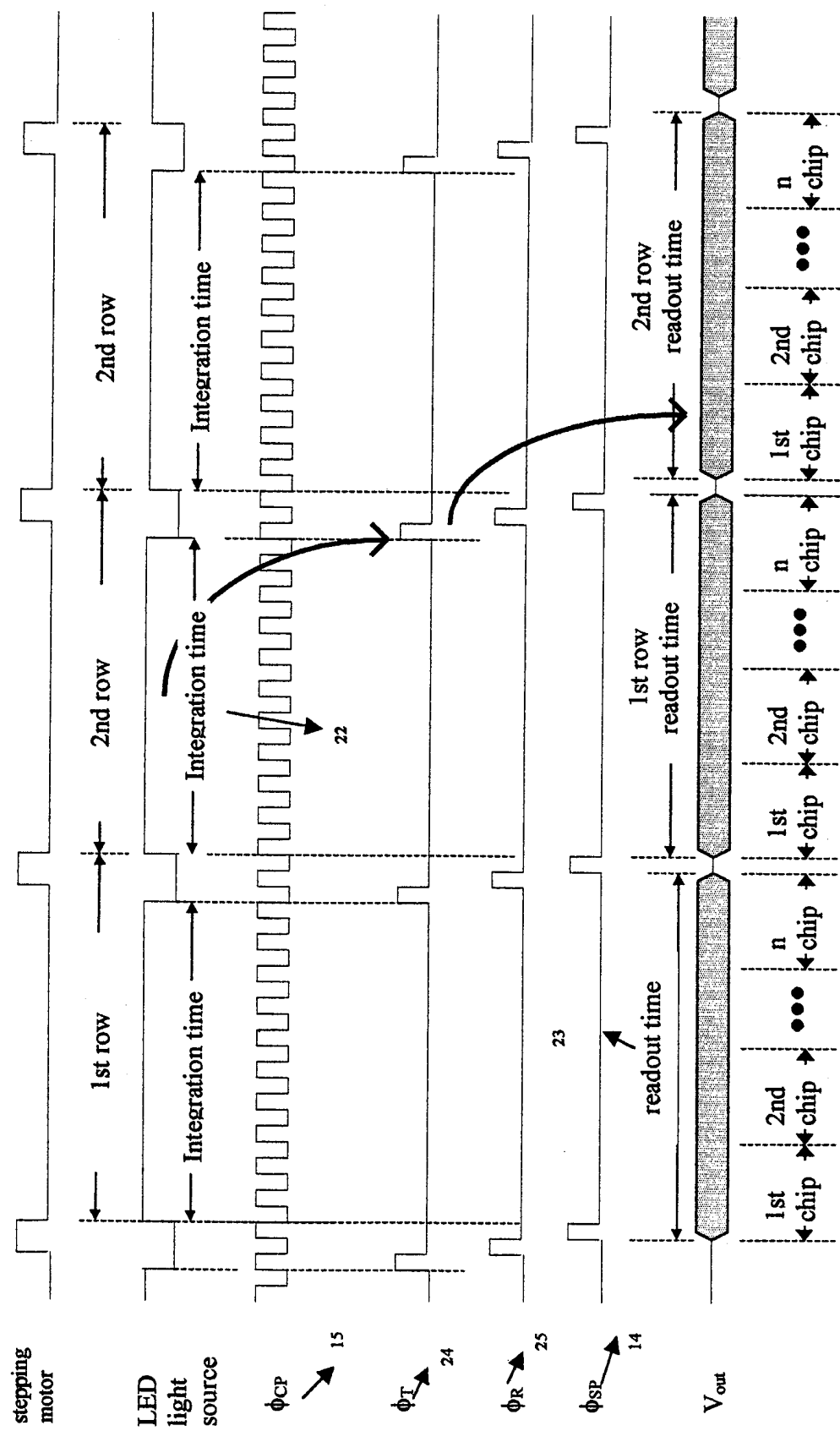


Figure 9.

											1st row
											2nd row
											3rd row
											4th row

Figure 10(a)

100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	1st row
100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	2nd row
100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	3rd row
100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	4th row

Figure 10(b)

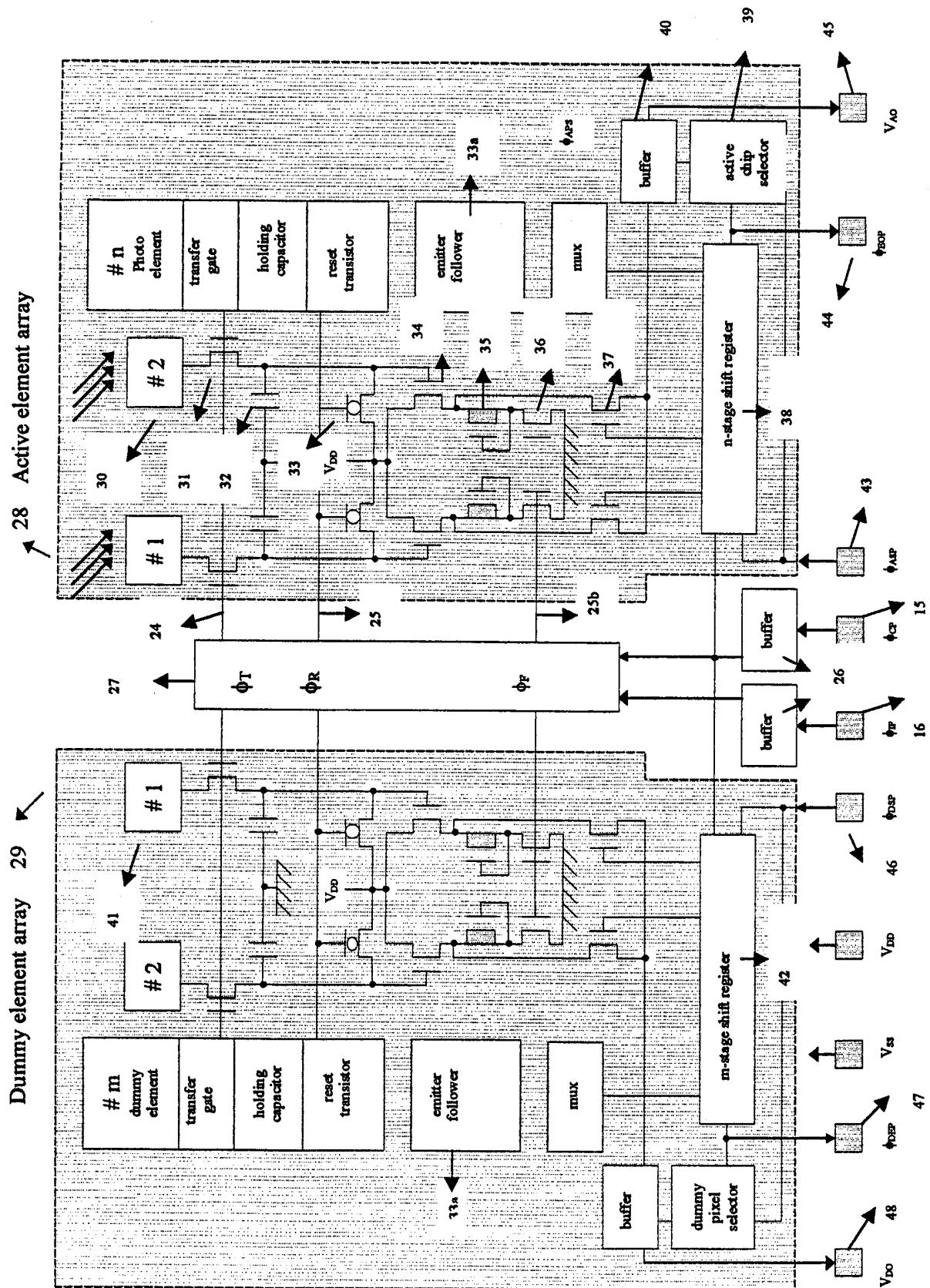


Figure 11

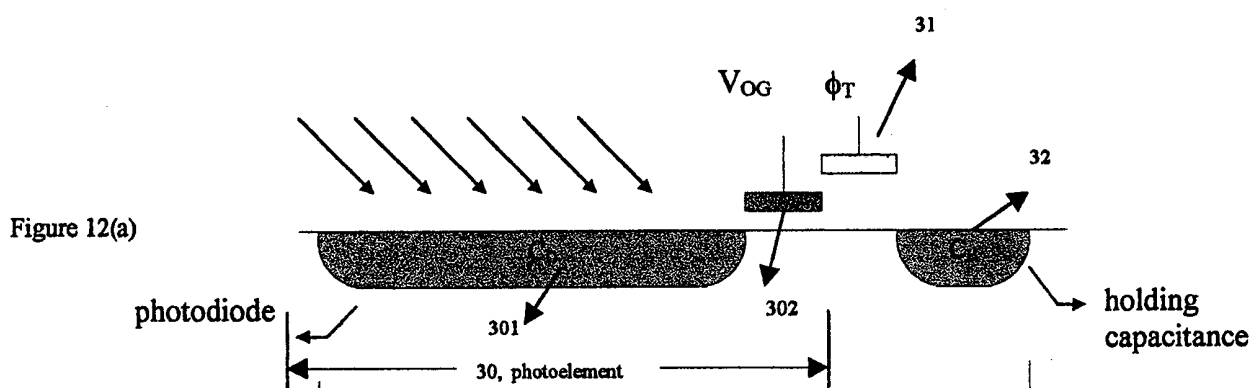


Figure 12(b)

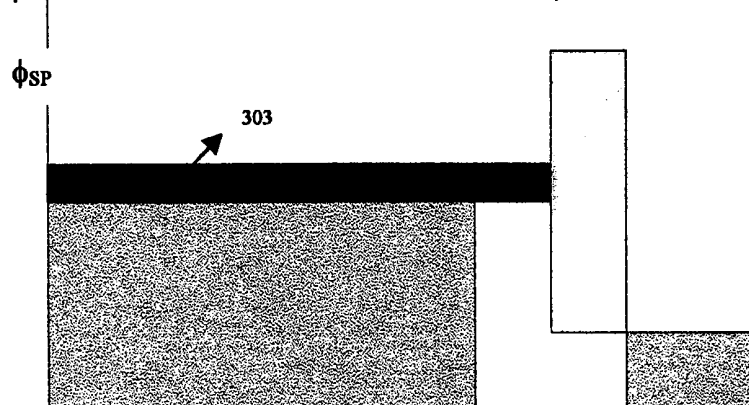


Figure 12(c)

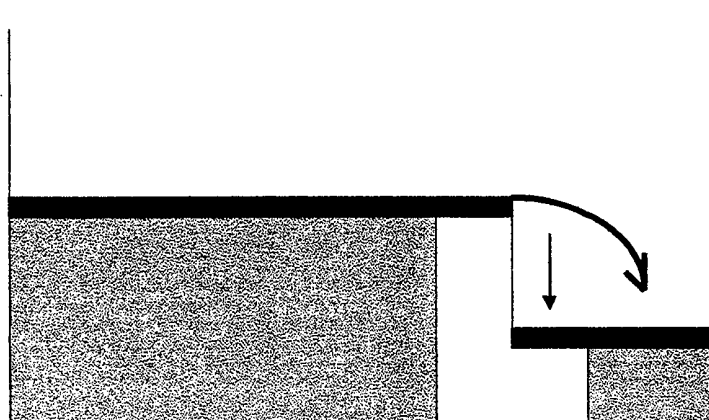
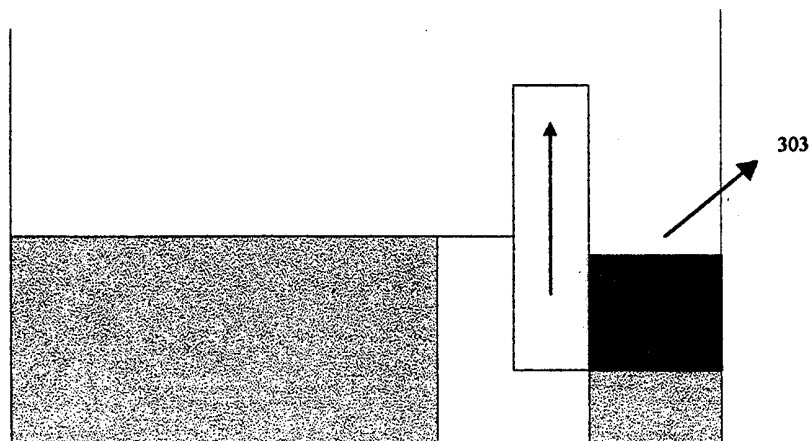


Figure 12(d)



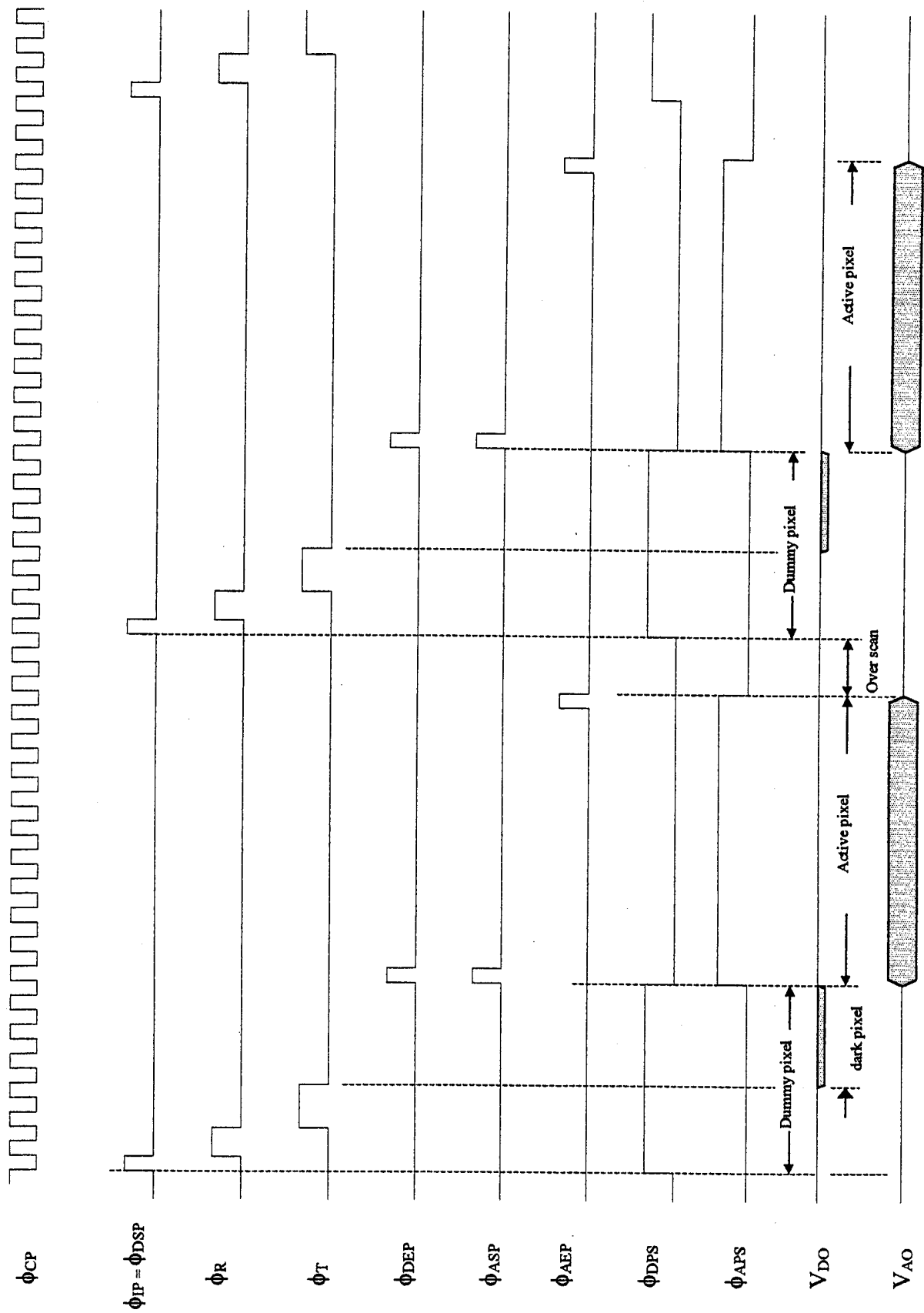


Figure 13

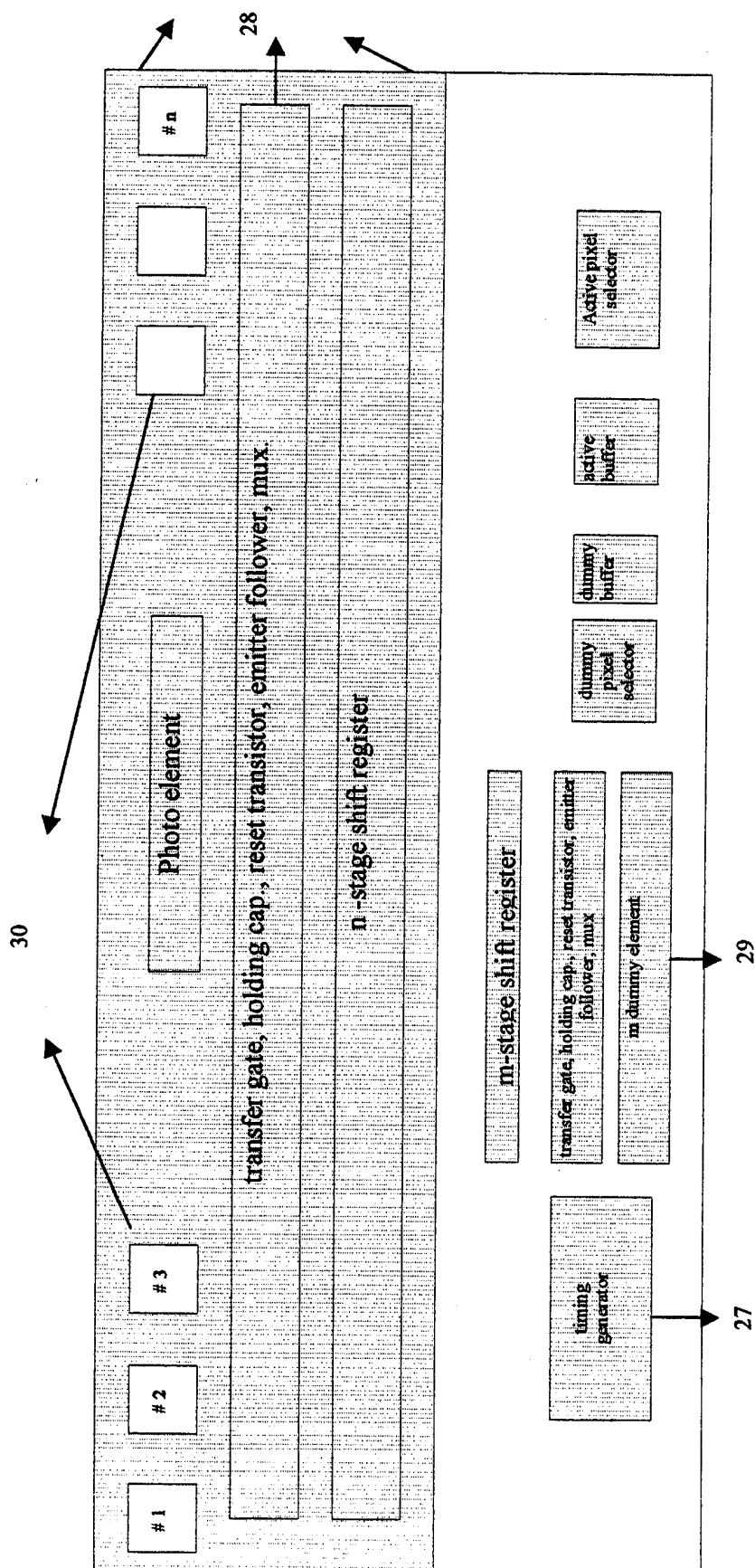


Figure 14. Chip layout

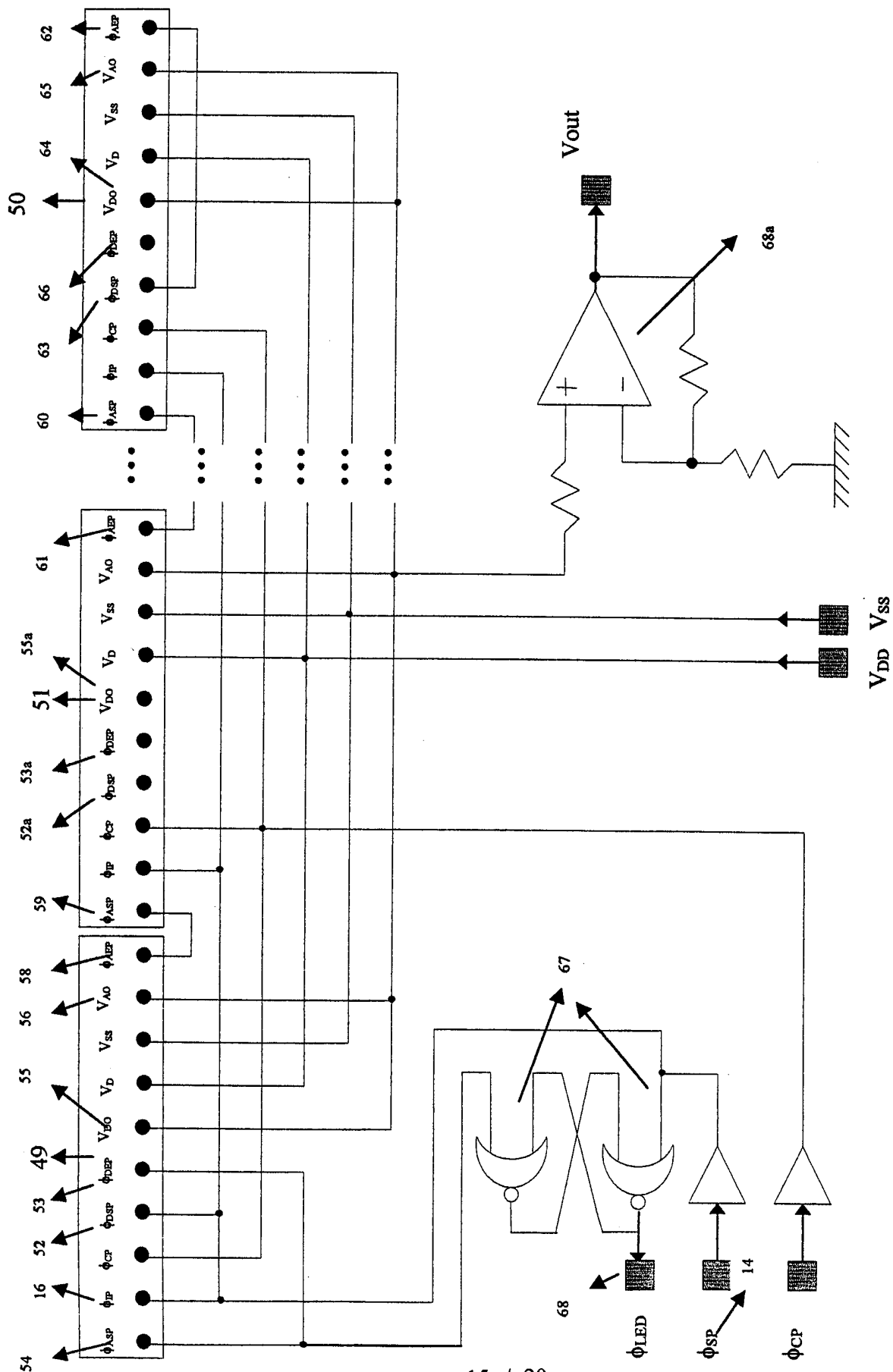


Figure 15

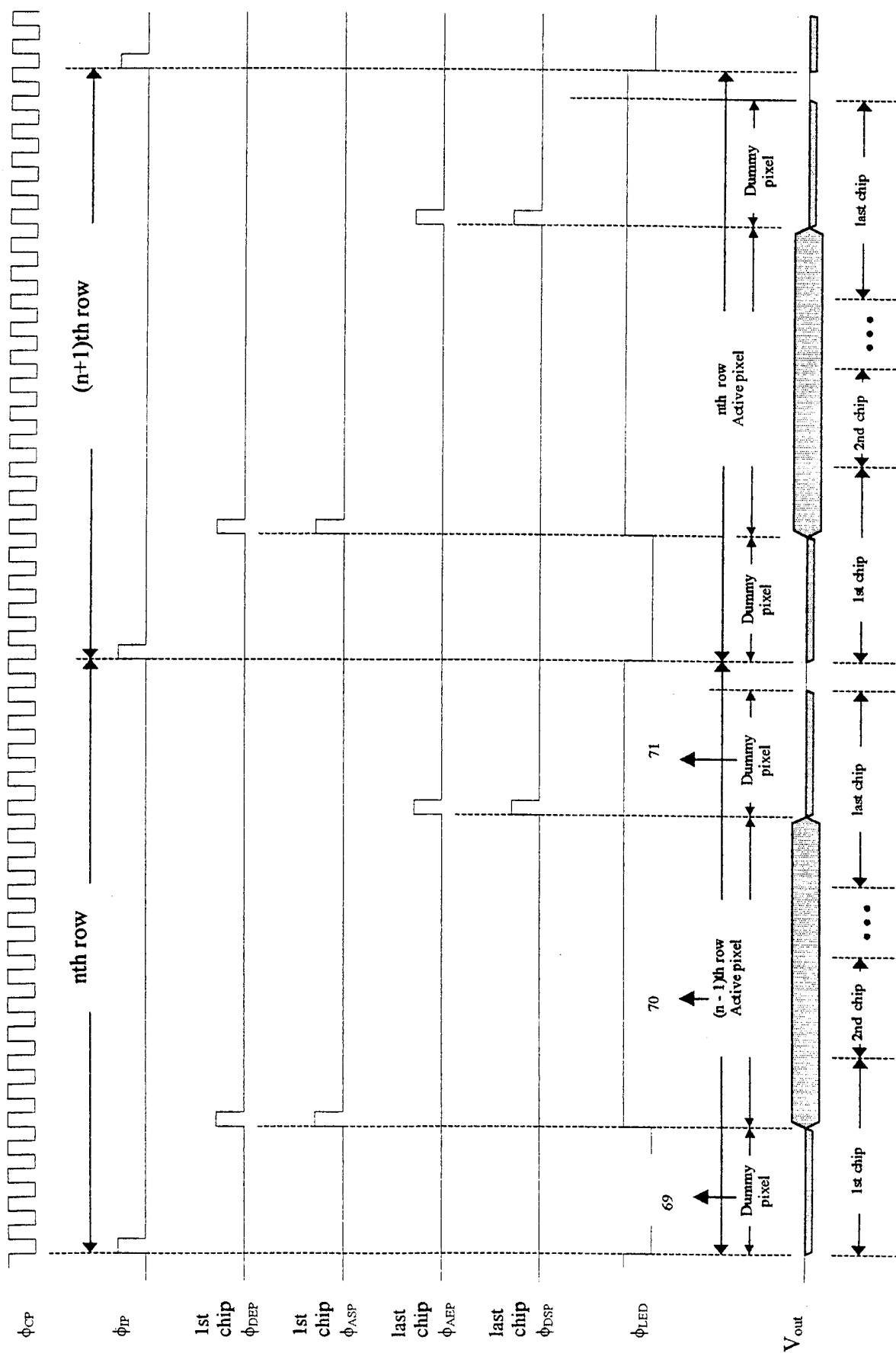


Figure 16

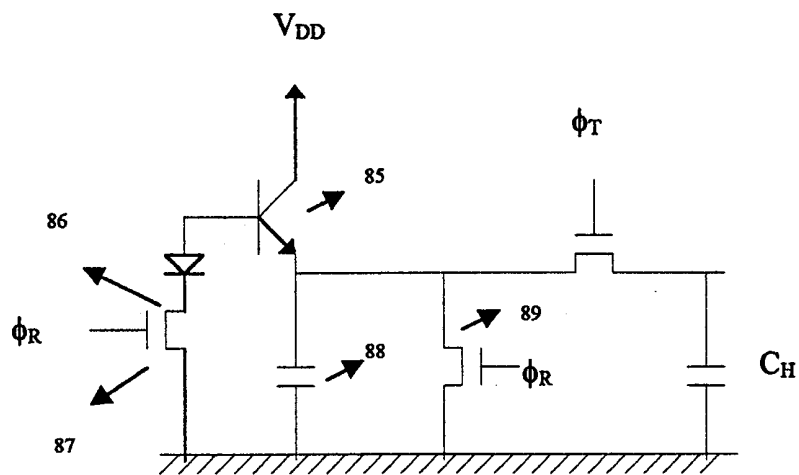


Figure 17.

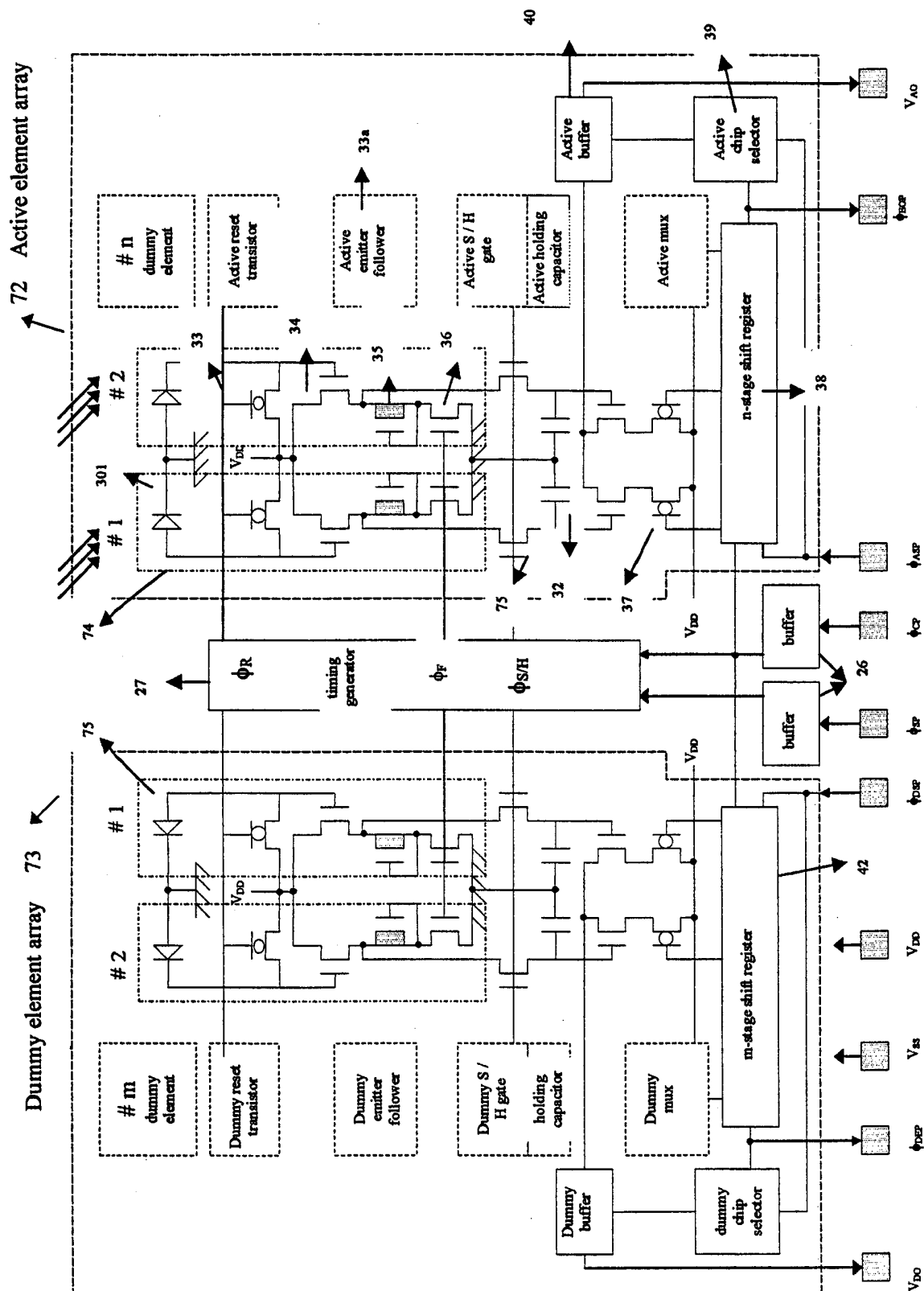


Figure 18

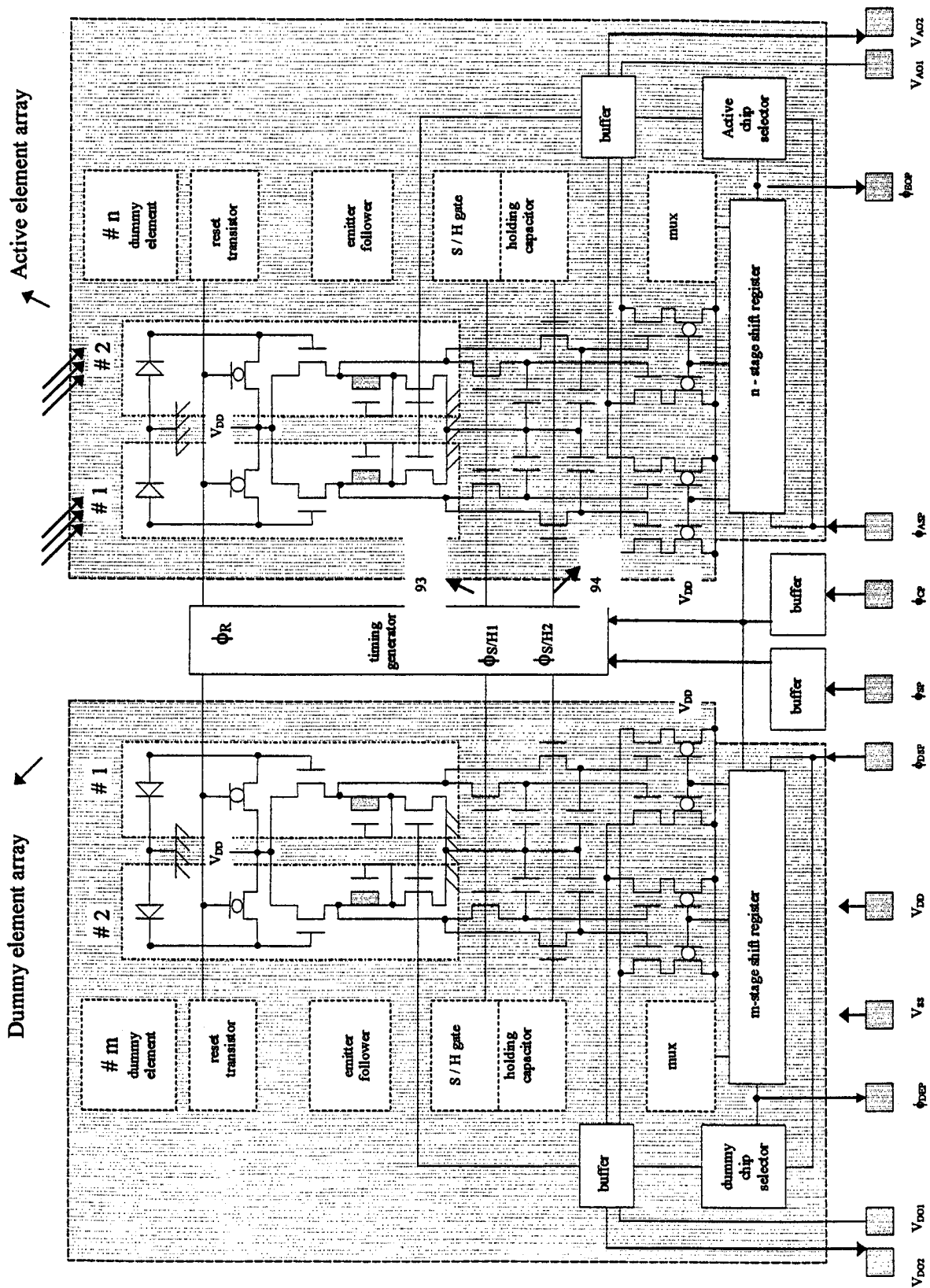


Figure 19

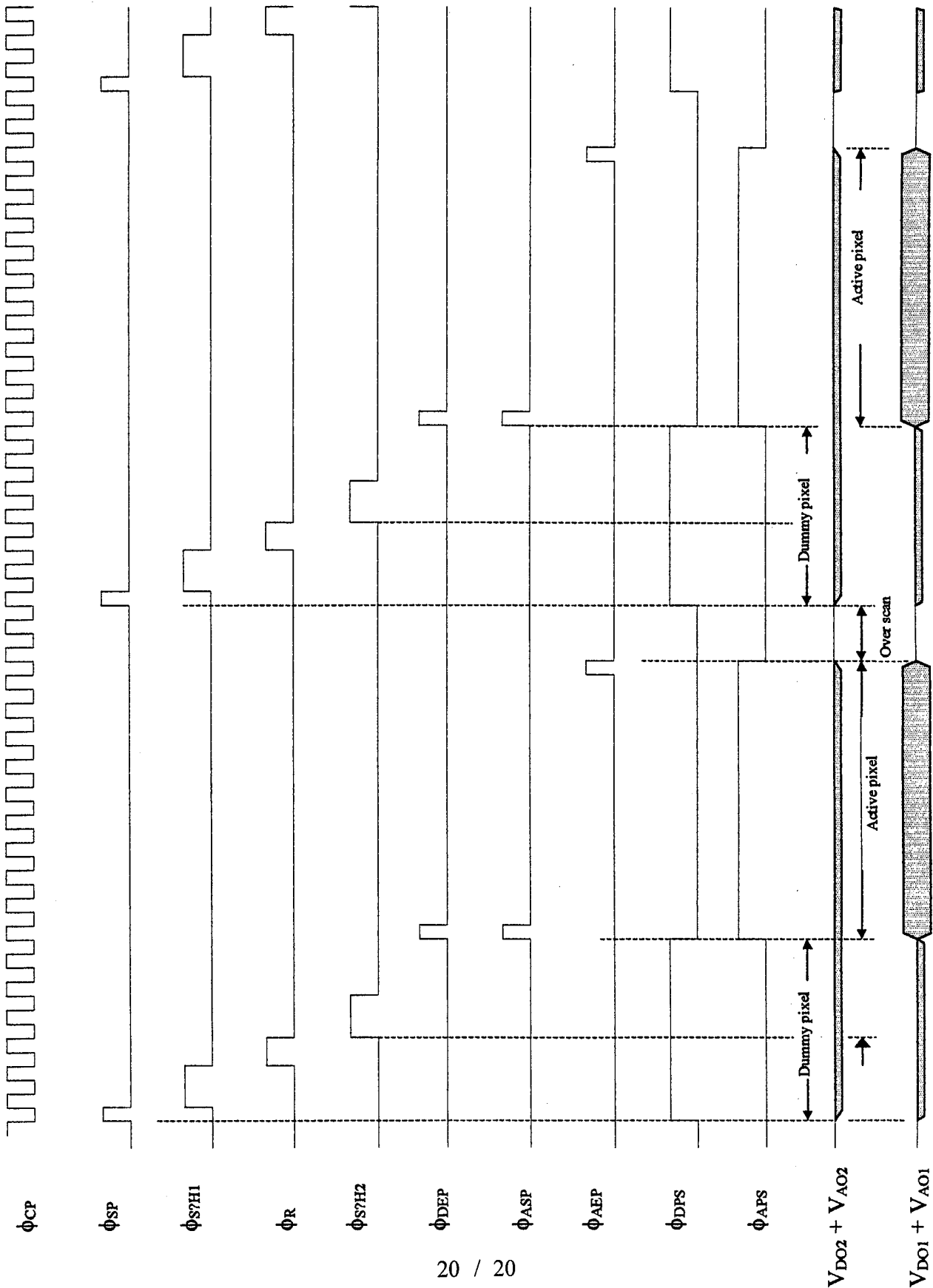


Figure 20

INTERNATIONAL SEARCH REPORT

Inter. onal Application No

PCT/US 99/15102

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H04N3/15

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 724 094 A (TSENG HSIN-FU ET AL) 3 March 1998 (1998-03-03) cited in the application column 3, line 41 -column 4, line 21 ---	1,5
Y	US 5 650 864 A (TSENG HSIN-FU ET AL) 22 July 1997 (1997-07-22) column 8, line 47 - line 52 column 5, line 31 - line 32 column 8, line 23 - line 38 ---	1,5
A	US 5 543 838 A (HOSIER PAUL A ET AL) 6 August 1996 (1996-08-06) column 2, line 15 - line 24 column 3, line 24 - line 34 column 3, line 57 -column 4, line 6 --- -/--	1

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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 "E" earlier document but published on or after the international filing date
 "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
 "O" document referring to an oral disclosure, use, exhibition or other means
 "P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
 "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
 "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
 "&" document member of the same patent family

Date of the actual completion of the international search

5 October 1999

Date of mailing of the international search report

22/12/1999

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Authorized officer

Bequet, T

INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 99/15102

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 455 311 A (CANON KK) 6 November 1991 (1991-11-06) column 21, line 34 - line 40 -----	1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US 99/15102

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