Title: ULTRA-THIN SMART CARD MODULES WITH CHIP BUMPS DISPOSED IN SUBSTRATE VIA HOLES AND METHODS OF FABRICATING THE SAME

Abstract: Disclosed are ultra-thin smart card modules (300, 400, 500A, 500B, 500C, 600) that can achieve a package thickness of less than 500 micrometres. Such a smart card module (300, 400, 500A, 500B, 500C, 600) comprises a substrate (310, 410, 510, 610) having a first conductive pattern (320, 420, 520, 620) on a first face, a second face that is opposite the first face, and a plurality of via holes; at least a chip (330, 430, 530, 530A, 530B, 630) having a first plurality of conductive bumps (350, 450, 550, 650) formed on a first major surface of the chip (330, 430, 530, 530A, 530B, 630), the chip (330, 430, 530, 530A, 530B, 630) being arranged so that the first plurality of conductive bumps (350, 450, 550, 650) are disposed in the plurality of via holes and electrically connected to the first conductive pattern (320, 420, 520, 620); an encapsulant (340, 440, 540, 640) disposed to encapsulate the chip (330, 430, 530, 530A, 530B, 630); and an underfill material (360, 460, 560, 660) disposed at least in a space between the chip (330, 430, 530, 530A, 530B, 630) and the second face of the substrate (310, 410, 510, 610). The first plurality of conductive bumps (350, 450, 550, 650) may be bonded with the plurality of via holes through the underfill material (360, 560) or alternatively may be seated on a plurality of conductive coatings (470, 670) provided in the plurality of via holes and electrically connected to the first conductive pattern (420, 620). The substrate (510, 610) may include a second conductive pattern (522, 522A, 522B, 622) on the second face, in which case the chip (530, 530A, 530B, 630) further includes a second plurality of conductive bumps (552, 652) formed on.
the first major surface and disposed on the second conductive pattern (522, 522A, 522B, 622) and electrically connected thereto. During the method of manufacturing the smart card module (300, 400, 500A, 500B, 500C, 600), the underfill material (360, 460, 560, 660) is provided on the substrate (310, 410, 510, 610) before chip (330, 430, 530, 530A, 530B, 630) placement and cured after arranging the chip (330, 430, 530, 530A, 530B, 630) so that the first plurality of conductive bumps (350, 450, 550, 650) are disposed in the via holes.
ULTRA-THIN SMART CARD MODULES WITH CHIP BUMPS DISPOSED IN SUBSTRATE VIA HOLES AND METHODS OF FABRICATING THE SAME

Background

Field of Invention

Embodiments of the invention relate to ultra-thin smart card modules and methods of fabricating such ultra-thin smart card modules.

Description of Related Art

Smart cards, which contain a chip module mounted or inserted into a card carrier body, are used in a variety of applications, e.g. telecommunications, payment cards, etc. Due to the universal demand for smart cards, there have been numerous chip module arrangements and methods of production which attempt to increase reliability and form factor of the chip module.

Figure 1 is a cross-sectional view of a chip module 100 which comprises a substrate 110, a conductor layer 120 of copper, gold and nickel applied to a first side of the substrate, a chip 130 arranged on a second opposed side of the substrate, gold wire bonds 150 connecting the chip 130 to the conductor layer 120, and a mold cap 140 encapsulating the wire-bonded chip 130. The wire bonds 150 are connected from the rear side of a bonding hole on the substrate 110 to the conductive pads of the chip 130. The conductor layer 120 is to provide a contact surface to a desired application, e.g. phone or reader terminal. As breakage of the wire bonds 150 is the most common cause of package failure, there is a lower limit to the length of the wire bonds 150 in order to prevent breakage. It thus follows that there is a lower limit to the thickness of such packages.
Figure 2 is a cross-sectional view of a chip module 200 which comprises a PET substrate 210, conductor layers 220 of gold, nickel and copper applied to both sides of the substrate 210, a chip 230 arranged on one side of the substrate 210, and conductive bumps 250 of the chip 230 seated on one of the two conductor layers 220. The conductor layer 220 which is remote from the bumps 250 is to provide a contact surface to a desired application, e.g. phone or reader terminal.


Accordingly, an improved smart card module and method of producing the same that address the above and other problems are highly desirable.

Summary

Embodiments of the invention relate to ultra-thin smart card modules that can achieve a module thickness of less than 500 microns.

According to one aspect of the invention, a smart card module comprises a substrate having a first conductive pattern on a first face, a second face that is opposite the first face, and a plurality of via holes; at least a chip having a first plurality of conductive bumps formed on a first major surface of the chip, the chip being arranged so that the first plurality of conductive bumps are disposed in the plurality of via holes and electrically connected to the first conductive pattern; an encapsulant disposed to encapsulate the chip; and an underfill material disposed at least in a space between the chip and the second face of the substrate.
According to another aspect of the invention, a method of fabricating a smart card module, comprises: providing at least a chip which is attached with a first plurality of conductive bumps; providing a substrate being perforated with via holes and having a first conductive pattern applied on a first face of the substrate; providing an underfill material on the substrate; arranging the chip on the substrate so that the first plurality of conductive bumps are disposed in the via holes; curing the underfill material; and encapsulating the chip.

**Brief Description of the Drawings**

Embodiments of the invention are disclosed hereinafter with reference to the drawings, in which:

- Figures 1 and 2 illustrate existing chip modules;
- Figure 3 shows a schematic cross-sectional illustration of a smart card module according to one embodiment of the invention;
- Figure 4 shows a schematic cross-sectional illustration of a smart card module according to another embodiment of the invention;
- Figure 5A shows a schematic cross-sectional illustration of a smart card module according to another embodiment of the invention;
- Figure 5B shows a schematic cross-sectional illustration of a dual interface smart card module according to another embodiment of the invention;
- Figure 5C shows a schematic cross-sectional illustration of a multi-chip smart card module according to another embodiment of the invention;
- Figure 6 shows a schematic cross-sectional illustration of a smart card module according to another embodiment of the invention;
Figure 7 illustrates a method of fabricating a smart card module of Figure 3; and

Figure 8 illustrates a method of fabricating a smart card module of Figure 4.

5 Detailed Description

In the following description, numerous specific details are set forth in order to provide a thorough understanding of various illustrative embodiments of the invention. It will be understood, however, to one skilled in the art, that embodiments of the invention may be practiced without some or all of these specific details. In other instances, well known process operations have not been described in detail in order not to unnecessarily obscure pertinent aspects of embodiments being described.

The present invention provides ultra-thin smart card modules which are configured for contact, contactless, dual interface and/or multi-chips smart card applications. The module package structures and methods for producing the same will be described in the following paragraphs.

Figure 3 shows a schematic cross-sectional illustration of a smart card module 300 according to one embodiment of the invention. The smart card module 300 comprises a substrate 310 having a first conductive pattern 320 on a first face, a second face that is opposite the first face, and a plurality of via holes. The substrate 310 may be provided as a flexible substrate so that bending loads on the smart card containing the module are absorbed in particular by non-encapsulated edge regions of the module. The substrate 310 may include glass epoxy, polyimide, polyethylene naphthalate (PEN), polyethylene terephthalate (PET) or other suitable materials. The first conductive pattern 320 is to provide a contact surface which is to be interfaced or
electrically connected with a desired application, e.g. handphone. In certain embodiments, the first conductive pattern 320 includes copper and nickel, and is free of gold. In certain other embodiments, the first conductive pattern 320 includes copper, nickel and gold. The substrate 310 is perforated with via holes which extend from the first face to the second face of the substrate 310.

The smart card module 300 of Figure 3 further comprises a chip 330 having a first plurality of conductive bumps 350 formed on a first major surface of the chip 330. The chip 330 is being arranged so that the first plurality of conductive bumps 350 are disposed in the plurality of via holes and electrically connected to the first conductive pattern 320. In one embodiment, the chip 330 may be provided as a flip chip having the first plurality of conductive bumps 350 formed on an active area of the chip 330. The chip 330 is mounted on the second face of the substrate 310 such that the conductive bumps 350 are seated in the via holes and on the first conductive pattern 320.

The smart card module 300 of Figure 3 further comprises an encapsulant 340 disposed to fully encapsulate the chip 330 to protect the chip 330 from environment and mechanical stresses. The encapsulant 340 may be provided as a mold compound, thermal or ultraviolet (UV) cured resin or other suitable materials. An underfill material 360 is disposed at least in a space between the chip 330 and the second face of the substrate 310 to reduce stress due to mismatch of the coefficient of thermal expansion of the chip 330 and the substrate 310. In certain embodiments, the underfill material 360 may fill the via holes and act as an adhesive to bond the first plurality of conductive bumps 350 to the substrate 310.

Figure 4 shows a schematic cross-sectional illustration of a smart card module 400 according to another embodiment of the invention. As there are similarities in
the smart card modules of Figure 4 and Figure 3, only the differences will be described. In the embodiment of Figure 4, the via holes are provided with thin conductive coatings 470 on the walls of the via holes. The conductive coatings 470 extend from a first end of the via holes to a second end which is distal to the first end.

Conductive coatings 470 disposed at the first end of the via holes are electrically connected to the first conductive pattern 420. Conductive coatings 470 disposed at the second end of the via holes are electrically connected to the first plurality of conductive bumps 450 of the chip 430, which are seated thereon. Accordingly, the first plurality of conductive bumps 450 of the chip 430 are electrically connected to the first conductive pattern 420 through the conductive coatings 470. In this embodiment, an underfill material 460 is disposed in a space between the chip 430 and the second face of the substrate 410. The via holes may be substantially free of the underfill material 460.

Figure 5A shows a schematic cross-sectional illustration of a smart card module 500A according to another embodiment of the invention. As there are similarities in the smart card modules of Figure 5A and Figure 3, only the differences will be described. In Figure 5A, the substrate 510 includes a first conductive pattern 520, and further includes a second conductive pattern 522 which is provided on the second face of the substrate 510. The chip 530 is provided with a first plurality of conductive bumps 550 which are electrically connected to the first conductive 520 pattern, and a second plurality of conductive bumps 552 which are electrically connected to the second conductive pattern 522. The first plurality of conductive bumps 550 are disposed in the via holes. Particularly, the first plurality of conductive bumps 550 are seated on the first conductive pattern 520. The second plurality of conductive bumps 552 are seated on the second conductive pattern 522. An
encapsulant 540 is disposed to fully encapsulate the chip 530 and the second conductive pattern 522. An underfill material 560 is disposed in a space between the chip 530 and the second face of the substrate 510 and in a space between the chip 530 and the second conductive pattern 522. The via holes may also be filled with the underfill material 560.

Figure 5B shows a schematic cross-sectional illustration of a smart card module 500B according to another embodiment of the invention. As there are similarities in the smart card modules of Figure 5B and Figure 5A, only the differences will be described. In the embodiment of Figure 5B, the encapsulant 540B is disposed to fully encapsulate the chip 530 and partially encapsulate the second conductive pattern 522. The embodiment of Figure 5B may be used in a dual interface smartcard where the first conductive pattern 520 is to be electrically connected to a contact interface whereas the second conductive pattern 522 is an antenna pad to be electrically connected to a radio frequency circuit external of the second conductive pattern 522. In an alternative embodiment, the second conductive pattern 522 may be disposed with a radio frequency circuit within for implementing an antenna device.

Figure 5C shows a schematic cross-sectional illustration of a smart card module 500C according to another embodiment of the invention. As there are similarities in the smart card modules of Figure 5C and Figure 5A, only the differences will be described. The smart card module of Figure 5C includes a plurality of chips 530A, 530B which are electrically connected to a first conductive pattern 520 and a plurality of second conductive patterns 522A, 522B. An encapsulant 540 is disposed to fully encapsulate the chips 530A, 530B and the plurality of second conductive patterns 522A, 522B.
Figure 6 shows a schematic cross-sectional illustration of a smart card module 600 according to another embodiment of the invention. As there are similarities in the smart card modules of Figure 6 and Figure 5, only the differences will be described. In the embodiment of Figure 6, the via holes are provided with thin conductive coatings 670 on the walls of the via holes. The conductive coatings 670 extend from a first end of the via holes to a second end which is distal to the first end. Conductive coatings 670 disposed at the first end of the via holes are electrically connected to the first conductive pattern 620. Conductive coatings 670 disposed at the second end of the via holes are electrically connected to the first plurality of conductive bumps 650 of the chip 630, which are seated thereon. Accordingly, the first plurality of conductive bumps 650 of the chip 630 are electrically connected to the first conductive pattern 620 through the conductive coatings 670. The second plurality of conductive bumps 652 are seated on the second conductive pattern 622 to be electrically connected thereto.

In the embodiment of Figures 5A to 5C and 6, the first and the second conductive patterns may or may not be electrically connected to each other depending on product requirements. Particularly, the first conductive pattern may be connected to a contact interface for smart card applications while the second conductive pattern may be connected to a contactless interface, e.g. radio frequency circuit (not shown) for smart card applications. Routing connections from the conductive patterns to the contact or contactless interface are known in the art and will not be described here.

Figure 7 illustrates a method 700 of fabricating a smart card module such as the module of Figure 3. The method includes providing a semiconductor chip or die which is attached with a first plurality of conductive bumps (block 702). The method
also includes providing a substrate that is perforated with via holes and having a first conductive pattern applied on a first face of the substrate (block 704). Via holes may be formed in the substrate by suitable methods, e.g. punching or laser drilling. The via holes are suitably positioned to complement the arrangement of the first plurality of conductive bumps of the chip. The first conductive pattern may be applied to the substrate by a photo-etching process on a copper layer which is laminated onto the substrate. After the photo-etching process, the substrate undergoes a plating process to plate nickel onto the etched copper layer to provide the first conductive pattern.

An underfill material or adhesive is dispensed onto the substrate (block 706). The underfill material may be a conductive or non-conductive paste. Thereafter, the chip is arranged on the substrate so that the first plurality of conductive bumps are disposed in via holes (block 708). More particularly, the first plurality of conductive bumps are seated on the first conductive pattern. The assembly obtained at this stage is then subject to thermal compression (block 710). The thermal compression process cures the underfill material to bond the first plurality of conductive bumps to the substrate and to collapse the first plurality conductive bumps within the via holes. Thereafter, the chip is encapsulated (block 712). This can be done by providing an encapsulant over the chip and thereafter curing the encapsulant.

Figure 8 illustrates a method of fabricating a smart card module such as the module of Figure 4. The method includes providing a semiconductor chip or die which is attached with conductive bumps (block 802). The method also includes providing a substrate that is perforated with via holes, the substrate having a first conductive pattern applied on a first face of the substrate, and having conductive coatings provided on walls of the via holes (block 804). Via holes may be formed in
the substrate by suitable methods, e.g. punching or laser drilling. The via holes are suitably positioned to complement the arrangement of conductive bumps of the chip. The first conductive pattern may be applied to the substrate by a photo-etching process on a copper layer which is laminated onto the substrate. After the photo-etching process, the substrate undergoes a plating process to plate nickel onto the etched copper layer to provide the first conductive pattern.

An underfill material or adhesive is dispensed onto the substrate (block 806). The underfill material may be a conductive or non-conductive paste. The chip is arranged on the substrate so that the first plurality of conductive bumps are disposed in the via holes (block 808). More particularly, the conductive bumps are seated on the conductive coatings of the via holes. The assembly obtained at this stage is then subject to thermal compression (block 810). The thermal compression process cures the underfill material to bond the conductive bumps to the substrate and to slightly collapse the conductive bumps onto the conductive coatings. Thereafter, the chip is encapsulated (block 812). This can be done by providing an encapsulant over the chip and thereafter curing the encapsulant.

The above-described methods of Figures 7 and 8 may be applied to fabricating a smart card module of any of Figures 5A to 5C with the following modifications. In blocks 702 and 802, the semiconductor chip is provided with a first plurality of conductive bumps having a first height and a second plurality of conductive bumps having a second height which is different from the first height. In blocks 704 and 804, the substrate is further provided with a second conductive pattern on a second face of the substrate, which is opposite to the first face of the substrate. In blocks 708 and 708, the chip is arranged on the substrate so that the first plurality of conductive bumps are disposed in the via holes and the second
plurality of conductive bumps are disposed or seated on the second conductive pattern. In blocks 712 and 812, the chip and the second conductive pattern are encapsulated.

Embodiments of the invention are advantageous in achieving an ultra-thin chip module thickness of 200 microns to less than 500 microns.

Other embodiments will be apparent to those skilled in the art from consideration of the specification and practice of the invention. Furthermore, certain terminology has been used for the purposes of descriptive clarity, and not to limit the disclosed embodiments of the invention. The embodiments and features described above should be considered exemplary, with the invention being defined by the appended claims.
What is claimed is:

1. A smart card module comprising:
   a substrate having a first conductive pattern on a first face, a second face that is opposite the first face, and a plurality of via holes;
   at least a chip having a first plurality of conductive bumps formed on a first major surface of the chip, the chip being arranged so that the first plurality of conductive bumps are disposed in the plurality of via holes and electrically connected to the first conductive pattern;
   an encapsulant disposed to encapsulate the chip; and
   an underfill material disposed at least in a space between the chip and the second face of the substrate.
2. The smart card module of claim 1, wherein the underfill material is disposed in the plurality of via holes and bonded with the first plurality of conductive bumps.
3. The smart card module of claim 1, wherein the first conductive pattern is free of gold.
4. The smart card module of claim 1, wherein a thickness of the chip module is between 200 microns to less than 500 microns.
5. The smart card module of any of the claim 1, wherein the first plurality of conductive bumps are seated on the first conductive pattern.
6. The smart card module of any of claim 1, wherein the first plurality of conductive bumps are seated on a plurality of conductive coatings provided in the plurality of via holes, wherein the plurality of conductive coatings are electrically connected to the first conductive pattern.
7. The smart card module of any of claims 1 to 6, wherein the substrate further includes a second conductive pattern on the second face of the substrate, wherein the chip further includes a second plurality of conductive bumps formed on the first major surface of the chip, the chip being arranged so that the second plurality of conductive bumps are disposed on the second conductive pattern and electrically connected thereto.

8. The smart card module of claim 7, wherein the encapsulant is further disposed to partially encapsulate the second conductive pattern.

9. The smart card module of claim 8, wherein the first and the second conductive patterns are electrically unconnected from each other, and wherein the second conductive pattern is electrically connected to a radio frequency circuit which is disposed within or external of the second conductive pattern.

10. A method of fabricating a smart card module, the method comprising:

   providing at least a chip which is attached with a first plurality of conductive bumps;
   providing a substrate being perforated with via holes and having a first conductive pattern applied on a first face of the substrate;
   providing an underfill material on the substrate;
   arranging the chip on the substrate so that the first plurality of conductive bumps are disposed in the via holes;
   curing the underfill material; and
   encapsulating the chip.

11. The method of claim 10, wherein arranging the chip on the substrate includes seating the first plurality of conductive bumps on the first conductive pattern.
12. The method of claim 10, wherein providing a substrate being perforated with via holes and having a first conductive pattern applied on a first face of the substrate includes providing the substrate with a plurality of conductive coatings in the plurality of via holes, wherein the plurality of conductive coatings are electrically connected to the first conductive pattern.

13. The method of claim 10 or 11, wherein providing a chip which is attached with a first plurality of conductive bumps includes providing the chip which is further attached with a second plurality of conductive bumps, wherein providing a substrate being perforated with via holes and having a first conductive pattern applied on a first face of the substrate includes providing the substrate further having a second conductive pattern applied on a second face of the substrate, wherein arranging the chip on the substrate so that the first plurality of conductive bumps are disposed in the via holes further includes arranging the chip on the substrate so that the second plurality of conductive bumps are disposed on the second conductive pattern.

14. The method of claim 13, wherein encapsulating the chip includes partially encapsulating the second conductive pattern.

15. The method of claim 14, further comprising: electrically connecting the first conductive pattern to a contact interface for smart card application; and electrically connecting the second conductive pattern to a radio frequency circuit which is disposed within or external of the second conductive pattern.
Figure 1
(Prior art)

Figure 2
(Prior art)
Provide a semiconductor chip which is attached with a first plurality of conductive bumps

Provide a substrate that is perforated with via holes and having a first conductive pattern applied on a first face of the substrate

Dispense an underfill material onto the substrate

Arrange chip on the substrate so that the first plurality of conductive bumps are disposed in via holes, i.e. seated on the first conductive pattern

Thermal compression

Encapsulate the chip

Figure 7
Provide a semiconductor chip which is attached with a first plurality of conductive bumps

Provide a substrate that is perforated with via holes, the substrate having a first conductive pattern applied on a first face of the substrate, and having conductive coatings provided on walls of the via holes

Dispense an underfill material onto the substrate

Arrange chip on the substrate so that the first plurality of conductive bumps are disposed in via holes, i.e. seated on the conductive coatings

Thermal compression

Encapsulate the chip

Figure 8
**INTERNATIONAL SEARCH REPORT**

**A. CLASSIFICATION OF SUBJECT MATTER**

INv. H01L21/60 H01L23/485 H01L23/498 H01L21/56

**ADD.**

According to International Patent Classification (IPC) and national classification.

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched.

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data, INSPEC, COMPENDEX

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

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Further documents are listed in the continuation of Box C.

**See patent family annex.**

**Date of the actual completion of the international search**

11 March 2014

**Date of filing of the international search report**

25/03/2014

**Name and mailing address of the ISA**

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Authorized officer

Maslankiewicz, Pawel
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This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.: because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.: because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.: because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

This International Searching Authority found multiple inventions in this international application, as follows:

      see additional sheet

1. ☑ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:  

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:  

Remark on Protest
☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
☒ No protest accompanied the payment of additional search fees.
This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-5, 10-12

See the sub-inventions listed under items 1.1-1.5 below

1.1. claims: 1, 2, 10

A method of fabricating a smart card module, the method comprising:
providing at least a chip which is attached with a first plurality of conductive bumps;
providing a substrate being perforated with via holes and having a first conductive pattern applied on a first face of the substrate;
providing an underfill material on the substrate;
arranging the chip on the substrate so that the first plurality of conductive bumps are disposed in the via holes;
curing the underfill material; and
encapsulating the chip, as well as a corresponding device, wherein the underfill material is disposed in the plurality of via holes and bonded with the first plurality of conductive bumps.

1.2. claim: 3

A smart card module comprising:
a substrate having a first conductive pattern on a first face, a second face that is opposite the first face, and a plurality of via holes;
at least a chip having a first plurality of conductive bumps formed on a first major surface of the chip, the chip being arranged so that the first plurality of conductive bumps are disposed in the plurality of via holes and electrically connected to the first conductive pattern;
an encapsulant disposed to encapsulate the chip; and
an underfill material disposed at least in a space between the chip and the second face of the substrate,
wherein the first conductive pattern is free of gold.

1.3. claim: 4

A smart card module comprising:
a substrate having a first conductive pattern on a first face, a second face that is opposite the first face, and a plurality of via holes;
at least a chip having a first plurality of conductive bumps formed on a first major surface of the chip, the chip being arranged so that the first plurality of conductive bumps are disposed in the plurality of via holes and electrically connected to the first conductive pattern;
an encapsulant disposed to encapsulate the chip; and
an underfill material disposed at least in a space between
the chip and the second face of the substrate, where the thickness of the chip module is between 200
microns to less than 500 microns

1.4. claims: 5, 11

A method of fabricating a smart card module, the method comprising:
providing at least a chip which is attached with a first plurality of conductive bumps;
providing a substrate being perforated with via holes and having a first conductive pattern applied on a first face of the substrate;
providing an underfill material on the substrate;
arranging the chip on the substrate so that the first plurality of conductive bumps are disposed in the via holes;
curing the underfill material; and
encapsulating the chip,
wherein arranging the chip on the substrate includes seating the first plurality of conductive bumps on the first conductive pattern, as well as a corresponding device

1.5. claim: 12

A method of fabricating a smart card module, the method comprising:
providing at least a chip which is attached with a first plurality of conductive bumps;
providing a substrate being perforated with via holes and having a first conductive pattern applied on a first face of the substrate;
providing an underfill material on the substrate;
arranging the chip on the substrate so that the first plurality of conductive bumps are disposed in the via holes;
curing the underfill material; and
encapsulating the chip,
wherein providing a substrate being perforated with via holes and having a first conductive pattern applied on a first face of the substrate includes providing the substrate with a plurality of conductive coatings in the plurality of via holes, wherein the plurality of conductive coatings are electrically connected to the first conductive pattern

2. claim: 6

A smart card module comprising:
a substrate having a first conductive pattern on a first face, a second face that is opposite the first face, and a plurality of via holes;
at least a chip having a first plurality of conductive bumps formed on a first major surface of the chip, the chip being arranged so that the first plurality of conductive bumps are disposed in the plurality of via holes and electrically
connected to the first conductive pattern; an encapsulant disposed to encapsulate the chip; and an underfill material disposed at least in a space between the chip and the second face of the substrate, wherein the first plurality of conductive bumps are seated on a plurality of via holes, wherein the plurality of conductive coatings are electrically connected to the first conductive pattern.

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3. claims: 7-9, 13-15

A method of fabricating a smart card module, the method comprising: providing at least a chip which is attached with a first plurality of conductive bumps; providing a substrate being perforated with via holes and having a first conductive pattern applied on a first face of the substrate; arranging the chip on the substrate so that the first plurality of conductive bumps are disposed in the via holes; curing the underfill material; and encapsulating the chip, wherein providing a chip which is attached with a first plurality of conductive bumps includes providing the chip further attached with a second plurality of conductive bumps, wherein providing a substrate being perforated with via holes and having a first conductive pattern applied on a first face of the substrate includes providing the substrate further having a second conductive pattern applied on a second face of the substrate, wherein arranging the chip on the substrate so that the first plurality of conductive bumps are disposed in the via holes further includes arranging the chip on the substrate so that the second plurality of conductive bumps are disposed on the second conductive pattern, as well as a corresponding device.

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