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(71) Applicant: **APPLE INC.** [US/US]; One Apple Park Way,
Cupertino, California 95014 (US).

(72) Inventors: **LI, Weiping**; One Apple Park Way, Cupertino,
California 95014 (US). **LAFLAQUIERE, Arnaud**; 7,
Ang Mo Kio Street 64, Singapore 569086 (SG). **FANG, Xi-**
aolong; One Apple Park Way, Cupertino, California 95014
(US).

(74) Agent: **KLIGLER, Daniel**; P. O. Box 57651, 61576 Tel
Aviv (IL).

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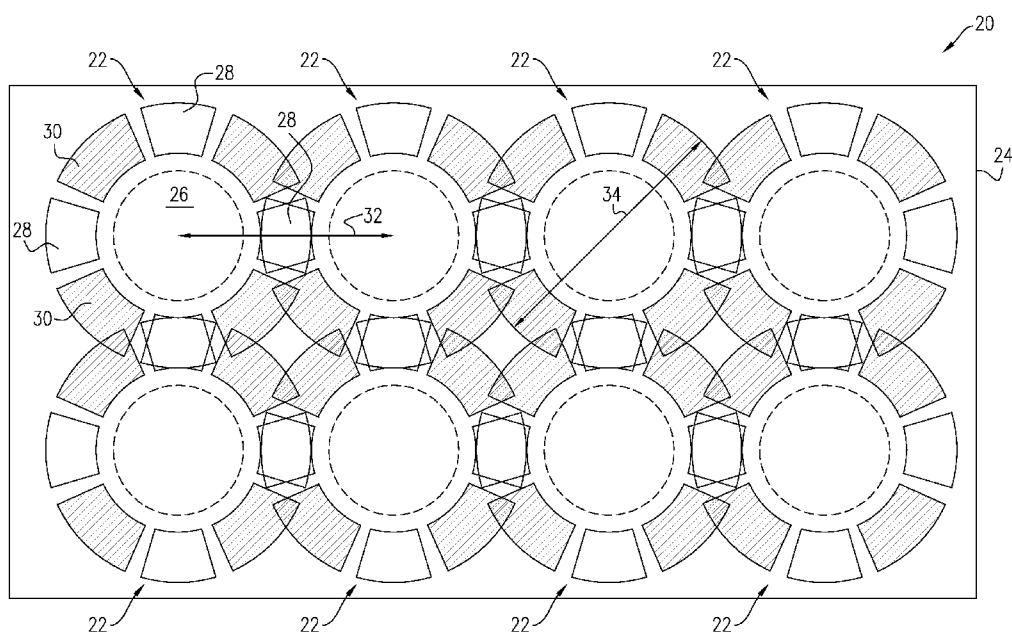


FIG. 1

(57) Abstract: An optoelectronic device (20, 120) includes a semiconductor substrate (24). A first set of thin-film layers is disposed on the substrate and defines a lower distributed Bragg-reflector (DBR) stack (42). A second set of thin-film layers (40, 46) is disposed over the lower DBR stack and defines an optical emission region (43), which is contained in a mesa defined by multiple trenches (28, 128), which are disposed around the optical emission region without fully surrounding the optical emission region. A third set of thin-film layers is disposed over the optical emission region and defines an upper DBR stack (44, 124). Electrodes (30, 130) are disposed around the mesa in gaps between the trenches and are configured to apply an excitation current to the optical emission region.

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VCSEL ARRAY WITH TIGHT PITCH AND HIGH EFFICIENCY**FIELD OF THE INVENTION**

The present invention relates generally to optoelectronic devices, and more particularly solid-state emitter arrays and methods for their manufacture.

BACKGROUND

In vertical-cavity surface-emitting layer (VCSEL) arrays that are known in the art, multiple VCSELs are formed on a common substrate. The optical emission region of each VCSEL (which typically comprises a quantum well structure) is contained in a mesa surrounded by a trench or multiple trenches. The optical aperture of the VCSEL is defined by an oxide confinement layer surrounding the optical emission region. A metal anode contact for each VCSEL is formed over the mesa, typically in the form of a ring, which surrounds the optical aperture of the VCSEL. A common cathode contact is formed on the opposite side of the substrate.

The concentric arrangement of the optical aperture, surrounded by the anode contact, which is surrounded in turn by the trenches, sets a lower limit on the pitch of the VCSEL array: The distance between adjacent VCSELs includes both the width of the trenches and the width of the metal anode contacts.

SUMMARY

Embodiments of the present invention that are described hereinbelow provide improved solid-state emitter arrays and methods for their manufacture.

There is therefore provided, in accordance with an embodiment of the invention, an optoelectronic device, including a semiconductor substrate. A first set of thin-film layers is disposed on the substrate and defines a lower distributed Bragg-reflector (DBR) stack. A second set of thin-film layers is disposed over the lower DBR stack and defines an optical emission region, which is contained in a mesa defined by multiple trenches, which are disposed around the optical emission region without fully surrounding the optical emission region. A third set of thin-film layers is disposed over the optical emission region and defines an upper DBR stack. Electrodes are disposed around the mesa in gaps between the trenches and are configured to apply an excitation current to the optical emission region.

In a disclosed embodiment, the device includes a transparent conductive layer in electrical contact with the electrodes and extending across the mesa over at least the second set of thin-film layers.

In some embodiments, the third set of thin-film layers includes dielectric layers. Typically, the electrodes include a metal, which is deposited in vias that extend through the third set of thin-film layers.

Additionally or alternatively, the third set of thin-film layers includes epitaxial semiconductor layers. In a disclosed embodiment, the electrodes are deposited over the third set of thin-film layers.

In some embodiments, the first, second and third sets of thin-film layers and the electrodes are disposed on an upper side of the semiconductor substrate, and the device includes a cathode layer on a lower side of the semiconductor substrate, opposite the upper side.

There is also provided, in accordance with an embodiment of the invention, an optoelectronic device, including a semiconductor substrate. A first set of thin-film layers is disposed on the substrate and defines a lower distributed Bragg-reflector (DBR) stack. A second set of thin-film layers is disposed over the lower DBR stack and defines a plurality of optical emission regions, contained in respective mesas defined by multiple trenches, which are disposed around each of the optical emission regions without fully surrounding the optical emission regions. A third set of thin-film layers is disposed over each of the optical emission regions and defines an upper DBR stack. Electrodes are disposed around each of the mesas in gaps between the trenches and are configured to apply an excitation current to each of the optical emission regions.

In a disclosed embodiment, at least one of the trenches is common to a pair of neighboring mesas. Additionally or alternatively, at least one of the electrodes is common to a pair of neighboring mesas.

In some embodiments, the first, second and third sets of thin-film layers and the electrodes are disposed on an upper side of the semiconductor substrate, and the device includes a cathode layer on a lower side of the semiconductor substrate, opposite the upper side, wherein the cathode layer is common to the plurality of the optical emission regions.

There is additionally provided, in accordance with an embodiment of the invention, a method for producing an optoelectronic device. The method includes depositing a first set of thin-film layers on a semiconductor substrate so as to define a lower distributed Bragg-reflector (DBR) stack. A second set of thin-film layers is deposited over the lower DBR stack so as to an optical emission region. Multiple trenches are formed around the optical emission region without fully surrounding the optical emission region, thereby defining a mesa containing the optical emission region. A third set of thin-film layers is deposited over the optical emission region so as to define an upper DBR stack. Electrodes are deposited around the mesa in gaps between the trenches.

Electrical contacts are coupled to the electrodes so as to apply an excitation current to the optical emission region.

The present invention will be more fully understood from the following detailed description of the embodiments thereof, taken together with the drawings in which:

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic frontal view of an optoelectronic device comprising an array of VCSELs, in accordance with an embodiment of the invention;

Figs. 2A and 2B are schematic frontal and sectional views, respectively, of a pair of VCSELs in an array, in accordance with an embodiment of the invention;

Figs. 3A and 3B are schematic frontal and sectional views, respectively, of a pair of VCSELs in an array, in accordance with an alternatively embodiment of the invention;

Figs. 4A-4G are schematic sectional views showing successive stages in the fabrication of an array of VCSELs, in accordance with an embodiment of the invention;

Figs. 5A and 5B are schematic frontal and sectional views, respectively, of a pair of VCSELs in an array, in accordance with another embodiment of the invention;

Figs. 6A and 6B are schematic frontal and sectional views, respectively, of a pair of VCSELs in an array, in accordance with a further alternative embodiment of the invention; and

Figs. 7A-7F are schematic sectional views showing successive stages in the fabrication of an array of VCSELs, in accordance with another embodiment of the invention.

DETAILED DESCRIPTION OF EMBODIMENTS

OVERVIEW

Embodiments of the present invention that are described herein provide a new design, in which the minimum pitch between emitters in the VCSEL array is significantly reduced by moving the metal contact ring completely out of the emitter mesa. The trenches defining the mesa are disposed around the optical emission region of the VCSEL without fully surrounding it. The electrodes (configured, for example, as metal anode contacts) are disposed around the mesa in the gaps between the trenches.

Using this design approach, the pitch of the VCSEL array can be reduced relative to devices that are known in the art, and the density of emitters on a chip can be increased. This innovation makes it possible to increase the overall radiation flux emitted from a chip of a given size, as well as generating patterns of finer resolution when the VCSEL beams are used to produce patterned

illumination. Although the figures show VCSELs with a certain number of trenches and electrodes arranged symmetrically in a ring around the mesa, the principles of the present invention may alternatively be implemented using larger or smaller numbers of trenches and electrodes, which may be of the same or different relative sizes, in both symmetrical and non-symmetrical arrangements.

The changes in VCSEL geometry and reduction in size of the electrodes associated with embodiments of the present invention tend to increase the electrical resistance of the VCSEL circuits, and thus could reduce the electrical efficiency of the VCSEL array. To counteract such effects, in some embodiments a transparent conductive layer, in electrical contact with the electrodes, extends across the mesa over the optical emission region. This layer, comprising indium tin oxide (ITO), for example, can be formed either above or below the metal layer of the electrodes. It is useful in reducing the device resistance and increasing the power conversion efficiency from electrical to optical power.

The principles of the present invention can be implemented in a variety of different device technologies. For example, the VCSELs in the array may have upper mirrors comprising a distributed Bragg reflector (DBR) made up of multiple dielectric layers, or made up of multiple epitaxial p-type layers. Furthermore, the principles of the present invention may be applied in arrays of VCSELs of other types, as well as in other sorts of solid-state emitter arrays, as will be apparent to those skilled in the art after reading the present description. All such alternative implementations are considered to be within the scope of the present invention.

Fig. 1 is a schematic frontal view of an optoelectronic device 20 comprising an array of VCSELs 22, in accordance with an embodiment of the invention. The structures shown in this overview figure and processes by which they can be produced are described in greater detail hereinbelow.

VCSELs 22 are formed on a semiconductor substrate 24, such as a GaAs wafer. Each VCSEL 22 emits optical radiation (typically in the near-infrared range) from an optical emission region through an aperture 26, which is defined by an oxide confinement layer within the mesa of the VCSEL. VCSELs 22 are separated from their neighbors, physically and electrically, by trenches 28 surrounding the mesas. Trenches 28 are disposed around the optical emission region of each VCSEL 22 without fully surrounding it. As a result, electrodes 30 can be disposed around the mesas in the gaps between trenches 28. These electrodes serve as anodes to apply excitation currents to the optical emission regions of the VCSELs. (The cathode, not shown in this figure, is on the lower side of substrate 24.)

The design shown in Fig. 1 is advantageous in that electrodes 30 are located outside the area of the VCSEL mesa, thus reducing an overall diameter 34 of each VCSEL relative to designs that are known in the art. Trenches 28 or electrodes 30 of neighboring VCSELs may be overlapped, meaning that a certain trench or electrode is common to each pair of neighboring VCSELs. This overlap enables the array of VCSELs 22 to be formed on substrate 24 with a pitch 32 that is substantially smaller than diameter 34. (Fig. 1 shown an array with overlapping trenches 28, but schemes that include overlapping electrodes are also shown in the figures that follow.)

In Fig. 1, as well as in the figures that follow, some of trenches 28 and electrodes 30 are shown schematically as having arcuate shapes that overlap certain trenches and electrodes of the neighboring VCSEL 22. This feature is shown simply for convenience of illustration. In practice, trenches 28 that overlap one another actually constitute a single trench, which is shared by the neighboring VCSELs. Two electrodes 30 that overlap may actually be formed as a single electrode, which is shared by the neighboring VCSELs; or they may alternatively be limited in size so that they do not overlap, in which case each electrode serves only its own VCSEL.

Although Fig. 1 shows a rectilinear array of VCSELs, with four trenches and four electrodes of equal sizes surrounding each VCSEL, in alternative embodiments (not shown in the figures) different numbers, sizes and arrangements of trenches may be used, along with electrodes of other sizes and shapes in the gaps between the trenches surrounding the mesas. Such arrangements can also support different array geometries of the VCSELs, for example hexagonal arrays.

VCSEL ARRAY WITH DIELECTRIC DBR

Figs. 2A and 2B are schematic frontal and sectional views, respectively, of a pair of VCSELs 22 in an array 36, in accordance with an embodiment of the invention. The sectional view in Fig. 2B is taken along the line marked "IIB-IIB" in Fig. 2A. The sectional views in Figs. 3B, 5B and 6B are defined by similar section lines in the corresponding frontal views. In Fig. 2A, VCSELs 22 are oriented so that electrodes 30 of the neighboring VCSELs overlap; whereas in Fig. 3A, the overlap is between trenches 28 (as in Fig. 1).

Array 36 is formed by thin-film layers deposited on the upper side of semiconductor substrate 24. (The terms "upper" and "lower" are used arbitrarily, for the sake of convenience, to indicate the order of layers in the views shown in the sectional drawings.) A first set of thin-film layers on substrate 24, typically n-type epitaxial layers having different, respective indices of refraction, define a lower distributed Bragg-reflector (DBR) stack 42. A second set of thin-film

layers, deposited over lower DBR stack 42, includes a multi-quantum well (MQW) layer 40 and an overlying oxide layer 46. Trenches 28 are etched through MQW layer 40 to define the mesa of each VCSEL 22 (as shown explicitly in Fig. 3B). Oxide layer 46 is etched in each mesa to create apertures 26, which in turn define an optical emission region 43 within each mesa.

5 A third set of thin-film layers are formed over MQW layer 40 (and thus over optical emission region 43) to define an upper DBR stack 44. In the present embodiment, upper DBR stack 44 comprises alternating dielectric layers having different, respective indices of refraction. Vias are etched through upper DBR 44 and are then filled with metal to create electrodes 30 in the gaps between trenches 28.

10 In the pictured embodiment, a transparent conductive layer 50 extends across the mesas of VCSELs 22, above MQW layer 40 and oxide layer 46, and makes electrical contact with electrodes 30. Layer 50 may comprise indium tin oxide (ITO), for example. In addition, the sidewalls of trenches 28 (as seen in Fig. 3B) may be coated with a passivation layer 48. Alternatively or additionally, the trenches may be filled with the one or more of the dielectric materials that are
15 deposited to form upper DBR stack 44.

Finally, metal contact pads 54 are formed on the upper surface of upper DBR stack 44, contacting electrodes 30; and a common metal cathode layer 52 is formed on the lower surface of substrate 24. (Typically, substrate 24 is thinned before application of cathode layer 52.) When an excitation current is applied between pads 54 and cathode layer 52, it gives rise to emission of
20 respective beams 56 of radiation from optical emission regions 43 of VCSELs 22.

Figs. 3A and 3B are schematic frontal and sectional views, respectively, of a pair of VCSELs 22 in an array 58, in accordance with an alternative embodiment of the invention. VCSELs 22 in this embodiment are substantially identical to those shown and described above; and like elements in this and subsequent figures are marked with the same indicator numbers as
25 those in Figs. 2A and 2B. In array 58, however, trenches 28 of adjacent VCSELs overlap one another, in contrast to array 36, in which electrodes 30 overlap. The sectional view of Fig. 3B thus shows trenches 28 extending through MQW layer 40 to the upper part of lower DBR stack 42 and separating the mesas of the adjacent VCSELs.

Figs. 4A-4G are schematic sectional views showing successive stages in the fabrication of
30 an array of VCSELs 22, such as array 36 or array 58, in accordance with an embodiment of the invention. For the sake of compact illustration, Figs. 4C-4G combine the separate views of Figs. 2B and 3B, meaning that electrodes 30 are shown as though they overlapped trenches 28, rather

than showing two different cross-sections at each stage. Passivation layer 48 is also omitted from these figures for the sake of simplicity.

In preparation for VCSEL formation, a succession of epitaxial layers are deposited on substrate 24, as shown in Fig. 4A, beginning with n-type lower DBR stack 42, followed by MQW layer 40. An oxide aperture layer 60 is formed over the MQW layer. As a base for deposition of electrodes 30, a metal contact layer 62 is deposited over layer 60 at the intended location of each electrode, as shown in Fig. 4B. Transparent conductive layer 50 is then deposited over contact layer 62. Alternatively, the order of deposition of layers 50 and 62 may be reversed.

Next, as shown in Fig. 4C, trenches 28 are etched through layers 50, 60 and 40, down to lower DBR stack 42, thus defining a respective mesa 64 of each VCSEL 22 that is to be formed in the array. In addition, to increase the electrical efficiency of the VCSELs, protons may be implanted outside the mesa areas to provide electrical isolation between the mesas, thus reducing the current leakage through the area between the mesas and forcing all the currents to pass through emission regions 43. Oxide aperture layer 60 is processed, for example by etching laterally inward from trenches 28, to produce oxide layer 46, which defines apertures 26, as shown in Fig. 4D. Oxide layer 46 provides for confinement of both electrical current flow to emission region 43 and the resulting optical emission from the emission region within each mesa 64.

Alternating dielectric layers are now deposited over transparent conductive layer 50 in order to form upper DBR stack 44, as shown in Fig. 4E. Vias are etched through upper DBR stack 44, down to contact layer 62. These vias are filled with metal to form electrodes 30, as shown in Fig. 4F. Metal contact pads 54 are deposited over the upper surface of upper DBR stack 44 to connect with electrodes 30. At this stage, substrate 24 is typically thinned, for example by etching or polishing (not illustrated in the figures), and metal cathode layer 52 is deposited on the back side of the substrate, as shown in Fig. 4G. Application of an electrical current between contact pads 54 and cathode layer 52 will now give rise to laser emission through apertures 26.

VCSEL ARRAY WITH SEMICONDUCTOR DBR

Figs. 5A and 5B are schematic frontal and sectional views, respectively, of a pair of VCSELs 122 in an array 120, in accordance with a further embodiment of the invention. This embodiment is similar to that shown in Figs. 2A/B and described above, except that upper DBR stack 124 in VCSELs 122 comprises a stack of alternating p-type epitaxial layers. Because of the conductivity of these layers, electrodes 130 can be deposited over the upper surface of upper DBR stack 124, rather than in vias penetrating through the stack as in the preceding embodiments.

Other than these differences, VCSELs 122 are similar to VCSELs 22, as described above, and like elements in this and subsequent figures are marked with the same indicator numbers as those in Figs. 2A and 2B. As in Fig. 2A, VCSELs 122 in array 120 are oriented so that electrodes 130 of the neighboring VCSELs overlap. Electrodes 130 are disposed around the mesas of the
5 respective VCSELs in gaps between trenches 128.

Figs. 6A and 6B are schematic frontal and sectional views, respectively, of a pair of VCSELs 122 in an array 132, in accordance with an alternative embodiment of the invention. VCSELs 122 in this embodiment are substantially identical to those shown and described above with reference to Figs. 5A/B. In array 132, however, trenches 128 of adjacent VCSELs overlap
10 one another, in contrast to array 120, in which electrodes 130 overlap. The sectional view of Fig. 6B thus shows trenches 128 extending through upper DBR stack 124 and MQW layer 40 to the upper part of lower DBR stack 42 and separating the mesas of the adjacent VCSELs. Trenches 128 may be filled for example, by passivation layer 48, as shown in Fig. 6B, or alternatively or additionally, by metal from the layer of contact pads 54.

Figs. 7A-7F are schematic sectional views showing successive stages in the fabrication of an array of VCSELs 122, such as array 120 or array 132, in accordance with an embodiment of the invention. Again, for the sake of compact illustration, Figs. 7C-7F combine the separate views of Figs. 5B and 6B, meaning that electrodes 130 are shown as though they overlapped trenches 128, rather than showing two different cross-sections at each stage. Passivation layer 48 is also
20 omitted from these figures for the sake of simplicity.

In preparation for VCSEL formation, a succession of epitaxial layers are deposited on substrate 24, as shown in Fig. 7A, beginning with n-type lower DBR stack 42, followed by MQW layer 40. Oxide aperture layer 60 is formed over the MQW layer, and p-type upper DBR stack 124 is deposited over layer 60. As a base for deposition of electrodes 130, metal contact layer 62
25 is deposited over upper DBR stack 124 at the intended location of each electrode, as shown in Fig. 7B. Transparent conductive layer 50 is then deposited over contact layer 62. Alternatively, the order of deposition of layers 50 and 62 may be reversed.

Next, as shown in Fig. 7C, trenches 128 are etched through layer 50, upper DBR stack 124, and layers 60 and 40, down to lower DBR stack 42. Trenches 128 thus define mesa 64 for
30 each VCSEL 122 that is to be formed in the array. Protons may be implanted in the areas between the mesas to increase the electrical efficiency, as explained above. Oxide aperture layer 60 is processed, for example by etching laterally inward from trenches 28, to produce oxide layer 46, thus defining apertures 26, as shown in Fig. 7D.

Next, as shown in Fig. 4E, metal electrodes 130 are deposited over contact layer 62, and contact pads 54 are deposited over the upper surface of upper DBR stack 124 to connect with electrodes 130. At this stage, substrate 24 is typically thinned, for example by etching or polishing (not illustrated in the figures), and metal cathode layer 52 is deposited on the back side of the substrate, as shown in Fig. 7F. Application of an electrical current between contact pads 54 and cathode layer 52 will now give rise to laser emission through apertures 26.

Although the embodiments that are shown in the figures and described above relate specifically to VCSELs, the principles of the present invention may similarly be applied to other sorts of surface-emitting solid-state devices, such as resonant-cavity light-emitting diodes (RCLEDs). It will thus be appreciated that the embodiments described above are cited by way of example, and that the present invention is not limited to what has been particularly shown and described hereinabove. Rather, the scope of the present invention includes both combinations and subcombinations of the various features described hereinabove, as well as variations and modifications thereof which would occur to persons skilled in the art upon reading the foregoing description and which are not disclosed in the prior art.

CLAIMS

1. An optoelectronic device, comprising:
a semiconductor substrate;
a first set of thin-film layers disposed on the substrate and defining a lower distributed
5 Bragg-reflector (DBR) stack;
a second set of thin-film layers disposed over the lower DBR stack and defining an optical
emission region, which is contained in a mesa defined by multiple trenches, which are disposed
around the optical emission region without fully surrounding the optical emission region;
a third set of thin-film layers disposed over the optical emission region and defining an
10 upper DBR stack; and
electrodes, which are disposed around the mesa in gaps between the trenches and are
configured to apply an excitation current to the optical emission region.
2. The device according to claim 1, and comprising a transparent conductive layer in electrical
contact with the electrodes and extending across the mesa over at least the second set of thin-film
15 layers.
3. The device according to claim 1, wherein the third set of thin-film layers comprises
dielectric layers.
4. The device according to claim 3, wherein the electrodes comprise a metal, which is
deposited in vias that extend through the third set of thin-film layers.
- 20 5. The device according to claim 1, wherein the third set of thin-film layers comprises
epitaxial semiconductor layers.
6. The device according to claim 5, wherein the electrodes are deposited over the third set of
thin-film layers.
7. The device according to any of claims 1-6, wherein the first, second and third sets of thin-
25 film layers and the electrodes are disposed on an upper side of the semiconductor substrate, and
the device comprises a cathode layer on a lower side of the semiconductor substrate, opposite the
upper side.
8. An optoelectronic device, comprising:
a semiconductor substrate; and

a first set of thin-film layers disposed on the substrate and defining a lower distributed Bragg-reflector (DBR) stack;

a second set of thin-film layers disposed over the lower DBR stack and defining a plurality of optical emission regions, contained in respective mesas defined by multiple trenches, which are
5 disposed around each of the optical emission regions without fully surrounding the optical emission regions;

a third set of thin-film layers disposed over each of the optical emission regions and defining an upper DBR stack; and

electrodes, which are disposed around each of the mesas in gaps between the trenches and
10 are configured to apply an excitation current to each of the optical emission regions.

9. The device according to claim 8, wherein at least one of the trenches is common to a pair of neighboring mesas.

10. The device according to claim 8, wherein at least one of the electrodes is common to a pair of neighboring mesas.

11. The device according to any of claims 8-10, and comprising a transparent conductive layer in electrical contact with the electrodes and extending across the mesas over at least the second set of thin-film layers.
15

12. The device according to any of claims 8-10, wherein the first, second and third sets of thin-film layers and the electrodes are disposed on an upper side of the semiconductor substrate, and
20 the device comprises a cathode layer on a lower side of the semiconductor substrate, opposite the upper side, wherein the cathode layer is common to the plurality of the optical emission regions.

13. A method for producing an optoelectronic device, the method comprising:

depositing a first set of thin-film layers on a semiconductor substrate so as to define a lower distributed Bragg-reflector (DBR) stack;

25 depositing a second set of thin-film layers over the lower DBR stack so as to an optical emission region;

forming multiple trenches around the optical emission region without fully surrounding the optical emission region, thereby defining a mesa containing the optical emission region;

depositing a third set of thin-film layers over the optical emission region so as to define an
30 upper DBR stack;

depositing electrodes around the mesa in gaps between the trenches; and

coupling electrical contacts to the electrodes so as to apply an excitation current to the optical emission region.

14. The method according to claim 13, and comprising depositing a transparent conductive layer in electrical contact with the electrodes and extending across the mesa over at least the second set of thin-film layers.
15. The method according to claim 13, wherein the third set of thin-film layers comprises dielectric layers.
16. The method according to claim 15, wherein depositing the electrodes comprises etching vias through the third set of thin-film layers, and filling the vias with a metal.
17. The method according to claim 13, wherein the third set of thin-film layers comprises epitaxial semiconductor layers.
18. The method according to claim 17, wherein the electrodes are deposited over the third set of thin-film layers.
19. The method according to any of claims 13-18, wherein the first, second and third sets of thin-film layers and the electrodes are deposited on an upper side of the semiconductor substrate, and the method comprises depositing a cathode layer on a lower side of the semiconductor substrate, opposite the upper side.

AMENDED CLAIMS**received by the International Bureau on 06 August 2020 (06.08.2020)**

1. An optoelectronic device, comprising:
a semiconductor substrate;
5 a first set of thin-film layers disposed on the substrate and defining a lower distributed Bragg-reflector (DBR) stack;
a second set of thin-film layers disposed over the lower DBR stack and defining an optical emission region, which is contained in a mesa defined by multiple trenches, which are disposed around the optical emission region without fully surrounding the optical emission region;
10 a third set of thin-film layers disposed over the optical emission region and defining an upper DBR stack;
a transparent conductive layer extending across the mesa over at least the second set of thin-film layers; and
electrodes, which are disposed around the mesa in gaps between the trenches in electrical
15 contact with the transparent conductive layer and are configured to apply an excitation current through the transparent conductive layer to the optical emission region.
2. The device according to claim 1, wherein the transparent conductive layer comprises indium tin oxide (ITO).
3. The device according to claim 1, wherein the third set of thin-film layers comprises
20 dielectric layers.
4. The device according to claim 3, wherein the electrodes comprise a metal, which is deposited in vias that extend through the third set of thin-film layers.
5. The device according to claim 1, wherein the third set of thin-film layers comprises epitaxial semiconductor layers.
- 25 6. The device according to claim 5, wherein the electrodes are deposited over the third set of thin-film layers.
7. The device according to any of claims 1-6, wherein the first, second and third sets of thin-film layers and the electrodes are disposed on an upper side of the semiconductor substrate, and the device comprises a cathode layer on a lower side of the semiconductor substrate, opposite the
30 upper side.

8. An optoelectronic device, comprising:
a semiconductor substrate;
a first set of thin-film layers disposed on the substrate and defining a lower distributed Bragg-reflector (DBR) stack;

5 a second set of thin-film layers disposed over the lower DBR stack and defining a plurality of optical emission regions, contained in respective mesas defined by multiple trenches, which are disposed around each of the optical emission regions without fully surrounding the optical emission regions;

10 a third set of thin-film layers disposed over each of the optical emission regions and defining an upper DBR stack; and

electrodes, which are disposed around each of the mesas in gaps between the trenches and are configured to apply an excitation current to each of the optical emission regions, wherein at least one of the electrodes is common to a pair of neighboring mesas and is shared in providing the excitation current to both of the mesas in the pair.

15 9. The device according to claim 8, wherein at least one of the trenches is common to a pair of neighboring mesas.

10. The device according to claim 8 or 9, and comprising a transparent conductive layer in electrical contact with the electrodes and extending across the mesas over at least the second set of thin-film layers.

20 11. The device according to claim 8 or 9, wherein the first, second and third sets of thin-film layers and the electrodes are disposed on an upper side of the semiconductor substrate, and the device comprises a cathode layer on a lower side of the semiconductor substrate, opposite the upper side, wherein the cathode layer is common to the plurality of the optical emission regions.

12. A method for producing an optoelectronic device, the method comprising:

25 depositing a first set of thin-film layers on a semiconductor substrate so as to define a lower distributed Bragg-reflector (DBR) stack;

depositing a second set of thin-film layers over the lower DBR stack so as to an optical emission region;

30 forming multiple trenches around the optical emission region without fully surrounding the optical emission region, thereby defining a mesa containing the optical emission region;

depositing a third set of thin-film layers over the optical emission region so as to define an upper DBR stack;

depositing electrodes around the mesa in gaps between the trenches;

depositing a transparent conductive layer in electrical contact with the electrodes and

5 extending across the mesa over at least the second set of thin-film layers; and

coupling electrical contacts to the electrodes so as to apply an excitation current through the transparent conductive layer to the optical emission region.

13. The method according to claim 12, wherein the transparent conductive layer comprises indium tin oxide (ITO).

10 14. The method according to claim 12, wherein the third set of thin-film layers comprises dielectric layers.

15. The method according to claim 14, wherein depositing the electrodes comprises etching vias through the third set of thin-film layers, and filling the vias with a metal.

16. The method according to claim 12, wherein the third set of thin-film layers comprises epitaxial semiconductor layers.

17. The method according to claim 16, wherein the electrodes are deposited over the third set of thin-film layers.

18. The method according to any of claims 12-17, wherein the first, second and third sets of thin-film layers and the electrodes are deposited on an upper side of the semiconductor substrate, and the method comprises depositing a cathode layer on a lower side of the semiconductor substrate, opposite the upper side.

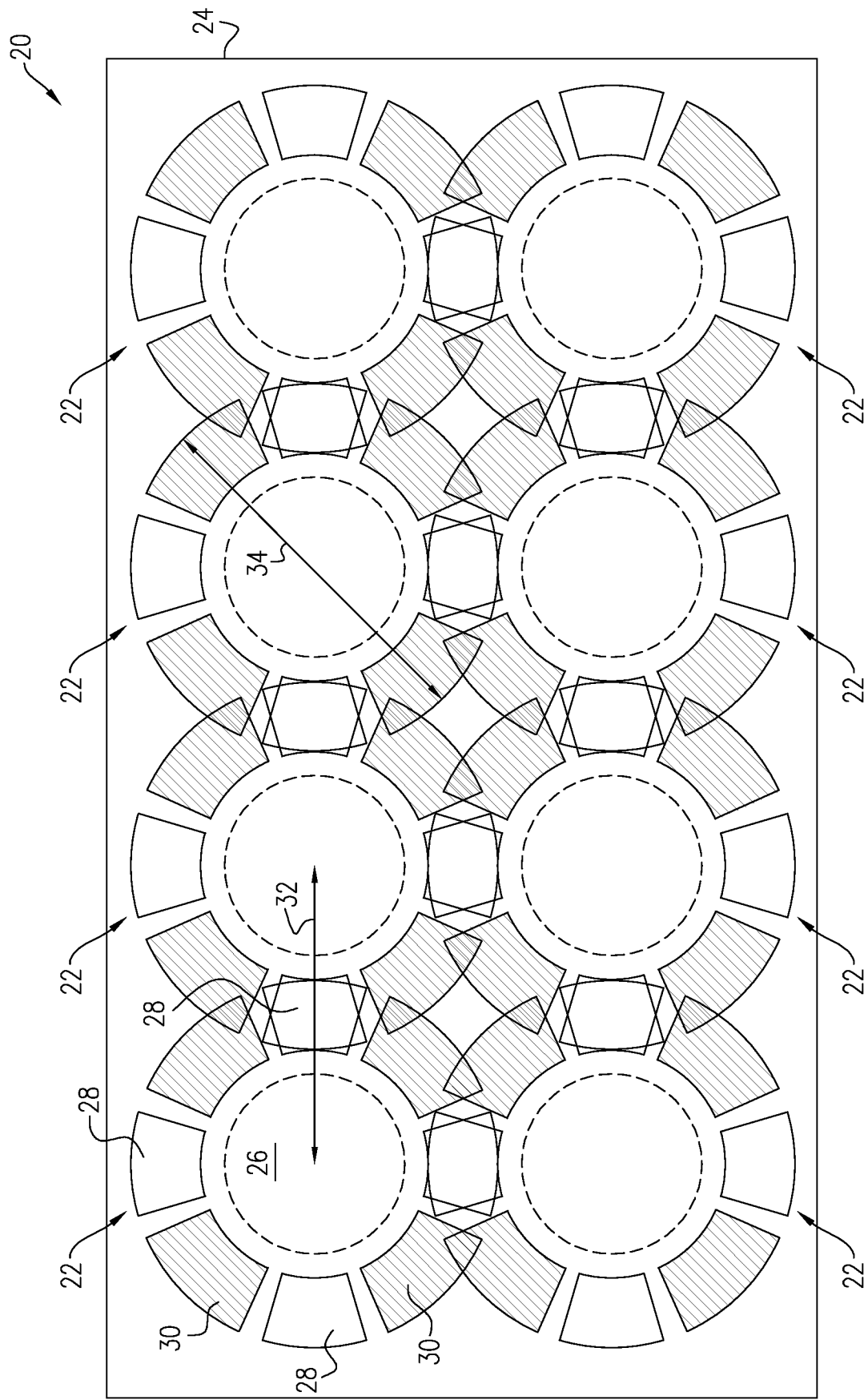


FIG. 1

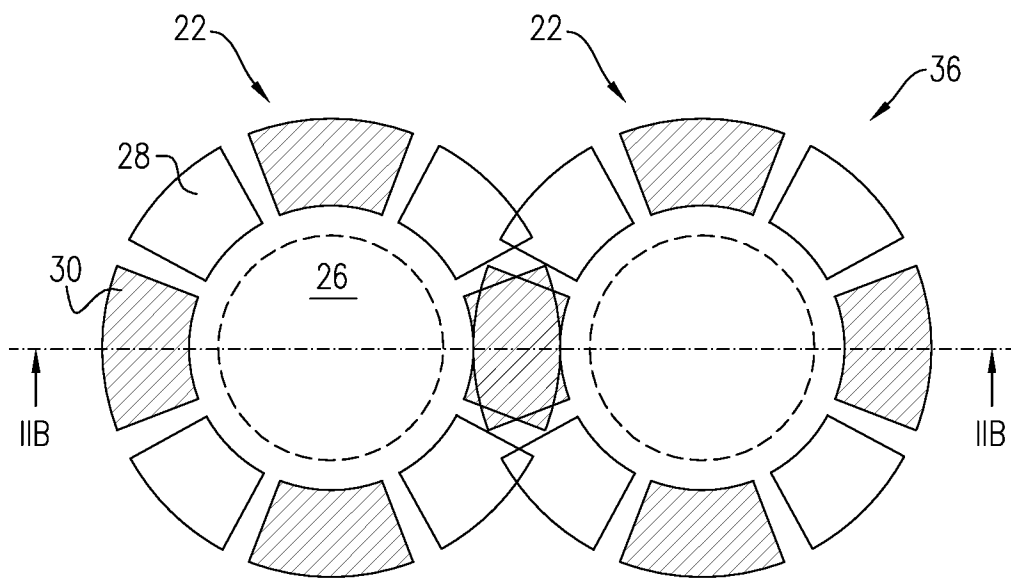


FIG. 2A

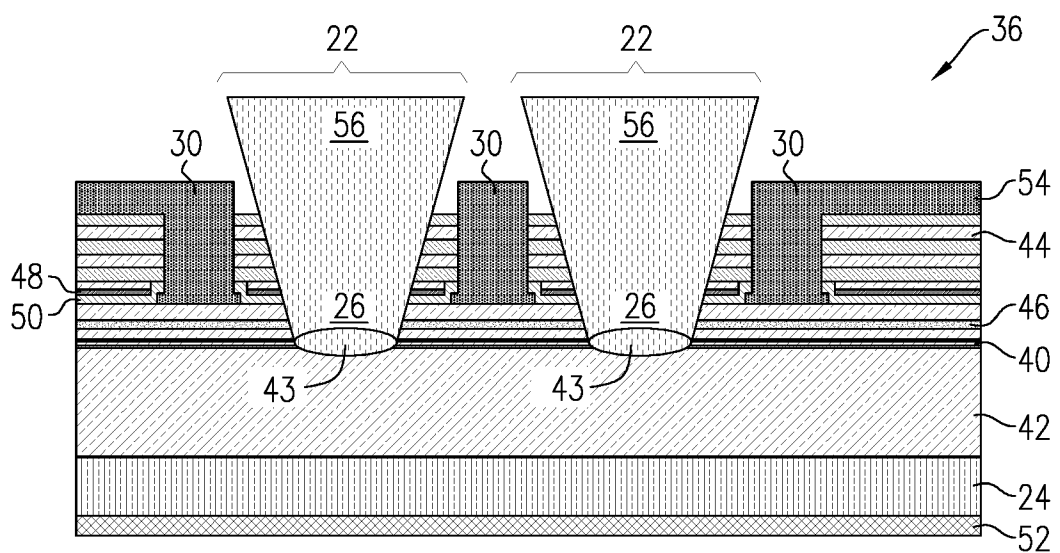


FIG. 2B

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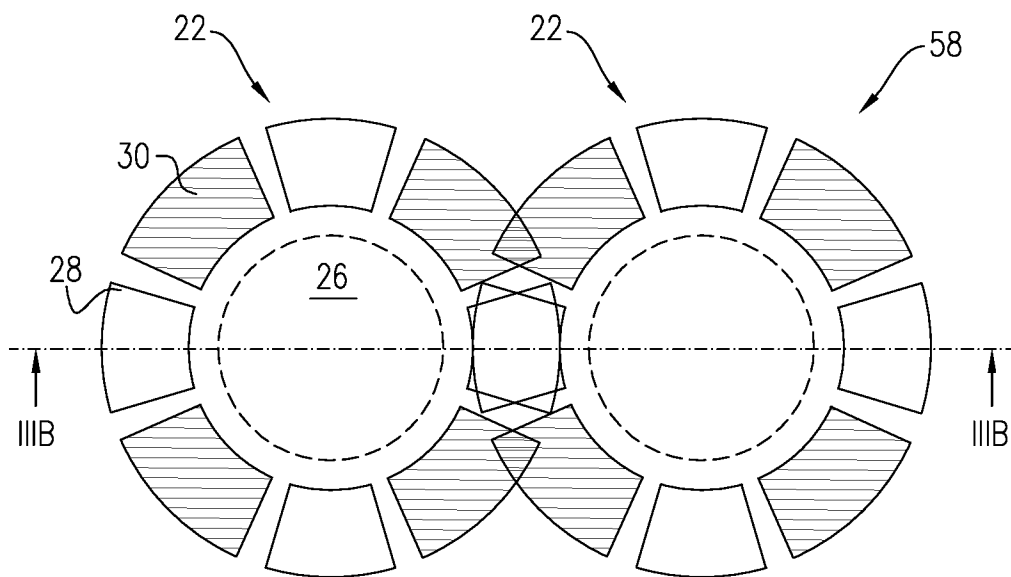


FIG. 3A

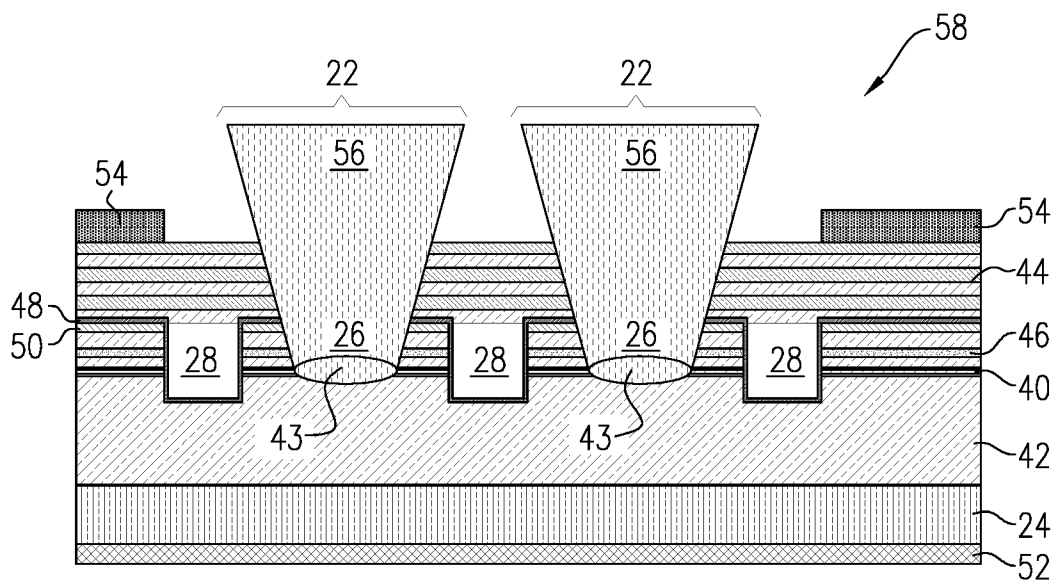


FIG. 3B

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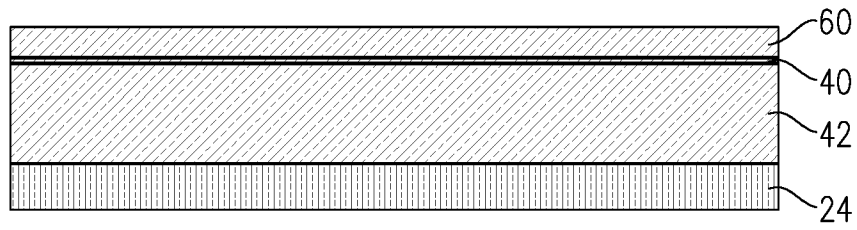


FIG. 4A

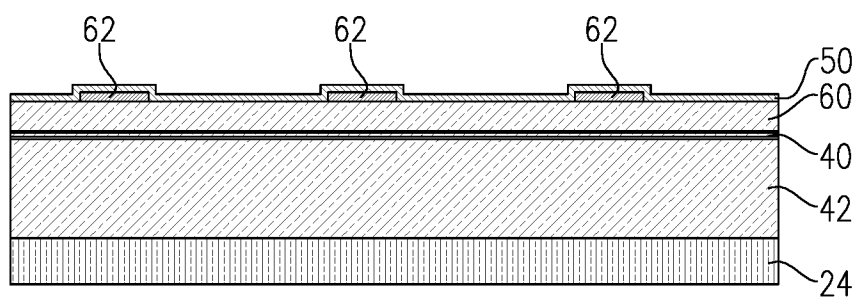


FIG. 4B

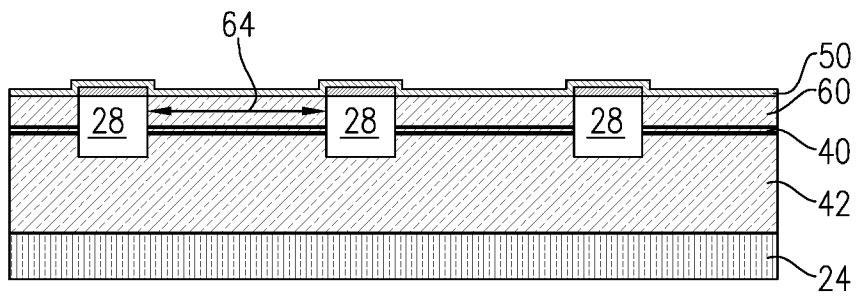


FIG. 4C

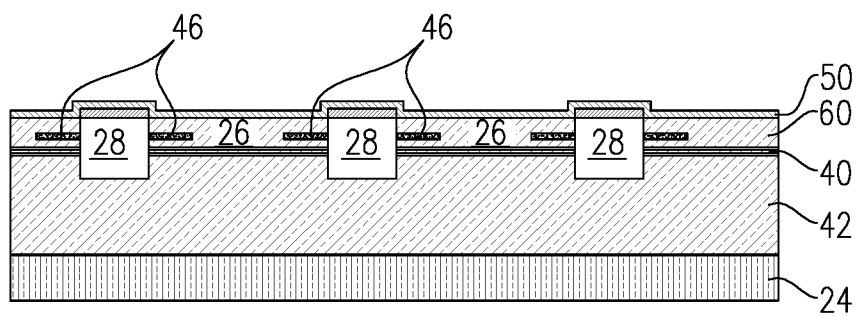


FIG. 4D

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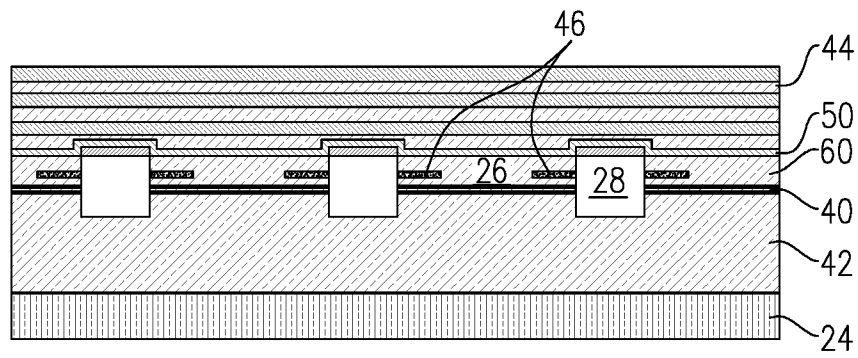


FIG. 4E

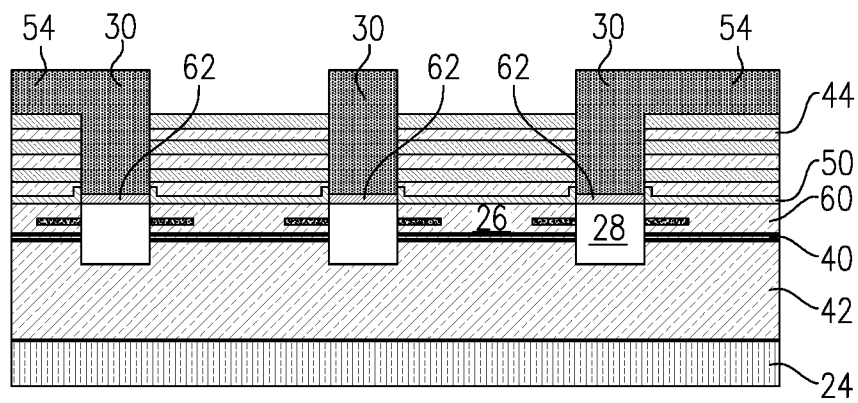


FIG. 4F

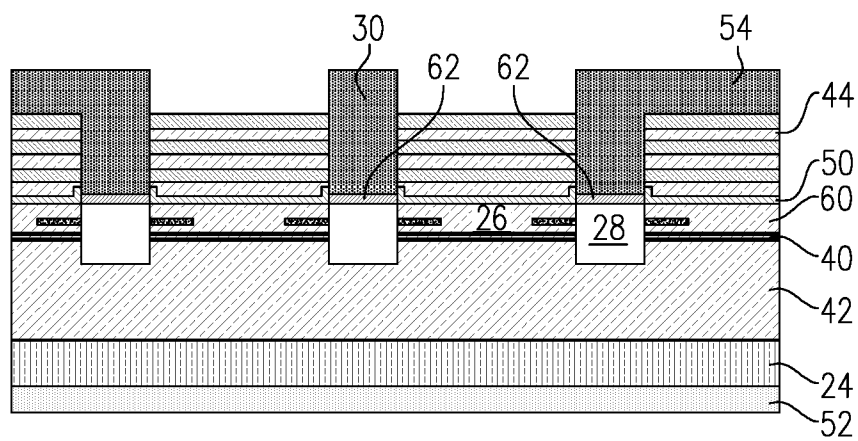


FIG. 4G

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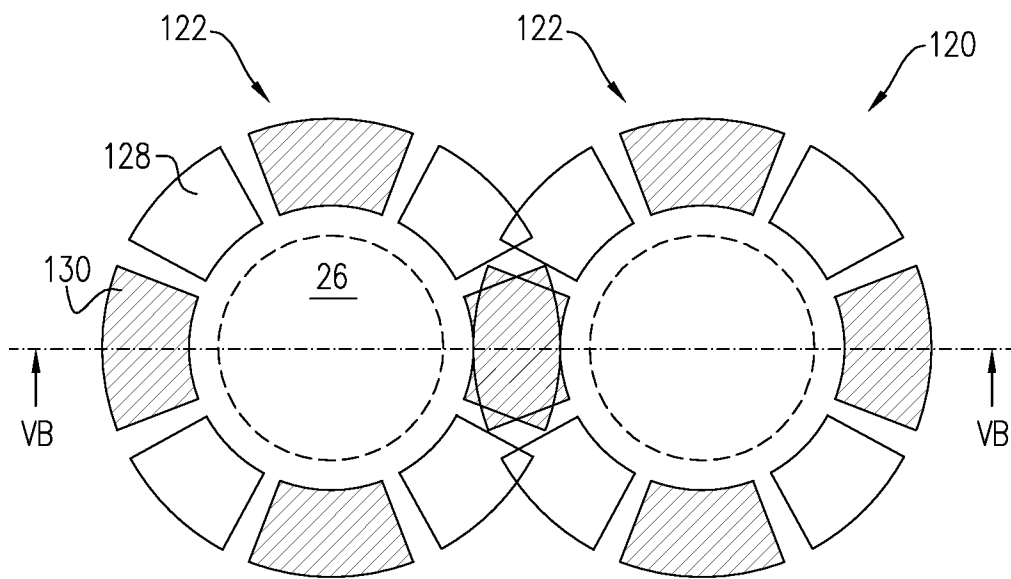


FIG. 5A

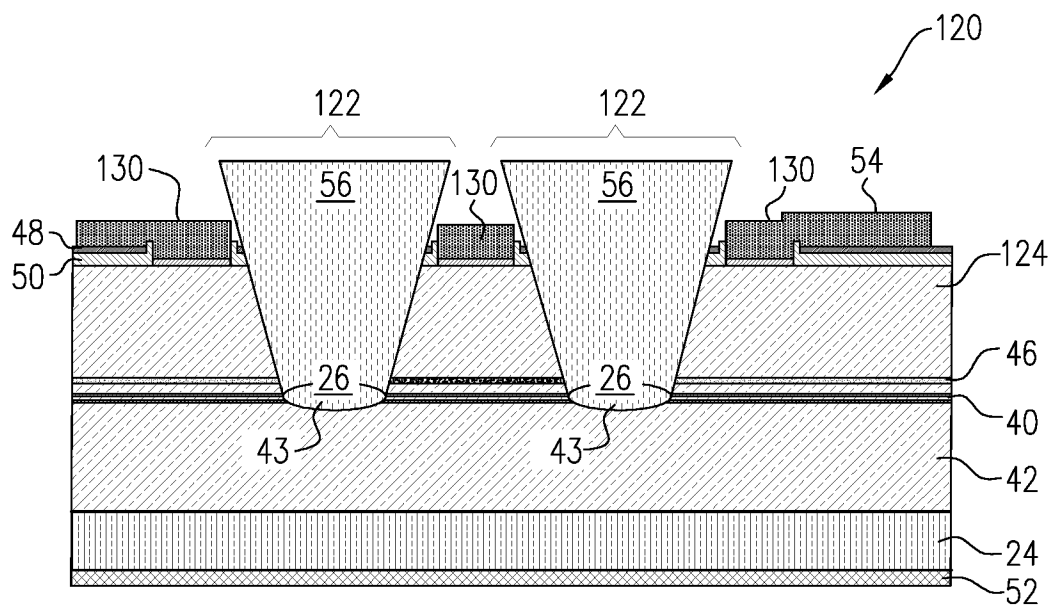


FIG. 5B

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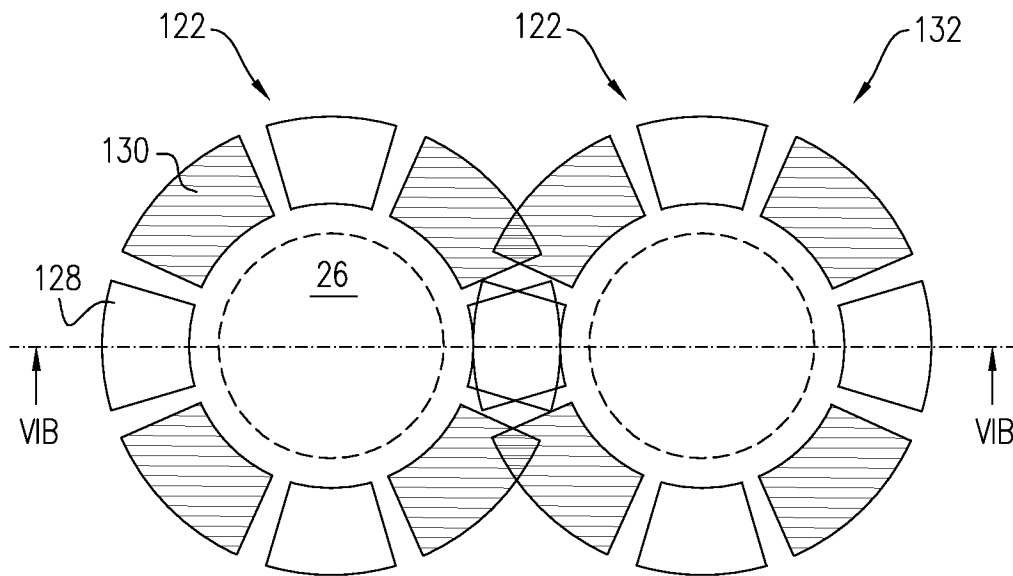


FIG. 6A

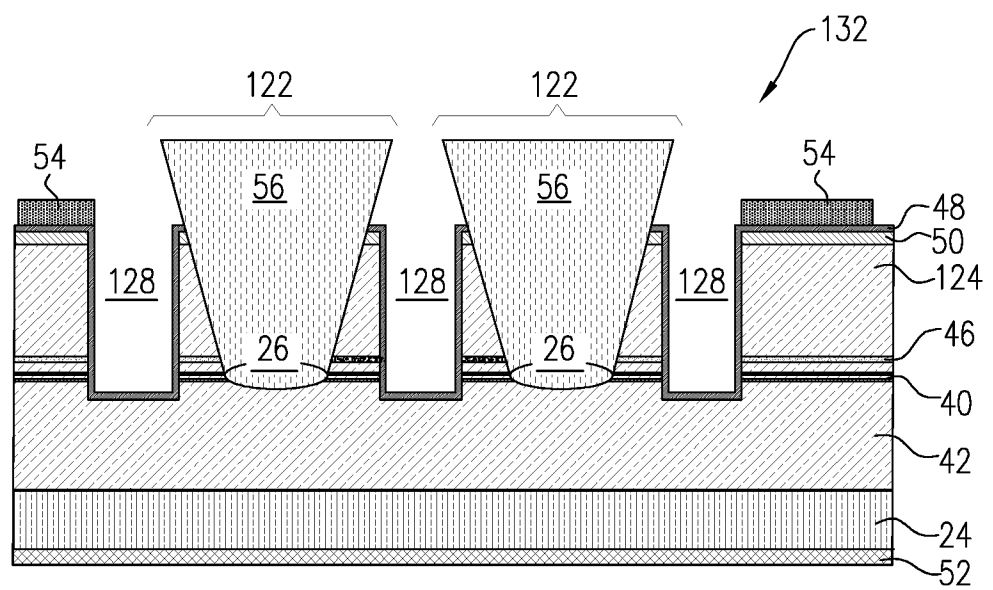


FIG. 6B

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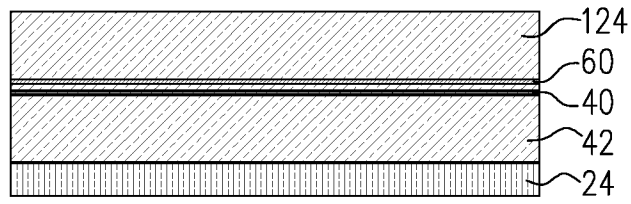


FIG. 7A

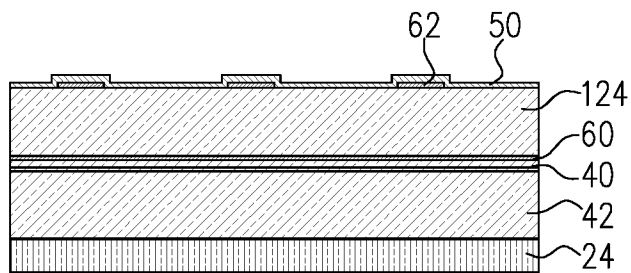


FIG. 7B

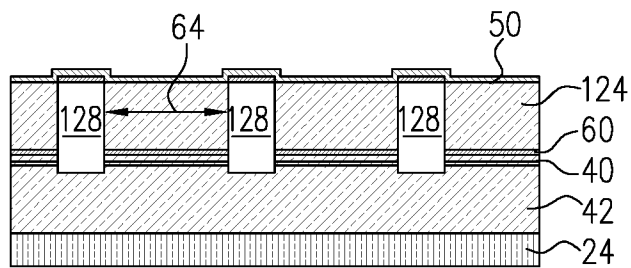


FIG. 7C

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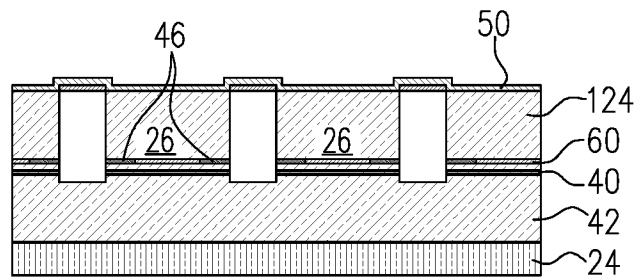


FIG. 7D

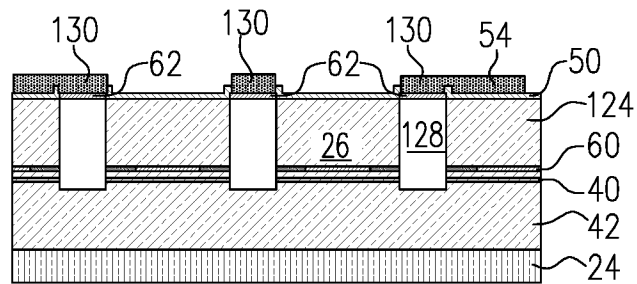


FIG. 7E

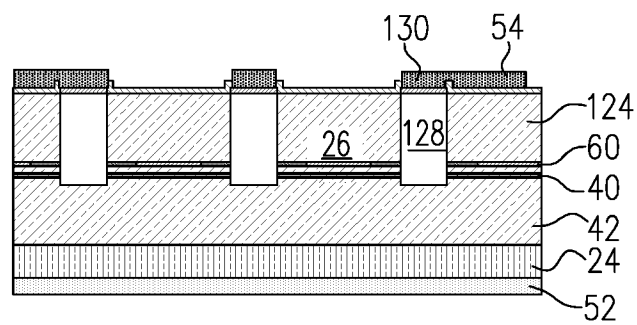


FIG. 7F

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2020/021631

A. CLASSIFICATION OF SUBJECT MATTER INV. H01S5/042 H01S5/42 H01S5/183 ADD. H01S5/026 H01S5/022 H01S5/20		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H01S		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EPO-Internal, COMPENDEX, INSPEC, WPI Data		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 9 742 153 B1 (LUMENTUM OPERATIONS LLC [US]) 22 August 2017 (2017-08-22) column 2, line 29 - column 8, line 22; figures 1-3	1-19
X	US 2017/353012 A1 (BARVE AJIT VIJAY [US] ET AL) 7 December 2017 (2017-12-07) paragraphs [0017] - [0071]; figures 1-4	1-7
A	US 2010/203660 A1 (TANAKA AKIMASA [JP]) 12 August 2010 (2010-08-12) paragraphs [0053] - [0070]; figure 2	2,4,11, 14,16
X,P	US 2019/305522 A1 (YUEN ALBERT [US] ET AL) 3 October 2019 (2019-10-03) paragraphs [0016] - [0064]; figures 1-4	1,5-10, 12,13, 17-19
☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents : "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 4 June 2020		Date of mailing of the international search report 16/06/2020
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016		Authorized officer Laenen, Robert

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

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