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(54) **Title**: METHOD AND DEVICE FOR ESTIMATION AND CORRECTION OF I/Q MISMATCH USING ITERATIVE LOOPS

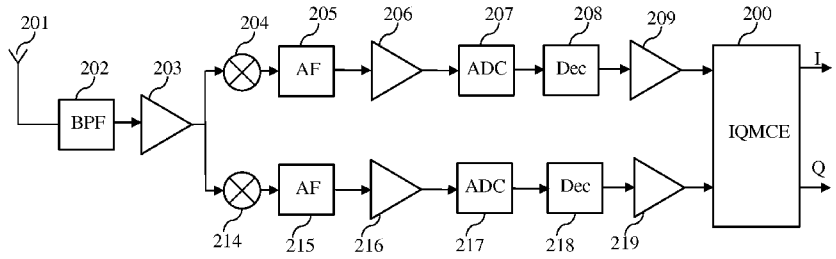

Fig. 2

(57) **Abstract**: The invention proposes a method for correcting and/or estimating an in- phase/quadrature-phase mismatch on a random received signal in a radio receiving device, said method causing the device to perform: -processing the random received signal in order to obtain an in-phase component and a quadrature-phase component, -amplifying and digitally converting the in-phase component in order to obtain in-phase samples, -amplifying and digitally converting the quadrature-phase component in order to obtain quadrature-phase samples, -correcting and/or estimating in-phase/quadrature-phase mismatch based on in- phase samples and quadrature-phase samples, the estimating of the in- phase/quadrature-phase mismatch being performed using two estimation loops.

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METHOD AND DEVICE FOR ESTIMATION AND CORRECTION OF I/Q MISMATCH USING ITERATIVE LOOPS

The present invention generally relates to a method and a device for correcting and/or estimating the mismatch between both in-phase (I) and quadrature-phase (Q) baseband signal components of a received radio-frequency (RF) signal in a radio receiving device. The mismatch between both in-phase and quadrature-phase baseband signal components is usually referred to as in-phase/quadrature-phase mismatch, or shortly as IQ mismatch (IQM) or also IQ imbalance.

A radio receiver uses two distinct orthogonal channels to form the in-phase (I) and the quadrature-phase (Q) components of the received signal. Each channel is composed of at least a mixer, at least one programmable gain amplifier and at least one filter. The mismatch or imbalance between in-phase and quadrature-phase channels regarding the filters, the at least one programmable gain amplifiers and the local oscillators can lead to imperfect phase quadrature, known as IQM phase error, and imperfect gain balancing, known as IQM gain error, between those two channels that may severely limit the performance of the receiver.

The present invention aims at providing a method and a device for correcting and/or estimating the mismatch between in-phase and quadrature-phase signal components on a received signal in a radio receiving device in order to improve the performance of the receiver.

To that end, the present invention concerns a method for correcting and/or estimating an in-phase/quadrature-phase mismatch on a random received signal in a radio receiving device, said method causing the device to perform:

- processing the random received signal in order to obtain an in-phase component and a quadrature-phase component,
- amplifying by at least a first programmable gain amplifier and digitally converting by a first analogue to digital converter the in-phase component in order to obtain in-phase samples,
- amplifying by at least a second programmable gain amplifier and digitally converting by a second analogue to digital converter the quadrature-phase component in order to obtain quadrature-phase samples,
- correcting and/or estimating in-phase/quadrature-phase mismatch based on in-phase samples and quadrature-phase samples, the estimating of the in-phase/quadrature-phase mismatch being performed using two estimation loops, each loop generating a coefficient, a gain loop comprising a first weighting module which weights the difference of in-phase samples and of quadrature-phase samples and a phase loop comprising a second weighting module which weights the result of a multiplication of in-phase samples and of quadrature-phase samples, the correcting being performed on in-phase samples and/or quadrature-phase samples using coefficients provided by the loops.

The present invention concerns also an apparatus for correcting and/or estimating an in-phase/quadrature-phase mismatch on a random received signal, comprising:

- means for processing the random received signal in order to obtain an in-phase component and a quadrature-phase component,
- means for amplifying by at least a first programmable gain amplifier and digitally converting by a first analogue to digital converter the in-phase component in order to obtain in-phase samples,

- means for amplifying by at least a second programmable gain amplifier and digitally converting by a second analogue to digital converter the quadrature-phase component in order to obtain quadrature-phase samples,

- means for correcting and/or estimating in-phase/quadrature-phase mismatch based on in-phase samples and quadrature-phase samples, the means for estimating the in-phase/quadrature-phase mismatch comprising two estimation loops, each loop providing a coefficient, a gain loop comprising a first weighting module which weights the difference of in-phase samples and of quadrature-phase samples and a phase loop comprising a second weighting module which weights the result of a multiplication of in-phase samples and of quadrature-phase samples, the means for correcting in-phase samples and/or quadrature-phase samples using the coefficients.

The present invention concerns also an apparatus for correcting and/or estimating an in-phase/quadrature-phase mismatch on a random received signal, the apparatus comprising circuitry causing the apparatus to perform:

- processing the random received signal in order to obtain an in-phase component and a quadrature-phase component,

- amplifying by at least a first programmable gain amplifier and digitally converting by a first analogue to digital converter the in-phase component in order to obtain in-phase samples,

- amplifying by at least a second programmable gain amplifier and digitally converting by a second analogue to digital converter the quadrature-phase component in order to obtain quadrature-phase samples,

- correcting and/or estimating in-phase/quadrature-phase mismatch based on in-phase samples and quadrature-phase samples, the estimating of the in-phase/quadrature-phase mismatch being performed using two estimation loops, each loop generating a coefficient, a gain loop comprising a first weighting module which weights the difference of in-phase samples and of quadrature-phase samples and a phase loop comprising a second weighting module which weights the result of a multiplication of in-phase samples and of quadrature-phase samples, the correcting being performed on in-phase samples and/or quadrature-phase samples using coefficients provided by the loops.

Thus, the performance of the receiver is improved.

By performing the correction and/or the estimation of the in-phase/quadrature-phase mismatch on in-phase and quadrature-phase samples after all the amplifications, the IQ mismatch gain and phase impairments can be corrected efficiently.

Furthermore, by using two loops for the estimating, the present invention enables a quick and reliable estimation.

By using two coefficients for the correction, the correction is reliable and does not need complex hardware or software implementation.

The present invention also concerns, in at least one embodiment, a radio access network system comprising an apparatus for correcting and/or estimating an in-phase/quadrature-phase mismatch according to the present invention.

The present invention also concerns, in at least one embodiment, a computer program that can be downloaded from a communication network and/or stored on a medium that can be read by a computer or processing device. This computer program comprises instructions for causing implementation of the aforementioned method, or any of its embodiments, when said program is run by a processor.

The present invention also concerns an information storage means, storing a computer program comprising a set of instructions causing implementation of the aforementioned method, or any of its embodiments, when the stored information is read from said information storage means and run by a processor.

The characteristics of the invention will emerge more clearly from a reading of the following description of an example embodiment, the said description being produced with reference to the accompanying drawings, among which:

Fig. 1 schematically represents an example architecture of a receiver device in which some embodiments of the present invention can be implemented;

Fig. 2 illustrates an example of the receiving part of the wireless interface of the receiver according to some embodiments of the present invention;

Fig. 3 schematically represents an example of architecture of an in-phase/quadrature-phase mismatch correction and/or estimation module according to some embodiments of the present invention;

Fig. 4 schematically represents an example of architecture of an in-phase/quadrature-phase mismatch correction module according to some embodiments of the invention;

Fig. 5 schematically represents an example of architecture of an in-phase/quadrature-phase mismatch estimation module according to some embodiments of the invention;

Fig. 6 schematically represents an architecture of a sample level detection module according to some embodiments of the invention;

Figs. 7a and 7b schematically represent some examples of loops weight values of the in-phase/quadrature-phase mismatch estimation module and/or of loop weight value of at least one direct current offset correction which evolve in the time;

Fig. 8 represents an example of a table used for determining, according to an automatic gain controller headroom value, the weight values of both the phase and gain loops;

Fig. 9 exemplifies sub-period indexes and their respective durations, further to phase and gain loop weight values for in-phase/ quadrature-phase mismatch estimation module assuming an auto gain controller headroom nominal value;

Fig. 10 represents an example of an algorithm for determining weight values of the phase and gain loops applied during different time periods according to some embodiments of the invention;

Fig. 11 represents an example of an algorithm for managing the operation of the in-phase/quadrature-phase mismatch correction module and/or of the in-phase/quadrature-phase mismatch estimation module according to some embodiments of the invention;

Fig. 12 schematically represents an example of architecture of a receiving part including at least one Direct Current Offset compensation loop according to some embodiments of the invention.

Fig. 1 schematically represents an example architecture of a receiver device in which some embodiments of the present invention can be implemented.

The receiver device 10 may be included into a mobile telecommunication system, and more precisely in a radio access network (RAN), for example like in a User Equipment (for reception in the DownLink) or a Base Station (for reception in the UpLink) compatible with Long Term Evolution, Wideband Code Division Multiple Access or Global System for Mobile Communications system.

The receiver device 10 comprises the following components interconnected by a communications bus 101: a processor, microprocessor, microcontroller or CPU

(*Central Processing Unit*) 100 and a memory (e.g. a RAM (*Random-Access Memory*) 103 and/or a ROM (*Read-Only Memory*) 102. The receiver device 10 may also comprise an SD (*Secure Digital*) card reader 104 or any other device adapted to read information stored on storage means. The receiver device 10 may also comprise a wireless interface I/F 105.

The wireless interface 105 allows the receiver 10 to wirelessly communicate with a transmitter device.

CPU 100 is able of executing instructions loaded into RAM 103 from ROM 102 or from an external memory, such as an SD card. When the receiver 10 is powered on, CPU 100 reads instructions from RAM 103 and executes the read instructions. The instructions form one computer program that causes CPU 100 to perform some or all of the steps of the algorithms described hereafter with regard to Figs. 10 and 11.

Any and all steps of the algorithms described hereafter with regard to Figs. 10 and 11 may be implemented in software by execution of a set of instructions or program by a programmable computing machine, such as a PC (*Personal Computer*), a DSP (*Digital Signal Processor*) or a microcontroller; or else implemented in hardware by a machine or a dedicated component, such as an FPGA (*Field-Programmable Gate Array*) or an ASIC (*Application-Specific Integrated Circuit*).

In other words, the receiver 10 includes circuitry, or a device including circuitry, causing the receiver device to perform the steps of the algorithms described hereafter with regard to Figs. 10 and 11.

Such a device including circuitry causing the receiver 10 to perform the steps of the algorithms described hereafter with regard to Figs. 10 and 11 may be an external device connectable to the receiver 10.

The receiver 10 may also be a part of another device, for example when the receiver 10 is a chip, a chipset, or a module. Alternatively, instead of being a part of another device or connected to a dedicated communication device, the receiver 10, according to the invention, may provide communication capability to any suitable device, such as a computer device, a machine, for example a vending machine or a vehicle like a car or truck.

The term circuitry refers either to hardware implementation, consisting in analogue and/or digital processing, or to a combination of hardware and software implementation, including instructions of computer program associated with

memories and processor causing the processor to perform any and all steps of the algorithm described hereafter with regard to Figs. 10 and 11.

Fig. 2 illustrates an example of the receiving part of the wireless interface of the receiver according to some embodiments of the present invention.

The receiving part of the wireless interface 105 comprises an analogue band pass filter 202 which filters signal received by an antenna 201 which is linked to the wireless interface 105 or included into the wireless interface 105.

Signals received by the antenna 201 are random signals, for example the one representative of data related to a communication with a remote telecommunication device.

The present invention is able to correct IQ mismatch without any need of known signals like the one representative of pilot symbols.

The filtered signal is amplified by a low noise amplifier 203. The gain of the low noise amplifier 203 is set by an automatic gain controller (AGC) not shown in Fig. 2.

The receiving part comprises two channels which respectively process signal provided by the low noise amplifier 203 in order to provide it to an IQ Mismatch Correction and Estimation module (IQMCE) 200 according to the invention.

A first channel is composed of a mixer 204, an analogue low-pass filter (AF) 205, a programmable analogue gain amplifier 206, an analogue-to-digital converter ADC 207, a decimator Dec 208 and a Programmable Digital Gain (PDG) 209. The first channel provides in-phase samples of the processed signal to the IQMCE module 200.

A second channel is composed of a mixer 214, an analogue low-pass filter (AF) 215, a programmable analogue gain amplifier 216, an ADC 217, a decimator Dec 218 and a PDG 219. The second channel provides quadrature-phase samples of the processed signal to the IQMCE module 200.

The global IQ mismatch can be modelled, without loss of generality, as an IQM gain error and an IQM phase error on the second mixer 214.

The output signal of the low noise amplifier 203 is converted into baseband signal in two in-phase (I) and quadrature-phase (Q) baseband components by the mixers 204 and 214.

The mixer 204, in order to provide the I baseband component of the received signal, multiplies the signal provided by the low noise amplifier 203 by

$cos(2\pi f_{LO}t)$ where f_{LO} is the local oscillator frequency of the receiver 10 and t is the time.

The mixer 214, in order to provide the Q baseband component of the received signal, multiplies the signal provided by the low noise amplifier 203 by $-\delta g.sin(2\pi f_{LO}.t-\delta\varphi)$ where δg denotes the IQM gain error and $\delta\varphi$ denotes the IQM phase error between the analogue components comprised in the first and second channels.

After conversion to I baseband component by the mixer 204, the I baseband component is filtered by the analogue baseband filter 205, amplified by the programmable analogue gain amplifier 206, digitally converted by the ADC 207, the digital output samples of which are decimated by the decimator 208 and the decimated samples are amplified by the PDG 209.

After conversion to Q baseband component by the mixer 214, the Q baseband component is as well filtered by the analogue baseband filter 215, amplified by the programmable analogue gain amplifier 216, digitally converted by the ADC 217, the digital output samples of which are decimated by the decimator 218 and the decimated samples are amplified by the PDG 219.

The IQMCE module 200 compensates the IQ mismatch impairment due to analogue components by performing an IQ mismatch correction and/or estimation.

According to some embodiments of the invention, the IQ mismatch correction is performed in the digital domain and more precisely on samples provided by the PDG modules 209 and 219.

Let 'n' denote the index corresponding in the sequel to the n^{th} sampled digital sample.

The correction for the IQ mismatch gain and phase impairments is performed using two real IQM correction coefficients, α and β.

$\boldsymbol{\alpha}$ is referred to as phase correction coefficient since its ideal value $\boldsymbol{\alpha_{ideal}}$ depends only on IQM phase error value $\delta\varphi$.

$\boldsymbol{\beta}$ is referred as gain correction coefficient since its ideal value $\boldsymbol{\beta_{ideal}}$ depends mainly on IQM gain error value δg.

$$\begin{cases} \alpha_{ideal} = \tan(\delta\varphi) \\ \beta_{ideal} = \dfrac{1}{\delta g \,.\cos(\delta\varphi)} \end{cases}$$

The IQMCE module 200 determines the IQ mismatch phase α and gain β correction coefficients values to be configured in order to compensate for overall receiver IQ mismatch. IQ mismatch estimation principle is to use an adaptive algorithm able to iteratively update the IQM phase correction coefficient α and the IQM gain correction coefficient β values in such a way that both α and β correction coefficients converge close to their respective ideal target value, that is:

$$\begin{cases} \alpha \rightarrow \alpha_{ideal} = \tan(\delta\varphi) & (1) \\ \beta \rightarrow \beta_{ideal} = \dfrac{1}{\delta g \,.\, \cos(\delta\varphi)} & (2) \end{cases}$$

Assuming (2) is verified, we get: $\cos(\delta\varphi) \rightarrow \dfrac{1}{\beta.\delta g}$

or $\beta.\delta g.\cos(\delta\varphi) \rightarrow 1$

and (1) can then be written as: $\alpha \rightarrow \beta.\delta g.\sin(\delta\varphi)$

The IQ mismatch estimation algorithm hence converges if both following relationships are simultaneously fulfilled:

$$\begin{cases} \varepsilon_p = \alpha - \beta.\delta g.\sin(\delta\varphi) \rightarrow 0 \\ \varepsilon_g = 1 - \beta.\delta g.\cos(\delta\varphi) \rightarrow 0 \end{cases}$$

According to some embodiments of the invention, the IQMCE module 200 comprises a combination of two estimation loops running simultaneously and using ε_g and ε_p as error signals, a phase estimation loop to iteratively update α correction coefficient value and a gain estimation loop to iteratively update β correction coefficient value.

The error signals ε_g and ε_p are respectively further accumulated and weighted with a gain loop weight called K_g and a phase loop weight K_p.

The IQMCE module 200 is disclosed in reference to Fig. 3.

Fig. 3 schematically represents an example of architecture of an in-phase/quadrature-phase mismatch correction and/or estimation module according to some embodiments of the present invention.

The IQMCE module 200 comprises an in-phase/quadrature-phase Mismatch Estimation module 300 (IQME) and an in-phase/quadrature-phase Mismatch correction module 310 (IQMC).

The I samples provided by the PDG 209 are provided to the IQME module 300 and to the IQMC module 310.

The Q samples provided by the PDG 219 are provided to the IQME module 300 and to the IQMC module 310.

For example, the IQMC module 310 possibly performs an IQM correction on Q samples provided by the PDG 209 based both on the I samples and the Q samples provided by the PDG 219 using correction coefficients α and β provided respectively by multiplexers 303 and 304.

It has to be noted here that with no loss of generality, the IQMC module 310 may perform the whole IQM correction on the Q samples. In a variant the IQMC module 310 may perform the IQM correction on the I samples or on I and Q samples.

The I samples provided by the PDG 209 and provided by the IQMC module 310 are noted I_{out} in Fig. 3 and the corrected Q samples are noted Q_{out} in Fig. 3. The IQMC module 310 will be disclosed more precisely in reference to Fig. 4.

The multiplexor 303 is controlled by an IQMCE_DRIVE module 307 which enables the transfer of the correction coefficient α determined by the IQME module 300 or the transfer of the correction coefficient α stored in RAM memory 103 to the IQMC module 310. The correction coefficient α stored in RAM memory 103 is a correction coefficient previously determined by the IQME module 300 and may be used when the IQME module 300 is disabled.

The multiplexor 304 is controlled by an IQMCE_DRIVE module 307 which enables the transfer of the correction coefficient β determined by the IQME module 300 or the transfer of the correction coefficient β stored in RAM memory 103 to the IQMC module 310. The correction coefficient β stored in RAM memory 103 is a correction coefficient previously determined by the IQME module 300 and may be used when the IQME module 300 is disabled.

The IQME module 300 determines the correction coefficient α and provides it to the multiplexer 303. The IQME module 300 determines the correction coefficient β and provides it to the multiplexer 304. The IQME module 300 will be disclosed more precisely in reference to Fig. 5.

Fig. 4 schematically represents an example of architecture of an in-phase/quadrature-phase mismatch correction module according to some embodiments of the invention.

The Q samples provided by the PDG 219 are multiplied by the correction coefficient β by a multiplier 402 and fed to a summation module 404.

The I samples provided by the PDG 209 are multiplied by the correction coefficient α by a multiplier 403 and fed to the summation module 404.

The output of the summation module 404 is linked to a multiplexor 406 which is linked to an IQMC_ENABLE module 405. The IQMC_ENABLE module 405 is controlled by the processor 100.

The Q samples provided by the PDG 219 are provided to the multiplexor 406. The multiplexor 406 enables the transfer of the Q corrected samples or the Q samples provided by the PDG 219 for further processing.

By such configuration, it is possible to enable or disable the operation of the IQMC module 310 independently of the IQME module 300.

For example, in some embodiments, the IQME module 300 is disabled when the reception conditions are poor. As it will be disclosed hereinafter, correction coefficients determined by the IQME module may be stored in RAM memory 103.

The processor 100 may also disable the operation of the IQMC module 310. In that case, the Q samples provided by the PDG 219 are output by the multiplexor 406.

Fig. 5 schematically represents an example of architecture of an in-phase/quadrature-phase mismatch estimation module according to some embodiments of the invention.

The IQME module 300 comprises a sample level detection module (IQME-LD) module 500 which performs on the I and Q samples provided by the PDG 209 and 219 a sample to sample selection based on the values of the r I and Q samples. The IQME-LD module 500 will be disclosed in more details in reference to Fig. 6.

The selected I and Q samples are provided to an IQM correction module (IQME-C) 501. The IQME-C module 501 performs an IQM correction as disclosed in Fig. 4. The IQME-C module 501 is a duplication of the IQMC module 310.

According to some embodiments, that duplication enables to make IQM estimation and IQM correction fully independent and possibly asynchronous. It is of particular interest for example to perform an IQM correction in the foreground using IQMC module 310 with some predefined constant α and β values that can result from a former IQM estimation loaded from RAM memory 103 whereas an IQM estimation is run in the background, using IQME module 300. Once estimation is completed, the result may be used to configure the IQMC module 310 with updated α and β values. The duplication of the IQM correction within the IQME module 300 allows IQME module 300 to operate both in synchronous and asynchronous modes.

For example, in the synchronous mode, the IQMC module 310 is configured with an updated set of α and β coefficients values originating from IQME module 300 for each new received I and Q samples.

For example, in the asynchronous mode, the IQMC module 310 is configured independently from IQME module 300.

The I and Q corrected samples at the output of the IQME-C module 501 are provided both to an IQM gain loop estimation constituted by the modules 502 to 508, and to an IQM phase loop estimation constituted by the modules 509 to 513.

The module 502 takes the absolute value of the I sample provided by the IQME-C module 501 and the module 503 takes the absolute value of the Q corrected sample provided by the IQME-C module 501.

A subtraction module 504 computes the IQM gain error ε_g as the difference between the sample output by the module 502 and the one output by the module 503.

The IQM gain error ε_g output by subtraction module 504 is then weighted by a weighting module 505, the weight of which K_g , also referred to as IQM gain loop weight value, is variable as it will be disclosed hereinafter in Figs. 7.

The IQM gain weighted error ε_g output by the digital weighting module 505 is provided to an integrator 506.

For an input sample x(n) and an output sample y(n), the integrator 506 performs the following processing:

y(n) = y(n-1) + x(n), i.e. a basic accumulation or integration of the input samples.

The integrator 506 adds the current sample provided by the weighting module 505 to its internal state and outputs the integrated sample.

The absolute value of the integrated sample is taken by the module 507 and is delayed by a one sample delay noted 508 in order to obtain the IQM gain correction coefficient value β.

The coefficient value β may be transferred to the IQME-C module 501 and may also be transferred to the IQMC module 310 according to synchronous or asynchronous operation mode under use.

The multiplier 509 multiplies together I and Q selected samples provided by the IQME-C module 501.

The sample resulting from the multiplier 509 is the IQM phase error ε_p and is weighted by a weighting module 510, the weight of which K_p, also referred to as IQM phase loop weight value, is variable as it will be disclosed hereinafter in Fig. 7.

The sample output by the weighting module 510 is provided to an integrator 511. The integrator 511 adds the current sample provided by the weighting module 510 to its internal state and outputs the integrated sample, the IQM phase integrated weighted error signal.

The integrator 511 is identical to the integrator 506.

The sign of the integrated sample is changed by the multiplier 512 which multiplies the integrated sample by minus one. The sample provided by the multiplier 512 is delayed by a one sample delay noted 513 in order to obtain the IQM phase correction coefficient value α.

The coefficient value α is transferred to the IQME-C module 501 and may also be transferred to the IQMC module 310 according to synchronous or asynchronous operation mode under use.

It has to be noted here that, the loop constituted by the modules 502 to 508 and/or the loop constituted by the modules 509 to 513 may be used for other purposes than IQM estimation. For example, the loop constituted by the modules 502 to 508 may be used for Direct Current (DC) offset estimation. A more detailed example is given in reference to Fig. 12. The weight values used by the weighting modules 505 and 506 may also be variable within different sub-period durations in a same manner as the ones that will be disclosed hereinafter in Figs. 7. The weight values used by the weighting modules 505 and 510 during the sub-periods may also be defined in a same manner as the ones that will be disclosed hereinafter in Figs. 8 and/or 9.

Fig. 6 schematically represents an architecture of a sample level detection module according to some embodiments of the invention.

The sample level detection module (IQME-LD) 500 comprises two absolute value modules 600 and 610.

The module 600 takes the absolute value of the I sample provided by the PDG 209 and the module 610 takes the absolute value of the Q sample provided by the PDG 219.

The samples output by the modules 600 and 610 are provided to a maximum detection module (MAX) 601 which selects the maximum among the two samples provided by the modules 600 and 610.

The selected sample is fed to two comparison modules 603 and 605.

The comparison module 603 compares the selected sample to an high threshold value A_max and if the selected sample is greater than the high threshold value A_max, the comparison module 603 outputs a binary value one.

The comparison module 605 compares the selected sample to a low threshold value A_min, and if the selected sample is less than the low threshold A_min, the comparison module 605 outputs a binary value one.

The high threshold value A_max and the low threshold A_min value are stored in dedicated registers and may be modified anytime.

The binary values provided by the comparison modules 603 and 605 are fed to an OR gate 606, the output of which commands two multiplexors 607 and 608.

The I samples provided by the PDG 209 are provided to the multiplexor 607 and the Q samples provided by the PDG 219 are provided to the multiplexor 608.

When the output level of the OR gate 606 is equal to one, the multiplexor 607 enables the transfer of the I sample provided by the PDG 209 and the multiplexor 608 enables the transfer of the Q sample provided by the PDG 219.

When the output level of the OR gate 606 is equal to null value, the multiplexors 607 and 608 do not provide any sample since its value is considered as not reliable for further processing.

Thanks to the IQME-LD module 500, it is possible to reject samples having too low amplitude or too high amplitude. Such samples may delay the convergence of the gain and phase estimation loops of the IQME module 300.

Figs. 7a and 7b schematically represent some examples of loops weight values of the in-phase/quadrature-phase mismatch estimation module and/or of at least one loop weight value of a direct current offset correction which evolve in the time.

Fig. 7a schematically represents some examples of phase loop weight values of the IQME module 300 which evolve in the time.

Fig. 7b schematically represents some examples of gain loop weight values of the IQME module 300 which evolve in the time.

According to some embodiments of the invention, the weight value K_p respectively K_g of the phase respectively gain loop of the IQME module 300 evolves in the time.

K_p and K_g values are modified several times during the whole estimation duration. The time duration during which the loop weight value is kept constant is

referred to as sub-period. Thereby, the whole estimation is split into a series of successive sub-periods.

According to some embodiments of the invention, each sub-period may have a specific duration. For example, the sub-period duration may follow a geometrical series with a factor *F1* equal to either 1, 2, 4 or 8. A given sub-period of specific duration *D* is followed by a next sub-period whose duration is *F1* times longer.

In the same way, the loop weight values (K_p and *Kg*) for both IQM estimation loops also follow a geometrical series with a factor *F2* lower *than one*. For example *F2* is equal to 0.5 or 0.25. A given sub-period applying a couple $\{K_p , K_g\}$ as loop weight values is followed by a next sub-period for which the loop weight values $\{K_p.F2, K_g.F2\}$ are $\frac{1}{F2}$ times lower.

Furthermore, the loop weight values K_p and K_g depend on an AGC headroom parameter. The AGC controls at least the gain of the low-noise amplifier 203, the programmable analogue gain amplifiers 206 and 216 and the PDG 209 and 219.

AGC headroom parameter value is a common way to express the digital signal level value referred to ADC full scale level. AGC headroom parameter is defined as the difference in decibels (dB) between ADC full scale level expressed in dB and the targeted signal level at the output of the ADC expressed in dB.

AGC headroom value is a strictly positive value expressed in dB. For example, the AGC headroom is typically equal to 15 dB.

In the examples given in Figs. 7a and 7b, the IQM estimation total available time duration referred to as D_{tot} is divided into five sub-periods. It has to be noted the number of sub-periods may be lower or greater than five. The first sub-period 70 has a first duration, the second sub-period 71 has a second duration which is four times the first duration, the third sub-period 72 has a third duration which is four times the second duration, the fourth sub-period has a duration which is equal to four times the third sub duration and the fifth sub-period 74 has a duration which is four times the fourth duration and is equal to ¾ of D_{tot}.

In the examples given in Figs. 7a and 7b, the IQM estimation weight values K_{p0} for phase loop, K_{g0} for gain loop during the first sub-period 70 is equal to a predetermined value dependent on the AGC headroom value. The weight value K_{p1}, respectively K_{g1}, during the second sub-period 71 is equal to half the weight value K_{p0} ,respectively K_{g0}. The weight value K_{p2}, respectively K_{g2}, during the third sub-period 72 is equal to half the weight value K_{p1}, respectively K_{g1}. The weight value K_{p3},

respectively K_{g3}, during the fourth sub-period (not shown in Fig. 7a) is equal to half the weight value K_{p2}, respectively K_{g2}. The weight value K_{p4}, respectively K_{g4}, during the fifth sub-period 74 is equal to half the weight value K_{p3}, respectively K_{g3}.

Let M_p holding for IQM phase estimation loop and M_g for IQM gain estimation loop denote the product of the last, the fifth in the example of Figs. 7a and 7b, sub-period duration by the loop weight value K_{p4} respectively K_{g4} used during said last fifth sub-period.

The product of the fourth sub-period duration by the loop weight value K_{p3} used during said fourth sub-period is equal to $M_p/2$. The product of the third sub-period duration by the loop weight value K_{p2} used during said third sub-period is equal to $M_p/4$. The product of the second sub-period duration by the weight value K_{p1} used during said second sub-period of time is equal to $M_p/8$. The product of the first sub-period duration by the weight value K_{p0} used during said first sub-period of time is equal to $M_p/16$.

The product of the fourth sub-period duration by the loop weight value K_{g3} used during said fourth sub-period is equal to $M_g/2$. The product of the third sub-period duration by the loop weight value K_{g2} used during said third sub-period is equal to $M_g/4$. The product of the second sub-period duration by the weight value K_{g1} used during said second sub-period of time is equal to $M_g/8$. The product of the first sub-period duration by the weight value K_{g0} used during said first sub-period of time is equal to $M_g/16$.

According to some embodiments of the invention, at least one weight value K_d of a DC offset correction loop which will be disclosed hereinafter in reference to Fig. 12 evolves in the time. For example, the weight value K_d of a DC offset correction loop for the channel providing I sample. Another weight value $K_{d'}$ of a DC offset correction loop for the channel providing Q samples.

K_d value is modified several times during the whole estimation duration. The time duration during which the DC offset weight value is kept constant is referred to as sub-period. Thereby, the whole estimation is split into a series of successive sub-periods.

According to some embodiments of the invention, each sub-period may have a specific duration. For example, the sub-period duration may follow a geometrical series with a factor *F1* equal to either 1, 2, 4 or 8. A given sub-period of specific duration *D* is followed by a next sub-period whose duration is *F1* times longer.

In the same way, the weight values K_d also follows a geometrical series with a factor *F2* lower *than one*. For example *F2* is equal to 0.5 or 0.25. A given sub-period applying K_d as loop weight value is followed by a next sub-period for which the loop weight values $\{K_d . F2\}$ are $\frac{1}{F2}$ times lower.

In the examples given in Figs. 7a and 7b, the DC offset estimation total available time duration referred to as D_{tot} is divided into five sub-periods as already disclosed. It has to be noted that the number of sub-periods may be lower or greater than five. The first sub-period 70 has a first duration, the second sub-period 71 has a second duration which is four times the first duration, the third sub-period 72 has a third duration which is four times the second duration, the fourth sub-period has a duration which is equal to four times the third sub duration and the fifth sub-period 74 has a duration which is four times the fourth duration and is equal to ¾ of D_{tot}.

In the present examples, the weight value K_{d1} during the second sub-period 71 is equal to half the weight value K_{d0}. The weight value K_{d2}, during the third sub-period 72 is equal to half the weight value K_{d1}. The weight value K_{d3}, during the fourth sub-period is equal to half the weight value K_{d2}. The weight value K_{d4}, during the fifth sub-period 74, is equal to half the weight value K_{d3}.

Let M_p holding for IQM phase estimation loop and M_g for IQM gain estimation loop denote the product of the last, the fifth in the example of Figs. 7a and 7b, sub-period duration by the loop weight value K_{p4} respectively K_{g4} used during said last fifth sub-period.

The product of the fourth sub-period duration by the loop weight value K_{d3} used during said fourth sub-period is equal to $M_d/2$. The product of the third sub-period duration by the loop weight value K_{d2} used during said third sub-period is equal to $M_d/4$. The product of the second sub-period duration by the weight value K_{d1} used during said second sub-period of time is equal to $M_d/8$. The product of the first sub-period duration by the weight value K_{d0} used during said first sub-period of time is equal to $M_d/16$.

Fig. 8 represents an example of a table used for determining, according to an automatic gain controller headroom value, the weight values of both the phase and gain loops.

Fig. 8 consists in a table containing M_p and M_g example values according to the AGC headroom parameter value. M_p and M_g values enable to derive the series of suitable loop weight values for both IQM phase and gain estimation loops, as well as

the convenient application duration for each of them, knowing from the whole IQM estimation duration selected value (D_{tot}) and from the selected number of sub-periods. The table shown in Fig. 8 is, for example, stored in the RAM memory 103.

The column noted 80 shows different possible values expressed in dB that the AGC headroom value can take.

For a given AGC headroom value given in column 80, the column 81, respectively 82, indicates the recommended M_p, respectively M_g value to be used.

The period of time D_{tot} is equal to a predetermined value for example stored in RAM memory 103, the different successive loop weight values like K_{p0} to K_{p4}, K_{g0} to K_{g4} shown in Figs. 7a and 7b can be deduced respectively from M_p and M_g.

Fig. 9 exemplifies sub-period indexes and their respective durations, further to phase and gain loop values for in-phase/quadrature-phase mismatch estimation module assuming an auto gain controller headroom nominal value.

The table shown in Fig. 9 is, for example, stored in the RAM memory 103.

The AGC headroom nominal value is, for example, equal to 15dB.

The line noted 90 shows the series of successive sub-period indexes.

The line noted 91 shows the series of successive sub-period time duration, expressed in number of samples.

The line noted 92 respectively. 93 shows the series of loop weight values K_p, respectively K_g for IQM phase respectively gain estimation loop.

Fig. 10 represents an example of an algorithm for determining weight values of the phase and gain loops applied during different time periods according to some embodiments of the invention.

The present algorithm may be executed by the CPU 100 of the receiver 10. The present algorithm will be disclosed in an example and in a non limitative way, wherein it is executed by the processor 100.

At step S100, the CPU 100 checks if any condition regarding the analogue part of the receiving chain has changed.

Condition change may be a modification of any analogue gain among the low noise amplifier 203, the programmable analogue gain amplifier 206 or 216, or the programmable digital gain 207 or 219 and/or of a change of the frequency band in which radio signals are received.

If any condition regarding the analogue part of the receiving chain changes, the CPU 100 moves to step S101. Otherwise, the CPU 100 moves to step S106.

At step S101, CPU 100 stores the context of the IQME module 300 in the RAM memory 103. The context of the IQME module 300 is, for example, the current state of the integrator 511, the current state of the integrator 506, the current index of the sub-period and one bit value which indicates if the current context has already been used or not. The context is further associated with the values of the different gains of the low noise amplifier 203, of the programmable analogue gain amplifiers 206 and 216, of the programmable digital gains 207 and 217 and/or the frequency band in which radio signals are received prior the change of conditions detected at step S100.

The memory 103 stores the contexts for the different supported analogue gain combinations and/or the frequency band in which radio signals are received.

At next step S102, it is checked if there is, in the memory 103, a context which corresponds to the combination of gains and/or the frequency band used once the condition change is detected.

If there is a context which corresponds to the combination of gains and/or the frequency band in which radio signals are received used once the condition change is detected, the CPU 100 moves to step S105. Otherwise, the CPU 100 moves to step S103.

At step S105, the CPU read in the RAM memory 103 the context which corresponds to the combination of gains and/or the frequency band in which radio signals are received once the condition change is detected and sets the state of the integrator 511 to the value stored in the context, the state of the integrator 506 to the value stored in the context, applies the loop weights K_p and K_g which correspond to the index of the sub-period index stored in the context.

After that, the CPU 100 moves to step S106.

At step S103, the CPU 100 determines, using the table shown in Fig. 9 and the knowledge of the AGC headroom value, the values M_p and M_g.

At next step S104, the CPU 100 determines, using the values M_p and M_g, the values of K_{p0} to K_{p4} and K_{g0} to K_{g4}.

At next step S106, the CPU 100 starts a sub-period of time. If CPU 100 was previously at step S105, the sub-period to fully replay is the one which corresponds to the index of sub-period stored in the context read from the memory 103.

If CPU 100 was previously at step S100, the sub-period of time which corresponds to the following index of sub-period of time as the previous one index is incremented since a new sub-period is started.

If CPU 100 was previously at step S104, the sub-period is the first sub-period.

At next step S107, the CPU 100, when the following sub-period has to start, applies the values of K_p and K_g which correspond to the next sub-period.

At next step S108, the CPU 100 checks that all sub-periods have been successively performed.

If all the sub-periods have been performed, the CPU 100 moves to step S109. Otherwise, the CPU moves to step S100.

At step S109, the CPU 100 stores, in RAM memory 103, the context of the IQME module 300. The context of the IQME module 300 is for example the current state of the integrator 511, the current state of the integrator 506, the current sub-period index and one bit value which indicates if the context has already been used or not. The context is further associated with the values of the different gains of the analogue low noise amplifier 203, of the programmable analogue gain amplifiers 206 and 216, of the programmable digital gains 207 and 217 and/or the frequency band in which radio signals are received prior the change of conditions detected at step S100.

In some embodiments, one bit value which indicates if the context has already been used or not avoids glitch in the quality of the received radio signal when both IQM estimation and correction are enabled in synchronous mode.

In some embodiments, when a given analog context is visited for the first time, this information is available thanks to the one-bit value, integrator 506 and 511 states are not reset with some prescribed values but advantageously initialized with the most likely values copied from another context for which IQM estimation has already started for a certain and as long as possible, amount of time.

After that, the CPU 100 returns to step S100.

Fig. 11 represents an example of an algorithm for managing the operation of the in-phase/quadrature-phase mismatch correction module and/or of the in-phase/quadrature-phase mismatch estimation module according to some embodiments of the invention.

The present algorithm may be executed by the CPU 100 of the receiver 10. The present algorithm will be disclosed in an example and in a non limitative way, wherein it is executed by the processor 100.

At step S110, the CPU 100 checks if the IQMC module 310 and the IQME module 300 need to be activated.

If the IQMC module 310 and the IQME module 300 need to be activated, the CPU 100 moves to step S111. Otherwise, the CPU 100 moves to step S113.

At step S111, the CPU 100 activates the IQMC module 310 and the IQME module 300.

At next step S112, the CPU 100 commands the IQMCE_DRIVE module 307 which enables the transfer of the correction coefficients α and β determined by the IQME module 300 to the IQMC module 310.

After that, the CPU returns to step S110.

At step S113, the CPU 100 checks if the IQME module 300 needs to be activated.

If the IQME module 300 needs to be activated, the CPU 100 moves to step S114. Otherwise, the CPU 100 maintains or sets the IQME module 300 in a deactivated mode and moves to step S118.

At step S114, the CPU activates the IQME module 300.

At step S115, the CPU 100 checks if the IQMC module 310 needs to be activated.

If the IQMC module 310 needs to be activated, the CPU 100 moves to step S116. Otherwise, the CPU 100 maintains or sets the IQMC module 310 in a deactivated mode and moves to step S117.

At step S116, the CPU 100 commands the IQMCE_DRIVE module 307 which enables the transfer of the correction coefficients α and β determined by the IQME module 300 to the IQMC module 310.

After that, the CPU 100 returns to step S110.

At step S117, the different correction coefficients or contexts determined by the IQME module 300 may be stored in the RAM memory 103.

After that, the CPU 100 returns to step S110.

At step S118, the CPU 100 checks if the IQMC module 310 needs to be activated.

If the IQMC module 310 needs to be activated, the CPU 100 moves to step S119. Otherwise, the CPU 100 maintains or sets the IQMC module 310 in a deactivated mode and moves to step S110.

At step S119, the CPU 100 commands the IQMCE_DRIVE module 307 which enables the transfer of the correction coefficients α and β stored in the RAM memory 103 to the IQMC module 310.

After that, the CPU 100 returns to step S110.

Fig. 12 schematically represents an example of architecture of a receiving part including Direct Current Offset compensation loop according to some embodiments of the invention.

The receiving part of the wireless interface 105 comprises an analogue band pass filter 1202 which filters signal received by an antenna 1201 which is linked to the wireless interface 105 or included into the wireless interface 105.

The filtered signal is amplified by a low noise amplifier 1203. The gain of the low noise amplifier 1203 is set by an automatic gain controller (AGC) not shown in Fig. 12.

The output signal of the low noise amplifier 1203 is converted into baseband signal by a mixer 1204 for a channel providing I samples, the channel providing I samples being composed of subtracting means 1205, an analogue baseband filter 1206, a programmable analogue gain amplifier 1207, an analogue to digital converter (ADC) 1208, a decimator 1209 and a programmable digital gain (PDG) 1210.

It has to be noted here that the output signal of the low noise amplifier 1203 is converted into baseband signal by at a mixer 1214 witch multiplies signal provided by the low noise amplifier 1203 by $-sin(2\pi f_{LO}t)$ for a channel providing Q samples, not shown in Fig. 12. The channel providing Q may be identical to the channel providing I samples.

The mixer 1204, in order to provide the baseband signal of the received signal, multiplies the signal provided by the low noise amplifier 1203 by $cos(2\pi f_{LO}t)$ where f_{LO} is the local oscillator frequency of the receiver 10 and t is the time.

After conversion to baseband signal by the mixer 1204, a DC correction value determined according to the present invention is subtracted to the base band signal by subtraction means 1205. The signal provided by the subtraction means is filtered by the analogue baseband filter 1206, amplified by the programmable analogue gain amplifier 1207, digitally converted by the ADC 1208, the digital output samples of which are decimated by the decimator 1209 and the decimated samples are amplified by the (PDG) 1210.

The samples provided by the PGD 1210 are provided to circuitry, not shown in Fig. 12, for further processing and provided to a weighting module 1211, the weight of which K_d, also referred to as DC Offset loop weight value, is variable as it has been disclosed in Figs. 7.

The output of the digital weighting module 1211 is provided to an integrator 1212.

For an input sample x(n) and an output sample y(n), the integrator 1212 performs the following processing:

$y(n) = y(n-1) + x(n)$, i.e. a basic accumulation or integration of the input samples.

The integrator 1212 adds the current sample provided by the weighting module 1211 to its internal state and outputs the integrated sample.

The integrated sample is provided to the subtraction means 1205.

CLAIMS

1) A method for correcting and/or estimating an in-phase/quadrature-phase mismatch on a random received signal in a radio receiving device, said method causing the device to perform:

- processing the random received signal in order to obtain an in-phase component and a quadrature-phase component,
- amplifying by at least a first programmable gain amplifier and digitally converting by a first analogue to digital converter the in-phase component in order to obtain in-phase samples,
- amplifying by at least a second programmable gain amplifier and digitally converting by a second analogue to digital converter the quadrature-phase component in order to obtain quadrature-phase samples,
- correcting and/or estimating in-phase/quadrature-phase mismatch based on in-phase samples and quadrature-phase samples, the estimating of the in-phase/quadrature-phase mismatch being performed using two estimation loops, each loop generating a coefficient, a gain loop comprising a first weighting module which weights the difference of in-phase samples and of quadrature-phase samples and a phase loop comprising a second weighting module which weights the result of a multiplication of in-phase samples and of quadrature-phase samples, the correcting being performed on phase samples and/or quadrature-phase samples using coefficients provided by the loops.

2) Method according to claim 1, wherein in-phase/quadrature-phase samples used for correcting and/or estimating in-phase/quadrature-phase mismatch are selected according to the amplitude of in-phase and/or quadrature-phase samples.

3) Method according to claim 1 or 2, wherein the weight values of the first and second weighting modules are modified during plural sub-periods.

4) Method according to claim 3, wherein each sub-period duration is different from the other sub-period durations.

5) Method according to claim 3, wherein each sub-period duration is proportional to the duration of the previous sub-period, the proportionality being comprised between two and eight.

6) Method according to claim 5, wherein the proportionality is equal to four.

7) Method according to any of the claims 3 to 6, wherein during each sub-period, the weight value of the first weighting module is proportional to the weight value of the first weighting module during the previous sub-period.

8) Method according to any of the claims 3 to 7, wherein during each sub-period, the weight value of the second weighting module is proportional to the weight value of the second weighting module during the previous sub-period.

9) Method according to the claim 7 or 8, wherein the proportionality between weight values is equal to an half or a quarter.

10) Method according to any of the claims 3 to 9, wherein the weight values depend on the signal level target value at the input of at least one of the analogue to digital convertors, the signal level target value being controlled by an automatic gain controller.

11) Method according to any of the claims 1 to 10, wherein the phase loop further comprises a first integrator which integrates the samples provided by the first weighting module, the gain loop further comprises a second integrator which integrates the samples provided by the second weighting module, the method comprises further steps of :

- modifying the gain of the programmable gain amplifiers from a first value to a second value and/or a changing of a frequency band in which the random signal is received from a first frequency band to a second frequency band,,
- storing data which correspond to the first gain value and/or to the first frequency band,
- checking if there is stored data which correspond to the second gain value and/or to the second frequency band ,

- applying, if there is stored data which correspond to the second gain value and/or to the second frequency band for the integrators.

12) Method according to claim 11, wherein stored data which correspond to gain values and/or frequency bands are an information indicating in which sub-period modification is applied in combination with states of integrators .

13) Method according to any of the claims 1 to 12, wherein the correcting of the in-phase/quadrature-phase mismatch is performed on selected samples of the digitally converted in-phase component and the digitally converted quadrature-phase component using a first and a second coefficients, the first and second coefficients being provided by the estimate of the in-phase/quadrature -phase mismatch or from a memory.

14) Method according to any of the claims 1 to 13 wherein the method comprises further step of activating or deactivating the correcting and/or estimating of the in-phase/quadrature-phase mismatch.

15) An apparatus for correcting and/or estimating an in-phase/quadrature-phase mismatch on a random received signal in a radio receiving device, the apparatus comprising circuitry causing the apparatus to perform:

- processing the random received signal in order to obtain an in-phase component and a quadrature-phase component,
- amplifying by at least a first programmable gain amplifier and digitally converting by a first analogue to digital converter the in-phase component in order to obtain in-phase samples,
- amplifying by at least a second programmable gain amplifier and digitally converting by a second analogue to digital converter the quadrature-phase component in order to obtain quadrature-phase samples,
- correcting and/or estimating in-phase/quadrature-phase mismatch based on in-phase samples and quadrature-phase samples, the estimating of the in-phase/quadrature-phase mismatch being performed using two estimation loops, each loop generating a coefficient, a gain loop comprising a first weighting module which weights the difference of in-phase samples and of quadrature-phase samples and a

phase loop comprising a second weighting module which weights the result of a multiplication of in-phase samples and of quadrature-phase samples, the correcting being performed on phase samples and/or quadrature-phase samples using coefficients provided by the loops.

16) Apparatus according to claim 15, wherein in-phase/quadrature-phase samples used for correcting and/or estimating in-phase/quadrature-phase mismatch are selected according to the amplitude of in-phase and/or quadrature-phase samples.

17) Apparatus according to claim 15 or 16, wherein the weight values of the first and second weighting modules are modified during plural sub-periods.

18) Apparatus according to claim 17, wherein each sub-period duration is different from the other sub-period durations.

19) Apparatus according to claim 18, wherein each sub-period duration is proportional to the duration of the previous sub-period, the proportionality being comprised between two and eight.

20) Apparatus according to claim 19, wherein the proportionality is equal to four.

21) Apparatus according to any of the claims 17 to 20, wherein during each sub-period, the weight value of the first weighting module is proportional to the weight value of the first weighting module during the previous sub-period.

22) Apparatus according to any of the claims 17 to 21, wherein during each sub-period, the weight value of the second weighting module is proportional to the weight value of the second weighting module during the previous sub-period.

23) Apparatus according to the claim 21 or 22, wherein the proportionality between weight values is equal to an half or a quarter.

24) Apparatus according to any of the claims 17 to 23 wherein the weight values depend on the signal level target value at the input of at least one of the analogue to digital convertors, the signal level target value being controlled by an automatic gain controller.

25) Apparatus according to any of the claims 15 to 24, wherein the phase loop further comprises a first integrator which integrates the samples provided by the first weighting module, the gain loop further comprises a second integrator which integrates the samples provided by the second weighting module and the apparatus further comprising circuitry causing the apparatus to perform :

- modifying the gain of the programmable gain amplifiers from a first value to a second value and/or a changing of a frequency band in which the random signal is received from a first frequency band to a second frequency band,
- storing data which correspond to the first gain value and/or to the first frequency band,
- checking if there is stored data which correspond to the second gain value and/or to the second frequency band,
- applying, if there is stored data which correspond to the second gain value and/or to the second frequency band for the integrators.

26) Apparatus according to claim 25, wherein stored data which correspond to gain values and/or frequency bands are an information indicating in which sub-period modification is applied in combination with states of integrators.

27) Apparatus according to any of the claims 15 to 26, wherein the correcting of the in-phase/quadrature-phase mismatch is performed on selected samples of the digitally converted in-phase component and/or the digitally converted quadrature-phase component using a first and a second coefficients, the first and second coefficients being provided by the estimate of the in-phase/quadrature-phase mismatch or from a memory.

28) Apparatus according to any of the claims 15 to 27 wherein the correcting and/or estimating in-phase/quadrature-phase mismatch are decomposed into estimating the in-phase/quadrature-phase mismatch and correcting the in-

phase/quadrature-phase mismatch and the apparatus further comprising circuitry causing the apparatus to perform activating or deactivating the correcting in-phase/quadrature-phase mismatch and/or the estimating of the in-phase/quadrature-phase mismatch.

29) Apparatus according to claim 28, wherein the circuitry causing the apparatus to perform estimating of the in-phase/quadrature-phase mismatch comprises circuitry causing the apparatus to perform correcting in-phase/quadrature-phase mismatch.

30) Apparatus according to any of the claims 15 to 29, wherein the apparatus comprises a User Equipment or a Base Station.

31) Apparatus according to any of the claims 15 to30, wherein the apparatus is configured for use in a Long Term Evolution, Wideband Code Division Multiple Access or Global System for Mobile Communications system.

32) A radio access network system comprising an apparatus for correcting and/or estimating an in-phase/quadrature-phase mismatch on a random received signal in a radio receiving device, the apparatus comprising circuitry causing the apparatus to perform:

- processing the random received signal in order to obtain an in-phase component and a quadrature-phase component,
- amplifying by at least a first programmable gain amplifier and digitally converting by a first analogue to digital converter the in-phase component in order to obtain in-phase samples,
- amplifying by at least a second programmable gain amplifier and digitally converting by a second analogue to digital converter the quadrature-phase component in order to obtain quadrature-phase samples,
- correcting and/or estimating in-phase/quadrature-phase mismatch based on in-phase samples and quadrature-phase samples, the estimating of the in-phase/quadrature-phase mismatch being performed using two estimation loops, each loop generating a coefficient, a gain loop comprising a first weighting module which weights the difference of in-phase samples and of quadrature-phase samples and a phase loop comprising a second weighting module which weights the result of a

multiplication of in-phase samples and of quadrature-phase samples, the correcting being performed on phase samples and/or quadrature-phase samples using coefficients provided by the loops.

33/ A computer program comprising program code instructions for performing the method according to any one of claims 1 to 14.

34/ Information storage means which store a computer program comprising program code instructions which can be loaded in a programmable device for implementing the method according to any one of claims 1 to 14, when the program code instructions are run by the programmable device.

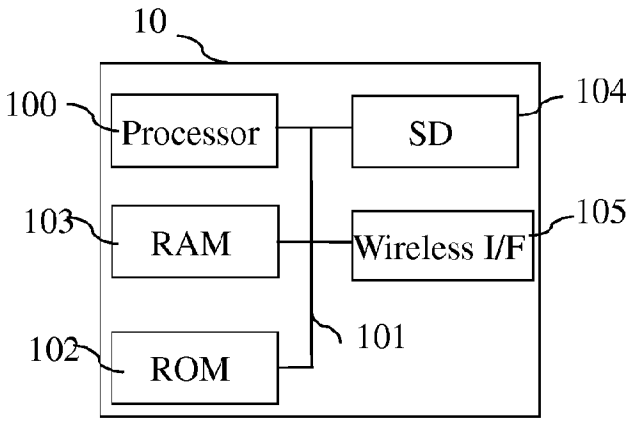
10
100
Processor
SD
104
103
RAM
Wireless I/F
105
101
102
ROM

Fig. 1

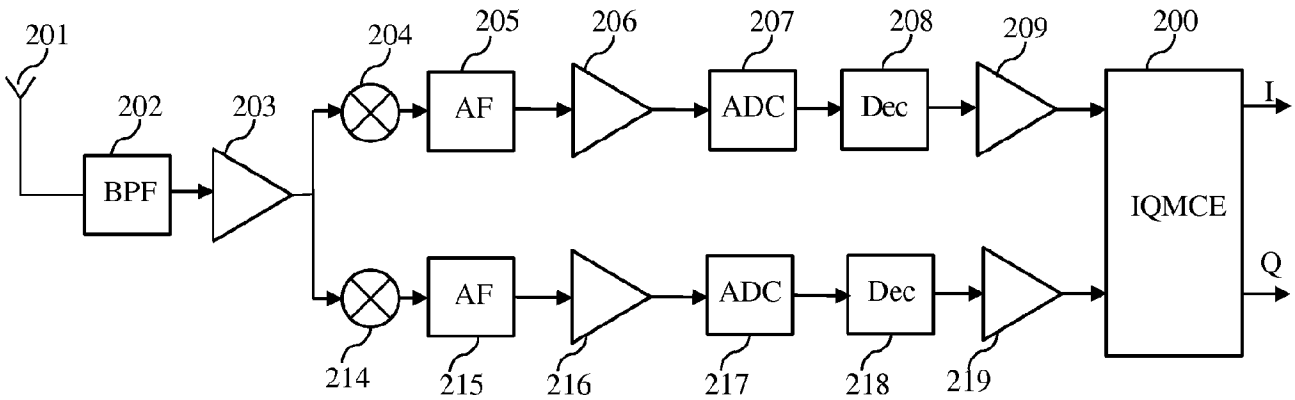
201
202
BPF
203
204
205
AF
206
207
ADC
208
Dec
209
200
IQMCE
I
Q
214
215
AF
216
217
ADC
218
Dec
219

Fig. 2

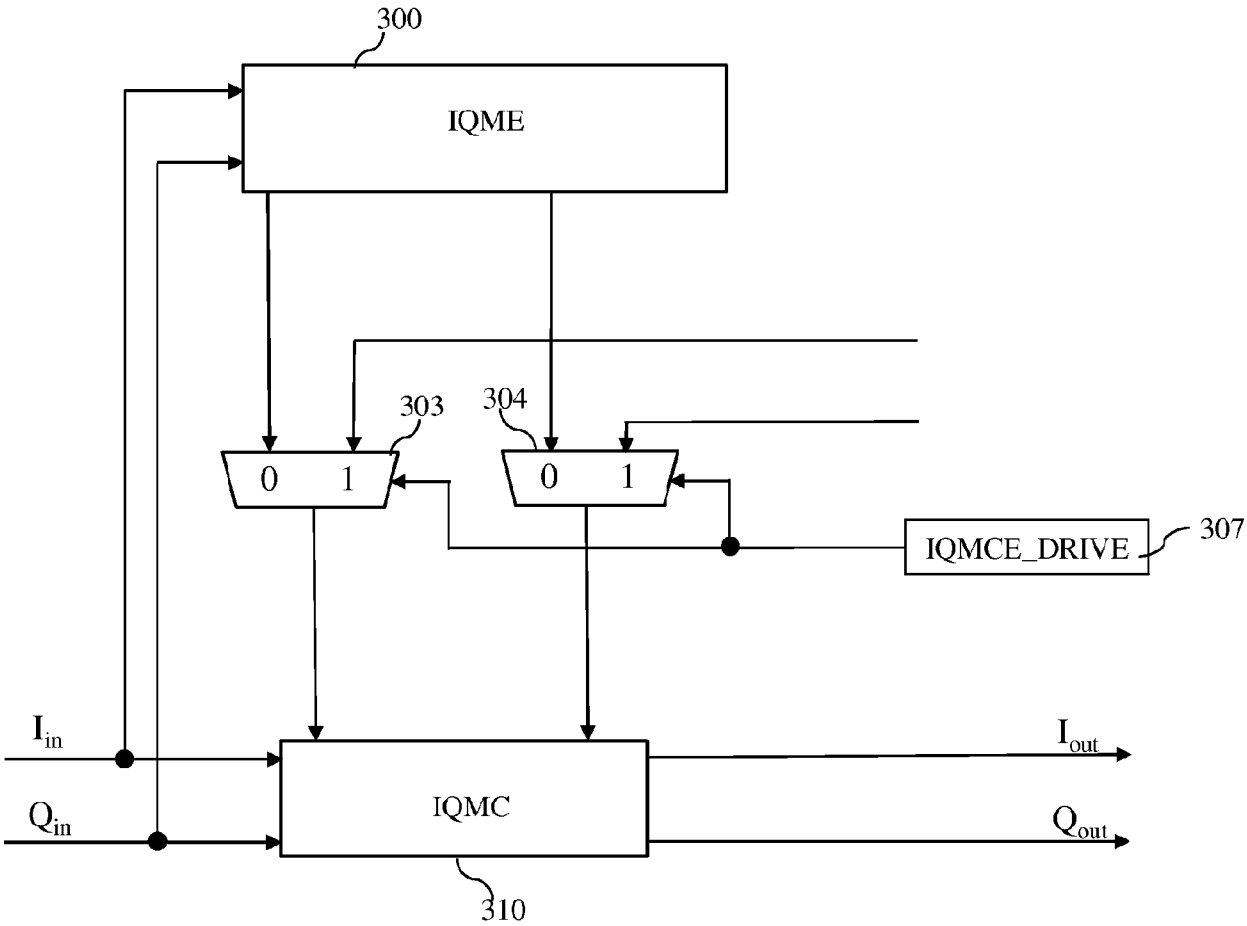
300
IQME
303
304
0
1
0
1
IQMCE_DRIVE
307
I_{in}
Q_{in}
IQMC
I_{out}
Q_{out}
310

Fig. 3

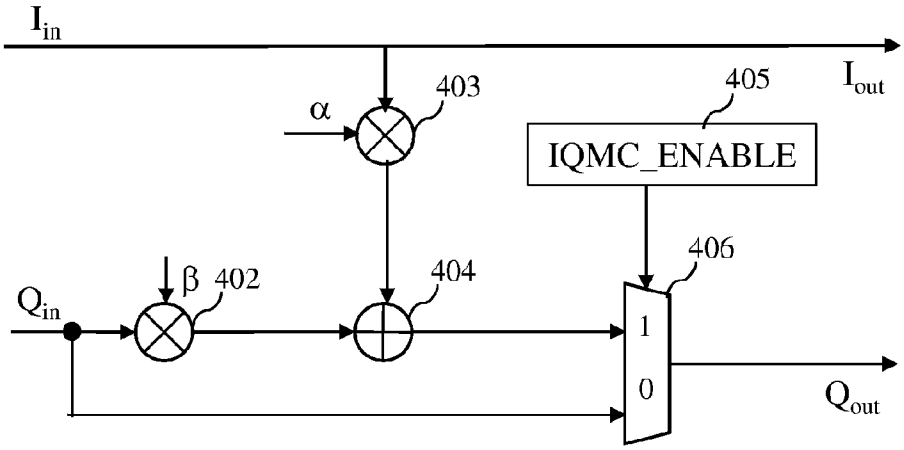
I_{in}
I_{out}
α
403
405
IQMC_ENABLE
406
β
402
404
Q_{in}
1
0
Q_{out}

Fig. 4

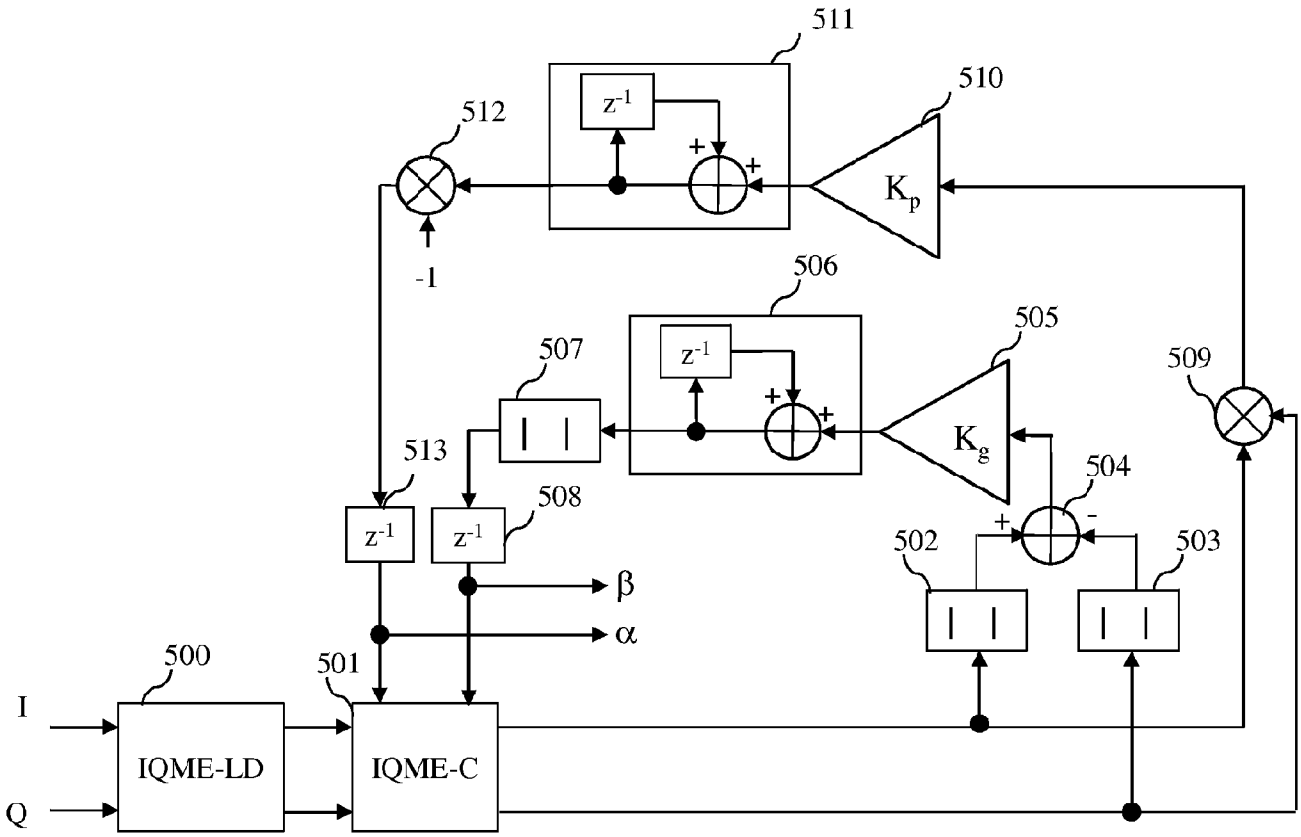
511
512
510
z^{-1}
K_p
-1
506
505
507
509
K_g
513
504
508
502
503
β
α
500
501
I
Q
IQME-LD
IQME-C

Fig. 5

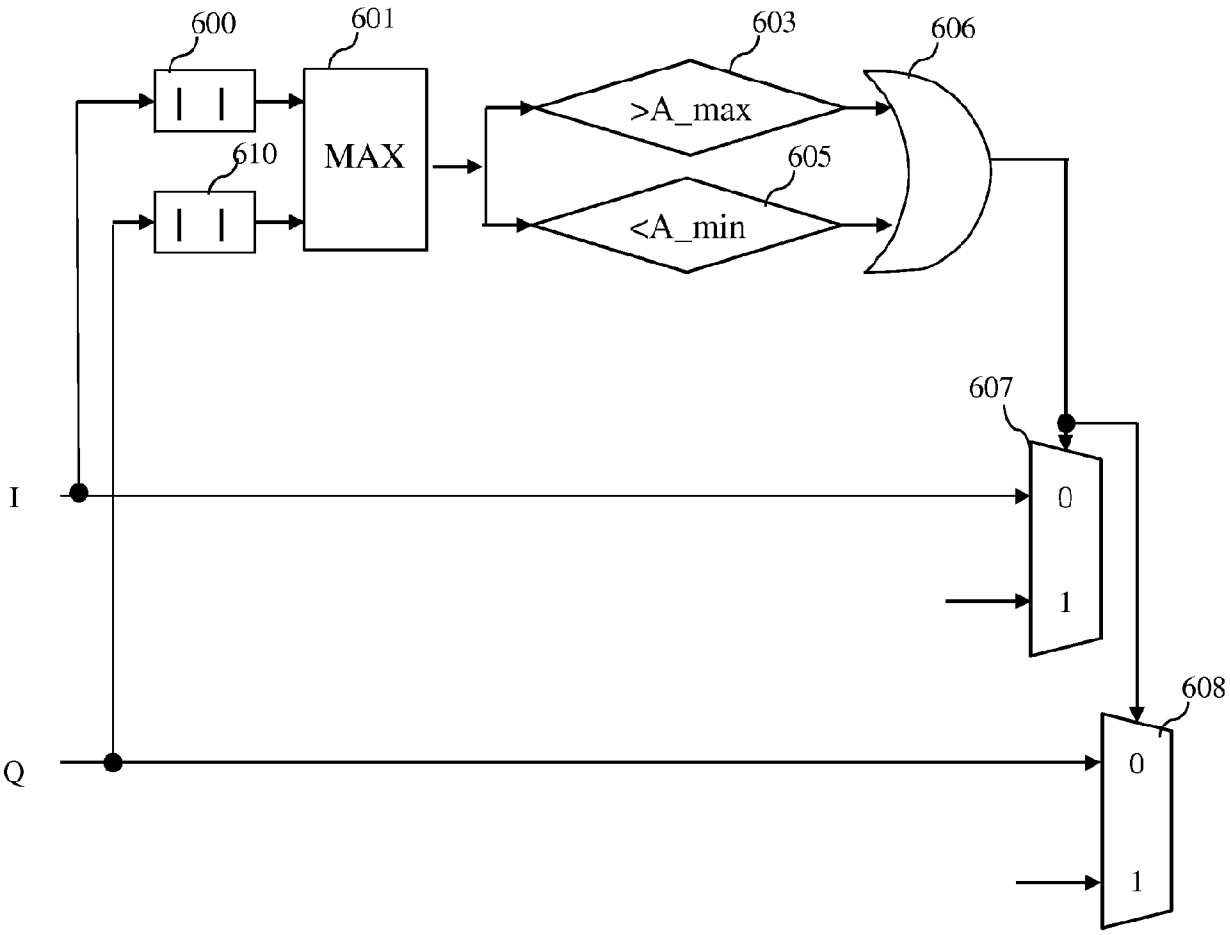

Fig. 6

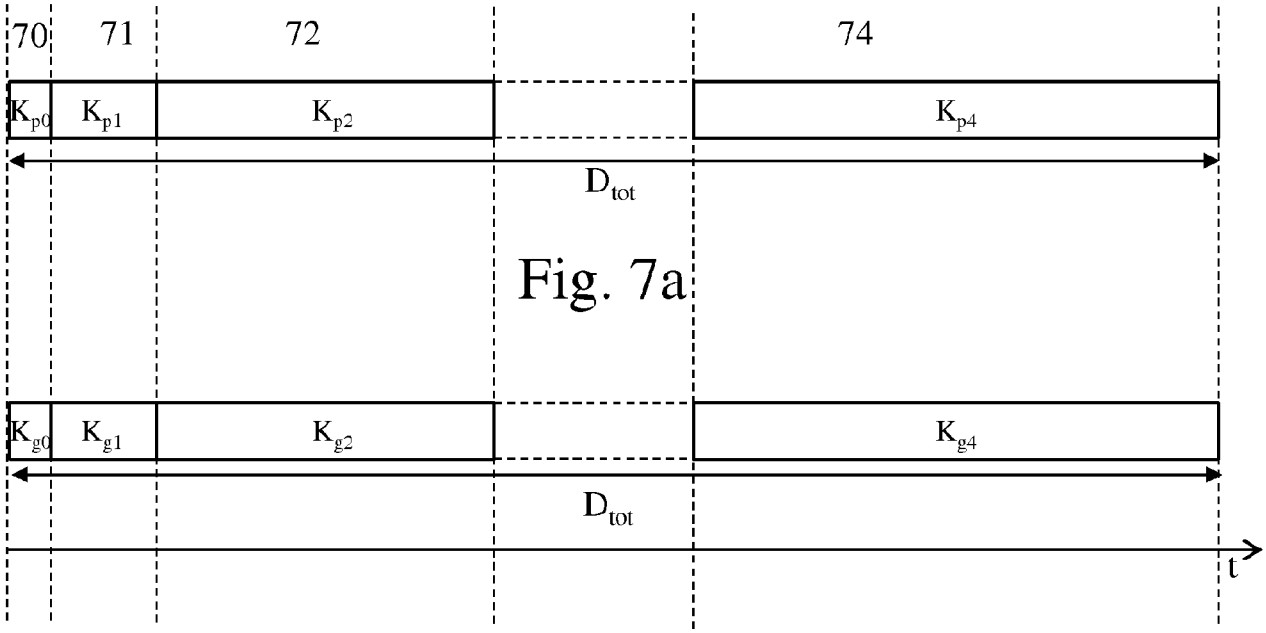

Fig. 7a

Fig. 7b

80	81	82
10.0	4.5	2.25
11.0	5.0	2.5
12.0	6.0	3.0
13.0	7.0	3.5
14.0	8.0	4.0
15.0	10.0	5.0
16.0	11.5	5.75
17.0	13.0	6.5
18.0	16.5	8.25
19.0	18.0	9.0
20.0	19.0	9.5

Fig. 8

90	0	1	2	3	4
91	160	640	2560	10240	40960
92	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}
93	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}

Fig. 9

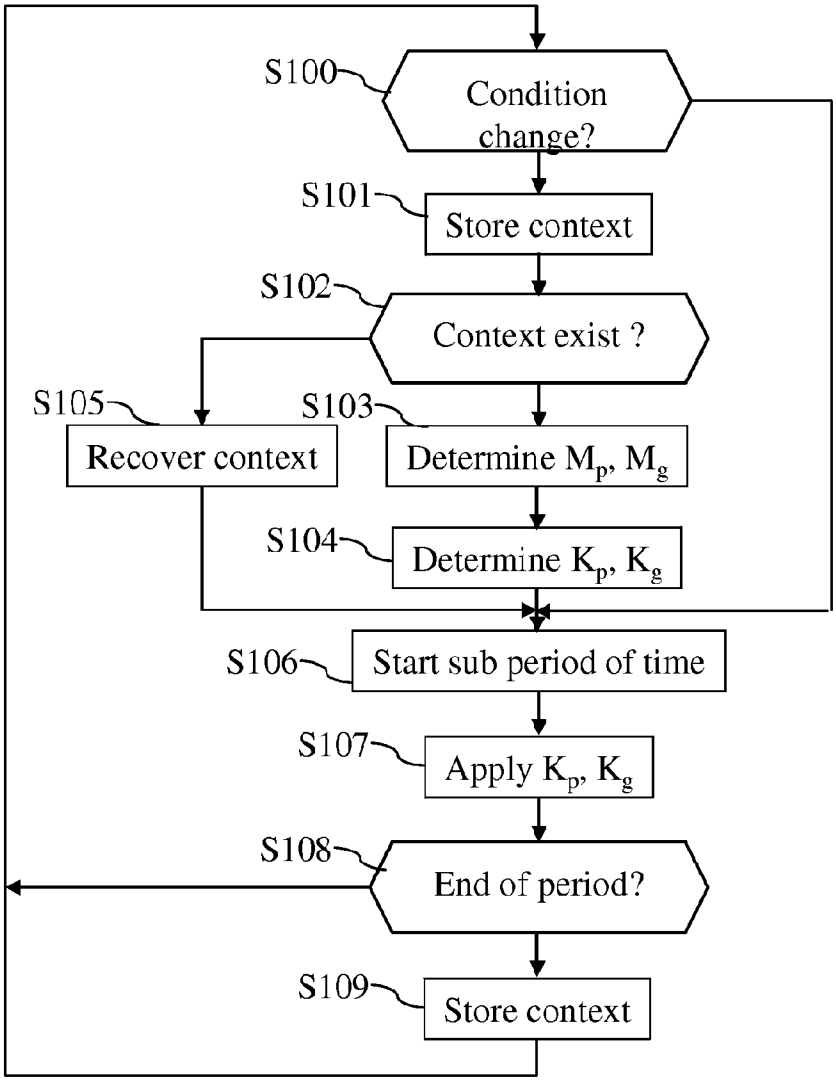
S100
Condition change?
S101
Store context
S102
Context exist ?
S105
Recover context
S103
Determine M_p, M_g
S104
Determine K_p, K_g
S106
Start sub period of time
S107
Apply K_p, K_g
S108
End of period?
S109
Store context

Fig. 10

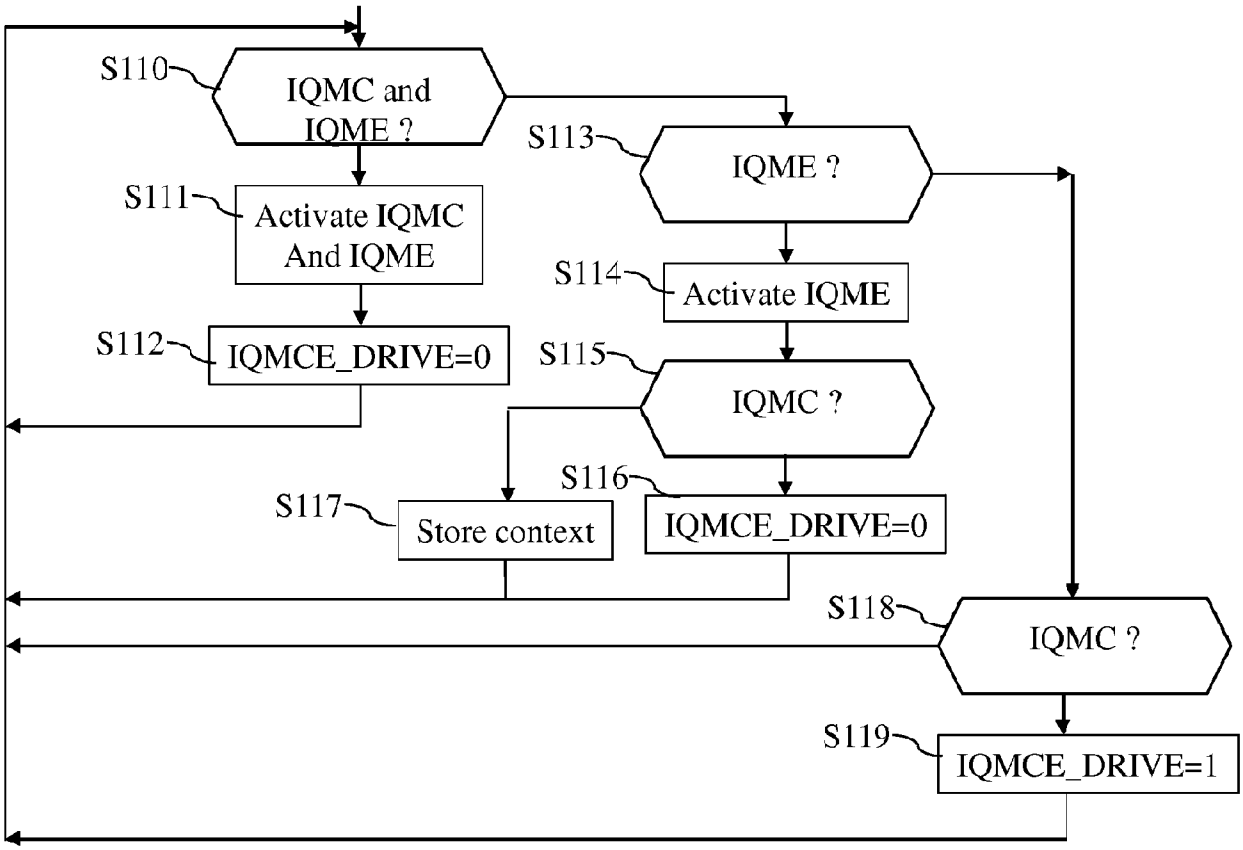
S110
IQMC and IQME ?
S111
Activate IQMC And IQME
S112
IQMCE_DRIVE=0
S113
IQME ?
S114
Activate IQME
S115
IQMC ?
S116
IQMCE_DRIVE=0
S117
Store context
S118
IQMC ?
S119
IQMCE_DRIVE=1

Fig. 11

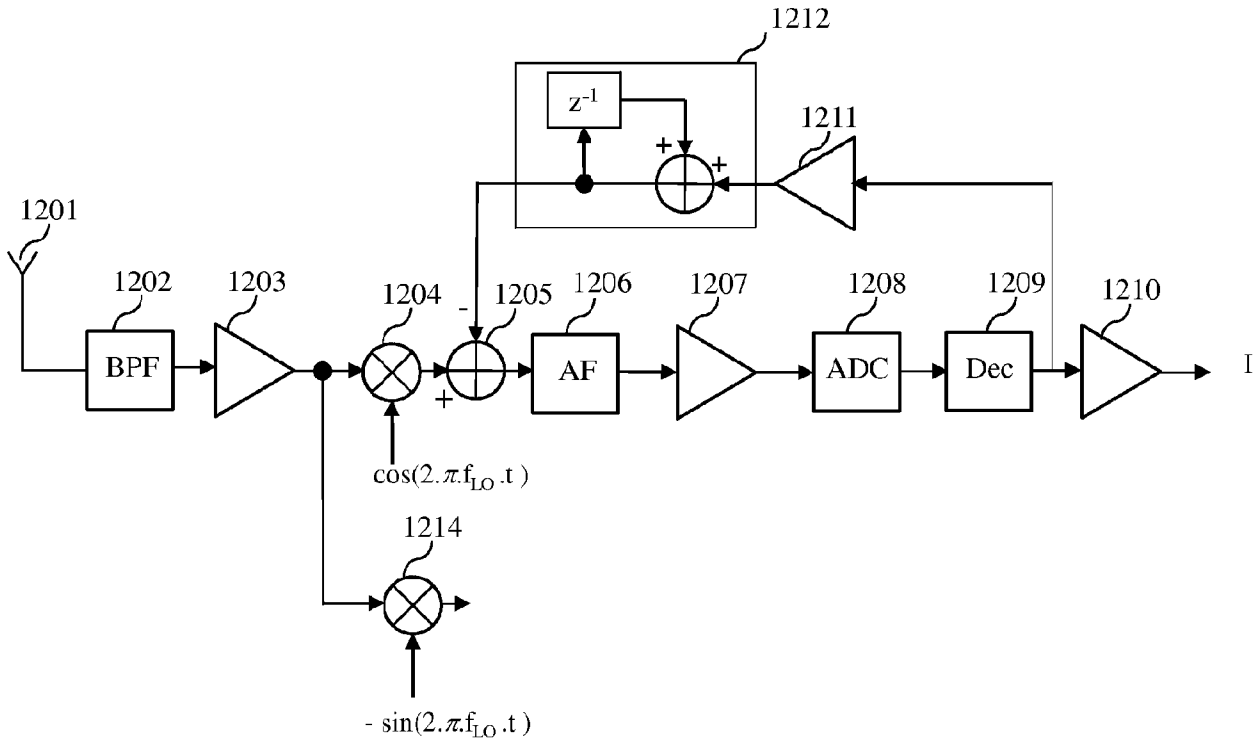
1212
z-1
1211
1201
1202
1203
1204
1205
1206
1207
1208
1209
1210
BPF
AF
ADC
Dec
I
cos(2.π.fLO.t)
1214
- sin(2.π.fLO.t)

Fig. 12

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2012/002870

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04L27/38 H04L27/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data, COMPENDEX, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	HARRIS F: "Digital filter equalization of analog gain and phase mismatch in I-Q receivers", 5TH IEEE INTERN ATIONAL CONFERENCE ON UNIVERSAL PERSONAL COMMUNICATIONS, vol. 2, 29 September 1996 (1996-09-29), - 2 October 1996 (1996-10-02), pages 793-796, XP010198531, NY, USA DOI: 10.1109/ICUPC.1996.562684 ISBN: 978-0-7803-3300-0 abstract page 793 - page 796 ----- -/--	1-34

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 August 2013	06/09/2013

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Dhibi, Youssef

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2012/002870

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012/270516 A1 (KANG YOUNG HWAN [KR] ET AL) 25 October 2012 (2012-10-25) abstract paragraph [0006] - paragraph [0012] paragraph [0029] - paragraph [0070] figures 2,3 -----	1-34

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2012/002870

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2012270516 A1	25-10-2012	JP 2012085302 A	26-04-2012
		KR 101127467 B1	12-07-2012
		US 2012270516 A1	25-10-2012