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(54) **Title:** PSEUDO-BYPASS MODE FOR POWER CONVERTERS

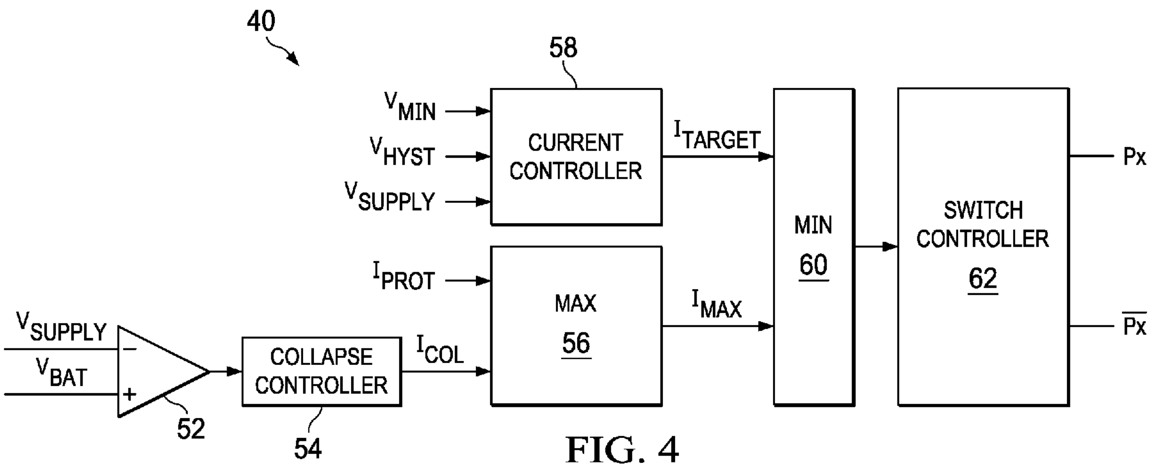

FIG. 4

(57) **Abstract:** A system may include a boost converter configured to receive an input voltage and boost the input voltage to an output voltage and control circuitry configured to enforce a maximum current limit to limit a current drawn by the boost converter and in response to the output voltage decreasing below the input voltage, dynamically increase the current above the maximum current limit to cause the output voltage to be approximately equal to the input voltage.

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PSEUDO-BYPASS MODE FOR POWER CONVERTERS

RELATED APPLICATION

The present disclosure claims priority to United States Provisional Patent Application Serial No. 63/236,739 filed August 25, 2021, which is incorporated by reference herein in its entirety.

FIELD OF DISCLOSURE

The present disclosure relates in general to circuits for electronic devices, including without limitation personal audio devices such as wireless telephones and media players, and more specifically, to implementation of a mode of operation of a power converter that regulates an output voltage generated by the power converter to an input voltage provided to the power converter.

BACKGROUND

Personal audio devices, including wireless telephones, such as mobile/cellular telephones, cordless telephones, mp3 players, and other consumer audio devices, are in widespread use. Such personal audio devices may include circuitry for driving a pair of headphones or one or more speakers. Such circuitry often includes a speaker driver including a power amplifier for driving an audio output signal to headphones or speakers. Oftentimes, a power converter may be used to provide a supply voltage to a power amplifier in order to amplify a signal driven to speakers, headphones, or other transducers. A switching power converter is a type of electronic circuit that converts a source of power from one direct current (DC) voltage level to another DC voltage level. Examples of such switching DC-DC converters include but are not limited to a boost converter, a buck converter, a buck-boost converter, an inverting buck-boost converter, and other types of switching DC-DC converters. Thus, using a power converter, a DC voltage such as that provided by a battery may be converted to another DC voltage used to power the power amplifier. A power converter may be used to provide supply voltage rails to one or more components in a device. A power converter may also be used in other applications besides driving audio transducers, such as driving haptic actuators or other electrical or electronic loads.

An output voltage generated by a boost converter may droop below its set point under current-limited constraints that may be placed on the boost converter. A system (e.g., mobile device) comprising such a boost converter may require the output voltage generated by the boost converter to not fall below an input voltage to the boost converter which is referred to herein as "a collapse condition." Typically, such requirement may be accomplished by closing a switch between the input voltage and output voltage during collapse conditions, resulting in a state transition between a regulation mode in which the boost converter regulates the output voltage and a bypass mode. However, such a state transition may add design complexity and have other disadvantages.

SUMMARY

In accordance with the teachings of the present disclosure, one or more disadvantages and problems associated with existing approaches to regulating an output voltage of a power converter may be reduced or eliminated.

In accordance with embodiments of the present disclosure, a system may include a boost converter configured to receive an input voltage and boost the input voltage to an output voltage and control circuitry configured to enforce a maximum current limit to limit a current drawn by the boost converter and in response to the output voltage decreasing below the input voltage, dynamically increase the current above the maximum current limit to cause the output voltage to be approximately equal to the input voltage.

In accordance with these and other embodiments of the present disclosure, a method may include enforcing a maximum current limit to limit a current drawn by a boost converter configured to receive an input voltage and boost the input voltage to an output voltage and in response to the output voltage decreasing below the input voltage, dynamically increasing the current above the maximum current limit to cause the output voltage to be approximately equal to the input voltage.

Technical advantages of the present disclosure may be readily apparent to one skilled in the art from the figures, description and claims included herein. The objects and advantages of the embodiments will be realized and achieved at least by the elements, features, and combinations particularly pointed out in the claims.

It is to be understood that both the foregoing general description and the following detailed description are examples and explanatory and are not restrictive of the claims set forth in this disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present embodiments and advantages thereof may be acquired by referring to the following description taken in conjunction with the accompanying drawings, in which like reference numbers indicate like features, and wherein:

FIGURE 1 illustrates an example mobile device, in accordance with embodiments of the present disclosure;

FIGURE 2 illustrates a block diagram of selected components internal to a mobile device, in accordance with embodiments of the present disclosure;

FIGURE 3A illustrates a block diagram of selected components of an example boost converter with multiple modes of operation depicting operation in a bypass mode, in accordance with embodiments of the present disclosure;

FIGURE 3B illustrates a block diagram of selected components of an example boost converter with multiple modes of operation depicting operation in a boost active mode, in accordance with embodiments of the present disclosure;

FIGURE 3C illustrates a block diagram of selected components of an example boost converter with multiple modes of operation depicting operation in a boost inactive mode, in accordance with embodiments of the present disclosure;

FIGURE 4 illustrates a block diagram of selected components of an example control circuit for a boost converter, in accordance with embodiments of the present disclosure;

FIGURE 5 depicts an example state machine that may be implemented by portions of the control circuit for the boost converter, in accordance with embodiments of the present disclosure; and

FIGURE 6 illustrates a graph depicting increase in a maximum current versus time in an attack state, in accordance with embodiments of the present disclosure.

DETAILED DESCRIPTION

FIGURE 1 illustrates an example mobile device 1, in accordance with embodiments of the present disclosure. FIGURE 1 depicts mobile device 1 coupled to a headset 3 in the form of a pair of earbud speakers 8A and 8B. Headset 3 depicted in FIGURE 1 is merely an example, and it is understood that mobile device 1 may be used in connection with a variety of audio transducers, including without limitation, headphones, earbuds, in-ear earphones, and external speakers. A plug 4 may provide for connection of headset 3 to an electrical terminal of mobile device 1. Mobile device 1 may provide a display to a user and receive user input using a touch screen 2, or alternatively, a standard liquid crystal display (LCD) may be combined with various buttons, sliders, and/or dials disposed on the face and/or sides of mobile device 1.

FIGURE 2 illustrates a block diagram of selected components integral to mobile device 1, in accordance with embodiments of the present disclosure. As shown in FIGURE 2, mobile device 1 may include a boost converter 20 configured to boost a battery voltage V_{BAT} to generate a supply voltage V_{SUPPLY} to a plurality of downstream components 18 of mobile device 1. Downstream components 18 of mobile device 1 may include any suitable functional circuits or devices of mobile device 1, including without limitation processors, audio coder/decoders, amplifiers, display devices, etc. As shown in FIGURE 2, mobile device 1 may also include a battery charger 16 for recharging battery 22.

In some embodiments of mobile device 1, boost converter 20 and battery charger 16 may comprise the only components of mobile device 1 electrically coupled to battery 22, and boost converter 20 may electrically interface between battery 22 and all downstream components of mobile device 1. However, in other embodiments of mobile device 1, some downstream components 18 may electrically couple directly to battery 22.

FIGURE 3A illustrates a block diagram of selected components of an example boost converter 20 with multiple modes of operation depicting operation in a bypass mode, in accordance with embodiments of the present disclosure. As shown in FIGURE 3A, boost converter 20 may include a battery 22, a plurality of inductive boost phases 24, a sense capacitor 26, a sense resistor 28, a bypass switch 30, and a control circuit 40. As shown in FIGURE 3A, each inductive boost phase 24 may include a power inductor 32, a charge switch 34, a rectification switch 36, and output capacitor 38.

Although FIGURES 3A-3C depict boost converter 20 having three inductive boost phases 24, embodiments of boost converter 20 may have any suitable number of inductive boost phases 24. In some embodiments, boost converter 20 may comprise three or more inductive boost phases 24. In other embodiments, boost converter 20 may comprise fewer than three phases (e.g., a single phase or two phases).

Boost converter 20 may operate in the bypass mode when supply voltage V_{SUPPLY} generated by boost converter 20 is greater than a threshold minimum voltage V_{MIN} and a voltage VDD_SENSE across sense capacitor 26 is greater than supply voltage V_{SUPPLY}. In some embodiments, such threshold minimum voltage V_{MIN} may be a function of a monitored current (e.g., a current through sense resistor 28). In some embodiments, such threshold minimum voltage V_{MIN} may be varied in accordance with variations in the monitored current, in order to provide desired headroom from components supplied from supply voltage V_{SUPPLY}. Thus, control circuit 40 may be configured to sense supply voltage V_{SUPPLY} and compare supply voltage V_{SUPPLY} to threshold minimum voltage V_{MIN}, as well as sense voltage VDD_SENSE and compare supply voltage V_{SUPPLY} to voltage VDD_SENSE. In the event that supply voltage V_{SUPPLY} is greater than threshold minimum voltage V_{MIN} and VDD_SENSE across sense capacitor 26 is greater than supply voltage V_{SUPPLY}, control circuit 40 may activate (e.g., enable, close, turn on) bypass switch 30 and one or more rectification switches 36 and deactivate (e.g., disable, open, turn off) charge switches 34. In such bypass mode, the resistances of rectification switches 36, power inductors 32, and bypass switch 30 may combine to minimize a total effective resistance of a path between battery 22 and supply voltage V_{SUPPLY}. In some embodiments, bypass switch 30 may not be present, and the bypass mode may be accomplished by activating one or more rectification switches 36 and deactivating charge switches 34.

FIGURE 3B illustrates a block diagram of selected components of example boost converter 20 depicting operation in a boost active mode, in accordance with embodiments of the present disclosure. In the boost active mode, control circuit 40 may deactivate (e.g., disable, open, turn off) bypass switch 30, and periodically commutate charge switches 34 (e.g., during a charging state of an inductive boost phase 24) and rectification switches 36 (e.g., during a transfer state of an inductive boost phase 24) of inductive boost phase 24 (as described in greater detail below) by generating appropriate control signals P_1, $\overline{P_1}$, P_2, $\overline{P_2}$, P_3, and $\overline{P_3}$, to deliver a current I_{BAT} and boost battery voltage V_{BAT} to a higher supply voltage V_{SUPPLY} in order to provide a programmed (or servoed) desired current (e.g., average current) to the electrical node of supply voltage V_{SUPPLY}, while maintaining supply voltage V_{SUPPLY} above threshold minimum voltage V_{MIN}. For example, control circuit 40 may operate in the boost active mode to maintain an inductor current I_L (e.g., I_{L1}, I_{L2}, I_{L3}) between a peak current and a valley current as described in U.S. Patent Application Serial No. 17/119,517 filed December 11, 2020 (the "'517 Application"), and incorporated by reference herein in its entirety. In the boost active mode, control circuit 40 may operate boost converter 20 by operating inductive boost phase 24 in a peak and valley detect operation, as described in greater detail below. The resulting switching frequency of charge switches 34 and rectification switches 36 of inductive boost phase 24 may be determined by the sense voltage VDD_SENSE, supply voltage V_{SUPPLY}, an inductance of power inductor 32A, and a programmed ripple parameter (e.g., a configuration of a target current ripple for an inductor current I_L).

FIGURE 3C illustrates a block diagram of selected components of boost converter 20 depicting operation in a boost inactive mode, in accordance with embodiments of the present disclosure. Boost converter 20 may operate in the boost inactive mode when supply voltage V_{SUPPLY} generated by boost converter 20 rises above hysteresis voltage V_{HYST} and a sense voltage VDD_SENSE remains below supply voltage V_{SUPPLY}. In the boost inactive mode, control circuit 40 may deactivate (e.g., disable, open, turn off) bypass switch 30, charge switches 34, and rectification switches 36. Thus, when sense voltage VDD_SENSE remains below supply voltage V_{SUPPLY}, control circuit 40 prevents boost converter 20 from entering the bypass mode in order to not backpower battery 22 from supply voltage V_{SUPPLY}. Further, if supply voltage V_{SUPPLY} should fall below threshold minimum voltage V_{MIN}, control circuit 40 may cause boost converter 20 to again enter the boost active mode in order to maintain supply voltage V_{SUPPLY} between threshold minimum voltage V_{MIN} and hysteresis voltage V_{HYST}.

Accordingly, via operation in the above-described modes, boost converter 20 may operate to provide hysteretic regulation of supply voltage V_{SUPPLY} between threshold minimum voltage V_{MIN} and a hysteresis voltage V_{HYST}.

It is understood that in some embodiments of the present disclosure, bypass switch 30 may be absent from boost converter 20. Accordingly, as described in greater detail below, in addition to or in lieu of the bypass function provided by bypass switch 30, boost converter 20 may be configured to regulate supply voltage V_{SUPPLY} at approximately battery voltage V_{BAT} during a voltage collapse condition that may exist at supply voltage V_{SUPPLY} as a result of current limiting of boost converter 20.

As described in U.S. Pat. Application Ser. No. 17/237,373 filed April 22, 2021 (the "'373 Application"), and incorporated by reference herein, one or more constraints may be placed on operation of a power converter which may place one or more limits on current that may be drawn from a battery by a power converter. In some instances, such current limits as applied to boost converter 20 may lead to a collapse condition, in which supply voltage V_{SUPPLY} falls to battery voltage V_{BAT}, and thus power converter 20 is not able to regulate supply voltage V_{SUPPLY}. As described in the Background section, in traditional approaches, control circuit 40 may activate bypass switch 30 (and/or one or more of rectification switches 36) to bypass battery voltage V_{BAT} to supply voltage V_{SUPPLY} as a result of current limiting of boost converter 20. However, in accordance with the present disclosure, boost converter 20 may be configured to regulate supply voltage V_{SUPPLY} approximately equal to battery voltage V_{BAT} in the event of a collapse condition.

FIGURE 4 illustrates a block diagram of selected components of example control circuit 40, in accordance with embodiments of the present disclosure. As shown in FIGURE 4, control circuit 40 may include a comparator 52, collapse controller 54, a maximum block 56, a current controller 58, a minimum block 60, and a switch controller 62.

Comparator 52 may be configured to compare supply voltage V_{SUPPLY} to battery voltage V_{BAT}, in order to control operation of collapse controller 54. For example, if supply voltage V_{SUPPLY} is greater than battery voltage V_{BAT}, comparator 52 may cause collapse controller 54 to operate in a release mode in which it decreases a collapse condition current I_{COL}. On the other hand, if supply voltage V_{SUPPLY} is lesser than battery voltage V_{BAT}, comparator 52 may cause collapse controller 54 to operate in an attack mode in which it increases collapse condition current I_{COL}

Maximum block 56 may select the maximum of a protection current I_{PROT} and collapse condition current I_{COL} to generate a maximum current I_{MAX} communicated to minimum block 60. Protection current I_{PROT} may represent a maximum current that can be drawn by boost converter 20 in order to satisfy any battery protection constraints and/or other protection constraints, for example as described in the '373 Application. Thus, in the presence of a collapse condition, collapse controller 54 in conjunction with maximum block 56 may temporarily override such protection current I_{PROT} in order to regulate supply voltage V_{SUPPLY}.

Current controller 58 may, based on supply voltage V_{SUPPLY}, threshold minimum voltage V_{MIN}, hysteresis voltage V_{HYST}, and/or any other suitable parameters, determine a target current I_{TARGET} to be drawn by boost converter 20 in order to regulate supply voltage V_{SUPPLY} at a desired voltage level. The determination of such target current based on supply voltage V_{SUPPLY} is beyond the scope of this disclosure, but may be determined in any suitable manner, including without limitation an approach that determines a target average current as described in the '517 Application.

Minimum block 60 may select the minimum of target current I_{TARGET} and maximum current I_{MAX} and communicate the result to switch controller 62. Based on the current value received, switch controller 62 may generate appropriate control signals P_1, $\overline{P_1}$, P_2, $\overline{P_2}$, P_3, and $\overline{P_3}$ to commutate switches 34 and 36 of boost converter 20 in order to draw such target current I_{TARGET}.

In operation, functionality of collapse controller 54 may be integrated with maximum block 56 to implement a state machine in order to generate maximum current I_{MAX}. As noted above, maximum current I_{MAX} may be based on protection current I_{PROT} for satisfying battery protection constraints and the output of comparator 52. When not in a collapse condition, maximum current I_{MAX} may equal protection current I_{PROT}. On the other hand, when in a collapse condition, maximum current I_{MAX} may exceed protection current I_{PROT}.

FIGURE 5 depicts an example state machine 70 that may be implemented by collapse controller 54 and maximum block 56, in accordance with embodiments of the present disclosure. As shown in FIGURE 5, state machine 70 may include four states: an idle state 72, an attack state 74, a release state 76, and a slow release state 78. Slow release state 78 is shown in dashed lines as such state may not be present in some embodiments of state machine 70.

In idle state 72, maximum current I_{MAX} may equal protection current I_{PROT}. From idle state 72, state machine 70 may transition to attack state 74 in response to battery voltage V_{BAT} exceeding supply voltage V_{SUPPLY} and supply voltage V_{SUPPLY} falling below a minimum acceptable regulation voltage V_{UV} (which may be equal to or below threshold minimum voltage V_{MIN} described above).

Collapse controller 54 may cause maximum current I_{MAX} to continually increase while in attack state 74. From attack state 74, state machine 70 may transition back to idle state 72 in response to maximum current I_{MAX} falling below protection current I_{PROT} and battery voltage V_{BAT} falling below supply voltage V_{SUPPLY}. In addition, from attack state 74, state machine 70 may transition to release state 76 in response to supply voltage V_{SUPPLY} exceeding battery voltage V_{BAT} and supply voltage V_{SUPPLY} remaining below minimum acceptable regulation voltage V_{UV}. Further, from attack state 74, state machine 70 may transition to slow release state 78 in response to supply voltage V_{SUPPLY} exceeding minimum acceptable regulation voltage V_{UV}.

Collapse controller 54 may cause maximum current I_{MAX} to continually decrease while in release state 76. From release state 76, state machine 70 may transition back to idle state 72 in response to maximum current I_{MAX} falling below protection current I_{PROT}. In addition, from release state 76, state machine 70 may transition back to attack state 74 in response to battery voltage V_{BAT} exceeding supply voltage V_{SUPPLY} and supply voltage V_{SUPPLY} remaining below minimum acceptable regulation voltage V_{UV}. Further, from release state 76, state machine 70 may transition to slow release state 78 in response to battery voltage V_{BAT} exceeding supply voltage V_{SUPPLY} and supply voltage V_{SUPPLY} rising above minimum acceptable regulation voltage V_{UV}.

Slow release state 78 may only be present in embodiments in which boost converter 20 has a dedicated bypass switch 30 which may be activated when supply voltage V_{SUPPLY} equals battery voltage V_{BAT} and supply voltage V_{SUPPLY} is above minimum acceptable regulation voltage V_{UV}. If collapse controller 54 is engaged (e.g., $I_{MAX} > I_{PROT}$) and supply voltage V_{SUPPLY} is above minimum acceptable regulation voltage V_{UV}, the control loop implemented by collapse controller 54 may be required to gracefully avoid adverse interaction with bypass switch 30. Such adverse interaction may be achieved by maximum current I_{MAX} continually decreasing while in slow release state 78, but at a rate which may be slower than the decrease in maximum current I_{MAX} occurring in release state 76.

In slow release state 78, collapse controller 54 may decrease maximum current I_{MAX} at a programmable rate slower than the rate of decrease in release state 76, which may reduce chattering of supply voltage V_{SUPPLY} near the boundary of minimum acceptable regulation voltage V_{UV}.

From slow release state 78, state machine 70 may transition back to idle state 72 in response to maximum current I_{MAX} falling below protection current I_{PROT}. In addition, from slow release state 78, state machine 70 may transition back to attack state 74 in response to battery voltage V_{BAT} exceeding supply voltage V_{SUPPLY} and supply voltage V_{SUPPLY} falling below minimum acceptable regulation voltage V_{UV}. Further, from slow release state 78, state machine 70 may transition to release state 76 in response to supply voltage V_{SUPPLY} exceeding battery voltage V_{BAT} and supply voltage V_{SUPPLY} falling below minimum acceptable regulation voltage V_{UV}.

Notably, minimum acceptable regulation voltage V_{UV} may only be relevant in state machine 70 in embodiments in which dedicated bypass switch 30 is present. Accordingly, in embodiments in which dedicated bypass switch 30 is absent and state machine 70 does not include slow release state 78, the comparisons to minimum acceptable regulation voltage V_{UV} shown in FIGURE 5 may be ignored.

When entering attack state 74, collapse controller 54 may continually increase maximum current I_{MAX} during the duration of time that state machine 70 remains in attack state 74. In some embodiments, as shown in FIGURE 6, such increase of maximum current I_{MAX} may include a programmable linear term (e.g., linearly increasing with time), a programmable quadratic term (e.g., exponentially increasing with time), and a programmable time delay after the beginning of attack state 74 at which the quadratic term is added to the linear term to generate a composite curve for maximum current I_{MAX}. Such composite ramp may allow steady state stability via the linear term and fast tracking of supply voltage V_{SUPPLY} versus battery voltage V_{BAT} via the quadratic term. Collapse controller 54 may generate a similar composite curve of decreasing maximum current I_{MAX} during release state 76 and slow release state 78.

In addition to the example waveforms described above, other waveforms that are dependent on time, current, and/or voltage may be used.

As used herein, when two or more elements are referred to as “coupled” to one another, such term indicates that such two or more elements are in electronic communication or mechanical communication, as applicable, whether connected indirectly or directly, with or without intervening elements.

This disclosure encompasses all changes, substitutions, variations, alterations, and modifications to the example embodiments herein that a person having ordinary skill in the art would comprehend. Similarly, where appropriate, the appended claims encompass all changes, substitutions, variations, alterations, and modifications to the example embodiments herein that a person having ordinary skill in the art would comprehend. Moreover, reference in the appended claims to an apparatus or system or a component of an apparatus or system being adapted to, arranged to, capable of, configured to, enabled to, operable to, or operative to perform a particular function encompasses that apparatus, system, or component, whether or not it or that particular function is activated, turned on, or unlocked, as long as that apparatus, system, or component is so adapted, arranged, capable, configured, enabled, operable, or operative. Accordingly, modifications, additions, or omissions may be made to the systems, apparatuses, and methods described herein without departing from the scope of the disclosure. For example, the components of the systems and apparatuses may be integrated or separated. Moreover, the operations of the systems and apparatuses disclosed herein may be performed by more, fewer, or other components and the methods described may include more, fewer, or other steps. Additionally, steps may be performed in any suitable order. As used in this document, “each” refers to each member of a set or each member of a subset of a set.

Although exemplary embodiments are illustrated in the figures and described below, the principles of the present disclosure may be implemented using any number of techniques, whether currently known or not. The present disclosure should in no way be limited to the exemplary implementations and techniques illustrated in the drawings and described above.

Unless otherwise specifically noted, articles depicted in the drawings are not necessarily drawn to scale.

All examples and conditional language recited herein are intended for pedagogical objects to aid the reader in understanding the disclosure and the concepts contributed by the inventor to furthering the art, and are construed as being without limitation to such specifically recited examples and conditions. Although embodiments of the present disclosure have been described in detail, it should be understood that various changes, substitutions, and alterations could be made hereto without departing from the spirit and scope of the disclosure.

Although specific advantages have been enumerated above, various embodiments may include some, none, or all of the enumerated advantages. Additionally, other technical advantages may become readily apparent to one of ordinary skill in the art after review of the foregoing figures and description.

To aid the Patent Office and any readers of any patent issued on this application in interpreting the claims appended hereto, applicants wish to note that they do not intend any of the appended claims or claim elements to invoke 35 U.S.C. § 112(f) unless the words “means for” or “step for” are explicitly used in the particular claim.

WHAT IS CLAIMED IS:

1. A system comprising:

a boost converter configured to receive an input voltage and boost the input voltage to an output voltage; and

control circuitry configured to:

enforce a maximum current limit to limit a current drawn by the boost converter; and

in response to the output voltage decreasing below the input voltage, dynamically increase the current above the maximum current limit to cause the output voltage to be approximately equal to the input voltage.

2. The system of Claim 1, wherein the maximum current limit is based on a determination of a maximum current level that ensures protection of components of the boost converter or components electrically coupled to the boost converter.

3. The system of Claim 1 or 2, wherein the control circuitry implements a feedback loop that controls the current to regulate the output voltage based on the output voltage and the input voltage.

4. The system of any of Claims 1-3, wherein the control circuitry is further configured to:

continuously increase the current when the output voltage is less than the input voltage and the current is greater than the maximum current limit; and

continuously decrease the current when the output voltage is greater than the input voltage and the current is greater than the maximum current limit.

5. The system of Claim 4, wherein:

when the output voltage is less than the input voltage and the current is greater than the maximum current limit, a rate of increase of the current is nonlinear; and

when the output voltage is greater than the input voltage and the current is greater than the maximum current limit, a rate of decrease of the current is nonlinear.

6. The system of Claim 5, wherein:

the rate of increase is a function of an amount of time since the control circuitry entered an attack state in which the output voltage is less than the input voltage and the current is greater than the maximum current limit; and

the rate of decrease is a function of an amount of time since the control circuitry entered a release state in which the output voltage is greater than the input voltage and the current is greater than the maximum current limit.

7. The system of any of Claims 4-6, wherein the control circuitry is further configured to continuously increase the current when the output voltage is greater than the input voltage and the output voltage is less than a threshold voltage.

8. The system of any of Claims 4-7, wherein the control circuitry is further configured to continuously decrease the current when the output voltage is greater than the threshold voltage and the current is greater than the maximum current limit, wherein a second rate of decrease occurring when the output voltage is greater than the threshold voltage and the current is greater than the maximum current limit is different than the rate of decrease when the output voltage is greater than the input voltage and the current is lesser than the maximum current limit.

9. The system of Claim 8, further wherein a second rate of decrease occurring when the output voltage is greater than the threshold voltage and the current is greater than the maximum current limit is less than the rate of decrease when the output voltage is greater than the input voltage and the current is lesser than the maximum current limit.

10. A method comprising:

enforcing a maximum current limit to limit a current drawn by a boost converter configured to receive an input voltage and boost the input voltage to an output voltage; and

in response to the output voltage decreasing below the input voltage, dynamically increasing the current above the maximum current limit to cause the output voltage to be approximately equal to the input voltage.

11. The method of Claim 10, wherein the maximum current limit is based on a determination of a maximum current level that ensures protection of components of the boost converter or components electrically coupled to the boost converter.

12. The method of Claim 10 or 11, further comprising implementing a feedback loop that controls the current to regulate the output voltage based on the output voltage and the input voltage.

13. The method of any of Claims 10-12, further comprising:

continuously increasing the current when the output voltage is less than the input voltage and the current is greater than the maximum current limit; and

continuously decreasing the current when the output voltage is greater than the input voltage and the current is greater than the maximum current limit.

14. The method of Claim 13, wherein:

when the output voltage is less than the input voltage and the current is greater than the maximum current limit, a rate of increase of the current is nonlinear; and

when the output voltage is greater than the input voltage and the current is greater than the maximum current limit, a rate of decrease of the current is nonlinear.

15. The method of Claim 14, wherein:

the rate of increase is a function of an amount of time since the control circuitry entered an attack state in which the output voltage is less than the input voltage and the current is greater than the maximum current limit; and

the rate of decrease is a function of an amount of time since the control circuitry entered a release state in which the output voltage is greater than the input voltage and the current is greater than the maximum current limit.

16. The method of any of Claims 13-15, further comprising continuously increasing the current when the output voltage is greater than the input voltage and the output voltage is less than a threshold voltage.

17. The method of any of Claims 13-16, further comprising continuously decreasing the current when the output voltage is greater than the threshold voltage and the current is greater than the maximum current limit, wherein a second rate of decrease occurring when the output voltage is greater than the threshold voltage and the current is greater than the maximum current limit is different than the rate of decrease when the output voltage is greater than the input voltage and the current is lesser than the maximum current limit.

18. The method of Claim 17, further wherein a second rate of decrease occurring when the output voltage is greater than the threshold voltage and the current is greater than the maximum current limit is less than the rate of decrease when the output voltage is greater than the input voltage and the current is lesser than the maximum current limit.

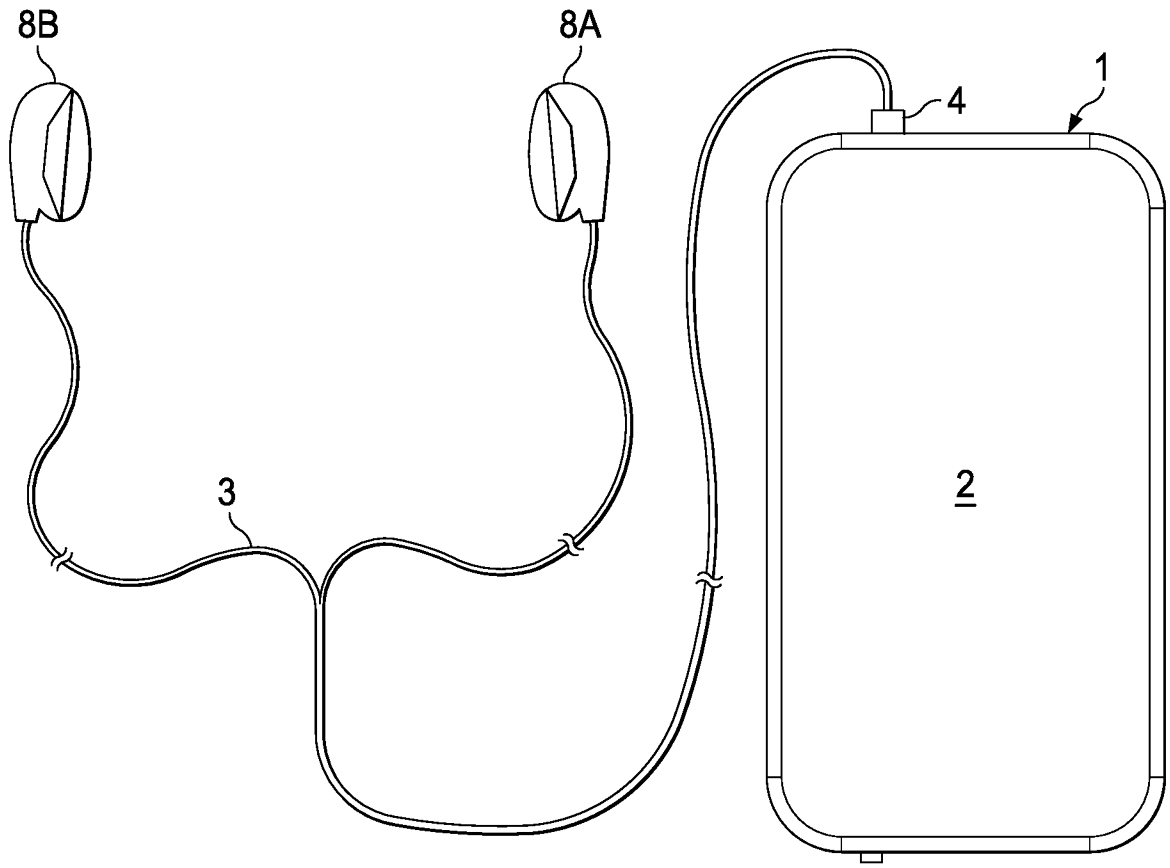

8B
8A
1
4
3
2

FIG. 1

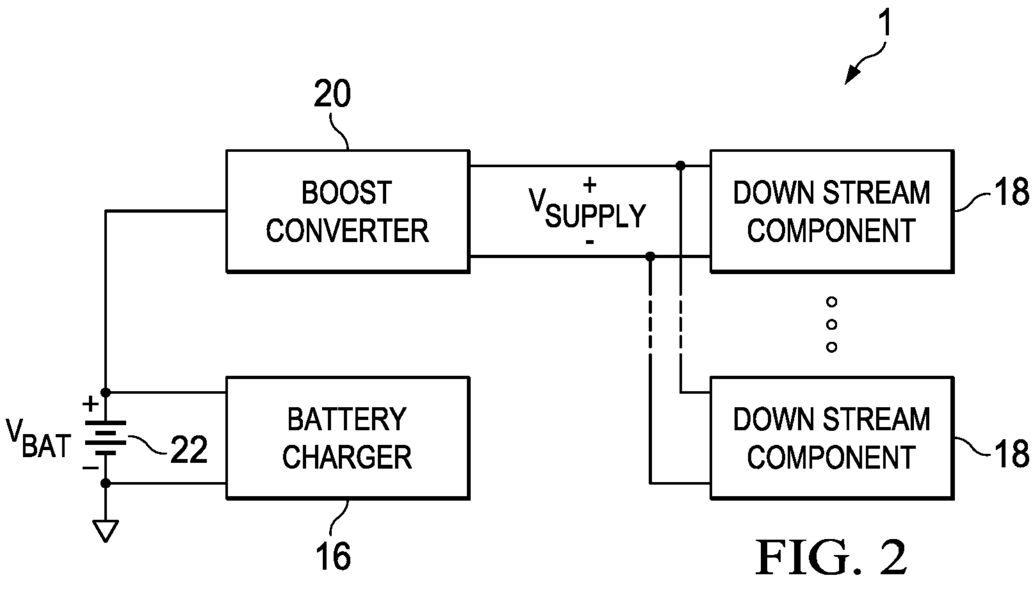

1
20
BOOST CONVERTER
+
V_{SUPPLY}
-
DOWN STREAM COMPONENT
18
DOWN STREAM COMPONENT
18
+
V_{BAT}
-
22
BATTERY CHARGER
16

FIG. 2

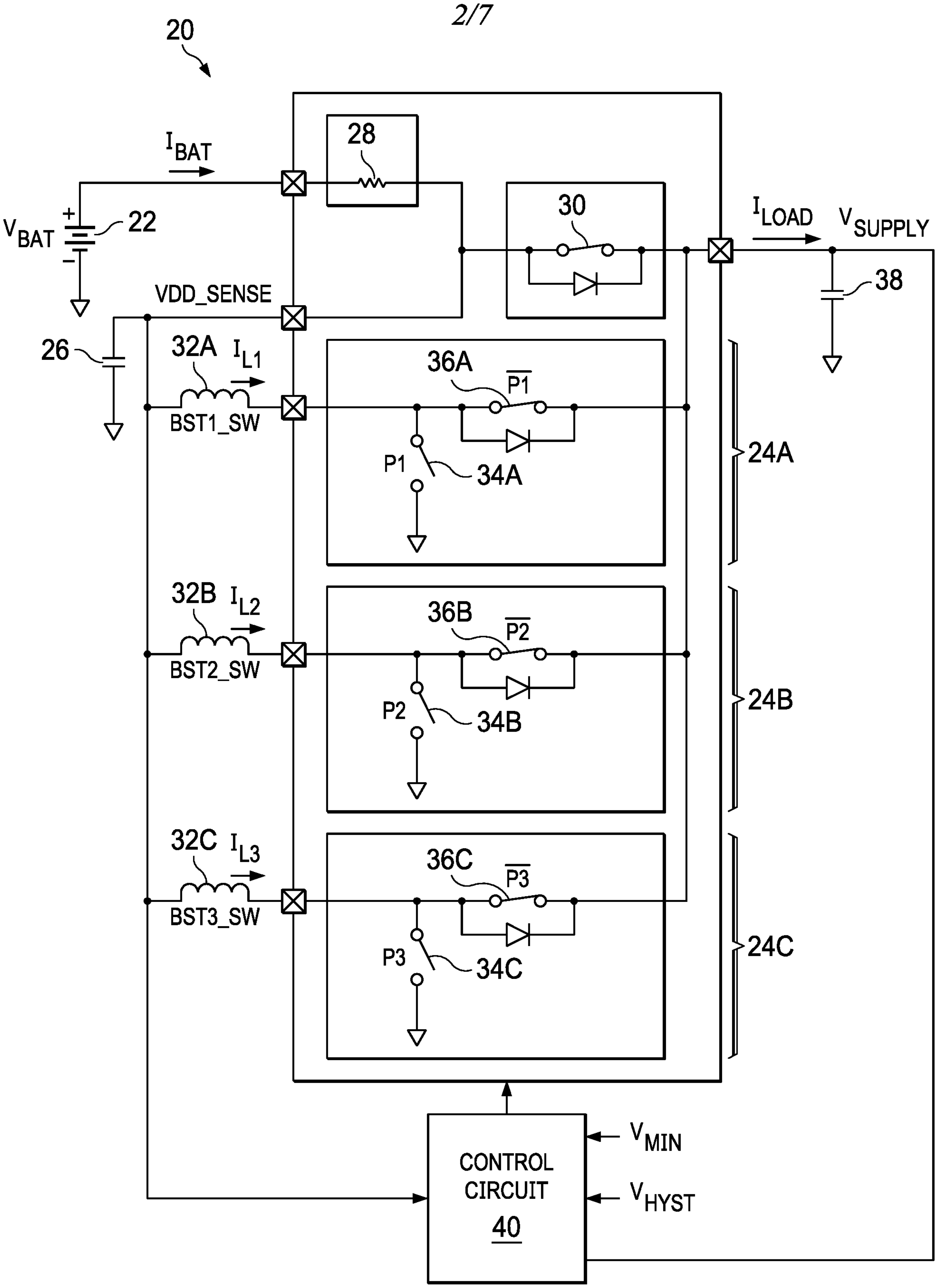

20
28
I_{BAT}
V_{BAT}
22
30
I_{LOAD}
V_{SUPPLY}
38
VDD_SENSE
26
32A
I_{L1}
BST1_SW
36A
$\overline{P1}$
P1
34A
24A
32B
I_{L2}
BST2_SW
36B
$\overline{P2}$
P2
34B
24B
32C
I_{L3}
BST3_SW
36C
$\overline{P3}$
P3
34C
24C
CONTROL CIRCUIT 40
V_{MIN}
V_{HYST}

FIG. 3A

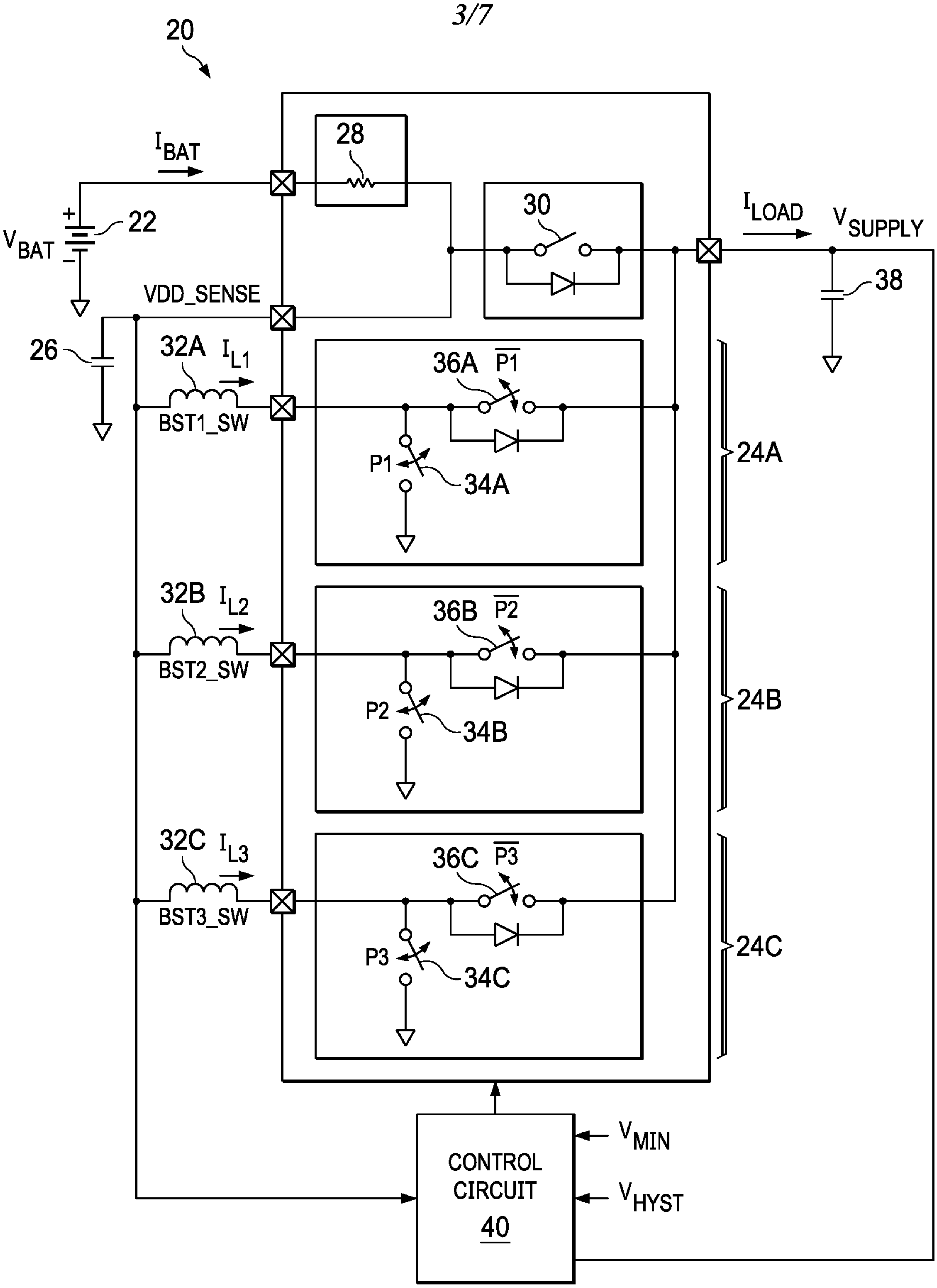

20
28
I_{BAT}
V_{BAT}
22
VDD_SENSE
30
I_{LOAD}
V_{SUPPLY}
38
26
32A
I_{L1}
BST1_SW
36A
$\overline{P1}$
P1
34A
24A
32B
I_{L2}
BST2_SW
36B
$\overline{P2}$
P2
34B
24B
32C
I_{L3}
BST3_SW
36C
$\overline{P3}$
P3
34C
24C
CONTROL CIRCUIT
40
V_{MIN}
V_{HYST}

FIG. 3B

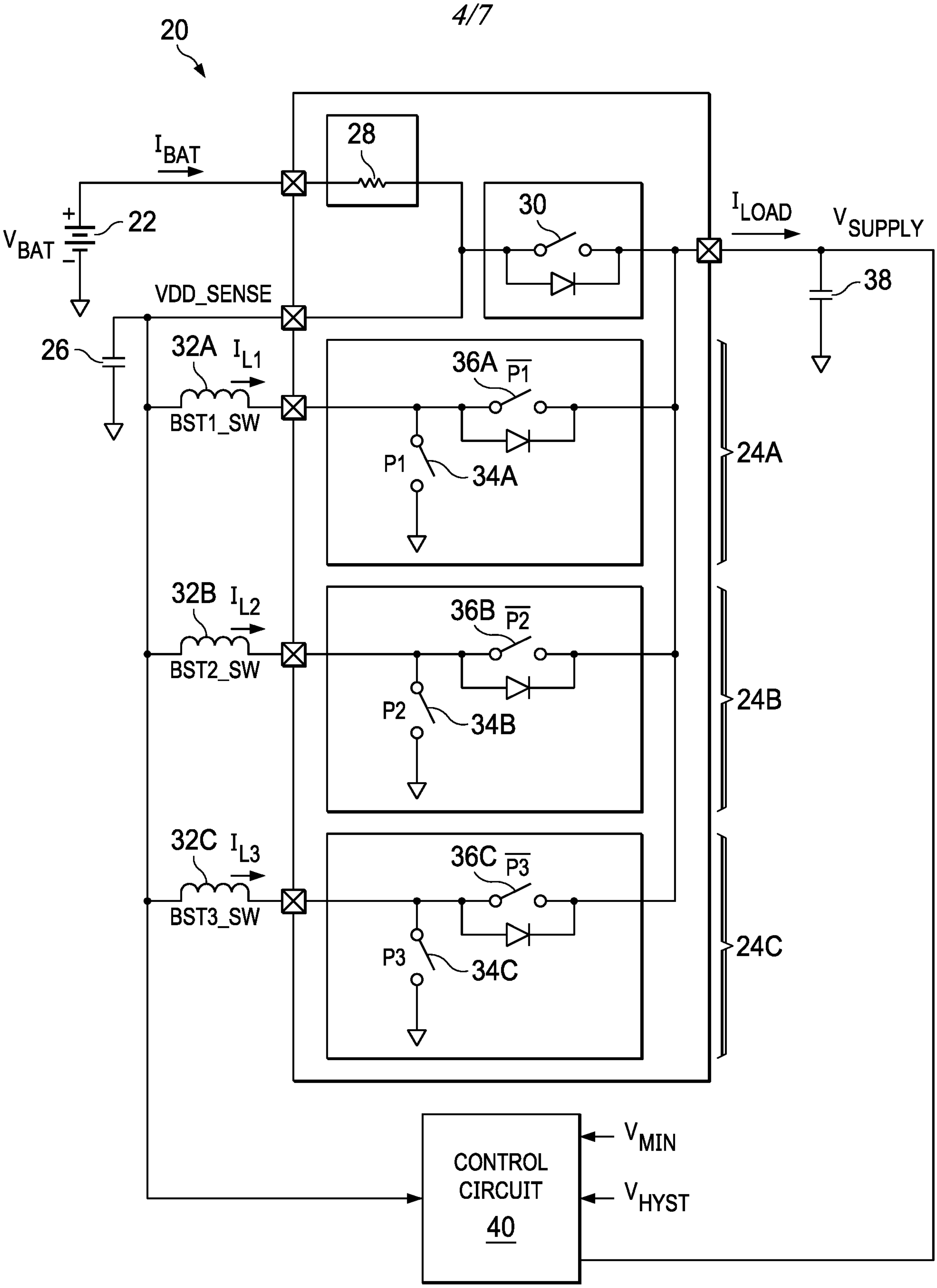

20
28
I_{BAT}
V_{BAT}
22
VDD_SENSE
26
30
I_{LOAD}
V_{SUPPLY}
38
32A
I_{L1}
BST1_SW
36A
$\overline{P1}$
P1
34A
24A
32B
I_{L2}
BST2_SW
36B
$\overline{P2}$
P2
34B
24B
32C
I_{L3}
BST3_SW
36C
$\overline{P3}$
P3
34C
24C
CONTROL CIRCUIT
40
V_{MIN}
V_{HYST}

FIG. 3C

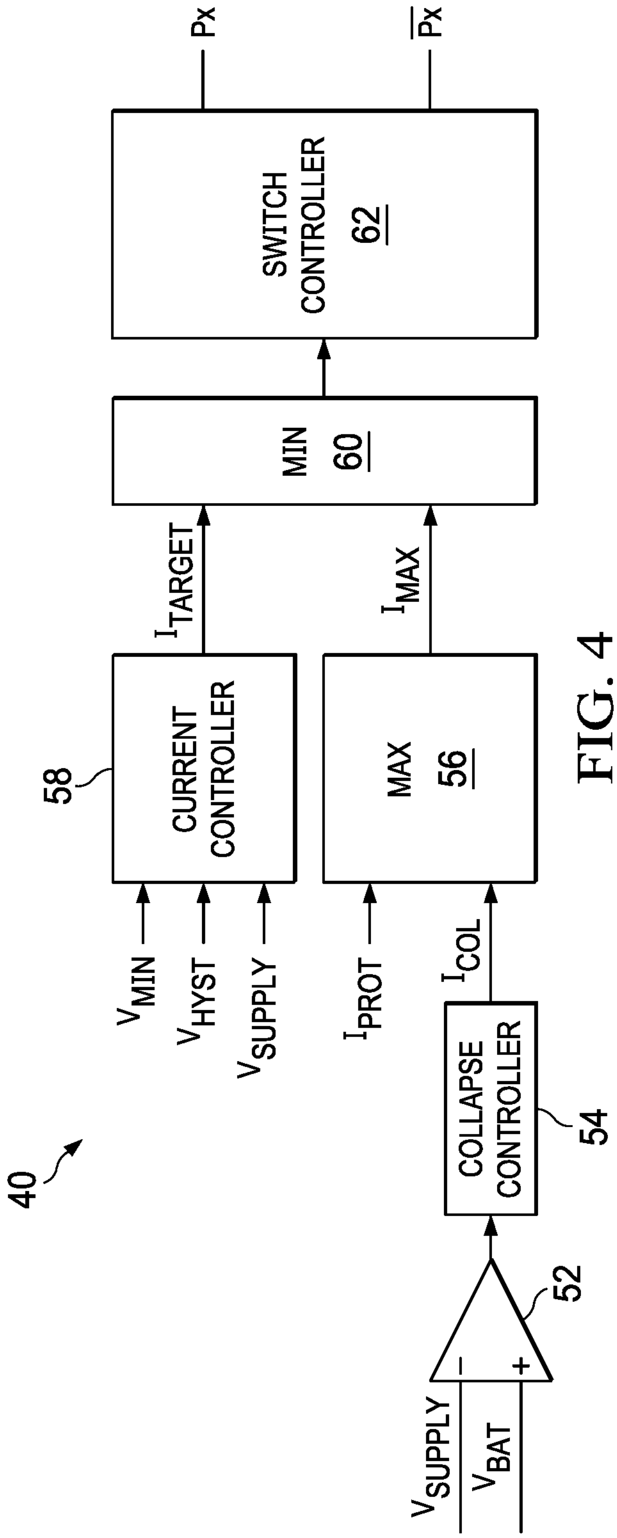

40
SWITCH CONTROLLER 62
Px
$\overline{Px}$
MIN 60
I_{TARGET}
I_{MAX}
58
CURRENT CONTROLLER
MAX 56
V_{MIN}
V_{HYST}
V_{SUPPLY}
I_{PROT}
I_{COL}
COLLAPSE CONTROLLER
54
52
−
+
V_{SUPPLY}
V_{BAT}

FIG. 4

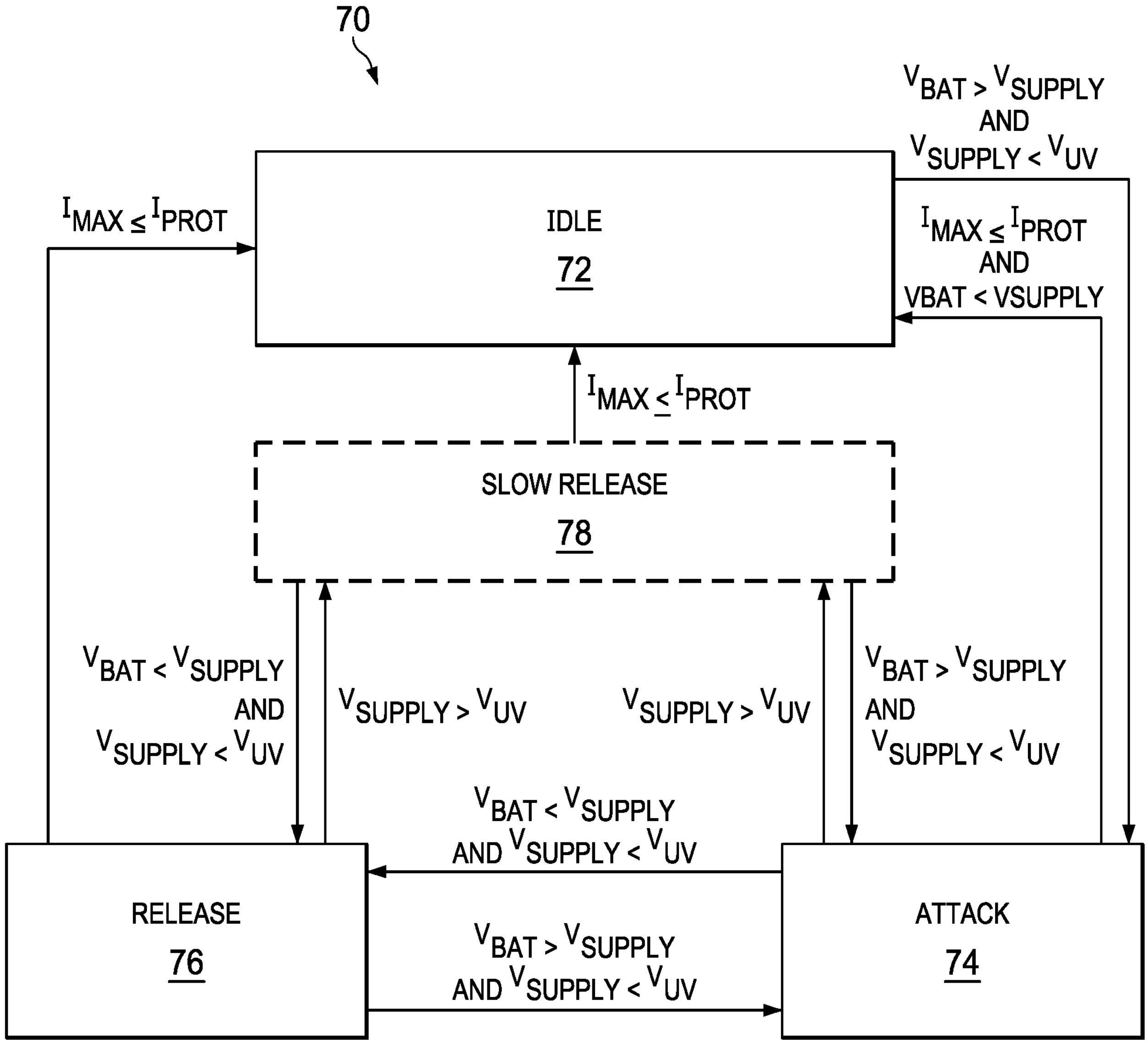
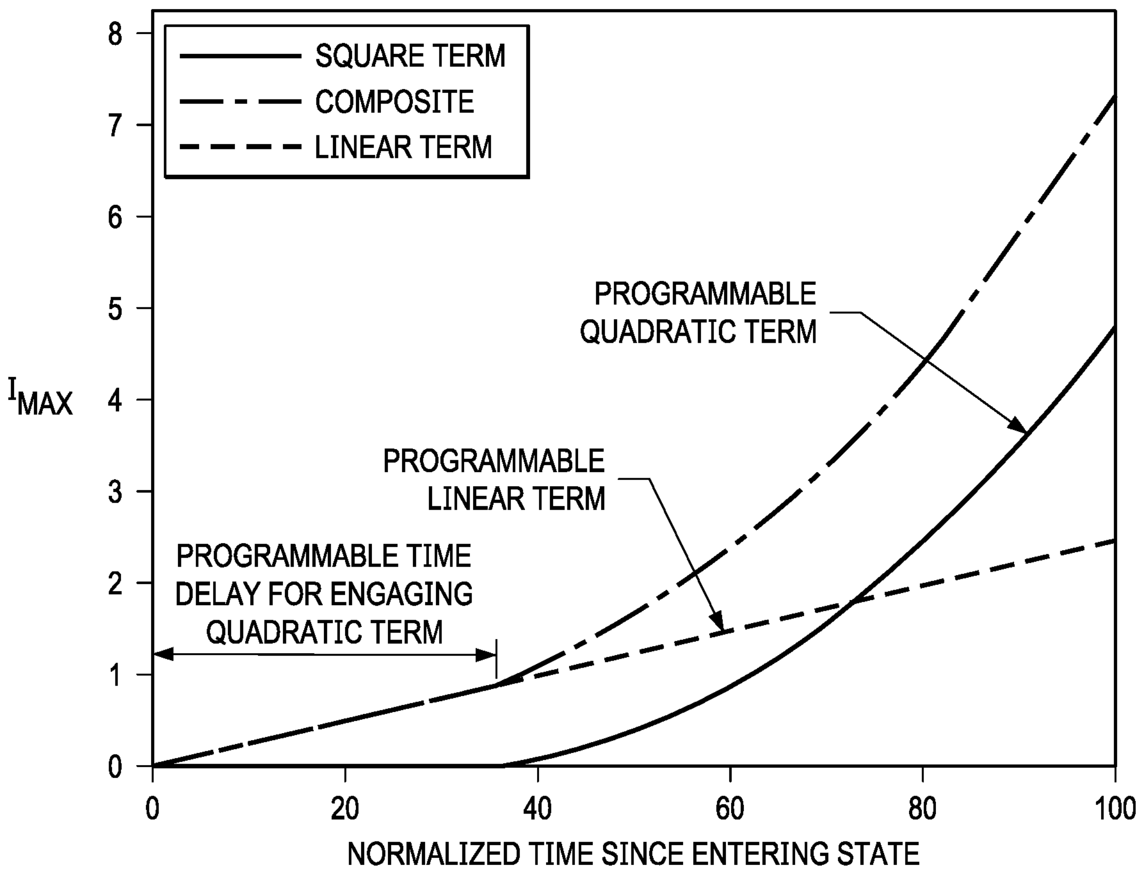

70
IDLE
72
SLOW RELEASE
78
RELEASE
76
ATTACK
74
$V_{BAT} > V_{SUPPLY}$ AND $V_{SUPPLY} < V_{UV}$
$I_{MAX} \leq I_{PROT}$
$I_{MAX} \leq I_{PROT}$ AND VBAT < VSUPPLY
$I_{MAX} \leq I_{PROT}$
$V_{BAT} < V_{SUPPLY}$ AND $V_{SUPPLY} < V_{UV}$
$V_{SUPPLY} > V_{UV}$
$V_{SUPPLY} > V_{UV}$
$V_{BAT} > V_{SUPPLY}$ AND $V_{SUPPLY} < V_{UV}$
$V_{BAT} < V_{SUPPLY}$ AND $V_{SUPPLY} < V_{UV}$
$V_{BAT} > V_{SUPPLY}$ AND $V_{SUPPLY} < V_{UV}$

FIG. 5

FIG. 6


SQUARE TERM
COMPOSITE
LINEAR TERM
PROGRAMMABLE QUADRATIC TERM
PROGRAMMABLE LINEAR TERM
PROGRAMMABLE TIME DELAY FOR ENGAGING QUADRATIC TERM
I MAX
0
1
2
3
4
5
6
7
8
0
20
40
60
80
100
NORMALIZED TIME SINCE ENTERING STATE

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2022/037855

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M3/156 H02M3/158
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN 112 953 242 A (SHENZHEN SOUTH CLOUD MICROELECTRONICS CO LTD) 11 June 2021 (2021-06-11)	1-3, 10-12
Y	corresponding parts of the description; figures 1-3	2-6, 11-15
A		7-9, 16-18

X	US 2020/388118 A1 (ROSENBERG ARON [US] ET AL) 10 December 2020 (2020-12-10)	1,10
Y	paragraph [0082] - paragraph [0118]; figures 5,6,14,16	3-6, 12-15
A		7-9, 16-18

	-/--	

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
14 October 2022	26/10/2022

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Kruip, Stephan

1

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2020/235712 A1 (MAY JEFFREY A [US] ET AL) 23 July 2020 (2020-07-23)	1,10
Y	paragraph [0077] - paragraph [0091]; figures 8-10	2,11
A	US 2016/352225 A1 (LANGLINAIS JAMIE L [US] ET AL) 1 December 2016 (2016-12-01) paragraph [0031] - paragraph [0035]; figures 2-3	1-18
A	US 9 768 689 B1 (PAZHAYAVEETIL ULLAS [US] ET AL) 19 September 2017 (2017-09-19) column 5 - column 11; figures 2-6	1-18
A	US 2011/285375 A1 (DEBOY GERALD [AT]) 24 November 2011 (2011-11-24) paragraph [0058] - paragraph [0061]; figure 11	1-18

1

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			US	2021183213	A1	17-06-2021
US 2020235712	A1	23-07-2020	NONE			
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			GB	2529994	A	09-03-2016
			US	9391517	B1	12-07-2016
			US	9768689	B1	19-09-2017
			US	9912238	B1	06-03-2018
			US	2015030183	A1	29-01-2015
			US	2015032396	A1	29-01-2015
			US	2017063318	A1	02-03-2017
			WO	2015013277	A1	29-01-2015
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			US	2013175883	A1	11-07-2013