

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
31 January 2008 (31.01.2008)

PCT

(10) International Publication Number
WO 2008/013871 A2

(51) International Patent Classification:
H02M 1/00 (2007.01)

(21) International Application Number:
PCT/US2007/016766

(22) International Filing Date: 26 July 2007 (26.07.2007)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/820,551 27 July 2006 (27.07.2006) US
11/782,774 25 July 2007 (25.07.2007) US

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

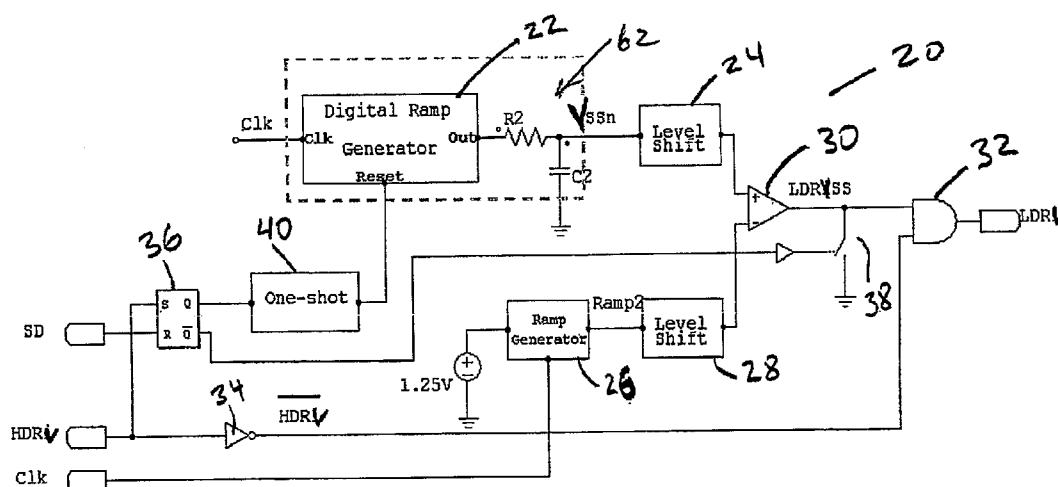
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— without international search report and to be republished upon receipt of that report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: PRE-BIAS PROTECTION CIRCUIT FOR CONVERTER



(57) Abstract: A pre-bias protection circuit for a converter circuit including a switching stage having high- and low-side switches connected in series at a switching node and an output stage connected to the switching node having a capacitor having a pre-existing pre-bias voltage at startup of the converter circuit, the pre-bias protection circuit controlling discharge of the pre-bias voltage when the low-side switch is turned ON during a start up of the converter circuit. The pre-bias protection circuit includes a first circuit for providing a first output; a second circuit providing a second output; and a comparator circuit for comparing the first output and the second output and producing a third output comprising a pulse width modulated signal for driving the low side switch such that the pulse width modulated signal starts with a small duty cycle and thereafter increases to a larger duty cycle, thereby to prevent the pre-bias voltage from discharging during startup.

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PRE-BIAS PROTECTION CIRCUIT FOR CONVERTER

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is based on and claims priority to U.S. Provisional Patent Application Serial No. 60/820,551, filed on 27 July 2006 and U.S. Patent Application Serial No. 11/782,774, filed 25 July 2007, the entire contents of which are hereby incorporated by reference herein.

BACKGROUND OF THE INVENTION

[0002] The present invention relates to converter circuits and more particularly to pre-bias protection circuits for the converter circuits.

[0003] Voltage, pre-existing at an output stage of a converter, for example, a converter circuit 8 having a transistor stage 10 illustrated in Figure 1, prior to start up is referred to as pre-bias voltage. When the converter circuit 8 starts up, high- and low-side switches 12 and 14 of the transistor stage 10 will be driven by high- and low-side switch control signals Hdrv and Ldrv from respective high- and low-side gate drivers. When the low-side switch control signal Ldrv is applied to the low-side switch 14 during startup, the output capacitor C_0 having the pre-bias voltage may discharge through the output inductor L and the low-side switch 14. Discharging the pre-bias voltage may result in glitches and cause problems in systems, e.g., multi-processor systems.

[0004] In order not to discharge the pre-bias voltage, specific attention needs to be taken during a start up of the converter circuit 8. Therefore, because discharge of the pre-bias voltage is undesirable, discharging of the output capacitor C_0 of the converter circuit 8 should be prevented and reversal of an inductor current must not be allowed.

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SUMMARY OF THE INVENTION

[0005] It is an object of the present invention to prevent discharge of the output voltage pre-bias during converter startup.

[0006] According to the invention, this is achieved by control of the duty cycle of the low-side switch control signal Ldrv during start up, so that the low-side switch control signal Ldrv delivers a starting small duty cycle to the low-side transistor during startup while the high-side transistor operates at a normal duty cycle.

[0007] A pre-bias protection circuit is provided for a converter circuit including a switching stage having high- and low-side switches connected in series at a switching node and an output stage also connected to the switching node including a capacitor having a pre-existing pre-bias voltage at startup, the pre-bias protection circuit controlling discharge of the pre-existing voltage when the low-side switch is turned ON during a start up of the converter circuit. The pre-bias protection circuit including first circuit for providing a first output; a second circuit for providing a second output; and a comparator circuit for comparing the first output and the second output and producing a third output comprising a pulse width modulated signal for driving the low side switch such that the pulse width modulated signal starts with a small duty cycle and thereafter increases to a larger duty cycle. The third output signal drives the low side switches at startup with a gradually increasing duty cycle to prevent the pre-bias voltage from discharging.

[0008] Other features and advantages of the present invention will become apparent from the following description of the invention that refers to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Figure 1 is a diagram of a converter circuit having a transistor output switching stage and a capacitor having the pre-bias voltage;

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[0010] Figure 2 is a diagram of a circuit of an embodiment of the present invention that receives the high-side control signal and provides the low-side control signal having an increasing ON duty cycle at startup to prevent pre-bias voltage discharge;

[0011] Figure 3 is a diagram of a digital ramp generator circuit of an embodiment the present invention;

[0012] Figure 4 is a graph of various signals produced by the circuit of Figure 2 using the high-side control and clock signals as input;

[0013] Figure 5a is a flow diagram of a digital pre-bias ramp generator;

[0014] Figure 5b is a diagram showing a function of fluctuations in the voltage V_{SSN} causing a step change of a signal L_{drvSS} turn ON time;

[0015] Figure 5c is a diagram of a Low Pass Filter of the digital ramp generator and a graph of its output;

[0016] Figures 6a – 6b are graphs of simulation results of a pre-bias control provided by the embodiment of the present invention in Figure 2;

[0017] Figure 7 is a diagram of a circuit of another embodiment of the present invention that provides the low-side control signal having an increasing ON duty cycle at startup to prevent pre-bias voltage discharge;

[0018] Figure 8 is a graph of various signals produced by the circuit of Figure 7; and

[0019] Figures 9a – 9c are graphs of simulation results of a pre-bias control provided by the embodiment of the present invention in Figure 7.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

[0020] The present invention provides a way of preventing discharge of the pre-bias voltage in the converter circuits. This is achieved by controlling the duty cycle on-time

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of the low-side transistor. Figure 2 illustrates a circuit 20 that receives the high-side switch control signal Hdrv and processes it into the low-side switch control signal Ldrv. The circuit 20 includes a digital ramp generator circuit 22 with a corresponding level shifter circuit 24, an analog ramp generator circuit 26 also with a corresponding level shifter circuit 28. Both ramp generator circuits 22 and 26 receive a clock signal Clk. An output of the digital ramp generator circuit 22 is filtered using a Low Pass Filter including a register R2 and a capacitor C2. An output of the level shifter circuits 24 and 28 is compared by a comparator circuit 30. Further, an AND circuit 32 is used to AND a signal Ldrv_{ss} of the comparator circuit 30 with an inverse of the high-side switch control signal Hdrv, inverted in the inverter circuit 34.

[0021] The circuit 20 also includes a flip-flop circuit 36 responsive to a shut down signal SD used to shut down the circuit 20 by connecting a switch 38 to the ground. The flip-flop circuit 36 also provides, when the shut down signal SD is OFF, responsive to the high-side switch control signal Hdrv, a signal to a one-shot circuit 40 to reset the digital ramp generator circuit 22.

[0022] Figure 3 illustrates the digital ramp generator circuit 22 that includes a counter and register circuit 50 counting the clock signal Clk and being reset by the reset signal from the one-shot circuit 40 (Figure 2) for resetting the count. The circuit 22 further includes a digital to analog converter (DAC) circuit 52 having a voltage reference 54 and outputting an analog converted value to an amplifier circuit 56 having a resistor 58 connected in parallel to its negative input and output terminals. One terminal of another resistor 59 is connected to an output terminal of the DAC circuit 52 and the negative input terminal of the amplifier circuit 56. A positive input terminal of the amplifier circuit 56 is connected to ground.

[0023] Figure 4 illustrates graphs of the signals produced by the circuit 20 using the high-side switch control and clock signals Hdrv and Clk. A Ramp2 signal is produced by the analog ramp generator circuit 26. At startup, as the high-side switch control signal Hdrv turns ON, voltage V_{SSN}, produced as the integrated output of the digital ramp

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generator circuits 22, starts to rise. The slope of the voltage V_{SSN} is fixed as is the pre-bias startup time. A pulse width modulated signal $Ldrv_{SS}$ is generated by the comparator 30 to be ON when the voltage V_{SSN} crosses the OFF Ramp2 signal and OFF when the voltage V_{SSN} crosses the ON Ramp2 signal. The low-side switch control signal $Ldrv$ is generated by the AND operation of the AND circuit 32 which assures that the low-side switch control signal $Ldrv$ is ON only when the inverse of the high-side switch control signal $Hdrv$ is ON or, in other words, when the high-side switch control signal $Hdrv$ is OFF.

[0024] Because the slope of the voltage V_{SSN} is fixed, the signal $Ldrv_{SS}$ and thus, the low-side switch control signal $Ldrv$ provide control of a duty cycle of the low-side transistor 14 so that at startup the low-side switch control signal $Ldrv$ delivers duty cycles to the low-side transistor that start from and increase over time while the high-side transistor operates at a normal duty cycle.

[0025] The operation of the switching stage 10 starts when voltage, e.g., at Comp pin of an IC controlling the stage is detected to be over some predefined offset voltage, for example 1V. Once the offset voltage is reached, the first $HDrv$ signal is generated and V_{ssn} starts to ramp in the meantime.

[0026] Figure 5a illustrates how the digital ramp generator specification and the characteristics of the Low Pass Filters ($R2$, $C2$) are designed. First, specifications of a negative voltage V_0 spike are received in step S70; a maximum allowed turn-ON time difference of the signal $Ldrv_{SS}$ is determined in step S72; a maximum allowed voltage fluctuation of voltage V_{ssn} is determined in step S74; the Low Pass Filter (LPF) corner frequency is determined in step S76; and the number of Bits needed for the digital ramp generator for adequate resolution is calculated in step S78.

Figure 5b illustrates fluctuations in the voltage V_{SSN} . As shown, fluctuation on voltage V_{SSN} causes step change on the turn-ON time of the signal $Ldrv_{SS}$, thus inducing negative voltage spike in a voltage $V_0(t)$, illustrated in a diagram 60 as the pre-bias voltage $V(0^+)$. At ON time $t1$, only a small amount of the current I_L is allowed to flow through the

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transistor 14 (Figure 2) causing imperceptible change in the voltage $V_0(t)$. At ON time t_2 , a longer duration than ON time t_1 , a larger amount of the current I_L is allowed to flow through the transistor 14 causing a larger change $\Delta V(0)$ in the voltage $V_0(t)$. The current flow during the ON-time of the signal $Ldrv_{SS}$ is calculated as

$$i_l(t) = C_1 e^{-\alpha t} \sin \omega_d t$$

$$v_o(t) = V(0^+) - \frac{1}{C_o} \int_0^t i_l(\tau) d\tau$$

where $\alpha = R_e / 2L$ and $\omega_d = \sqrt{1 / (LC)^2 - \alpha^2}$

[0027] Figure 5c illustrates an output of the LPF 62. Input to the LPF 62 is provided by the digital ramp generator circuit 22 (Figure 2) as voltage steps V_{step} . A lower corner frequency of the LPF provides smaller voltage increase within $1/F_{sw}$. A smaller V_{step} provides voltage increase within the $1/F_{sw}$. Thus, the voltage $V_0(t)$ may be calculated as $V_o(t) = V(0^+) + V_{step}(1 - e^{-t/R_f C_f})$, where $V(0^+)$ is the initial voltage on the capacitor C_f .

[0028] Figures 6a and 6b illustrate simulation results of the pre-bias control provided by the invention of the present application. In Figure 6a voltage $V_{IN}=5.5V$, $V_0=3.3V$, $F_{sw}=1.25MHz$, $L=300nH$, $C_o=10\mu F$, LPF($R_f=8MOhm$, $C_f=1pF$ ($F_c=20kHz$)), DACbit=5. In Figure 6b the following values were modified: $F_{sw}=1.5MHz$, $C_f=20pF$ ($F_c=500Hz$), DACbit=3.

[0029] Another embodiment of the present invention, illustrated in Figure 7, provides a way of preventing discharge of the pre-bias voltage in the converter circuits without the use of ramp generator circuits. While circuits 20 (Figures 2) and 120 illustrate two different embodiments of Pre-Bias protection circuits, where circuit 20 uses digital circuits to generate a V_{ssn} ramp and circuit 120 uses analog circuits to generate the V_{ssn} ramp, the ramp generation circuits for V_{ssn} are not limited to these two approaches. Any other ramp generation circuits may be suitable for this purpose.

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[0030] Figure 7 illustrates a circuit 120 that similar to the circuit 20 of Figure 2 receives the high-side switch control signal Hdrv and processes it into the low-side switch control signal Ldrv. The circuit 120 includes the level shifter circuits 24 and 28, the output of the level shifter circuits 24 and 28 is compared by the comparator circuit 30, and the AND circuit 32 is used to AND the signal Ldrv_{SS} of the comparator circuit 30 with an inverse of the high-side switch control signal Hdrv, inverted in the inverter circuit 34.

[0031] The circuit 120 also includes the flip-flop circuit 36 responsive to the shut down signal SD used to shut down the circuit 120 by connecting the switch 38 to the ground. The flip-flop circuit 36 also provides, when the shut down signal SD is OFF, responsive to the high-side switch control signal Hdrv, a signal to the one-shot circuit 40.

[0032] In the circuit 120, a digital ramp generator circuit is replaced with a sample and hold circuit 122 that receives an input voltage signal Vc. An output signal produced by the sample and hold circuit 122 is added to the signal Vc to produce the input voltage V_{SSn} supplied to the level shifter circuit 24. Further, a ramp generator circuit 126, receives an external clock signal CLK and a signal from an internal source 127 to produce a ramp signal RAMP to the level shifter circuit 28.

[0033] Figure 8 illustrates graphs of the signals produced by the circuit 120 using the high-side switch control and ramp signals Hdrv and RAMP. At startup, as the high-side switch control signal Hdrv turns ON, voltage V_{SSn}, produced as the integrated output of the sample and hold circuit 122 and the signal SS, starts to rise. The slope of the voltage V_{SSn} is fixed as is the pre-bias startup time. A pulse width modulated signal Ldrv_{SS} is generated by the comparator 30 to be ON when the voltage V_{SSn} crosses the OFF RAMP2 signal and OFF when the voltage V_{SSn} crosses the ON RAMP2 signal. The low-side switch control signal Ldrv is ON only when the inverse of the high-side switch control signal Hdrv is ON or, in other words, when the high-side switch control signal Hdrv is OFF.

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[0034] Because the slope of the voltage V_{SSN} is fixed, the signal $Ldrv_{SS}$ and thus, the low-side switch control signal $Ldrv$ provide control of a duty cycle of the low-side transistor 14 (Figure 1) so that at startup the low-side switch control signal $Ldrv$ delivers duty cycles to the low-side transistor that start from and increase over time while the high-side transistor operates at a normal duty cycle.

[0035] Figures 9a –9c illustrate simulation results of the pre-bias control provided by the circuit 120. Figures 9a and 9b show graphs taken over different time intervals for the following voltage values: $V_{PREBIAS}=1.36V$, $V_{IN}=5.5V$, $V_0=1.5V$, $F_{sw}=1.25MHz$, $L=300nH$, $C_{out}=40uF$. Figure 9c shows graphs for the following values were modified $V_{PREBIAS}=1.2V$, $V_{IN}=2.25V$, $V_0=1.5V$, $F_{sw}=1.25MHz$, $L=300nH$, $C_{out}=40uF$.

[0036] Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention not be limited by the specific disclosure herein.

WHAT IS CLAIMED IS:

1. A pre-bias protection circuit for a converter circuit including a switching stage having high- and low-side switches connected in series at a switching node and an output stage connected to the switching node having a capacitor having a pre-existing pre-bias voltage at startup of the converter circuit, the pre-bias protection circuit controlling discharge of the pre-bias voltage when the low-side switch is turned ON during a start up of the converter circuit, the pre-bias protection circuit comprising:
 - a first circuit for providing a first output;
 - a second circuit providing a second output; and
 - a first comparator circuit for comparing the first output and the second output and producing a third output comprising a pulse width modulated signal for driving the low side switch such that the pulse width modulated signal starts with a small duty cycle and thereafter increases to a larger duty cycle, thereby to prevent the pre-bias voltage from discharging during startup.
2. The circuit of claim 1, further comprising first and second level shifter circuits to shift levels of the first output and the second output prior to the comparison by the first comparator circuit.
3. The circuit of claim 2, further comprising a logic circuit for performing a logical operation on the third output and a signal related to the gate control signal of the high-side switch to produce a gate control signal of the low-side switch.
4. The circuit of claim 3, wherein the gate control signal of the low-side switch controls duration of a duty cycle ON-time of the low-side switch.
5. The circuit of claim 4, wherein the logic circuit assures that the gate control signal of the low-side switch is ON only when the inverse of the gate control signal of the high-side switch is ON.

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6. The circuit of claim 5, further comprising a circuit for receiving a shut down signal and shutting down the pre-bias protection circuit.

7. The circuit of claim 1, further comprising a resetting circuit for providing a resetting signal to the first circuit when a gate control signal for the high-side switch turns ON.

8. The circuit of claim 7, wherein the resetting circuit comprises a flip-flop circuit receiving said gate control signal for the high-side switch and for providing a signal to a one-shot circuit for resetting the first circuit.

9. The circuit of claim 6, wherein when the shut down signal is OFF the shutting down circuit is responsive to the gate control signal of the high-side switch to send a signal to reset the digital ramp generator circuit.

10. The circuit of claim 1, wherein the third output is ON when the first output crosses an ON portion of the second output and OFF when the first output crosses an OFF portion of the second output.

11. The circuit of claim 1, wherein the fixed slope of the first output is used to increase the duty cycle of the low-side transistor over time from the small duty cycle to the larger duty cycle, while the high-side transistor operates at a normal duty cycle.

12. The circuit of claim 1, wherein the first circuit comprises a digital ramp generator circuit.

13. The circuit of claim 12, wherein the digital ramp generator circuit comprises a digital converter circuit and further comprises a Low Pass Filter integrating the output of the digital converter circuit.

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14. The circuit of claim 12, wherein the digital ramp generator circuit comprises:

a counter and register circuit for receiving a clock signal for counting reset signals from the one-shot circuit;

a digital to analog converter circuit for receiving a voltage reference and a digital output from the counter and register circuit; and

an amplifier circuit having an input terminal connected to an output terminal of the digital to analog converter circuit for outputting a converted analog value as the first output.

15. The circuit of claim 1, wherein the first circuit comprises a sample and hold circuit.

16. The circuit of claim 8, further comprising:

a sample and hold circuit receiving a first external signal;

a second comparator for comparing the first external signal with a first internal source reference value and providing a second comparator output; and

an OR circuit for ORing the second comparator output with a reset signal from the flip-flop circuit and providing the product to the sample and hold circuit,

wherein the sample and hold circuit produces an output that is combined with the first external signal to produce the first output.

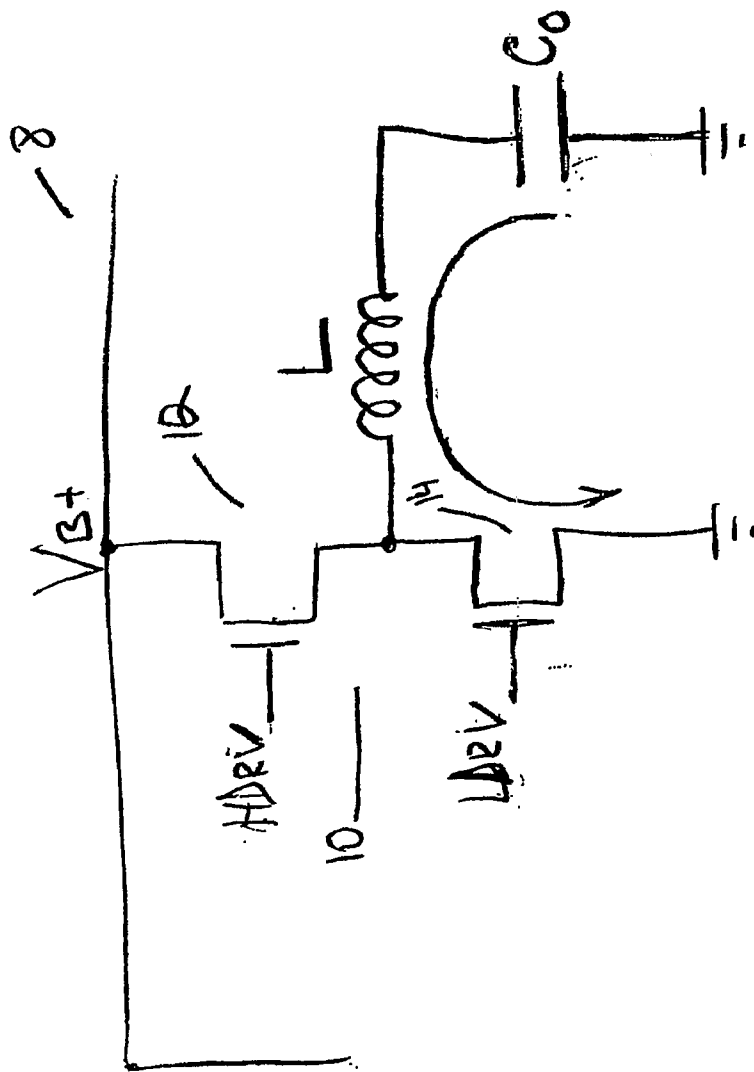


Figure 1

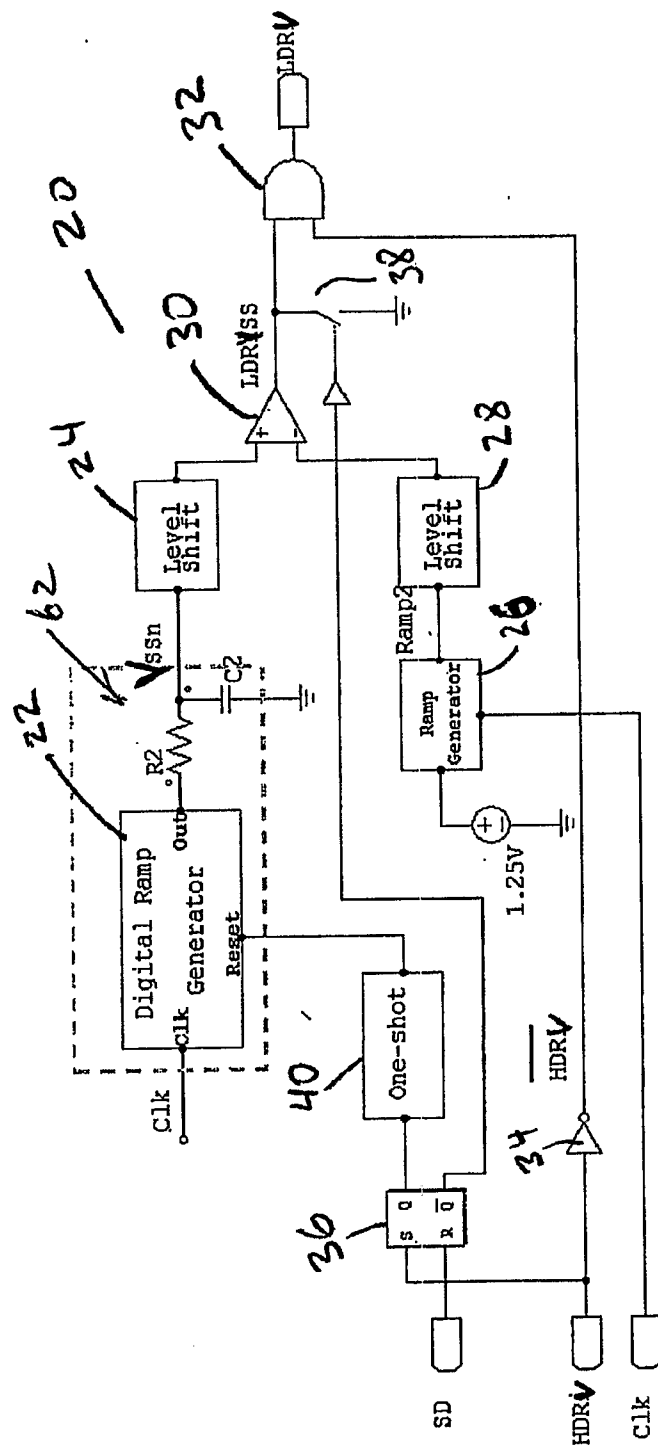


Figure 2

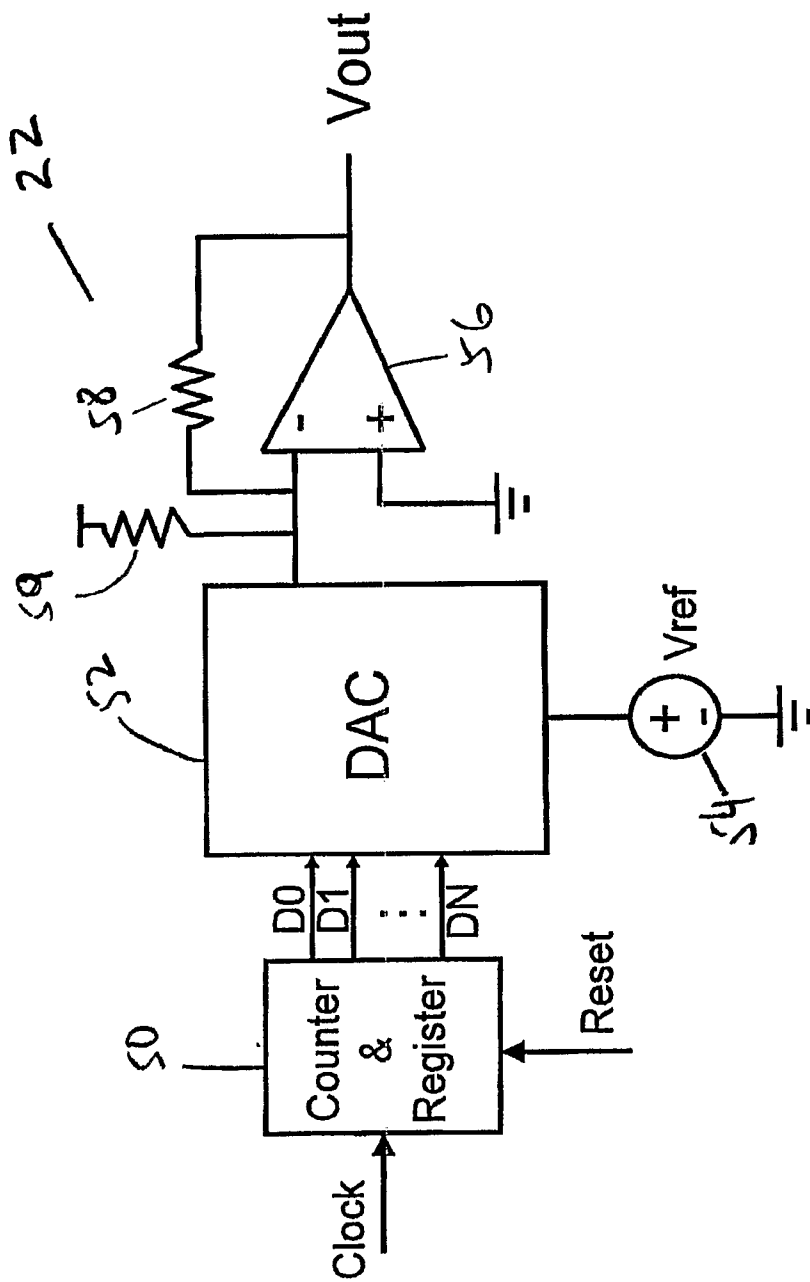


FIGURE 3

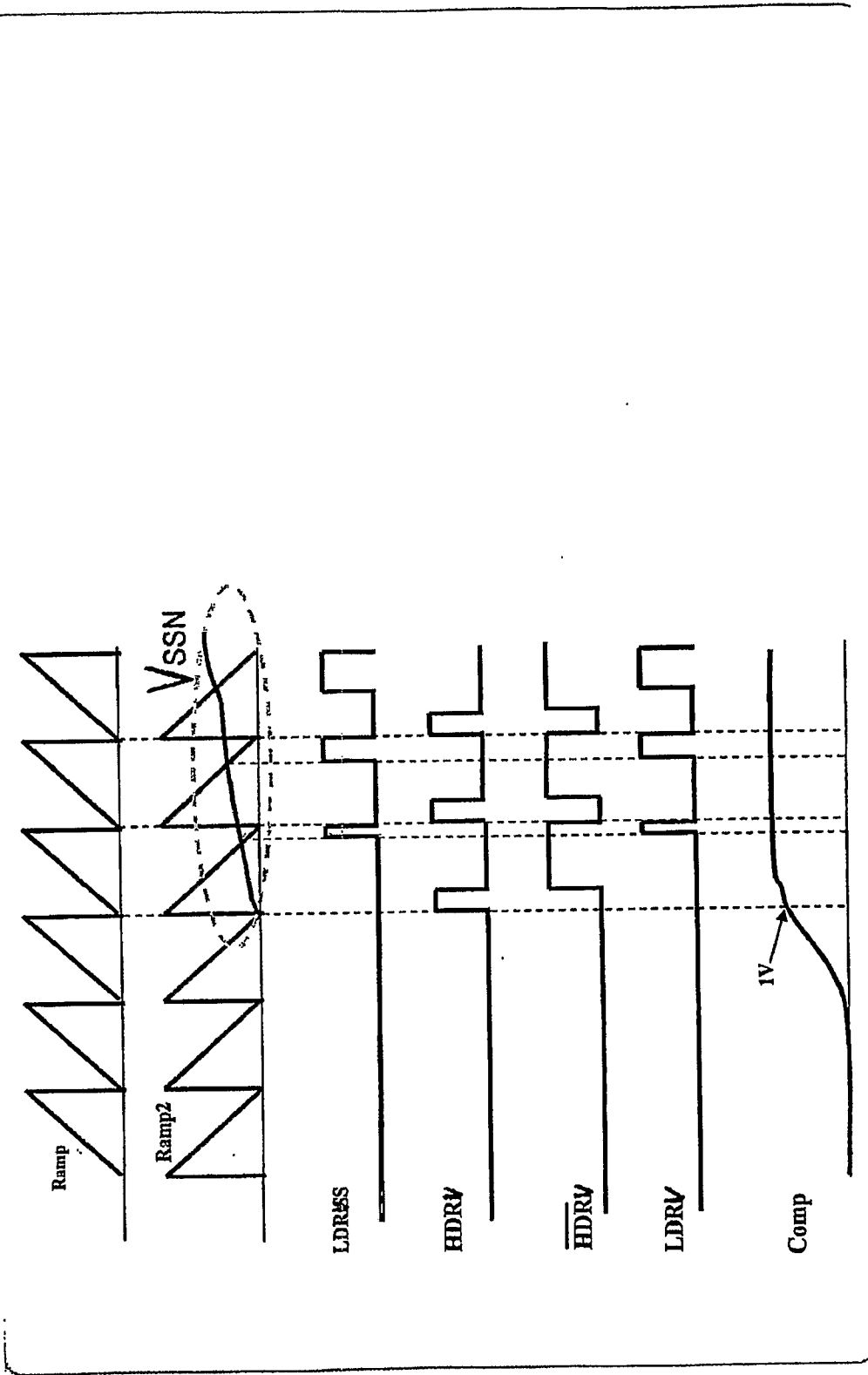


Figure 4

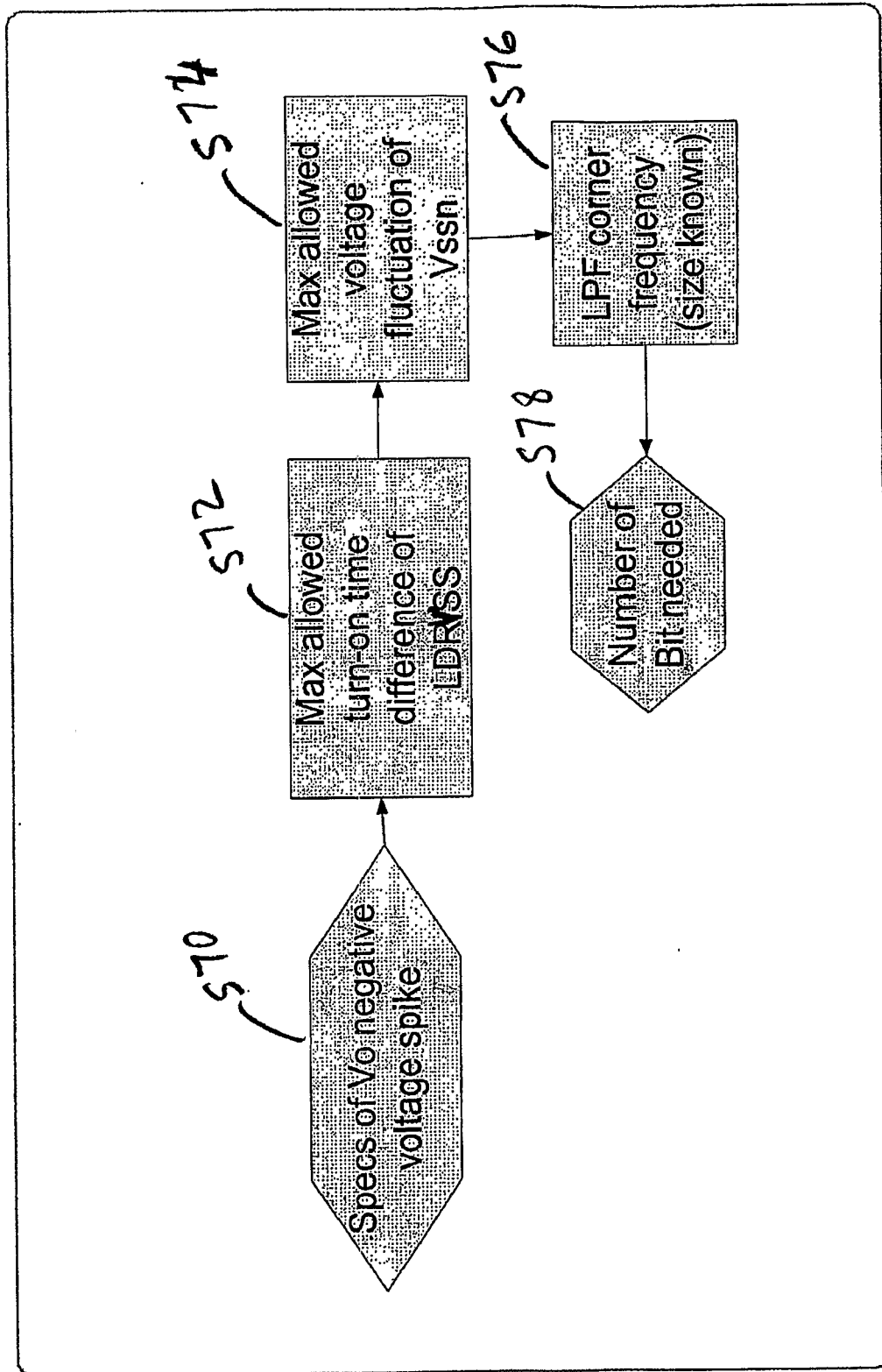


Figure 5a

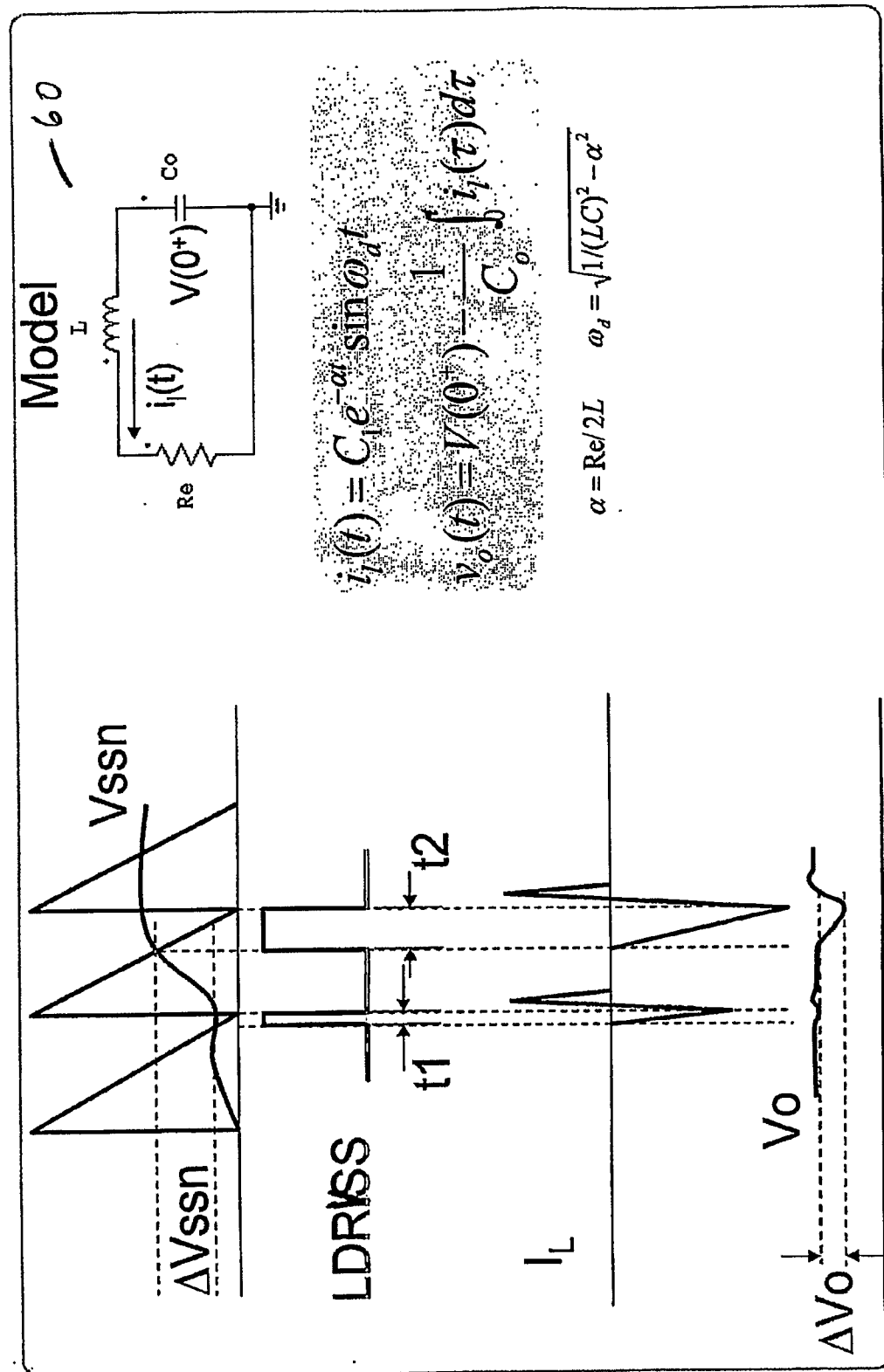


Figure 5b

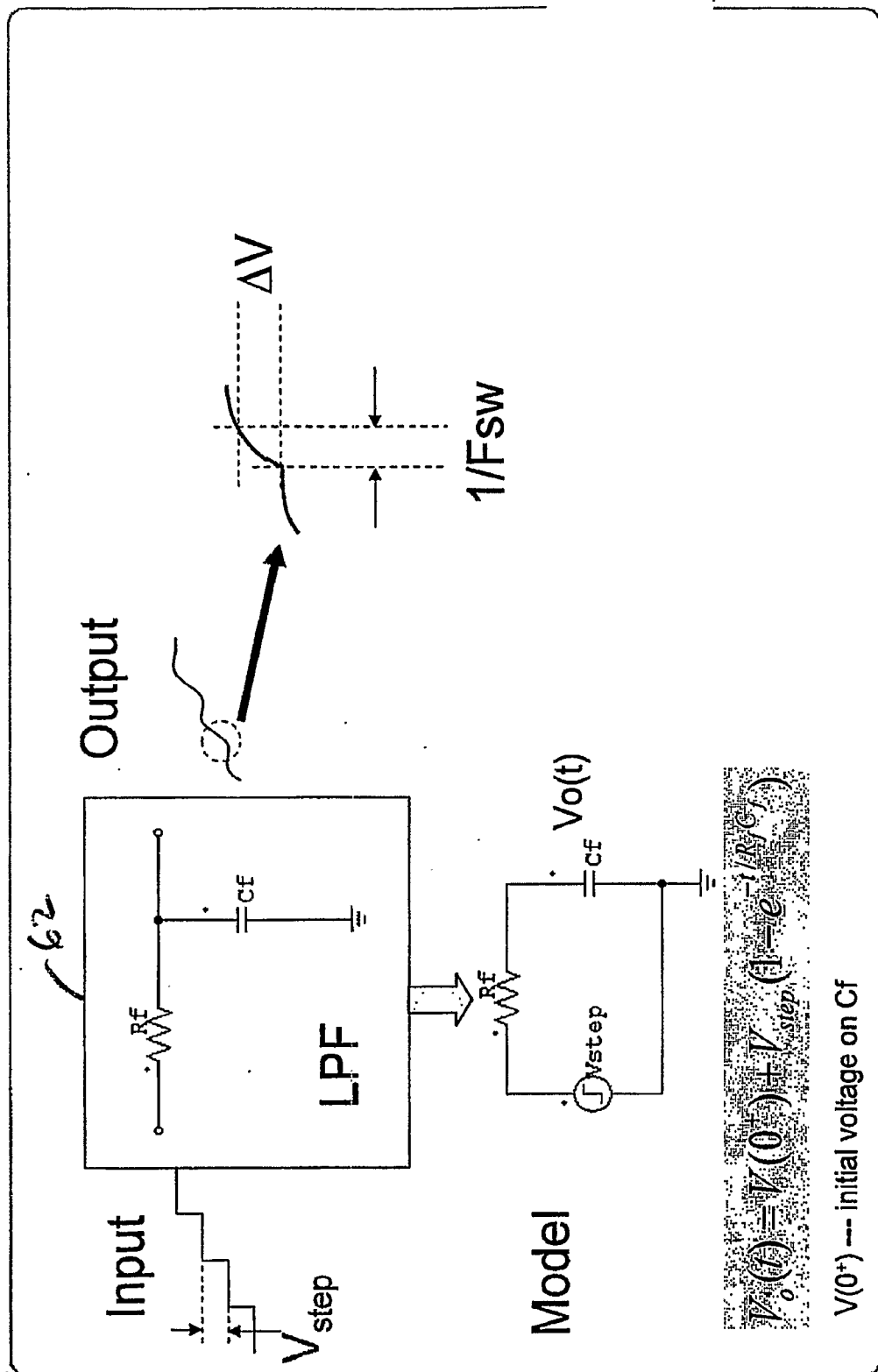
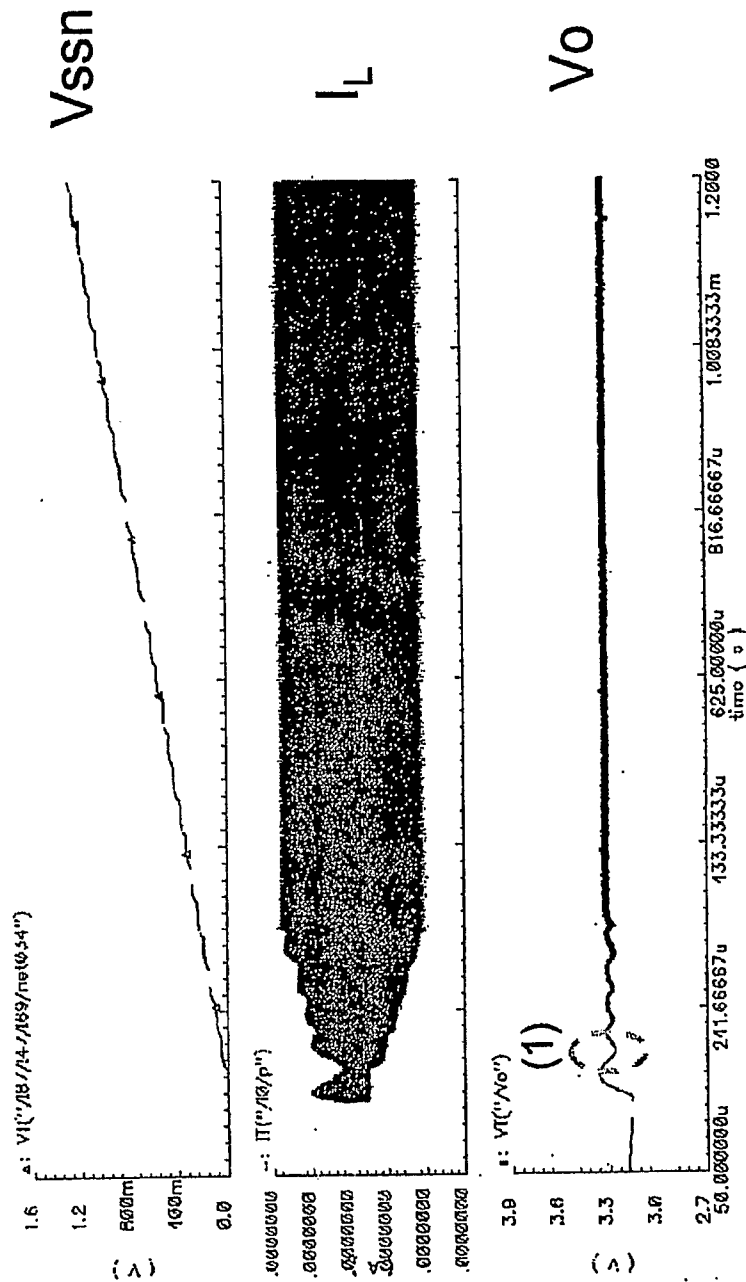
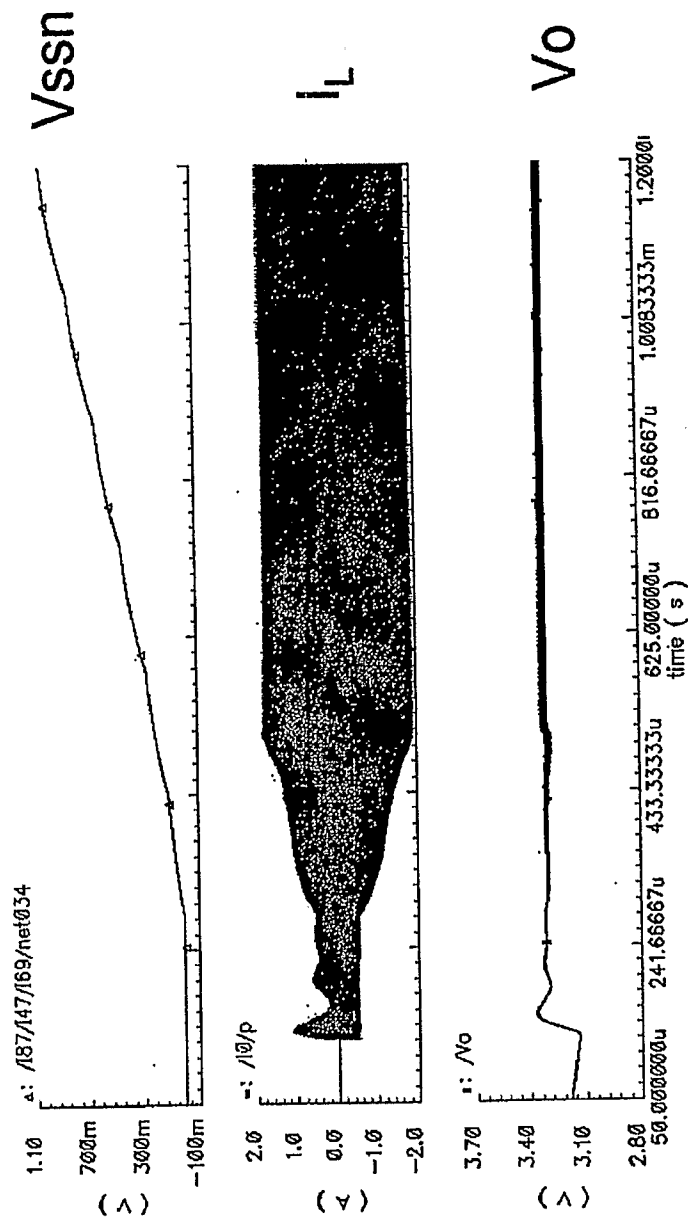


FIGURE 56



Specs: $V_{in}=5.5V$, $V_o=3.3V$ (regulated), $F_s=1.25MHz$, $L=300nH$, $C_o=10uF$.
 LPF $R_f=8MOhm$, $C_f=1pF$ ($F_c=20kHz$), DAC Bit=5.

Figure 6a.



Specs: $V_{in}=5.5V$, $V_o=3.3V$ (regulated), $F_s=1.5MHz$, $L=300nH$, $C_o=10\mu F$.
 LF filter $R_f=8M\Omega$, $C_f=20pF$ ($F_c=500Hz$), DAC Bit=3.

Figure 6b

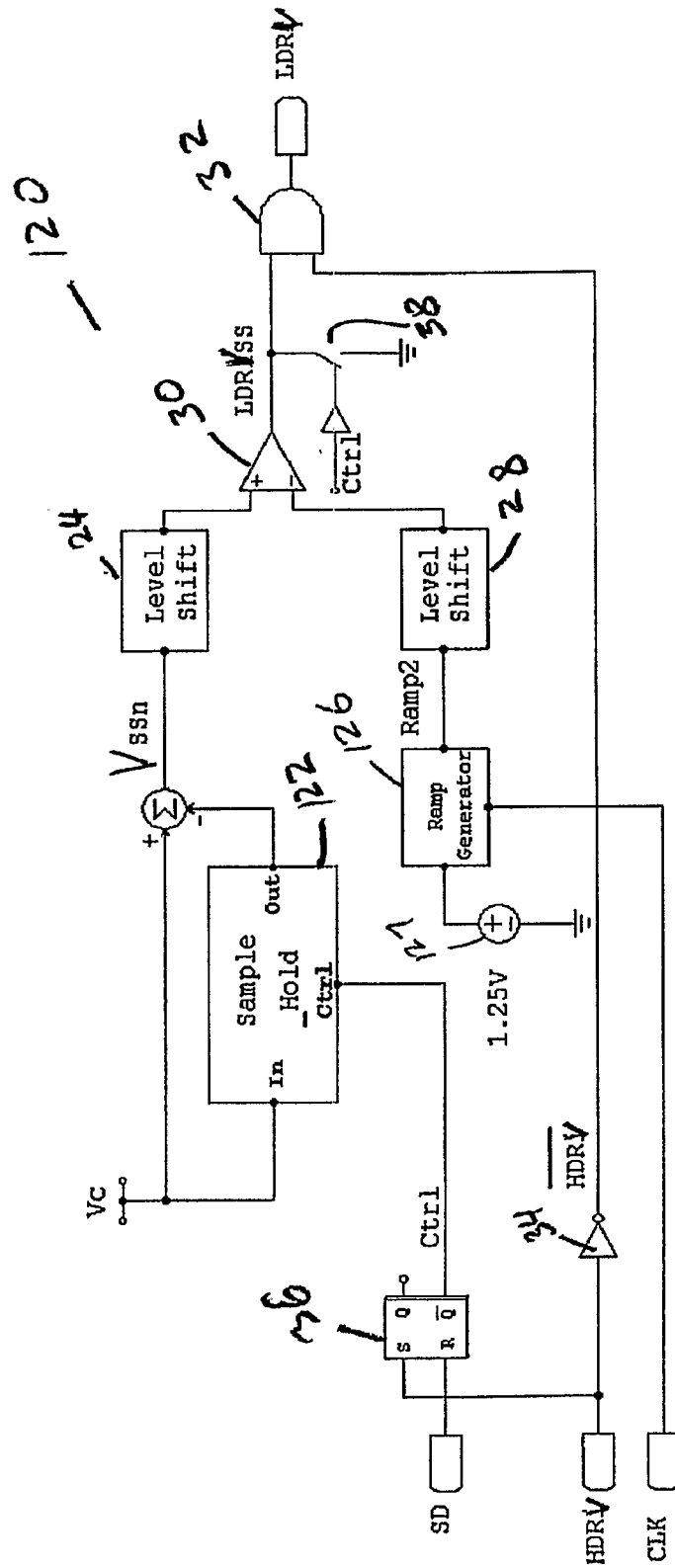


Figure 7

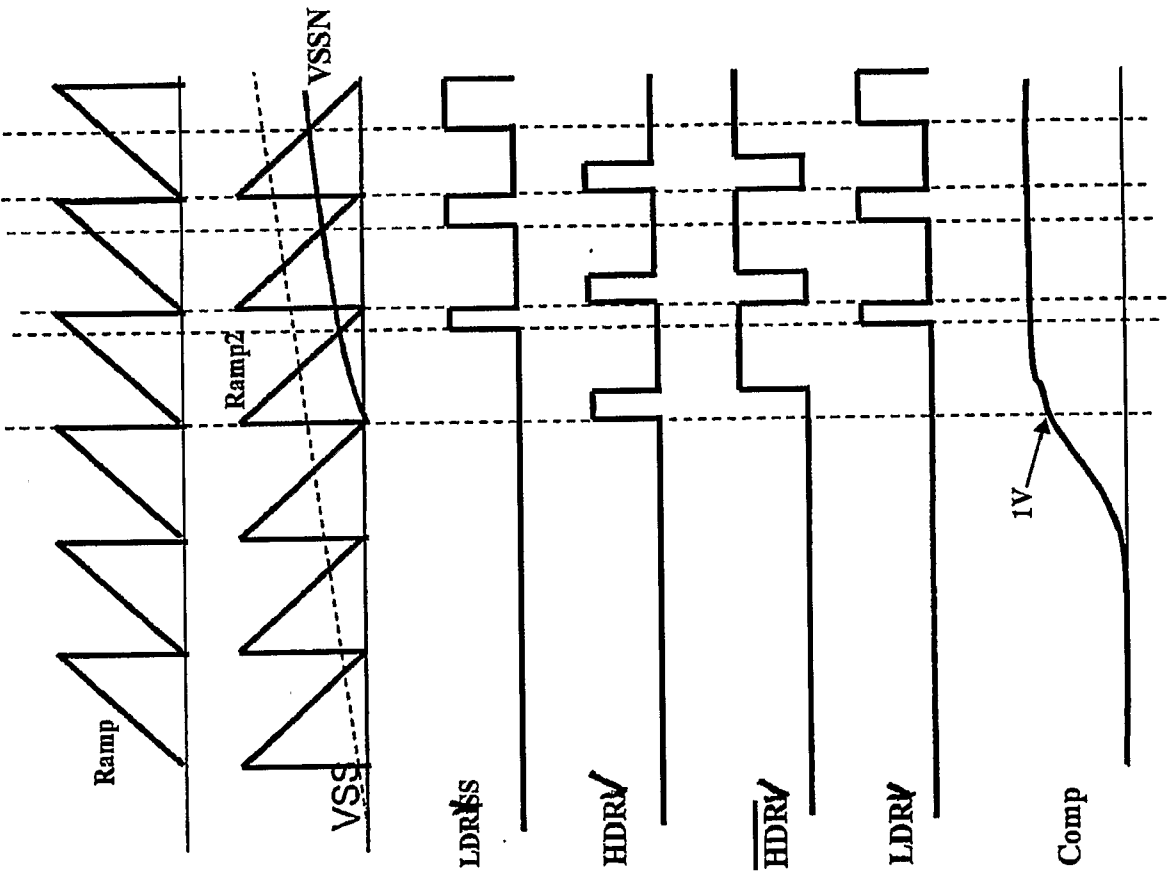


Figure 8

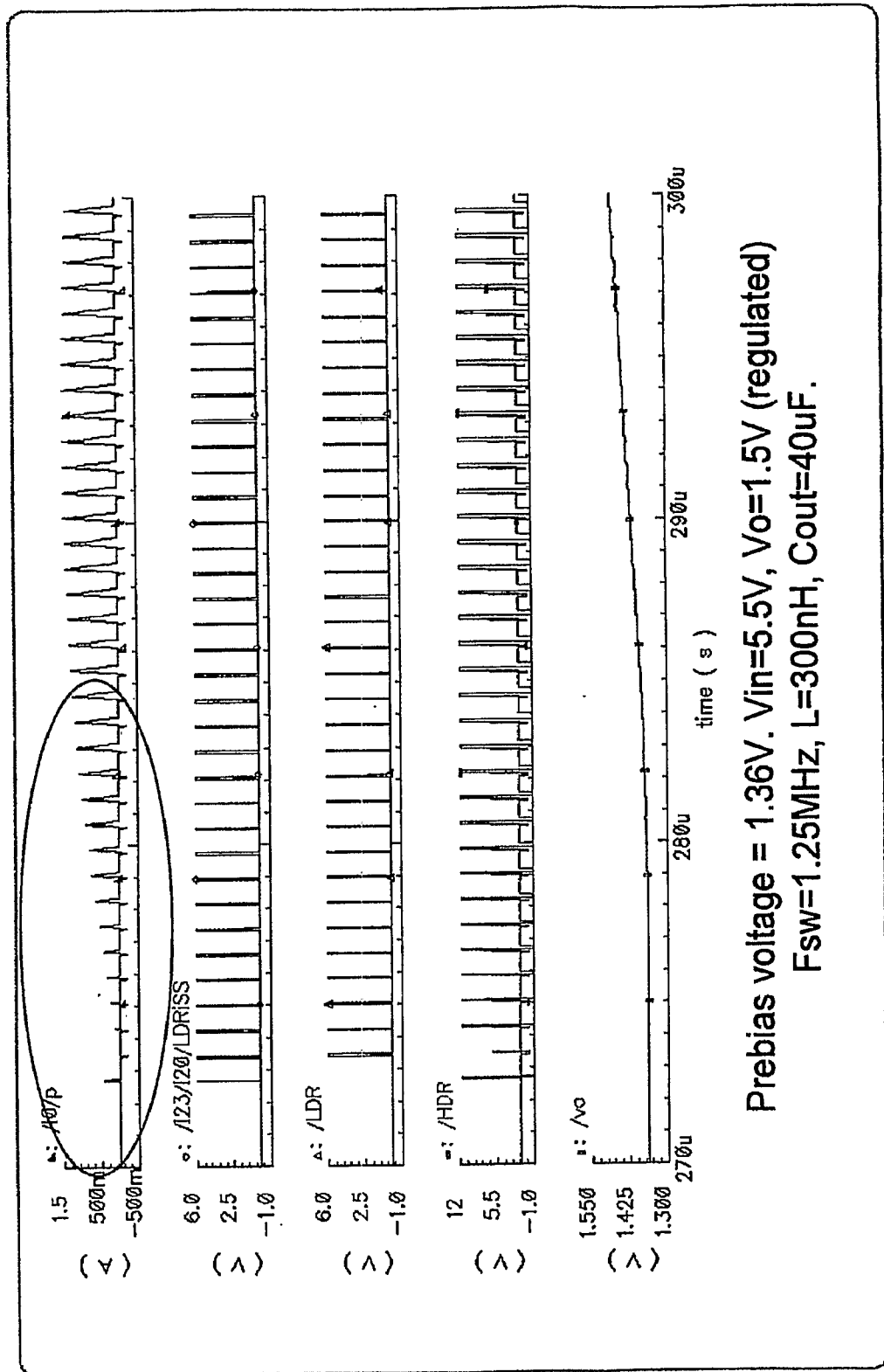
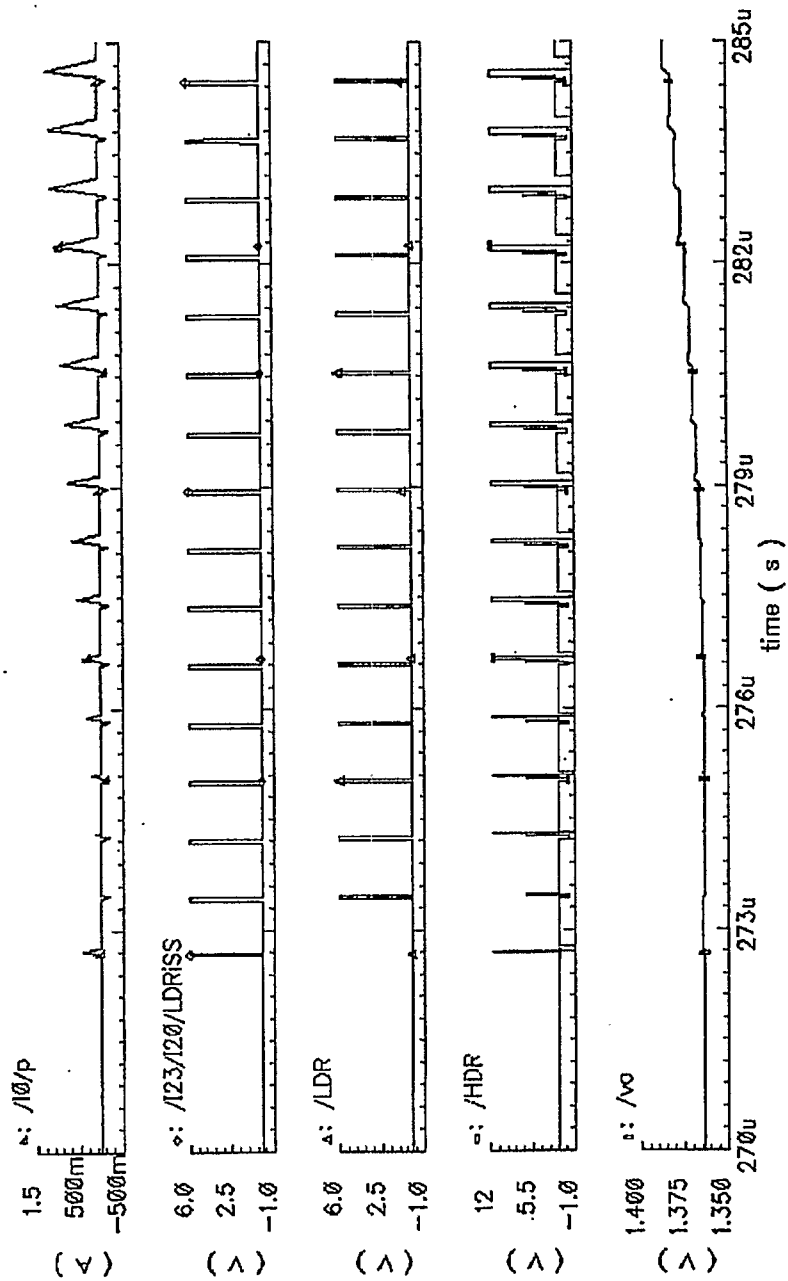


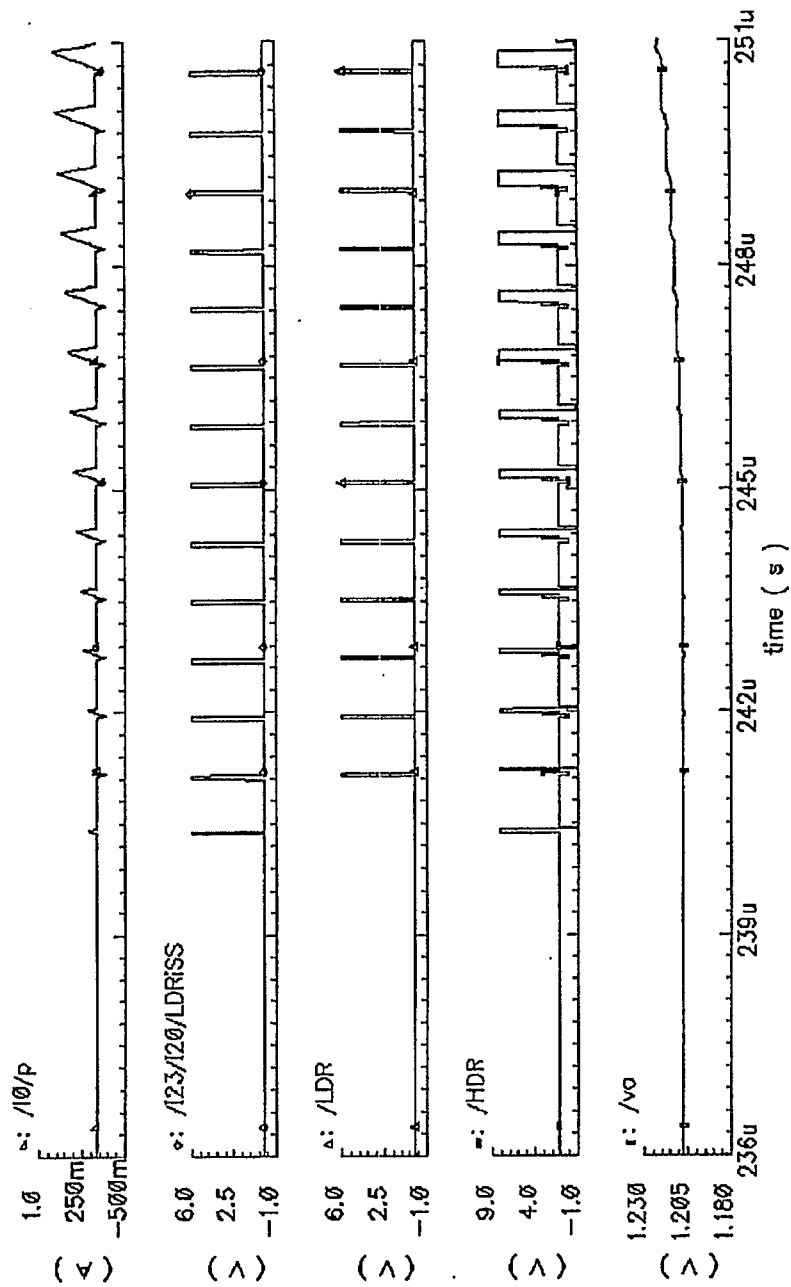
FIGURE 9a



Prebias voltage = 1.36V. $V_{in}=5.5V$, $V_o=1.5V$ (regulated)

$F_{sw}=1.25MHz$, $L=300nH$, $C_{out}=40\mu F$.

FIGURE 9b



Prebias voltage = 1.2V. $V_{in}=2.25V$, $V_o=1.5V$ (regulated)
 $F_{sw}=1.25MHz$, $L=300nH$, $C_{out}=40uF$.

Figure 9c