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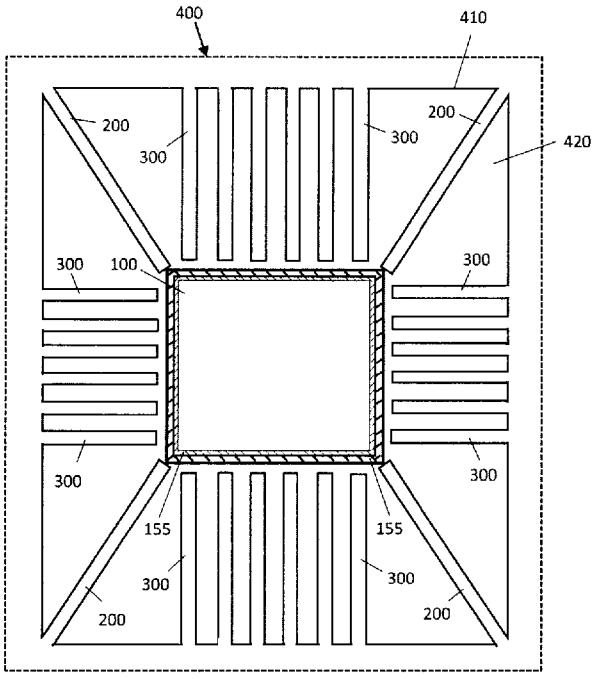

Figure 1

(57) Abstract: The present invention introduced a lead frame (400) with a base (100) that has both solder wettability and non-solder wettability features for single or multiple chip applications for separating chips (500) or isolating at least one chip (500) from electrical conductivity. The lead frame (400) enables a precise and uniform attachment of the chip (500) without affecting the bond line thickness (BLT) height, thus preventing the chip (500) from breaking and tilting. Besides that, the lead frame (400) reduce the capillarity of the solder (550) at the appropriate places during soldering and prevent the solder (550) from overflowing. The lead frame (400) comprises a framework (410); a base (100) with features for selective soldering; a plurality of tie bars (200); and a plurality of leads (300). The features for selective soldering include non solder-wettable region (155), at least one non solder-wettable stripe (160), at least one non solder-wettable patch (170), or a combination of the features.

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A LEAD FRAME FOR SELECTIVE SOLDERING

TECHNICAL FIELD OF THE INVENTION

This invention relates to a semiconductor packaging, and more particularly to a lead frame with a base that has both solder wettability and non-solder wettability properties for selective soldering.

BACKGROUND OF THE INVENTION

Soft soldering is a process of joining different types of metals, and is especially useful for small, intricate parts that are prone to damage by processes requiring higher temperatures. A lead frame for power package with an exposed heat sink is commonly used for soft soldering for heat dissipation in operation involving high temperature. The lead frame also provides a stable pad for the firm positioning and attachment of one or more chips. Besides that, the lead frame provides connections between the chip/s in the package and the external print circuit board (PCB).

In the soft soldering die attach process, soft solder is generally used as an adhesive to bond the chip to the pad due to its high thermal and electrical conductivity. As the size of chip packaging continues to shrink in current efforts to reduce cost and improve performance, chip size remains largely unchanged, causing the gap between the chip and the border of the pad to become critically smaller. This is especially evident in soft soldering, as the process is carried out with molten solder, complicating the control of solder flow. Further, during the bonding step in soft soldering, the chip needs to be pressed all the way down to the pad to eliminate potential air bubbles within the molten solder underneath the chip, which can cause voids in the bond line itself after bonding. This bonding step squeezes solder out towards the pad edge, but will flow back towards the pad when the bond force is released. When solder is squeezed out, it may come into contact with the pad edge or wall. The wetting nature of the pad edge allows solder to wet the pad edge. This prevents solder from flowing back towards the

pad, leading to low bond line thickness (BLT) or high chip tilt. Thus, limited control over the flow of the solder in the chip bonding step can contribute to higher chip failure rates.

Chip crack is commonly recognized as a critical failure mode, especially in power semiconductor applications. Chip crack occurrence may be contributed by the inconsistent flow of solder during the chip bonding. However, they are harder to detect due to their low occurrence rate and could fail during product service life. For maximum thermal performance and quality control of the soft soldering process, full and precise solder coverage needs to be applied appropriately under the chip to control BLT and chip tilt, and ensure reliable packaging without solder overflow from the pad.

In view of the problems above, there is a demand in the semiconductor industry to provide a method for more control over the soft solder process. Existing methods mainly control the dispensing and shaping of solder before the chip bonding step. For example, US Patent no. 6056184 A disclosed an apparatus for dispensing and shaping the shape of solder before positioning the chip. In another example, US Patent no. 5878939 A describes a method and apparatus to improve the dispensing and flow of liquid solder for chip bonding. Conversely, patent application WO 2001091175 A1 discloses a method and apparatus for effectively dispensing liquid solder while reducing leakages of solder through a frame with solder tight seal. However, the methods and apparatuses of the prior arts are inadequate in preventing the solder from flowing to the edge of the pad and the chip perimeter during the chip bonding process.

In US patent nos. 6,518,647 B1 and 8,716,069, it is disclosed that the lead frame has a base made of aluminium or aluminium alloy with many layers deposited onto the aluminium. However, the risk of overflowing solder wetting the spaces around the pad that contain materials of high solder wettability remains. In another example, the invention in US patent publication no. 20100009500 provides a method for manufacturing an aluminium alloy lead frame with a noble metal electroplating layer deposited on the lead frame. Not only is the method of

the prior art expensive, it risks molten solder wetting the metal, spaces around the pad, and the edge of the pad, potentially allowing solder flow outward from the pad to surrounding the chip. As the solder solidifies, it will be difficult to remove solder that flowed into undesired spaces, adversely affecting the overall electrical conductivity of the chip package.

It can be seen that a lead frame capable of selecting its solder wettability while allowing precise chip attachment to the chip carrier without affecting the BLT height is thus far unavailable in the industry. Accordingly, there is a need to provide a lead frame of such.

SUMMARY OF THE INVENTION

It is an objective of the present invention to provide a lead frame with a base capable of selecting its solder wettability by having both solder wettability and non-solder wettability features. The lead frame enables a precise attachment of a chip to the base as solder can be carefully dispensed onto the solder-wettable region of the base, resulting in better bond line thickness (BLT) through the improved control of solder flow.

It is a further objective of the present invention to provide a lead frame with a base that controls the flow of solder to control BLT and prevent chip tilt.

It is also an objective of the present invention to provide a lead frame with a base for selective soldering by having a non solder-wettable region that reduces the capillarity of solder at spaces unintended for solder wetting, preventing the solder from wetting and resting on the non solder-wettable region. The non-solder wettability feature of the base also prevents the solder from flowing out when the solder touches the non solder-wettable regions in soft soldering when the chip is pressed all the way down to the base and squeezes solder out towards the edge of the base.

It is an objective of the present invention to prevent the excessive flow of solder and allow the solder to confine itself to the solder-wettable regions. It is also an objective of the present invention to prevent solder from resting and solidifying on unintended surfaces through the use of non solder-wettable regions.

It is yet an objective of the present invention to provide a base that can be used for single chip application and multiple chip applications. The base of the lead frame may include at least one non solder-wettable stripe, at least one non solder-wettable patch, or a combination of both for separating chips or isolating at least one chip from electrical conductivity in multiple chip applications.

For single chip application, the present invention includes a lead frame for selective soldering comprising: a framework that defines a cavity, wherein a plurality of leads extend inwardly from the framework; a base located inside the cavity; a plurality of tie bars connecting the base to the lead frame; and a chip resting on the base through soldering; characterised in that: the base is solder-wettable for solder adhesion; and the base has a non solder-wetttable region at the edge of the base.

For multiple chip applications wherein all the chips are subjected to electrical conductivity, the lead frame may include: the framework that defines the cavity, wherein the plurality of leads extend inwardly from the framework; the base located inside the cavity; the plurality of tie bars connecting the base to the lead frame; and a plurality of chips resting on the base through soldering; characterised in that: the base is solder-wettable for solder adhesion; the base has the non solder-wetttable region at the edge of the base; and the base has at least one non solder-wettable stripe for separating each of the plurality of chips.

The present invention can also include a lead frame for multiple chip applications with at least one of the chips isolated from electrical conductivity, wherein the lead frame comprises: the framework that defines the cavity, wherein the plurality of leads extend inwardly from the framework; the base located inside the cavity; the plurality of tie bars connecting the base to the lead frame; and the

plurality of chips resting on the base through soldering; characterised in that: the base is solder-wettable for solder adhesion; the base has the non solder-wetttable region at the edge of the base; and the base has at least one non solder-wettable patch for isolating at least one of the plurality of chips from conductivity.

BRIEF DESCRIPTION OF THE DRAWINGS

The features of the invention will be more readily understood and appreciated from the following detailed description when read in conjunction with the accompanying drawings of the preferred embodiment of the present invention, in which:

Figure 1 shows a top view of a lead frame for single chip application.

Figure 2 shows a side view of a single chip on the lead frame.

Figure 3 shows a top view of the lead frame for separating the conductivity of a plurality of chips.

Figure 4 shows a side view of the lead frame with at least one non solder-wettable stripe for separating the plurality of chips.

Figure 5 shows a top view of the lead frame for isolating at least one of the plurality of chips from conductivity.

Figure 6 shows a side view of the lead frame with at least one chip conducted and at least another chip isolated from conductivity.

Figure 7 shows a top view of the lead frame with partial plating on a plurality of leads.

Figure 8 shows a top view of the lead frame with full plating on the plurality of leads.

Figure 9 shows a side view of the lead frame having a base without peripheral wall.

DETAILED DESCRIPTION OF THE INVENTION

The above-mentioned and other features and objects of this invention will become more apparent and better understood by reference to the following detailed description. It should be understood that the detailed description made known below is not intended to be exhaustive or to limit the invention to the precise disclosed form as the invention may assume various alternative forms. On the contrary, the detailed description covers all the relevant modifications and alterations made to the present invention, unless the claims expressly state otherwise. The present invention will now be described with reference to Figures 1 to 9.

Figures 1 and 2 are related to an embodiment of the present invention for single chip application. By referring to both Figure 1 to Figure 2, the present invention relates to a lead frame (400) for selective soldering comprises: a framework (410) that defines a cavity (420), wherein a plurality of leads (300) extend inwardly from the framework (410); a base (100) located inside the cavity (420); a plurality of tie bars (200) connecting the base (100) to the lead frame (400); and a chip (500) resting on the base (100) through soldering; characterised in that: the base (100) is solder-wettable for solder (550) adhesion; and the base (100) has a non solder-wetttable region (155) at the edge of the base (100). Figure 2 also shows a side view of the lead frame (400) when soldering the chip (500) to the base (100), wherein the solder (550) is evenly distributed on the base (100) for the chip (500) to sit flatly on it and not be tilted.

An embodiment of the present invention also allows the lead frame (400) to be used for multiple chip applications. Referring to Figure 3 and Figure 4, the lead

frame (400) for selective soldering for multiple chip application comprises: the framework (410) that defines the cavity (420), wherein the plurality of leads (300) extend inwardly from the framework (410); the base (100) located inside the cavity (420); the plurality of tie bars (200) connecting the base (100) to the lead frame (400); and a plurality of chips (500) resting on the base (100) through soldering; characterised in that: the base (100) is solder-wettable for solder adhesion (550); the base (100) has the non solder-wetttable region (155) at the edge of the base (100); and the base (100) has at least one non solder-wettable stripe (160) for separating each of the plurality of chips (500). Figure 4 also shows a side view of the lead frame (400) when soldering the plurality of chips (500) to the base (100), wherein the plurality of chips (500), including the solder (550), are separated by the non solder-wettable stripe (160).

The present invention is also related to multiple chip applications specifically for isolating at least one chip (500) from electrical conductivity. Referring to Figure 5 and Figure 6, the lead frame (400) for selective soldering for multiple chip applications specifically isolating at least one chip (500) from electrical conductivity comprises: the framework (410) that defines the cavity (420), wherein the plurality of leads (300) extend inwardly from the framework (410); the base (100) located inside the cavity (420); the plurality of tie bars (200) connecting the base (100) to the lead frame (400); and the plurality of chips (500) resting on the base (100) through soldering; characterised in that: the base (100) is solder-wettable for solder (550) adhesion; the base (100) has the non solder-wetttable region (155) at the edge of the base (100); and the base (100) has at least one non solder-wettable patch (170) for isolating at least one of the plurality of chips (500) from conductivity. Figure 6 also shows a side view of the lead frame (400) when soldering at least one of the plurality of chips (500) to the base (100) and isolating at least another chip (500) on the non solder-wettable patch (170) on the base (100).

In an embodiment of the present invention, the base (100) is made from materials comprising metal or metal alloy. In another embodiment of the present invention, the base (100) is made of copper or copper alloy. The metal or metal

alloy materials allow the base (100) to be solder-wettable. The base (100) can also have at least one non solder-wettable stripe (160), at least one non solder-wettable patch (170), or a combination of both for separating chips (500) or isolating at least one chip (500) from electrical conductivity in multiple chip applications. Besides that, the base (100) has the non solder-wettable region (155) surrounding the edge of the base (100) to restrict the flow of the solder (550) during the soldering process. In the present invention, the base (100) can take any shape and form, for example square or round and *etc.*, whichever a person skilled in the art thinks is fit for the lead frame (400) and chip packaging. In another embodiment of the present invention, the base (100) is suspended in the cavity (420) and supported by at least four tie bars (200).

In an embodiment of the present invention, the lead frame (400) is made from materials comprising metal or metal alloy. In another embodiment of the present invention, the lead frame (400) is made of copper or copper alloy. The lead frame (400) can be formed by cutting, stamping or etching, whichever a person skilled in the art would apply. The present invention also allows the lead frame (400) to take any desired shape and form as desired, for example, square or round *etc.*, whichever a person skilled in the art thinks is fit for the base (100) and chip packaging. The lead frame (400) also allows electrical conductivity to flow from the chip (500) to the other desired parts. In an embodiment of the present invention, the lead frame (400) comes in a plurality, wherein the plurality of the lead frames (400) are connected together and are linked to a main frame (not shown in the Figures).

The materials of the non solder-wettable region (155), the non solder-wettable stripe (160), and the non solder-wettable patch (170) exhibit characteristic that is capable of self-passivating itself or can be passivated to produce a stable passivation layer which then becomes the non solder-wettable region (155). A person skilled in the art would be able to identify the materials that are self-passivating and the list of materials included herein is not intended to limit the present invention. In an embodiment of the present invention, each of the non solder-wettable region (155), the non solder-wettable stripe (160), and the non

solder-wettable patch (170) is plated with materials comprising metal, metal oxide, or metal nitride. Due to the process of oxidation that occurs naturally in the atmosphere, the metal plating is oxidized to metal oxide which then becomes the passivation layer. In a further embodiment, each of the non solder-wettable region (155), the non solder-wettable stripe (160), and the non solder-wettable patch (170) is plated with nickel, nickel oxide, aluminium, aluminium oxide, zinc, zinc oxide, zincate, or chromium. It is an advantage to use metal oxide as all metal oxide reduction usually have a higher temperature compared to the temperature required for soft solder die attachment i.e. 300-400 °C. Nickel plating or nickel oxide is an embodiment preferred in the present invention as nickel is a common material used in existing lead frame plating industry without the need to undergo plating line modification. The reduction of the nickel occurs at the temperature of 600°C, which is highly unlikely to be affected by the lower soldering temperature.

In another embodiment of the present invention, the plurality of tie bars (200) and the plurality of leads (300) are made of metal or metal alloy. In an embodiment of the present invention, the plurality of tie bars (200) and the plurality of leads (300) are made of copper or copper alloy.

An embodiment of the present invention describes that both of the plurality tie bars (200) and the plurality of leads (300) are not plated with the non solder-wettable region (155) as shown in Figures 1 to 6.

In another embodiment of the present invention, the plurality of tie bars (200) are fully plated or partially plated with the non solder-wettable region (155) as shown in Figure 7 and Figure 8 respectively. In a further embodiment of the present invention, the plurality of leads (300) are partially plated with the non solder-wettable region (155) at the tip nearer to the base (100) as shown in Figure 7. It is also possible that the plurality of leads (300) are fully plated with the non solder-wettable region (155) as shown in Figure 8. The embodiments of the plurality of tie bars (200) and the plurality of leads (300) are applicable for single chip application and multiple chip applications. Although the plurality of leads

(300) are shown to have same length and width, the plurality of leads (300) may also vary in length in width.

In an embodiment of the present invention, the plurality of leads (300) are fully or partially plated with a dense and thermally stable passivation layer. The passivation layer protects the plurality of leads (300) from further oxidation, increases electrical resistance between the plurality of leads (300), and reduces electrical leakage in certain applications, while allowing for improved lead adhesion to molding compounds.

In a further embodiment of the present invention, the base (100) further comprises a peripheral wall (150) surrounding the base (100). The base (100) with the peripheral wall (150) is shown in Figures 2, 4, and 6. The peripheral wall (150) is capable of preventing the solder (550) from flowing out of the base (100). In another embodiment, the peripheral wall (150) also has the non solder-wettable region (155) for restricting the flow of the solder (550). During soldering process, the peripheral wall (150) prevents solder (550) from flowing excessively to the cavity (420). In an embodiment of the present invention, the non solder-wettable region (155) of the peripheral wall (150) is adapted to block the spreading of solder (550) from the base (100). By referring to Figure 2, Figure 4, and Figure 6, the non solder-wettable material may coat the inner side of the peripheral wall (150) where the possibility of the solder (550) touching the peripheral wall (150) is higher during the dispensing of the solder (550) onto the base (100). In the case where the solder (550) touches the peripheral wall (150) during the soldering process especially when the chip (500) is pressed all the way down to the base (100) and squeezes solder out towards the edge of the base (100), the solder (550) is unlikely to disperse due to the weak solder wettability and capillarity against the non solder-wettable region (155). This positive result reduces the risk of having an excessively low or a high BLT, and of tilting and chipping of the chip (500) during soldering. In another embodiment of the present invention, the base (100) is a flat structure and does not have the peripheral wall (150) as shown in Figure 9.

It is understood herein that the solder (550) acts as an adhesive to bond the chip (500) to the base (100). The base (100) herein can also refer to as a chip carrier, a substrate, or a pad. The present invention may include an embodiment wherein, the adhesion between the chip (500) to the base (100) should not be limited to solder (550) only, but other conductive adhesives that are suitable for bonding the chip (500) to the base (100).

It is also understood from Figure 2, Figure 4, and Figure 6 that the present invention has an embodiment wherein the non solder-wettable region (155) also include the intersection where the base (100) meets the peripheral wall (150). A person skilled in the art may coat any part of the base (100), the peripheral wall (150), the plurality of tie bars (200), the plurality of leads (300), and the framework (410), or wherever that the person regards as necessary to prevent unequal BLT height, chip (500) tilting and breaking, and overflow of solder (550).

Although the present invention has been described with reference to specific embodiments, it will be apparent for those skilled in the art that many variations and modifications can be done within the scope of the invention as described in the specification and defined in the following claims.

CLAIMS

1. A lead frame (400) for selective soldering comprising:

   a) a framework (410) that defines a cavity (420), wherein a plurality of leads (300) extend inwardly from the framework (410);
   b) a base (100) located inside the cavity (420);
   c) a plurality of tie bars (200) connecting the base (100) to the lead frame (400); and
   d) a chip (500) resting on the base (100) through soldering;

   characterised in that:

   e) the base (100) is solder-wettable for solder (550) adhesion; and
   f) the base (100) has a non solder-wetttable region (155) at the edge of the base (100).

2. A lead frame (400) according to claim 1, wherein the base (100) is made from materials comprising metal or metal alloy.

3. A lead frame (400) according to claim 1, wherein the lead frame (400) is made from materials comprising metal or metal alloy.

4. A lead frame (400) according to claim 1, wherein the non solder-wettable region (155) comprises a passivation layer.

5. A lead frame (400) according to claim 1, wherein the non solder-wettable region (155) is made from materials comprising metal, metal oxide, or metal nitride.

6. A lead frame (400) according to claim 1, wherein the plurality of leads (300) is fully plated with the non solder-wettable region (155).

7. A lead frame (400) according to claim 1, wherein the plurality of leads (300) is partially plated with the non solder-wettable region (155) at the tip nearer to the base (100).

8. A lead frame (400) according to claim 1, wherein the base (100) further comprises a peripheral wall (150).

9. A lead frame (400) according to claim 8, wherein the peripheral wall (150) further comprises the non solder-wettable region (155).

10. A lead frame (400) according to claim 1, wherein the base (100) comprises a flat structure and does not have a wall surrounding the edge of the base (100).

11. A lead frame (400) for selective soldering comprising :

a) a framework (410) that defines a cavity (420), wherein a plurality of leads (300) extend inwardly from the framework (410);
b) a base (100) located inside the cavity (420);
c) a plurality of tie bars (200) connecting the base (100) to the lead frame (400); and
d) a plurality of chips (500) resting on the base (100) through soldering;

characterised in that:

e) the base (100) is solder-wettable for solder adhesion (550);
f) the base (100) has a non solder-wetttable region (155) at the edge of the base (100); and
g) the base (100) has at least one non solder-wettable stripe (160) for separating each of the plurality of chips (500).

12. A lead frame (400) according to claim 11, wherein the base (100) is made from materials comprising metal or metal alloy.

13. A lead frame (400) according to claim 11, wherein the lead frame (400) is made from materials comprising metal or metal alloy.

14. A lead frame (400) according to claim 11, wherein the non solder-wettable stripe (160) is made from materials comprising metal, metal oxide, or metal nitride.

15. A lead frame (400) according to claim 11, wherein the non solder-wettable stripe (160) comprises a passivation layer.

16. A lead frame (400) according to claim 11, wherein the non solder-wettable region (155) is made from materials comprising metal, metal oxide, or metal nitride.

17. A lead frame (400) according to claim 11, wherein the non solder-wettable region (155) comprises a passivation layer.

18. A lead frame (400) according to claim 11, wherein the plurality of leads (300) is fully plated with the non solder-wettable region (155).

19. A lead frame (400) according to claim 11, wherein the plurality of leads (300) is partially plated with the non solder-wettable region (155) at the tip nearer to the base (100).

20. A lead frame (400) according to claim 11, wherein the base (100) further comprises a peripheral wall (150).

21. A lead frame (400) according to claim 20, wherein the peripheral wall (150) further comprises the non solder-wettable region (155).

22. A lead frame (400) according to claim 11, wherein the base (100) comprises a flat structure and does not have a wall surrounding the edge of the base (100).

23. A lead frame (400) for selective soldering comprising:

a) a framework (410) that defines a cavity (420), wherein a plurality of leads (300) extend inwardly from the framework (410);
b) a base (100) located inside the cavity (420);
c) a plurality of tie bars (200) connecting the base (100) to the lead frame (400); and
d) a plurality of chips (500) resting on the base (100) through soldering;

characterised in that:

a) the base (100) is solder-wettable for solder (550) adhesion;
b) the base (100) has a non solder-wetttable region (155) at the edge of the base (100); and
c) the base (100) has at least one non solder-wettable patch (170) for isolating at least one of the plurality of chips (500) from conductivity.

24. A lead frame (400) according to claim 23, wherein the base (100) is made from materials comprising metal or metal alloy.

25. A lead frame (400) according to claim 23, wherein the lead frame (400) is made from materials comprising metal or metal alloy.

26. A lead frame (400) according to claim 23, wherein the non solder-wettable patch (170) is made from materials comprising metal, metal oxide, or metal nitride.

27. A lead frame (400) according to claim 23, wherein the non solder-wettable patch (170) comprises a passivation layer.

28. A lead frame (400) according to claim 23, wherein the non solder-wettable region (155) is made from materials comprising metal, metal oxide, or metal nitride.

29. A lead frame (400) according to claim 23, wherein the non solder-wettable region (155) comprises a passivation layer.

30. A lead frame (400) according to claim 23, wherein the plurality of leads (300) is fully plated with the non solder-wettable region (155).

31. A lead frame (400) according to claim 23, wherein the plurality of leads (300) is partially plated with the non solder-wettable region (155) at the tip nearer to the base (100).

32. A lead frame (400) according to claim 23, wherein the base (100) further comprises a peripheral wall (150).

33. A lead frame (400) according to claim 32, wherein the peripheral wall (150) further comprises the non solder-wettable region (155).

34. A lead frame (400) according to claim 23, wherein the base (100) comprises a flat structure and does not have a wall surrounding the edge of the base (100).

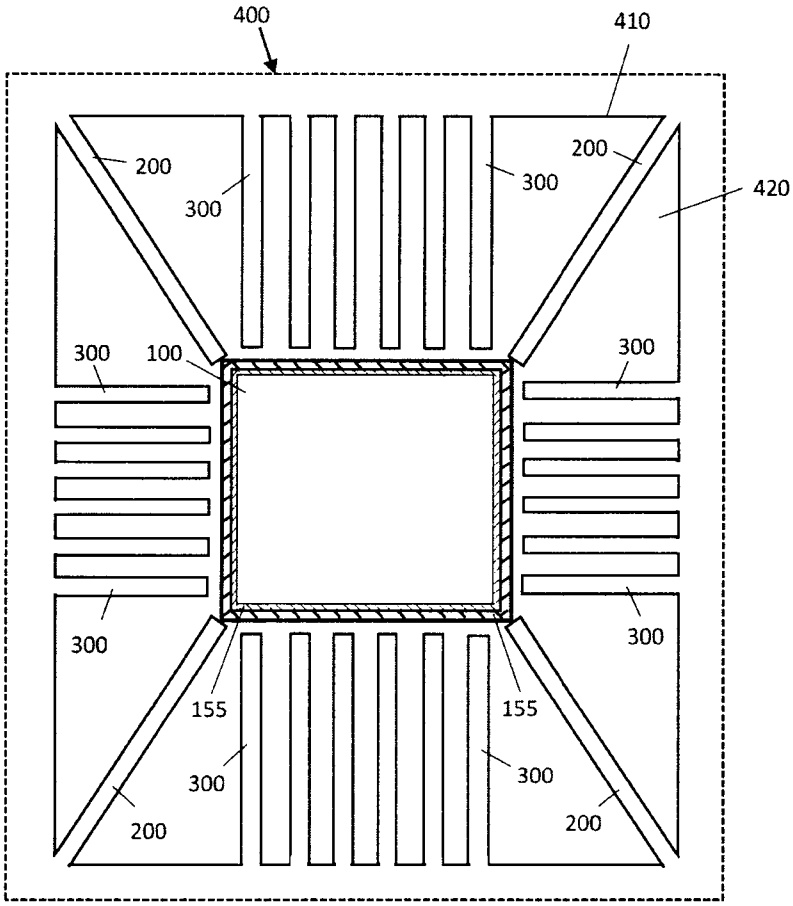

Figure 1

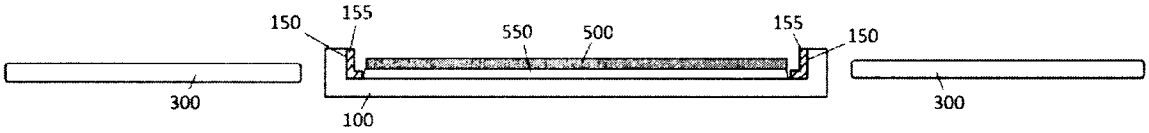

Figure 2

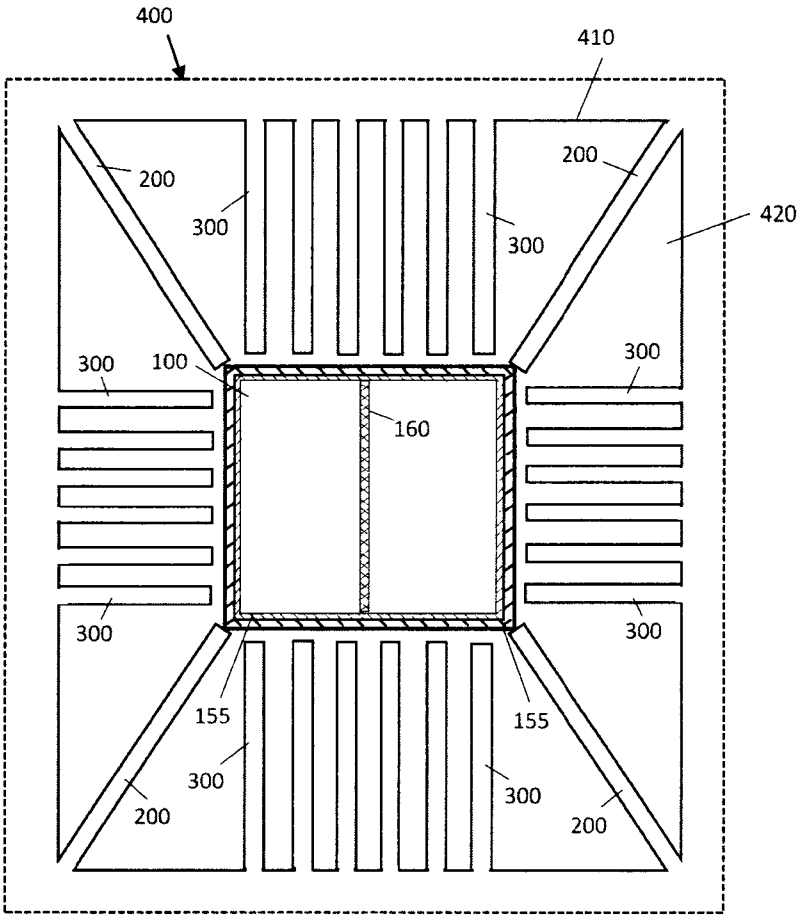

Figure 3

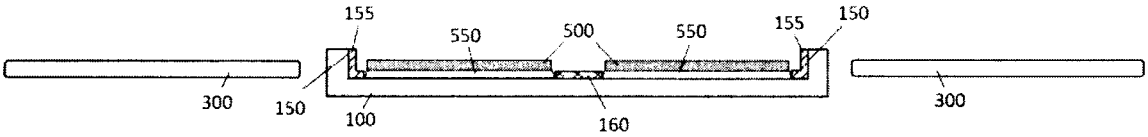

Figure 4

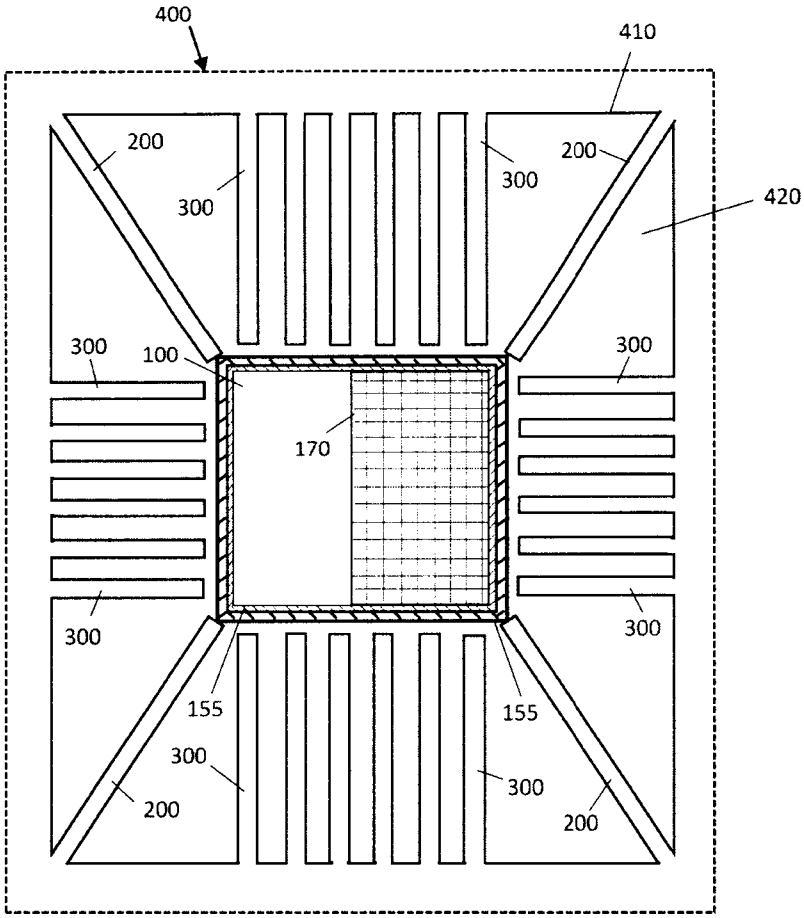

Figure 5

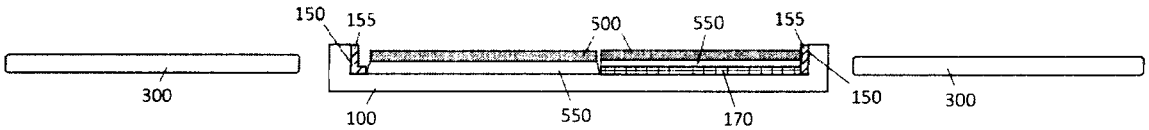

Figure 6

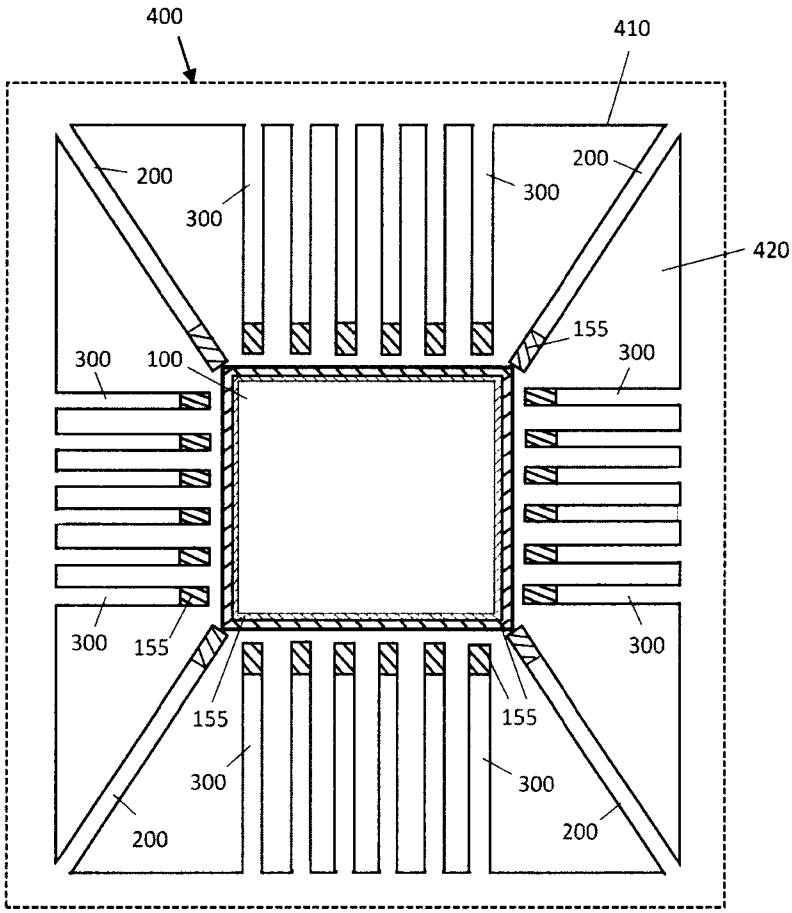
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Figure 7

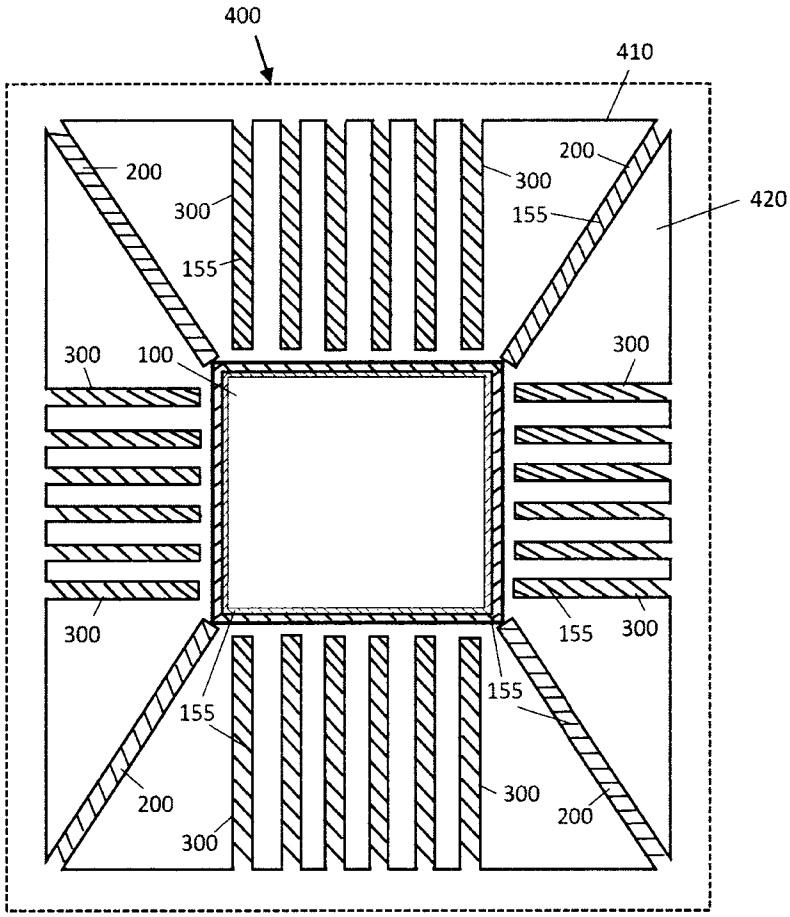

Figure 8

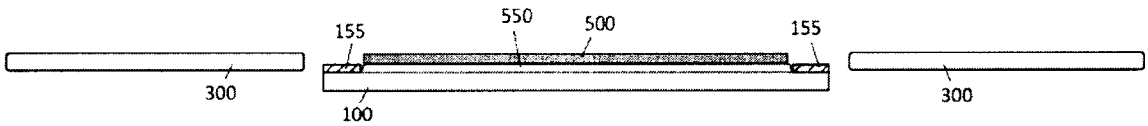

Figure 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/MY2016/000015

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H01L23/50(2006.01)i, H01L21/52(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H01L23/50, H01L21/52

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2016
Registered utility model specifications of Japan 1996-2016
Published registered utility model applications of Japan 1994-2016

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y A	JP 2013-58542 A (DAI NIPPON PRINTING CO., LTD.) 2013.03.28, paragraphs [0019]-[0028], [0057]-[0063], Figs. 1, 7-8 (Family:none)	1-3,10 4-9,11-22 23-34
Y	JP 8-23002 A (HITACHI, LTD.) 1996.01.23, paragraphs [0023]-[0024], Figs. 1-5 (Family:none)	4-7,14-19
Y	JP 2000-138335 A (MITSUBISHI SHINDOH CO., LTD.) 2000.05.16, paragraphs [0007]-[0012], [0033]-[0036], Figs. 5-7 (Family:none)	6-7,18-19

☑ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"P" document published prior to the international filing date but later than the priority date claimed
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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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Date of the actual completion of the international search	Date of mailing of the international search report
30.05.2016	07.06.2016

Name and mailing address of the ISA/JP	Authorized officer
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5D 5588

INTERNATIONAL SEARCH REPORT

International application No.
PCT/MY2016/000015

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 4-188660 A (KYUSHU NIPPON DENKI KABUSHIKI KAISHA) 1992.07.07, Page 1, lower right column, line 4- Page 2, upper right column, line 10, Fig. 1 (Family:none)	8-9,20-21
Y	JP 8-148647 A (TOSHIBA CORPORATION) 1996.06.07, paragraphs [0009]-[0012], Figs. 1-2 (Family:none)	11-22
A	US 2015/0001697 A1 (STMICROELECTRONICS SDN BHD) 2015.01.01, paragraphs [0018]-[0029], Figs. 3-4 (Family:none)	1-34
A	US 6025651 A (SAMSUNG ELECTRONICS CO., LTD.) 2000.02.15, column 2, lines 16-25, Fig. 3 & JP 11-17105 A & KR 10-0239750 B1 & TW 469606 B	23-34