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— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
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(54) Title: METHODS FOR SINGULATION AND PACKAGING

(57) Abstract: A method of singulating includes scribing a first scribe line on a first side of a substrate, scribing a second scribe line on a second side of the substrate, the first and second sides facing away from each other, the second scribe line being substantially parallel to the first scribe line, and simultaneously separating the substrate at the first scribe line and the second scribe line.

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METHODS FOR SINGULATION AND PACKAGING

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to pending U.S. Provisional Application No. 62/329,584, filed in the U.S. Patent and Trademark Office on April 29, 2016, and entitled "Methods for Singulation and Packaging," which is incorporated by reference herein in its entirety and for all purposes.

BACKGROUND

1. Field

[0002] Example embodiments relate to methods for singulation and packaging.

2. Description of the Related Art

[0003] Device manufacturing processes, e.g., semiconductor device manufacturing, MEMS (microelectromechanical systems) device manufacturing, optical device manufacturing, etc., may fabricate a plurality of devices on a wafer or mother substrate, after which the wafer or mother substrate may be singulated into units and packaged. Singulation and packaging may be performed in a number of ways, and singulation and packaging may include overlapping or interleaved operations, rather than being purely sequential.

SUMMARY

[0004] Embodiments are directed to a method of singulating, including scribing a first scribe line on a first side of a substrate, scribing a second scribe line on a second side of the substrate, the first and second sides facing away from each other, the second scribe line being substantially parallel to the first scribe line, and simultaneously separating the substrate at the first scribe line and the second scribe line.

[0005] Scribing may use a laser irradiated on the substrate in a stealth dicing operation.

[0006] The substrate may include first and second substrates in a stacked arrangement, the first scribe line being formed in the first substrate, and the second scribe line being formed in the second substrate.

[0007] The first and second scribe lines may be offset from one another.

[0008] The first scribe line may not separate the second substrate.

[0009] The second scribe line may not separate the first substrate.

[0010] The method may further include scribing a third scribe line on the second side of the substrate, the third scribe line being substantially parallel to the first scribe line, the second

and third scribe lines being spaced apart. The second and third scribe lines may form edges of a portion of the second substrate that is not attached to the first substrate.

[0011] The first substrate may include at least one circuit structure, and the second substrate may form a lid for the at least one circuit structure.

[0012] The method may further include attaching a dicing tape to the first wafer, the dicing tape being expanded after the second scribe line is formed. Embodiments are also directed to a device fabricated from a substrate having a plurality of devices and singulated according to the method according to an embodiment. The device may include a circuit die section and a lid die section, and at least one side surface of the circuit die section and at least one side surface of the lid die section may have ridges extending in a longitudinal direction.

[0013] Embodiments are also directed to a method of manufacturing a device, the method including providing a first wafer having a plurality of devices, providing a second wafer having a lid pattern delineating a plurality of lids, removing portions of a surface of the second wafer corresponding to lid edges in the lid pattern using a beveled dicing blade such that the lids have at least one sidewall that is at an angle relative to the second substrate, the angle being greater than 0 and less than 90 degrees, and attaching the first and second wafers together such that the lids cover the devices.

[0014] During removal of the portions of the surface of the second wafer corresponding to the lid edges, the dicing blade may not completely penetrate the second substrate.

[0015] The method may further include scribing scribe lines along the removed portions of the surface of the second wafer.

[0016] The scribing may use a laser irradiated on the second substrate in a stealth dicing operation.

[0017] Embodiments are also directed to a device package, including a device on a substrate, the substrate having a bond pad area that includes at least one bond pad, and a lid attached to the substrate, the lid covering the device, the lid exposing the bond pad area, the lid having a sidewall extending at an angle to the substrate, the angle being greater than 0 and less than 90 degrees.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] Features will become apparent to those of skill in the art by describing in detail example embodiments with reference to the attached drawings, in which:

[0019] FIG. 1A illustrates a cutaway view of a lid wafer with an etched lids pattern.

[0020] FIG. 1B illustrates a magnified portion of FIG. 1A.

[0021] FIG. 2A illustrates cutaway view of a bonding of a lid wafer and circuit wafer.

[0022] FIG. 2B illustrates a magnified portion of FIG. 2A.

[0023] FIG. 3A illustrates a cutaway view of a dicing tape mounted on the circuit wafer and laser scribing of the lid wafer.

[0024] FIG. 3B illustrates a magnified portion of FIG. 3A.

[0025] FIG. 4 illustrates a cutaway view of remounting a dicing tape on the scribed lid wafer and laser scribing of the circuit wafer.

[0026] FIG. 5 illustrates a cutaway view of expansion of the dicing tape to separate dies.

[0027] FIG. 6 illustrates a cutaway view of an example of an expanded WLP following singulation.

[0028] FIG. 7A illustrates a cutaway view of an example of an individual package following singulation, and FIG. 7B illustrates ridges produced by a stealth dicing process.

[0029] FIG. 8 illustrates a singulated package having a lid with straight edges.

[0030] FIG. 9 illustrates a singulated package having a lid with relieved edges.

[0031] FIG. 10 illustrates an enlarged cutaway view of a lid wafer with an etched lids pattern and beveled kerfs.

[0032] FIG. 11 illustrates a flowchart of a singulation process according to an embodiment.

[0033] FIG. 12 illustrates stealth dicing to induce defects along an angled plane.

DETAILED DESCRIPTION

[0034] Example embodiments will now be described more fully hereinafter with reference to the accompanying drawings; however, they may be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the example embodiments to those skilled in the art. Like reference numerals refer to like elements throughout.

[0035] According to an example embodiment, a singulation process flow uses two aligned back-to-front laser scribes with a single expansion that simultaneously singulates both lid and circuit bonded substrates of wafer level package (WLP) wafer stack.

[0036] A manufacturing process may form a plurality of sensors on a wafer. A general singulation process may include a saw dicing process to singulate a lid wafer into individual caps or lids above the sensor area. Such a process may result in significant yield loss, e.g., ~25%. For example, a dicing blade, while traveling above bond pad areas of a chip (sensor or chip having a sensor) may bombard the surface with wafer debris and lid chips, e.g., silicon debris, which may then damage electronic circuits.

[0037] A singulation process according to an embodiment will be described in connection with FIGS. 1 through 7 and the flowchart illustrated in FIG. 11.

[0038] FIG. 1A illustrates a cutaway view of a lid wafer with an etched lids pattern. FIG. 1B illustrates a magnified portion of FIG. 1A.

[0039] Referring to FIGS. 1A and 1B, a lid wafer may be prepared for inclusion in a WLP wafer stack. The lid wafer may have a plurality of lids (or caps) patterned therein, e.g., by etching. The etching may form recesses that will enclose a region of the circuit wafer, e.g., recesses that will cover respective sensors, circuits, etc. For example, referring to FIG. 2A, the rectangular regions on the upper surface in FIG. 2A may face inward, i.e., face the respective sensors, circuits, etc., when the lid wafer is combined with a circuit wafer in a WLP.

[0040] FIG. 2A illustrates cutaway view of bonding of a lid wafer and circuit wafer. FIG. 2B illustrates a magnified portion of FIG. 2A.

[0041] Referring to FIGS. 2A and 2B, and operation o100 in FIG. 11, the lid wafer may be bonded to a circuit wafer. The circuit wafer may include a plurality of sensors. The circuit wafer may be, e.g., a microbolometer circuit wafer.

[0042] FIG. 3A illustrates a cutaway view of a dicing tape mounted on the circuit wafer and laser scribing of the lid wafer. FIG. 3B illustrates a magnified portion of FIG. 3A.

[0043] Referring to FIGS. 3A and 3B, and operation o200 in FIG. 11, a dicing tape may be mounted on the circuit wafer of the stacked wafers. A laser scribing operation may be performed to scribe the lid wafer (operation o300 in FIG. 11). For example, the lid wafer may

be a silicon wafer, and a laser may be focused inside the silicon wafer to scribe the wafer. The laser may be, e.g., a near IR wavelength laser. The laser scribing operation may be stealth laser scribing or stealth dicing. The stealth dicing may be performed using a method as described in U.S. patent no. 8,268,704, which is incorporated by reference herein. Scribe lines formed by stealth dicing may be cracks, which may later be expanded in a dicing tape expansion operation. In an implementation, laser scribing of the lid wafer scribes the lid wafer without scribing the circuit wafer.

[0044] FIG. 4 illustrates a cutaway view of remounting a dicing tape on the scribed lid wafer and laser scribing of the circuit wafer. FIG. 5 illustrates a cutaway view of expansion of the dicing tape to separate dies.

[0045] Referring to FIGS. 4 and 5, the dicing tape may be removed from the circuit wafer (operation o400 in FIG. 11) and dicing tape may be attached to the lid wafer (operation o500 in FIG. 11). A laser scribing operation may then be performed to scribe the circuit wafer (operation o600 in FIG. 11). The laser scribing operation on the circuit wafer. In the present example embodiment, as illustrated in greater detail in FIG. 5, the laser scribing operation on the circuit wafer is aligned with packages corresponding to the laser scribing operation on the lid wafer. In an implementation, laser scribing may consist of two aligned back-to-front laser scribes. In an implementation, laser scribing of the lid wafer scribes the lid wafer without scribing the circuit wafer. In an implementation, scribed lines on the lid wafer may be offset from scribed lines on the circuit wafer. For example, in the singulated package, the lid section of the lid wafer may have different length and/or width dimensions (in plan view) as compared to the corresponding circuit section of the circuit wafer. In an implementation, two passes of the laser scribe may be made on the lid side of the stack such that residual pieces of the lid wafer remain between the lid sections. In an implementation, the lid section of the singulated package may have a shorter length and/or width than the attached circuit section such that a surface of the circuit section facing in the lid direction may be exposed. The exposed surface of the circuit section may have bond pads thereon.

[0046] Following the laser scribing operation on the circuit wafer, the dicing tape on the lid wafer may be expanded (indicated by arrows in FIG. 5) (operation o700 in FIG. 11). A single

expansion may be performed to simultaneously singulate both the lid and circuit substrates of WLP wafer stack, separating the WLP into individual packaged dies.

[0047] FIG. 6 illustrates a cutaway view of an example of an expanded WLP following singulation. FIG. 7A illustrates a cutaway view of an example of an individual package following singulation.

[0048] Referring to FIG. 6, the lid section of the lid wafer is formed with a different width dimension as compared to the corresponding circuit section of the circuit wafer. Also, two passes of the laser scribe on the lid side of the stack form lid residual pieces between the lid sections. In the example shown in FIG. 7A, the lid wafer is formed with different length and width dimensions as compared to the corresponding circuit section of the circuit wafer

[0049] As described above, a wafer stack of a WLP may be singulated into individual packaged dies without the use of a saw (dicing blade). The stealth dicing process may provide a die having an edge that shows lines or ridges in unique structure, the lines or ridges having a pitch related to the number of laser passes (see the laterally extending ridges in FIGS. 7A and 7B). These lines or ridges are detectable and easily distinguishable from, e.g., Bosch etch scallops or ground surface finish created by saw dicing.

[0050] According to another example embodiment, an individual packaged die may have a lid (or cap) having one or more relieved walls. In an implementation, one or more walls of the lid may be relieved by forming the wall at an angle or taper, such that the wall slopes toward the center of the package, away from the exposed bond pads.

[0051] In an example embodiment, a lid pattern in a lid wafer for a WLP may be formed such that one or more sidewalls of each of the respective lids in the lid pattern is angled relative to major surfaces of the lid wafer.

[0052] In an implementation, a beveled dicing blade (or beveled kerf saw) may be used to form a lid pattern in which one or more sidewalls of each of the respective lids is angled.

[0053] FIG. 8 illustrates a singulated package having a lid with straight edges. FIG. 9 illustrates a singulated package having a lid with relieved edges.

[0054] The package illustrated in FIG. 8 has a lid with straight edges, i.e., edges that are vertical to or normal to the major surface of the circuit die. The size of the lid is smaller than the corresponding circuit die such that the bond pads are exposed by the lid. When capillary

bonding is used to connect the bond pads, the size of the lid is reduced in order to provide an exposed bond pad area sufficient for the capillary bonding operation. Thus, this structure may have a substantial space or margin between the bond pads and the edge of the cap in order to provide free access of the wire bonding capillary.

[0055] The package illustrated in FIG. 9 has a lid with relieved edges, here, angled edges such that the lid has a pyramidal shape. The angled edges may provide sufficient relief at the top of the lid for the capillary bonding operation to take place, while at the same time covering more of the circuit die. The angle (as determined relative to the exposed surface of the circuit wafer) may be greater than 0 and less than 90 degrees, e.g., about 15 degrees, about 30 degrees, about 45 degrees, or about 60 degrees. In the package in which the lid edges are relieved, the area of the circuit die enclosed by the lid may be larger, relative to the straight-walled package (having 90 degree walls relative to the exposed surface of the circuit wafer) illustrated in FIG. 8. The circuit die exposed beyond the lid may form a planar area on at least one side of the lid. For example, a planar area of the circuit die may be exposed on four sides of a pyramidal lid.

[0056] In an embodiment, the package illustrated in FIG. 9 may be formed using a beveled dicing blade on the lid wafer of a wafer stack in a WLP, such that the bevel of the dicing blade forms the angled edges of the lid.

[0057] As described above, a singulated package may have a lid with tapered walls. The walls may have a taper angle that is larger than the one of the wire bonding capillary. The tapered walls may allow for reducing the spatial margin between the bond pads and the edge of the cap provided for wirebonding.

[0058] FIG. 10 illustrates an enlarged cutaway view of a lid wafer with an etched lids pattern and beveled kerfs.

[0059] In an implementation, stealth dicing as described above in connection with FIGS. 1A-7 may be combined with the use of a beveled dicing blade as described above in connection with FIG. 9. For example, referring to FIG. 10, the beveled dicing blade may be used to partially form the lid sidewalls, i.e., form an angled region of the lid sidewalls. Subsequently, stealth dicing may be used to singulate the packages from the WLP, the stealth dicing of the lid wafer forming the remaining portion of the lid sidewalls.

[0060] Further, to eliminate the requirement for a beveled dicing blade, the lid sidewall can be angled by re-programming the stealth dicing system to locate the laser-induced defects along an angled plane within the silicon, as shown in FIG. 12. This manner of stealth dicing angled planes within the silicon is may be used to singulate the lid wafer in a single process step while providing adequate space for wirebonding.

[0061] Example embodiments have been disclosed herein, and although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. In some instances, as would be apparent to one of ordinary skill in the art as of the filing of the present application, features, characteristics, and/or elements described in connection with a particular embodiment may be used singly or in combination with features, characteristics, and/or elements described in connection with other embodiments unless otherwise specifically indicated. Accordingly, it will be understood by those of skill in the art that various changes in form and details may be made without departing from the spirit and scope of the present invention as set forth in the following claims.

WHAT IS CLAIMED IS:

1. A method of singulating, comprising:

scribing a first scribe line on a first side of a substrate;

scribing a second scribe line on a second side of the substrate, the first and second sides facing away from each other, the second scribe line being substantially parallel to the first scribe line; and

simultaneously separating the substrate at the first scribe line and the second scribe line.

2. The method as claimed in claim 1, wherein scribing uses a laser irradiated on the substrate in a stealth dicing operation.

3. The method as claimed in claim 1, wherein the substrate includes first and second substrates in a stacked arrangement, the first scribe line being formed in the first substrate, and the second scribe line being formed in the second substrate.

4. The method as claimed in claim 3, wherein the first and second scribe lines are offset from one another.

5. The method as claimed in claim 3, wherein the first scribe line does not separate the second substrate.

6. The method as claimed in claim 5, wherein the second scribe line does not separate the first substrate.

7. The method as claimed in claim 3, further comprising scribing a third scribe line on the second side of the substrate, the third scribe line being substantially parallel to the first scribe line, the second and third scribe lines being spaced apart, wherein the second and third scribe lines form edges of a portion of the second substrate that is not attached to the first substrate.

8. The method as claimed in claim 3, wherein the first substrate includes at least one circuit structure, and the second substrate forms a lid for the at least one circuit structure.

9. The method as claimed in claim 3, further comprising attaching a dicing tape to the first wafer, the dicing tape being expanded after the second scribe line is formed.

10. The method as claimed in claim 1, wherein separating the substrate at the first scribe line and the second scribe line provides a singulated die having an angled sidewall in which an edge of the singulated die forms an angle greater than 0 degrees and less than 90 degrees with a face of the singulated die.

11. A device fabricated from a substrate having a plurality of devices and singulated according to the method as claimed in claim 1.

12. The device as claimed in claim 11, wherein the device includes a circuit die section and a lid die section, and at least one side surface of the circuit die section and at least one side surface of the lid die section have ridges extending in a longitudinal direction.

13. A method of manufacturing a device, the method comprising:

providing a first wafer having a plurality of devices;

providing a second wafer having a lid pattern delineating a plurality of lids;

removing portions of a surface of the second wafer corresponding to lid edges in the lid pattern using a beveled dicing blade such that the lids have at least one sidewall that is at an angle relative to the second substrate, the angle being greater than 0 and less than 90 degrees; and

attaching the first and second wafers together such that the lids cover the devices.

14. The method as claimed in claim 13, wherein, during removal of the portions of the surface of the second wafer corresponding to the lid edges, the dicing blade does not completely penetrate the second substrate.

15. The method as claimed in claim 14, further comprising scribing scribe lines along the removed portions of the surface of the second wafer.

16. The method as claimed in claim 15, wherein the scribing uses a laser irradiated on the second substrate in a stealth dicing operation.

17. A device manufactured according to the method as claimed in claim 13.

18. A device package, comprising:

a device on a substrate, the substrate having a bond pad area that includes at least one bond pad; and

a lid attached to the substrate, the lid covering the device, the lid exposing the bond pad area, the lid having a sidewall extending at an angle to the substrate, the angle being greater than 0 and less than 90 degrees.

19. A method of manufacturing a device, the method comprising:

providing a first wafer having a plurality of devices;

providing a second wafer having a lid pattern delineating a plurality of lids;

attaching the first and second wafers together such that the lids cover the devices; and

singulating the second wafer such that the lids have at least one angled sidewall that is at an angle relative to a major surface of the second wafer, the angle being greater than 0 and less than 90 degrees.

20. The method as claimed in claim 19, further comprising scribing scribe lines along removed portions of the surface of the second wafer to create the angled sidewall.

21. The method as claimed in claim 20, wherein the scribing uses a laser irradiated on the second substrate in a stealth dicing operation.

22. A device manufactured according to the method as claimed in claim 19.

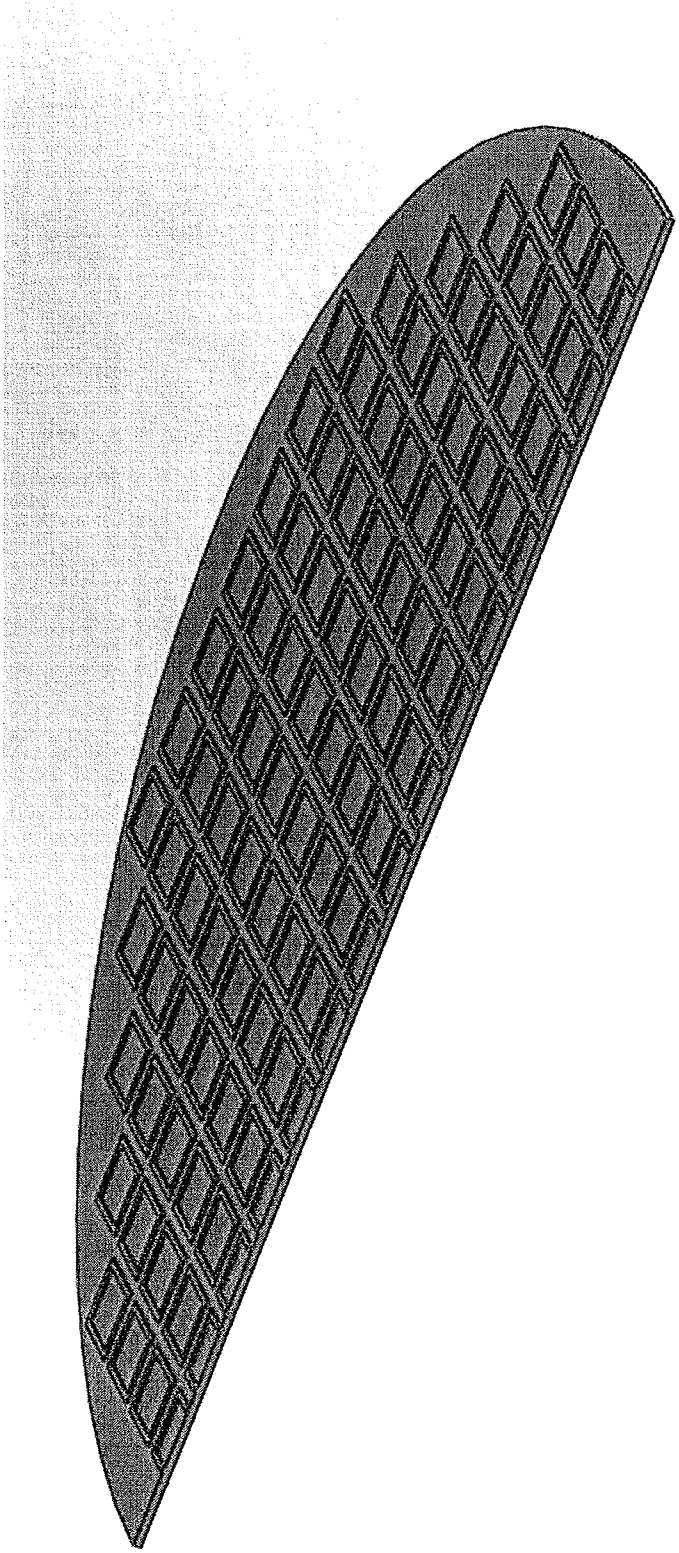
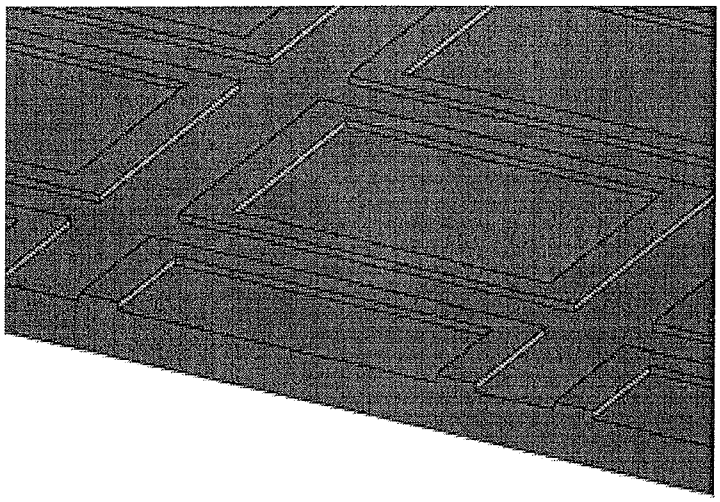


FIG. 1A

FIG. 1B



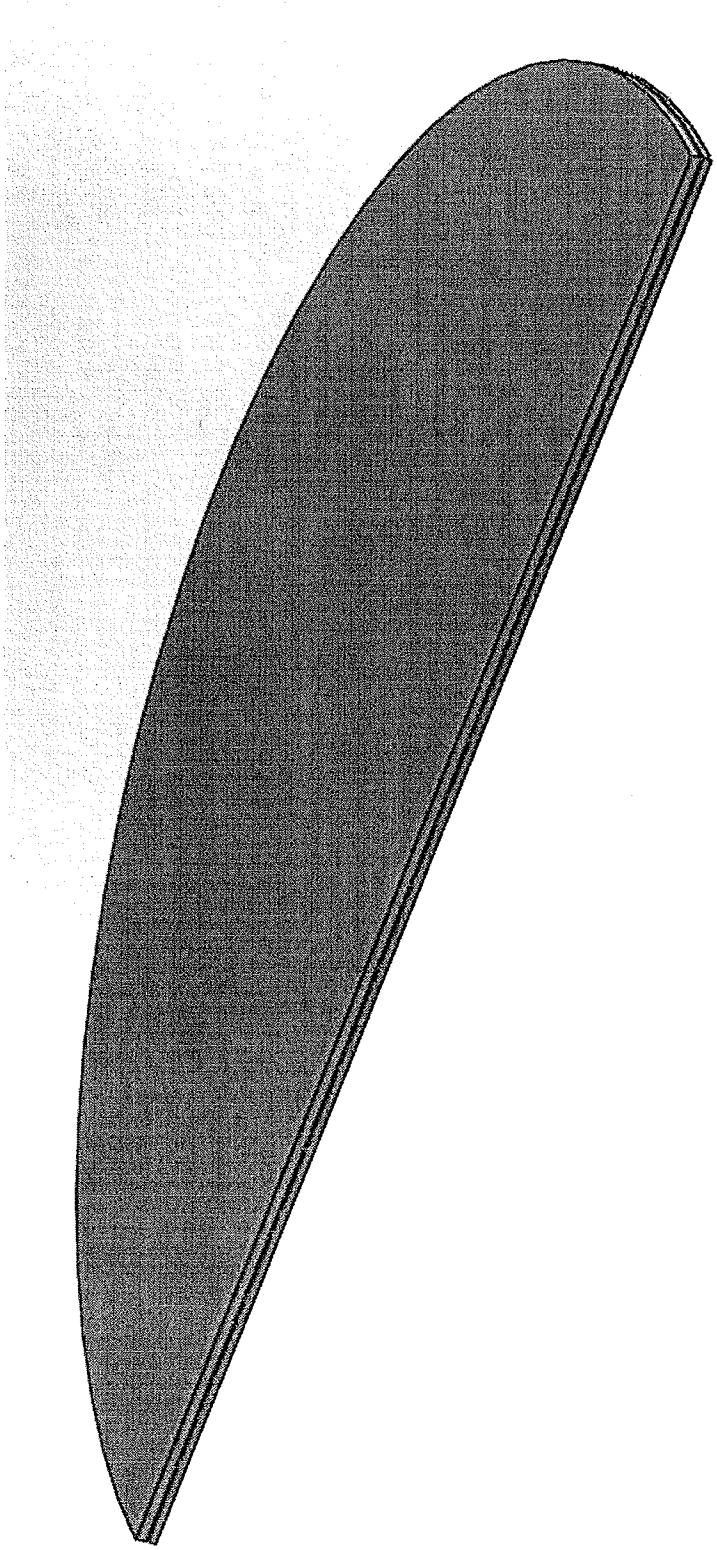
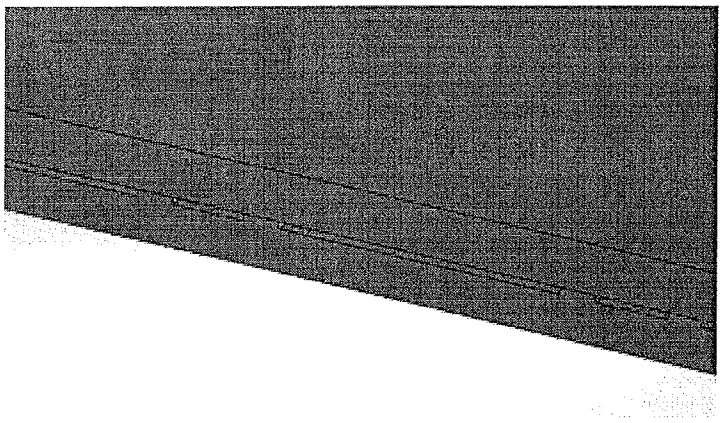


FIG. 2A

FIG. 2B



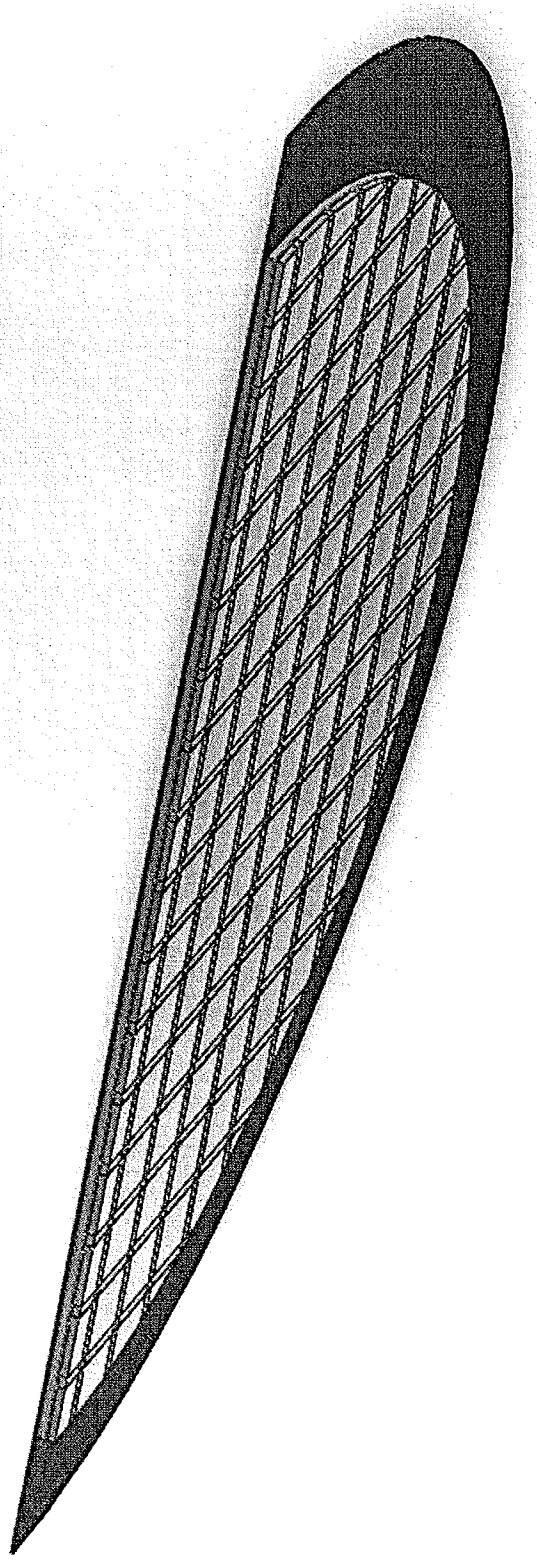
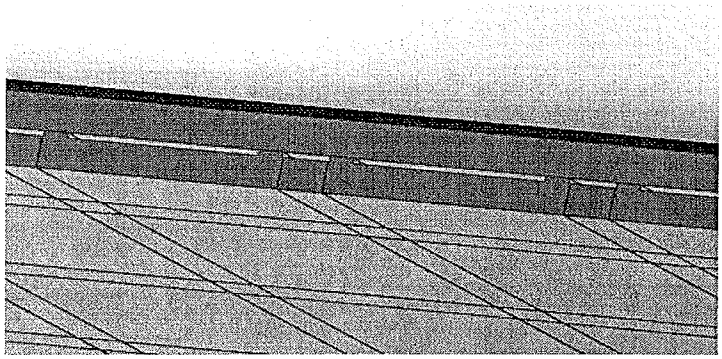


FIG. 3A

FIG. 3B



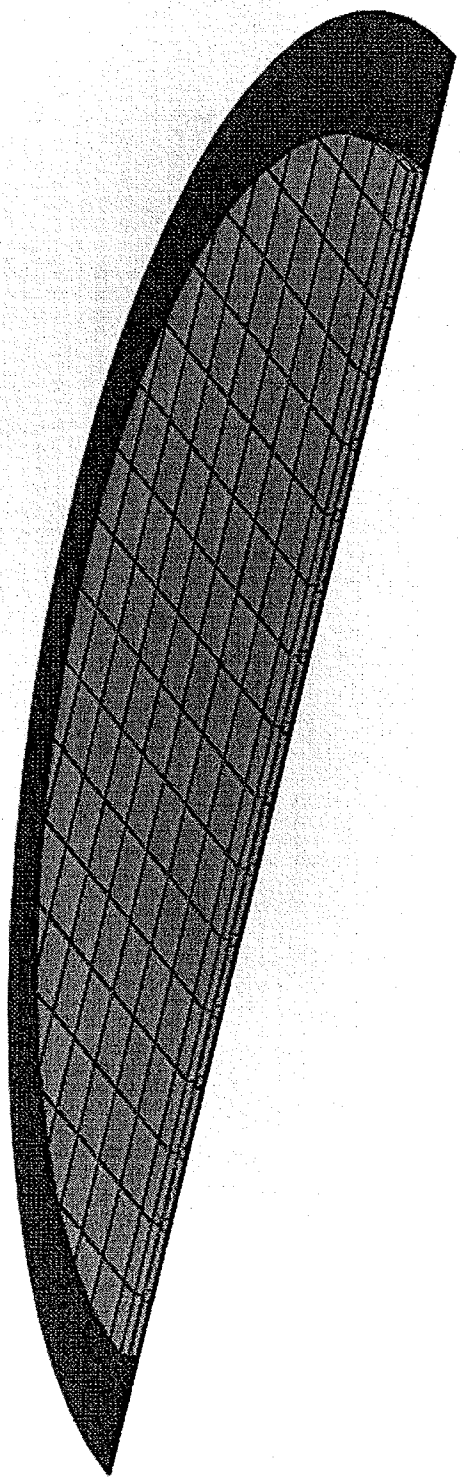


FIG. 4

FIG. 5

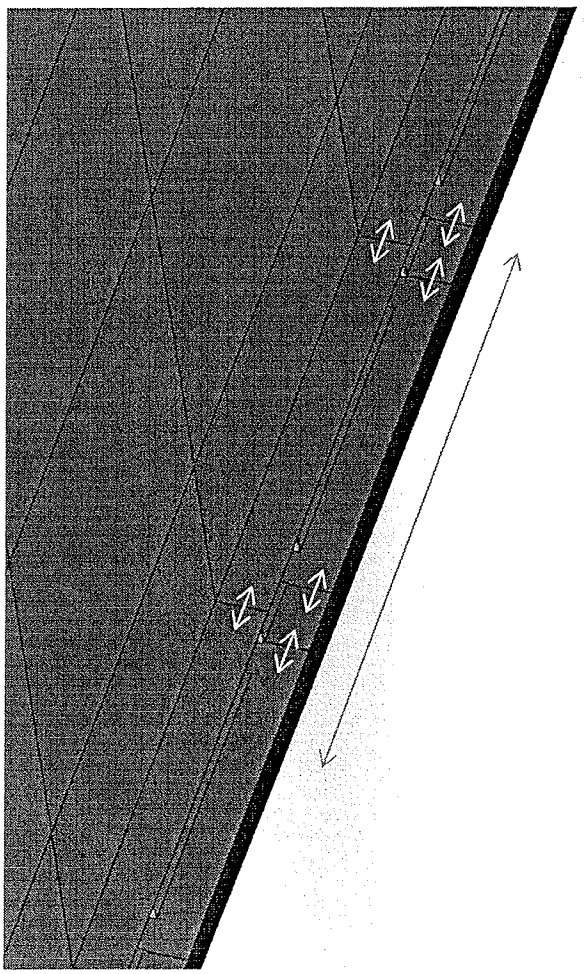


FIG. 6

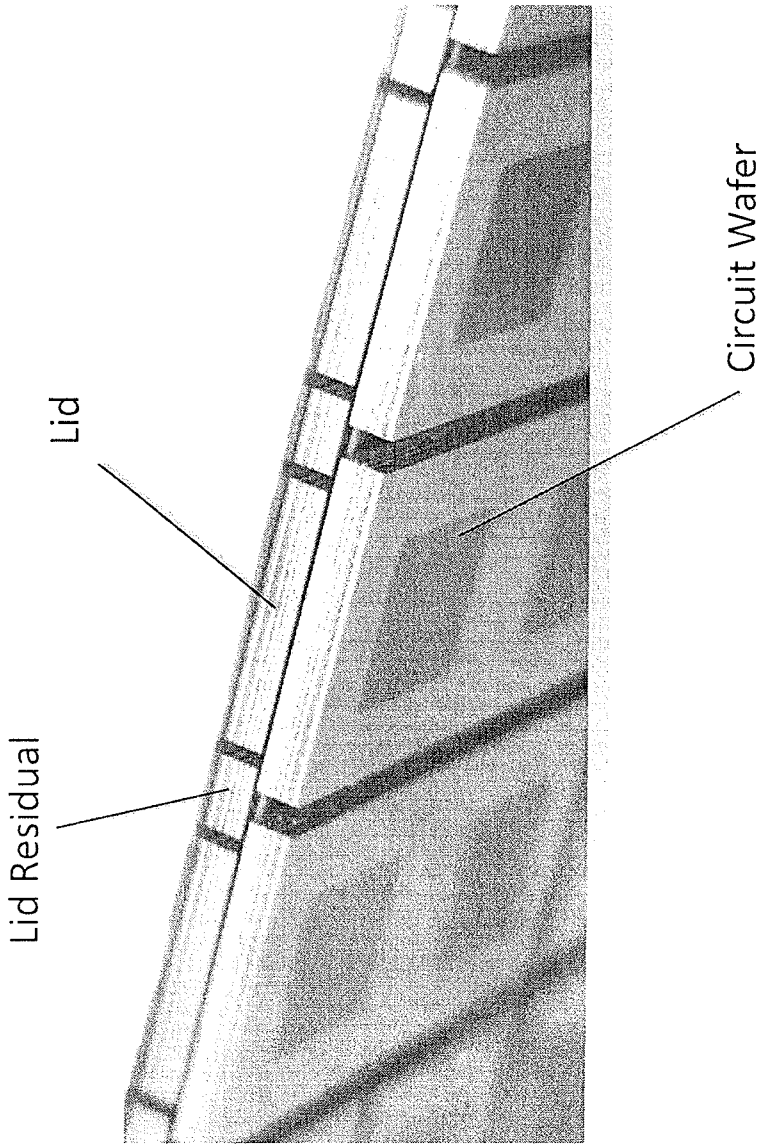


FIG. 7A

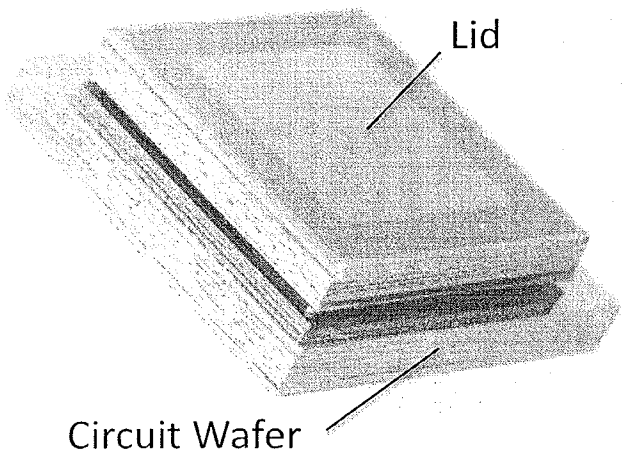


FIG. 7B

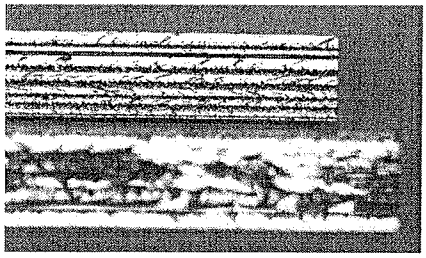


FIG. 8

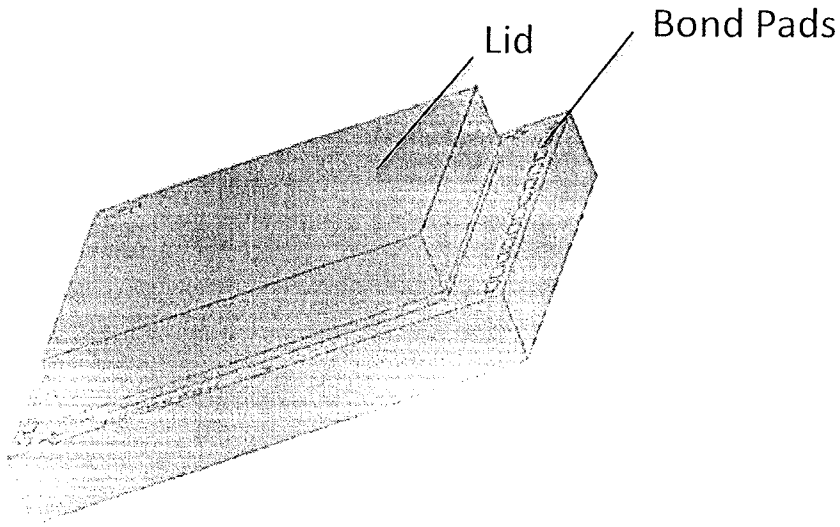


FIG. 9

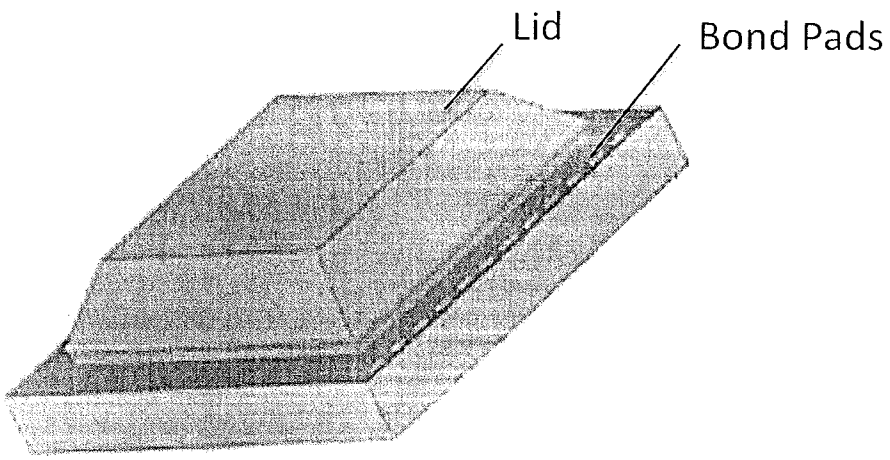


FIG. 10

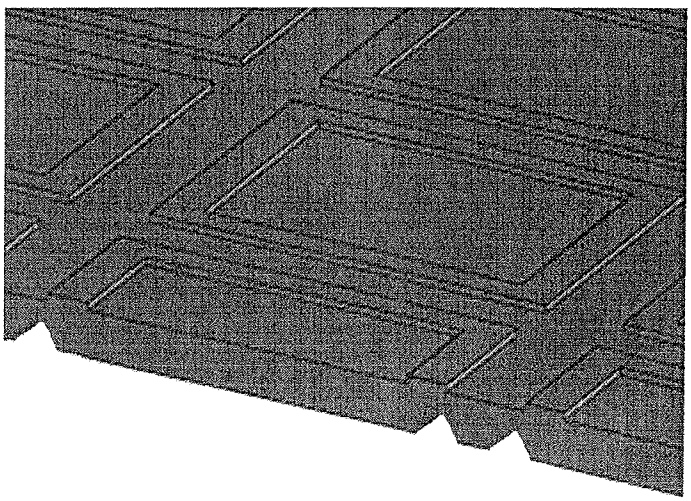


FIG. 11

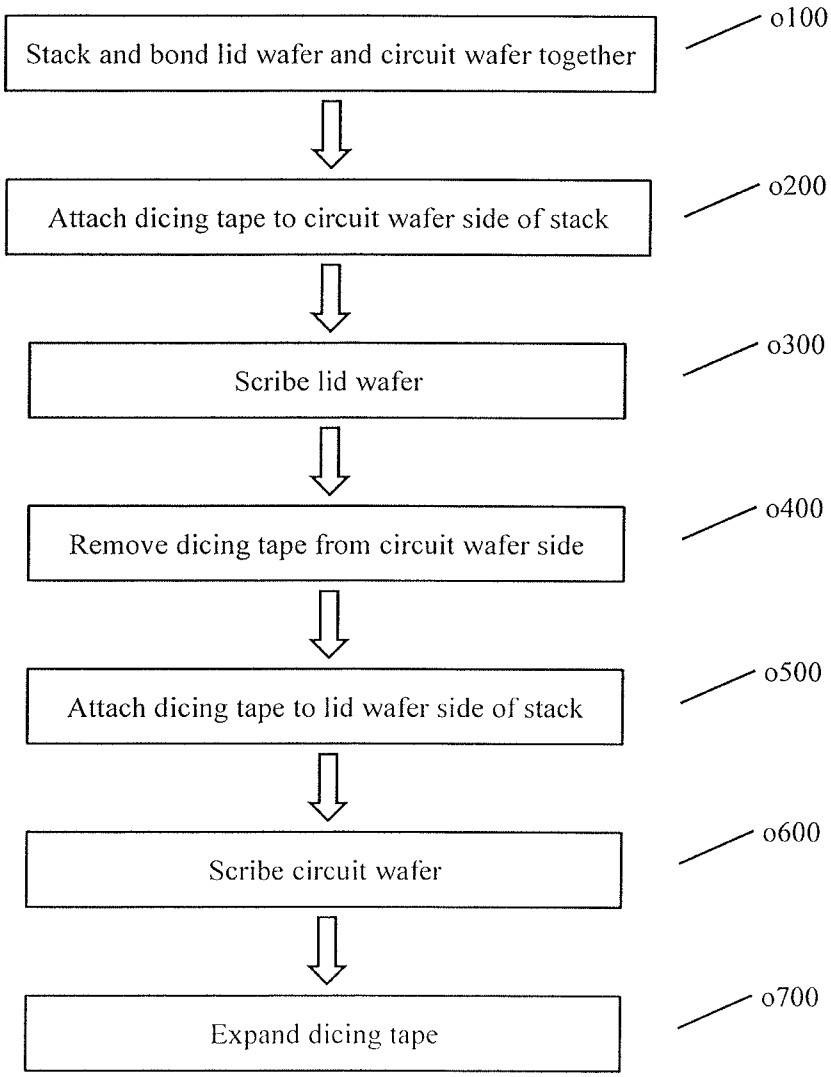
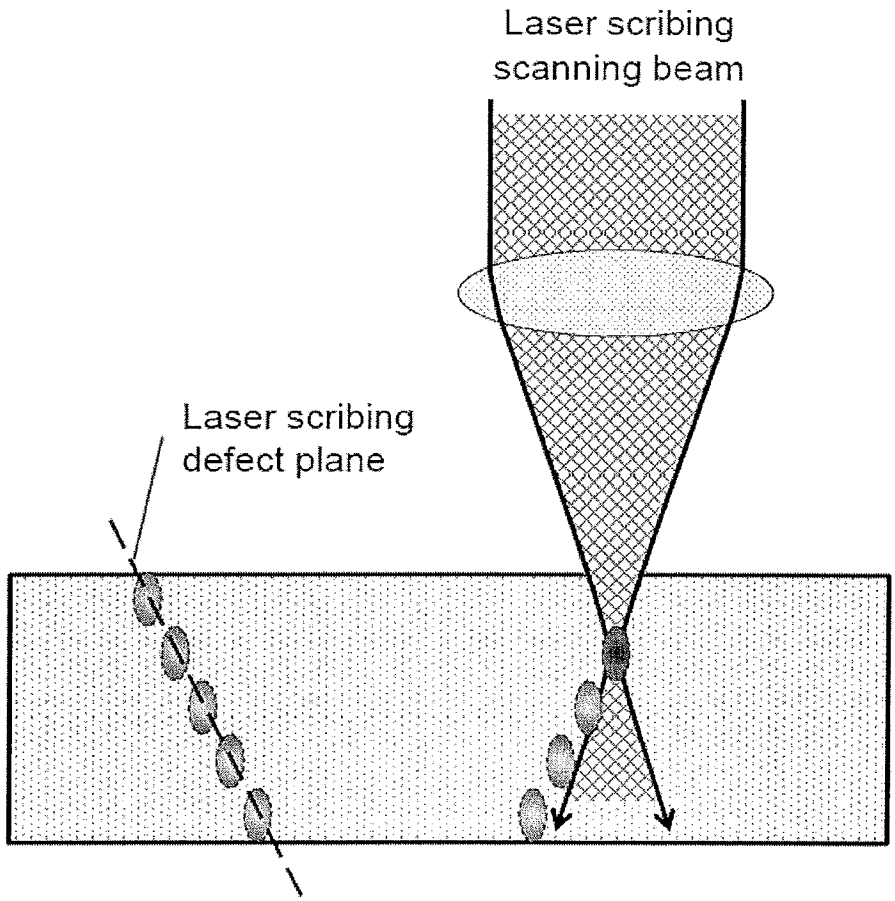

Stack and bond lid wafer and circuit wafer together
o100
Attach dicing tape to circuit wafer side of stack
o200
Scribe lid wafer
o300
Remove dicing tape from circuit wafer side
o400
Attach dicing tape to lid wafer side of stack
o500
Scribe circuit wafer
o600
Expand dicing tape
o700

FIG. 12



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 17/30215

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 23/31, H01L 23/00 (2017.01)
CPC - H01L23/3114; H01L24/11; B81C1/00269; H01L23/544; H01L21/78; B81C1/00865; H01L2223/5446; H01L21/6836

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
See Search History Document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
See Search History Document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
See Search History Document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 2007/0190691 A1 (HUMPSTON et al.) 16 August 2007 (16.08.2007) para [0005], [0134], [0136], [0139], [0172], [0223], [0241]-[0244], [0265], [0289]; figure 3A;	1, 11-12 ---------- 2-10
Y	US 2016/0071770 A1 (NXP B.V.) 10 March 2016 (10.03.2016) para [0022], [0041]; title	2
Y	US 2006/0088980 A1 (CHEN et al.) 27 April 2006 (27.04.2006) para [0021], [0025]-[0027]; figures 3a-3c	3-9
Y	US 9,165,832 B1 (PAPANU et al.) 20 October 2015 (20.10.2015) col 3, ln 57-60; col 9, ln 31-37; col 10, ln 18-30; claims 1, 5 and 11; figures 7A-7D	9
Y	US 2015/0001741 A1 (STATS CHIPPAC, LTD.) 1 January 2015 (01.01.2015) para [0001], [0009], [0042]; claim 1; abstract; figure 5B	10
A	US 2015/0270173 A1 (SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC) 24 September 2015 (24.09.2015); the entire document	1-12
A	US 2011/0244657 A1 (GRIVNA et al.) 6 October 2011 (06.10.2011); the entire document	1-12
A	US 2015/0028446 A1 (LEI et al.) 29 January 2015 (29.01.2015); the entire document	1-12

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 August 2017	08 SEP 2017

Name and mailing address of the ISA/US	Authorized officer:
Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

INTERNATIONAL SEARCH REPORT

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Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fees must be paid.

Group I: Claims 1-12, directed to a method of singulating, comprising: scribing a first scribe line on a first side of a substrate

Group II: Claims 13-22, directed to a method of manufacturing a device, comprising device/device-package.

The inventions listed as Groups I-II do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons:

please see the continuation at the end of this form

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-12

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

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continuation of Box III (Lakc of Unity)

Special Technical Features:

Group I requires method of scribing a first scribe line on a first side of a substrate; scribing a second scribe line on a second side of the substrate, the first and second sides facing away from each other, the second scribe line being substantially parallel to the first scribe line; and simultaneously separating the substrate at the first scribe line and the second scribe line, not required by groups II.

Groups II requires a method of manufacturing a device device(s) on a substrate/wafer; the lid covering the device; the lid having a sidewall extending at an angle to a substrate/wafer, the angle being greater than 0 and less than 90 degrees, not required by group I.

Common Technical Features:

Groups I and II share the technical feature of singulating; substrate/wafer; first and second; and separate/remove. However, these shared technical features do not represent a contribution over prior art, because the shared technical feature is being anticipated by US 2015/0332969 A1 (Grivna). Grivna teaches singulating (para [0047]; a method of singulating a wafer); substrate/wafer (para [0047]; a method of singulating a wafer); first and second (para [0047]; wafer has first and second opposing major surfaces); and separate/remove (para [0047]; elements 12, 14, 16, 18 formed on the wafer and separated from each other by spaces).

As the shared technical features were known in the art at the time of the invention, they cannot be considered common technical features that would otherwise unify the groups. Therefore, Groups I-II lack unity under PCT Rule 13.