INTEGRATED CIRCUIT PACKAGING USING ELECTROCHEMICALLY FABRICATED STRUCTURES

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Abstract

Embodiments of the invention provide a package for holding an integrated circuit or other electronic component and/or a packaged integrated circuit or electronic component which is formed at least in part via an electrochemical fabrication process from a plurality of adhered layers of conductive and dielectric materials.
INTEGRATED CIRCUIT PACKAGING USING ELECTROCHEMICALLY FABRICATED STRUCTURES

RELATED APPLICATIONS


FIELD OF THE INVENTION

[0002] The present invention relates generally to the field of electrochemical fabrication and the associated formation of three-dimensional structures (e.g. microscale or mesoscale structures). In particular, it relates to electrochemical fabrication methods for fabricating packages for integrated circuits where at least a portion of the package is formed using electrochemical fabrication techniques.

BACKGROUND OF THE INVENTION

[0003] A technique for forming three-dimensional structures (e.g. parts, components, devices, and the like) from a plurality of adhered layers was invented by Adam L. Cohen and is known as Electrochemical Fabrication. It is being commercially pursued by Microfabrica Inc. (formerly MEMGen Corporation) of Burbank, Calif. under the name EFAB®. This technique was described in U.S. Pat. No. 6,027,630, issued on Feb. 22, 2000. This electrochemical deposition technique allows the selective deposition of a material using a unique masking technique that involves the use of a mask that includes patterned conformable material on a support structure that is independent of the substrate onto which plating will occur. When desiring to perform an electrodeposition using the mask, the conformable portion of the mask is brought into contact with a substrate while in the presence of a plating solution such that the contact of the conformable portion of the mask to the substrate inhibits deposition at selected locations. For convenience, these masks might be generically called conformable contact masks; the masking technique may be generically called a conformable contact mask plating process. More specifically, in the terminology of Microfabrica Inc. (formerly MEMGen Corporation) of Burbank, Calif., such masks have come to be known as INSTANT MASK™ and the process known as INSTANT MASKING™ or INSTANT MASK™ plating. Selective depositions using conformable contact mask plating may be used to form single layers of material or may be used to form multi-layer structures. The teachings of the ’630 patent are hereby incorporated herein by reference as if set forth in full herein. Since the filing of the patent application that led to the above noted patent, various papers about conformable contact mask plating (i.e. INSTANT MASKING) and electrochemical fabrication have been published:


[0013] The disclosures of these nine publications are hereby incorporated herein by reference as if set forth in full herein.

[0014] The electrochemical deposition process may be carried out in a number of different ways as set forth in the above patent and publications. In one form, this process involves the execution of three separate operations during the formation of each layer of the structure that is to be formed:

[0015] (1) Selectively depositing at least one material by electrodeposition upon one or more desired regions of a substrate.

[0016] (2) Then, blanket depositing at least one additional material by electrodeposition so that the additional deposit covers both the regions that were previously selectively deposited onto, and the regions of the substrate that did not receive any previously applied selective depositions.

[0017] (3) Finally, planarizing the materials deposited during the first and second operations to produce a smooth surface of a first layer of desired thickness having at least one region containing the at least one material and at least one region containing at least the one additional material.

[0018] After formation of the first layer, one or more additional layers may be formed adjacent to the immediately preceding layer and adhered to the smooth surface of that preceding layer. These additional layers are formed by repeating the first through third operations one or more times wherein the formation of each subsequent layer treats the previously formed layers and the initial substrate as a new and thickening substrate.
Once the formation of all layers has been completed, at least a portion of at least one of the materials deposited is generally removed by an etching process to expose or release the three-dimensional structure that was intended to be formed.

The preferred method of performing the selective electrodeposition involved in the first operation is by conformable contact mask plating. In this type of plating, one or more conformable contact (CC) masks are first formed. The CC masks include a support structure onto which a patterned conformable dielectric material is adhered or formed. The conformable material for each mask is shaped in accordance with a particular cross-section of material to be plated. At least one CC mask is needed for each unique cross-sectional pattern that is to be plated.

The support for a CC mask is typically a plate-like structure formed of a metal that is to be selectively electroplated and from which material to be plated will be dissolved. In this typical approach, the support will act as an anode in an electroplating process. In an alternative approach, the support may instead be a porous or otherwise perforated material through which deposition material will pass during an electroplating operation on its way from a distal anode to a deposition surface. In either approach, it is possible for CC masks to share a common support, i.e. the patterns of conformable dielectric material for plating multiple layers of material may be located in different areas of a single support structure. When a single support structure contains multiple plating patterns, the entire structure is referred to as the CC mask while the individual plating masks may be referred to as “submasks.” In the present application such a distinction will be made only when relevant to a specific point being made.

In preparation for performing the selective deposition of the first operation, the conformable portion of the CC mask is placed in registration with and pressed against a selected portion of the substrate (or onto a previously formed layer or onto a previously deposited portion of a layer) on which deposition is to occur. The pressing together of the CC mask and substrate occur in such a way that all openings, in the conformable portions of the CC mask contain plating solution. The conformable material of the CC mask that contacts the substrate acts as a barrier to electrodeposition while the openings in the CC mask that are filled with electroplating solution act as pathways for transferring material from an anode (e.g. the CC mask support) to the non-contacted portions of the substrate (which act as a cathode during the plating operation) when an appropriate potential and/or current are supplied.

An example of a CC mask and CC mask plating are shown in FIGS. 1A-1C. FIG. 1A shows a side view of a CC mask 8 consisting of a conformable or deformable (e.g. elastomeric) insulator 10 patterned on an anode 12. The anode has two functions. FIG. 1A also depicts a substrate 6 separated from mask 8. One is as a supporting material for the patterned insulator 10 to maintain its integrity and alignment since the pattern may be topologically complex (e.g., involving isolated “islands” of insulator material). The other function is as an anode for the electroplating operation. CC mask plating selectively deposits material 22 onto a substrate 6 by simply pressing the insulator against the substrate then electrodepositing material through apertures 26a and 26b in the insulator as shown in FIG. 1B. After deposition, the CC mask is separated, preferably non-destructively, from the substrate 6 as shown in FIG. 1C. The CC mask plating process is distinct from a “through-mask” plating process in that in a through-mask plating process the separation of the masking material from the substrate would occur destructively. As with through-mask plating, CC mask plating deposits material selectively and simultaneously over the entire layer. The plated region may consist of one or more isolated plating regions where these isolated plating regions may belong to a single structure that is being formed or may belong to multiple structures that are being formed simultaneously. In CC mask plating as individual masks are not intentionally destroyed in the removal process, they may be usable in multiple plating operations.

Another example of a CC mask and CC mask plating is shown in FIGS. 1D-1F. FIG. 1D shows an anode 12 separated from a mask 8 that includes a patterned conformable material 10 and a support structure 20. FIG. 1D also depicts substrate 6 separated from the mask 8. FIG. 1E illustrates the mask 8 being brought into contact with the substrate 6. FIG. 1F illustrates the deposit 22 that results from conducting a current from the anode 12 to the substrate 6. FIG. 1G illustrates the deposit 22 on substrate 6 after separation from mask 8. In this example, an appropriate electrolyte is located between the substrate 6 and the anode 12 and a current of ions coming from one or both of the solution and the anode are conducted through the opening in the mask to the substrate where material is deposited. This type of mask may be referred to as an anodeless INSTANT MASK™ (AIM) or an anodeless conformable contact (ACC) mask.

Unlike through-mask plating, CC mask plating allows CC masks to be formed completely separate from the fabrication of the substrate on which plating is to occur (e.g. separate from a three-dimensional (3D) structure that is being formed). CC masks may be formed in a variety of ways, for example, a photolithographic process may be used. All masks can be generated simultaneously, prior to structure fabrication rather than during it. This separation makes possible a simple, low-cost, automated, self-contained, and internally-clean “desktop factory” that can be installed almost anywhere to fabricate 3D structures, leaving any required clean room processes, such as photolithography to be performed by service bureaus or the like.

An example of the electrochemical fabrication process discussed above is illustrated in FIGS. 2A-2F. These figures show that the process involves deposition of a first material 2 which is a sacrificial material and a second material 4 which is a structural material. The CC mask 8, in this example, includes a patterned conformable material (e.g. an elastomeric dielectric material) 10 and a support 12 which is made from deposition material 2. The conformal portion of the CC mask is pressed against substrate 6 with a plating solution 14 located within the openings 16 in the conformable material 10. An electric current, from power supply 18, is then passed through the plating solution 14 via (a) support 12 which doubles as an anode and (b) substrate 6 which doubles as a cathode. FIG. 2A, illustrates that the passing of current causes material 2 within the plating solution and material 2 from the anode 12 to be selectively transferred to and plated on the cathode 6. After electroplating the first deposition material 2 onto the substrate 6 using CC mask 8, the CC mask 8 is removed as shown in FIG. 2B. FIG. 2C depicts the second deposition material 4 as having been blanket-deposited (i.e. non-selectively deposited) over the previously deposited first deposition material 2 as well as over the other portions of the substrate 6. The blanket deposition occurs by electroplating.
from an anode (not shown), composed of the second material, through an appropriate plating solution (not shown), and to the cathode/substrate 6. The entire two-material layer is then planarized to achieve precise thickness and flatness as shown in FIG. 2D. After repetition of this process for all layers, the multi-layer structure 20 formed of the second material 4 (i.e., structural material) is embedded in first material 2 (i.e., sacrificial material) as shown in FIG. 2E. The embedded structure is etched to yield the desired device, i.e., structure 20, as shown in FIG. 2F.

[0027] Various components of an exemplary manual electrochemical fabrication system 32 are shown in FIGS. 3A-3C. The system 32 consists of several subsystems 34, 36, 38, and 40. The substrate holding subsystem 34 is depicted in the upper portions of each of FIGS. 3A to 3C and includes several components: (1) a carrier 48, (2) a metal substrate 6 onto which the layers are deposited, and (3) a linear slide 42 capable of moving the substrate 6 up and down relative to the carrier 48 in response to drive force from actuator 44. Subsystem 34 also includes an indicator 46 for measuring differences in vertical position of the substrate which may be used in setting or determining layer thicknesses and/or deposition thicknesses. The subsystem 34 further includes feet 68 for carrier 48 which can be precisely mounted on subsystem 36.

[0028] The CC mask subsystem 36 shown in the lower portion of FIG. 3A includes several components: (1) a CC mask 8 that is actually made up of a number of CC masks (i.e., submasks) that share a common support/anode 12, (2) precision X-stage 54, (3) precision Y-stage 56, (4) frame 72 on which the feet 68 of subsystem 34 can mount, and (5) a tank 58 for containing the electrolyte 16. Subsystems 34 and 36 also include appropriate electrical connections (not shown) for connecting to an appropriate power source for driving the CC masking process.

[0029] The blanket deposition subsystem 38 is shown in the lower portion of FIG. 3B and includes several components: (1) an anode 62, (2) an electrolyte tank 64 for holding plating solution 66, and (3) frame 74 on which the feet 68 of subsystem 34 may sit. Subsystem 38 also includes appropriate electrical connections (not shown) for connecting the anode to an appropriate power source for driving the blanket deposition process.

[0030] The planarization subsystem 40 is shown in the lower portion of FIG. 3C and includes a lapping plate 52 and associated motion and control systems (not shown) for planarizing the depositions.

[0031] Another method for forming microstructures from electroplated metals (i.e., using electrochemical fabrication techniques) is taught in U.S. Pat. No. 5,190,637 to Henry Guckel, entitled “Formation of Microstructures by Multiple Level Deep X-ray Lithography with Sacrificial Metal Layers”. This patent teaches the formation of metal structure utilizing mask exposures. A first layer of a primary metal is electroplated onto an exposed plating base to fill a void in a photoresist, the photoresist is then removed and a secondary metal is electroplated over the first layer and over the plating base. The exposed surface of the secondary metal is then machined down to a height which exposes the first metal to produce a flat uniform surface extending across the both the primary and secondary metals. Formation of a second layer may then begin by applying a photoresist layer over the first layer and then repeating the process used to produce the first layer. The process is then repeated until the entire structure is formed and the secondary metal is removed by etching. The photoresist is formed over the plating base or previous layer by casting and the voids in the photoresist are formed by exposure of the photoresist through a patterned mask via X-rays or UV radiation.

[0032] Even though electrochemical fabrication as taught and practiced to date, has greatly enhanced the capabilities of microfabrication, and in particular added greatly to the number of metal layers that can be incorporated into a structure and to the speed and simplicity in which such structures can be made, room for enhancing the state of electrochemical fabrication exists as well as for adding to the types of devices that can be formed or co-fabricated with other devices.

**SUMMARY OF THE INVENTION**

[0033] Objects and advantages of various aspects of the invention will be apparent to those of skill in the art upon review of the teachings herein. The various aspects of the invention, set forth explicitly herein or otherwise ascertained from the teachings herein, may address one or more of the above objects alone or in combination, or alternatively may address some other object of the invention ascertained from the teachings herein. It is not necessarily intended that all objects be addressed by any single aspect of the invention even though that may be the case with regard to some aspects.

[0034] In a first aspect of the invention a fabrication process for fabricating a package for holding an electronic component includes: (a) forming and adhering a layer of material to a previously formed layer and/or to a substrate, wherein the layer comprises a desired pattern of at least one material; and (b) repeating the forming and adhering operation of (a) a plurality of times to build up a configuration of conductive interconnect elements in a configuration of a desired package, wherein the plurality of layers are adhered to one another and comprise at least one of (i) at least one structural material and at least one sacrificial material or (ii) at least two structural materials one of which is a conductor and one of which is a dielectric.

[0035] In a specific variation of the first aspect, the package includes a dielectric deposited or electroless deposited on a layer by layer basis where the height of at least some layers is set by a planarization operation that planarizes an interconnect material and at least one other material.

[0036] In a specific variation of the first aspect, the package includes vias and traces that coexist on at least some layers.

[0037] In a specific variation of the first aspect, the package includes at least one more coaxial interconnects.

[0038] In a specific variation of the first aspect, the package includes interconnects having traces having at least two different widths.

[0039] In a specific variation of the first aspect, the package includes interconnects comprising vias that have at least two different widths.

[0040] In a specific variation of the first aspect, the package includes interconnects have trace thicknesses that are at least as thick as some planarized thicknesses of a dielectric material.

[0041] In a specific variation of the first aspect, the package includes interconnects having trace thicknesses that are at least as thick as the differential height between some interconnect traces.

[0042] In a specific variation of the first aspect, at least one layer of the package is formed using a process comprising: patterning a first material, applying a non-planar seed layer,
electrodepositing a second material, and trimming off at least a portion of the deposited first material.

[0043] In a second aspect of the invention, a fabrication process for fabricating a packaged electronic component includes: providing a substrate having conductive vias; forming routing elements on the substrate which have first and second ends, where at least some of the first ends are connectable to a first electronic component and at least some of the second ends connect to vias on the substrate; and attaching the first electronic component to at least some of the first ends.

[0044] In a third aspect of the invention, a fabrication process for fabricating a packaged electronic component includes: providing a substrate; forming routing elements on the substrate which have first and second ends, where at least some of the first ends are connectable to a first electronic component and at least some of the second ends are connectable to a second electronic component; and attaching the first and second electronic components to at least some of the first ends and second ends, respectively.

[0045] Further aspects of the invention will be understood by those of skill in the art upon reviewing the teachings herein. Other aspects of the invention may involve combinations of the above noted aspects of the invention. Other aspects of the invention may involve apparatus that can be used in implementing one or more of the above method aspects of the invention. These other aspects of the invention may provide various combinations of the aspects presented above as well as provide other configurations, structures, functional relationships, and processes that have not been specifically set forth above.

BRIEF DESCRIPTION OF THE DRAWINGS

[0046] FIGS. 1A-1C schematically depict side views of various stages of a CC mask plating process, while FIGS. 1D-G schematically depict side views of various stages of a CC mask plating process using a different type of CC mask.

[0047] FIGS. 2A-2F schematically depict side views of various stages of an electrochemical fabrication process as applied to the formation of a particular structure where a sacrificial material is selectively deposited while a structural material is blanket deposited.

[0048] FIGS. 3A-3C schematically depict side views of various example subassemblies that may be used in manually implementing the electrochemical fabrication method depicted in FIGS. 2A-2F.

[0049] FIGS. 4A-4F schematically depict the formation of a first layer of a structure using adhered mask plating where the blanket deposition of a second material overlays both the openings between deposition locations of a first material and the first material itself.

[0050] FIG. 4G depicts the completion of formation of the first layer resulting from planarizing the deposited materials to a desired level.

[0051] FIGS. 4I and 4i respectively depict the state of the process after formation of the multiple layers of the structure and after release of the structure from the sacrificial material.

[0052] FIGS. 5A-5D schematically depict side views of various stages in a process for attaching an example IC to an example package where interconnects from the IC to at least one other component include vias that extend through a substrate on which electrochemically fabricated routing elements are formed.

[0053] FIG. 6 schematically depicts a side view of two example ICs attached to and at least partially electrically interconnected to one another via an example package and where at least a portion of the interconnects extend through routing elements formed via electrochemical fabrication.

[0054] FIG. 7 schematically depicts a side view of an example IC attached to an alternative example package configuration, where the package configuration includes a conductive substrate, routing elements that provide interconnect paths from a surface of the package to the IC, and which includes passive components such as inductors and capacitors.

[0055] FIG. 8 schematically depicts a side view of an example IC attached to a package configuration similar to that of FIG. 7 with the exception that the substrate includes a passage for allowing a cooling fluid to pass through the substrate.

[0056] FIG. 9 schematically depicts a side view of two example ICs and a package with routing element and which further includes an added packaging element that takes the form of a heat sink that is located above one of the ICs and which includes a passage through which a cooling liquid may flow.

[0057] FIG. 10 schematically depicts a side view of routing elements formed via electrochemical fabrication where a substrate on which the layers were formed has been removed and an IC attached.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

[0058] FIGS. 1A-1G, 2A-2F, and 3A-3C illustrate various features of one form of electrochemical fabrication. Other electrochemical fabrication techniques are set forth in the '630 patent referenced above, in the various previously incorporated publications, in various other patents and patent applications incorporated herein by reference. Still others may be derived from combinations of various approaches described in these publications, patents, and applications, or are otherwise known or ascertainable by those of skill in the art from the teachings set forth herein. All of these techniques may be combined with those of the various embodiments of various aspects of the invention to yield enhanced embodiments. Still other embodiments may be derived from combinations of the various embodiments explicitly set forth herein.

[0059] FIGS. 4A-4l illustrate various stages in the formation of a single layer of a multi-layer fabrication process where a second metal is deposited on a first metal as well as in openings in the first metal so that the first and second metal form part of the layer. In FIG. 4A a side view of a substrate 82 is shown, onto which patternable resists 84 is cast as shown in FIG. 4B. In FIG. 4C, a pattern of resist is shown that results from the curing, exposing, and developing of the resist. The patterning of the photoresist 84 results in openings or apertures 92(a)-92(c) extending from a surface 86 of the photoresist through the thickness of the photoresist to surface 88 of the substrate 82. In FIG. 4D a metal 94 (e.g. nickel) is shown as having been electroplated into the openings 92(a)-92(c). In FIG. 4E the photoresist has been removed (i.e. chemically stripped) from the substrate to expose regions of the substrate 82 which are not covered with the first metal 94. In FIG. 4F a second metal 96 (e.g. silver) is shown as having been blanket electroplated over the entire exposed portions of the substrate 82 (which is conductive) and over the first metal 94 (which is also conductive). FIG. 4G depicts the completed first layer of the structure which has resulted from the pla-
narization of the first and second metals down to a height that exposes the first metal and sets a thickness for the first layer. In FIG. 4H the result of repeating the process steps shown in FIGS. 4I-4G several times to form a multi-layer structure are shown where each layer consists of two materials. For most applications, one of these materials is removed as shown in FIG. 4I to yield a desired 3-D structure 98 (e.g. component or device).

[0060] Various embodiments of various aspects of the invention are directed to formation of three-dimensional structures from materials some of which may be electrodeposited or electroless deposited. Some of these structures may be formed from a single build level formed from one or more deposited materials while others are formed from a plurality of build layers each including at least two materials (e.g. two or more layers, more preferably five or more layers, and most preferably ten or more layers). In some embodiments, layer thicknesses may be as small as one micron or as large as fifty microns. In other embodiments, thinner layers may be used while in other embodiments, thicker layers may be used. In some embodiments structures having features positioned with micron level precision and minimum features size on the order of tens of microns are to be formed. In other embodiments structures with less precise feature placement and/or larger minimum features may be formed. In still other embodiments, higher precision and smaller minimum feature sizes may be desirable.

[0061] The various embodiments, alternatives, and techniques disclosed herein may form multi-layer structures using a single patterning technique on all layers or using different patterning techniques on different layers. For example, various embodiments of the invention may perform selective patterning operations using conformable contact masks and masking operations (i.e. operations that use masks which are contacted to but not adhered to a substrate), proximity masks and masking operations (i.e. operations that use masks that at least partially selectively shield a substrate by their proximity to the substrate even if contact is not made), non-conformable masks and masking operations (i.e. masks and operations based on masks whose contact surfaces are not significantly conformable), and/or adhered masks and masking operations (masks and operations that use masks that are adhered to a substrate onto which selective deposition or etching is to occur as opposed to only being contacted to it). Conformable contact masks, proximity masks, and non-conformable contact masks share the property that they are pre-formed and brought to, or in proximity to, a surface which is to be treated (i.e. the exposed portions of the surface are to be treated). These masks can generally be removed without damaging the mask or the surface that received treatment to which they were contacted, or located in proximity to. Adhered masks are generally formed on the surface to be treated (i.e. the portion of that surface that is to be masked) and bonded to that surface such that they cannot be separated from that surface without being completely destroyed damaged beyond any point of reuse. Adhered masks may be formed in a number of ways including (1) by application of a photoresist, selective exposure of the photoresist, and then development of the photoresist, (2) selective transfer of pre-patterned masking material, and/or (3) direct formation of masks from computer controlled depositions of material.

[0062] Patterning operations may be used in selectively depositing material and/or may be used in the selective etching of material. Selectively etched regions may be selectively filled in or filled in via blanket deposition, or the like, with a different desired material. In some embodiments, the layer-by-layer build up may involve the simultaneous formation of portions of multiple layers. In some embodiments, depositions made in association with some layer levels may result in depositions to regions associated with other layer levels (i.e. regions that lie within the top and bottom boundary levels that define a different layer’s geometric configuration). Such use of selective etching and interlaced material deposition in association with multiple layers is described in U.S. patent application Ser. No. 10/434,519, by Smalley, and entitled “Methods of and Apparatus for Electrochemically Fabricating Structures Via Interlaced Layers or Via Selective Etching and Filling of Voids layer elements” which is hereby incorporated herein by reference as if set forth in full.

[0063] Temporary substrates on which structures may be formed may be of the sacrificial-type (i.e. destroyed or damaged during separation of deposited materials to the extent they can not be reused), non-sacrificial-type (i.e. not destroyed or excessively damaged, i.e. not damaged to the extent they may not be reused, e.g. with a sacrificial or release material layer located between the substrate and the initial layers of a structure that is formed). Non-sacrificial substrates may be considered reusable, with little or no rework (e.g. replanarizing one or more selected surfaces or applying a release layer, and the like) though they may or may not be reused for a variety of reasons.

DEFINITIONS

[0064] This section of the specification is intended to set forth definitions for a number of specific terms that may be useful in describing the subject matter of the various embodiments of the invention. It is believed that the meanings of most if not all of these terms is clear from their general use in the specification but they are set forth hereinafter to remove any ambiguity that may exist. It is intended that these definitions be used in understanding the scope and limits of any claims that use these specific terms. As far as interpretation of the claims of this patent disclosure are concerned, it is intended that these definitions take presence over any contradictory definitions or allusions found in any materials which are incorporated herein by reference.

[0065] “Build” as used herein refers, as a verb, to the process of building a desired structure or plurality of structures from a plurality of applied or deposited materials which are stacked and adhered upon application or deposition or, as a noun, to the physical structure or structures formed from such a process. Depending on the context in which the term is used, such physical structures may include a desired structure embedded within a sacrificial material or may include only desired physical structures which may be separated from one another or may require dicing and/or slicing to cause separation.

[0066] “Build axis” or “build orientation” is the axis or orientation that is substantially perpendicular to substantially planar levels of deposited or applied materials that are used in building up a structure. The planar levels of deposited or applied materials may be or may not be completely planar but are substantially so in that the overall extent of their cross-sectional dimensions are significantly greater than the height of any individual deposit or application of material (e.g. 100, 500, 1000, 5000, or more times greater). The planar nature of the deposited or applied materials may come about from use of a process that leads to planar deposits or it may result from
a planarization process (e.g. a process that includes mechanical abrasion, e.g. lapping, fly cutting, grinding, or the like) that is used to remove material regions of excess height. Unless explicitly noted otherwise, “vertical” as used herein refers to the build axis or nominal build axis (if the layers are not stacking with perfect registration) while “horizontal” refers to a direction within the plane of the layers (i.e. the plane that is substantially perpendicular to the build axis).

[0067] “Build layer” or “layer of structure” as used herein does not refer to a deposit of a specific material but instead refers to a region of a build located between a lower boundary level and an upper boundary level which generally defines a single cross-section of a structure being formed or structures which are being formed in parallel. Depending on the details of the actual process used to form the structure, build layers are generally formed on and adhered to previously formed build layers. In some processes the boundaries between build layers are defined by planarization operations which result in successive build layers being formed on substantially planar upper surfaces of previously formed build layers. In some embodiments, the substantially planar upper surface of the preceding build layer may be textured to improve adhesion between the layers. In other build processes, openings may exist in or be formed in the upper surface of a previous but only partially formed build layers such that the openings in the previous build layers are filled with materials deposited in association with current build layers which will cause inter-lacing of build layers and material deposits. Such interlacing is described in U.S. patent application Ser. No. 10/434,519. This referenced application is incorporated herein by reference as if set forth in full. In most embodiments, a build layer includes at least one primary structural material and at least one primary sacrificial material. However, in some embodiments, two or more primary structural materials may be used without a primary sacrificial material (e.g. when one primary structural material is a dielectric and the other is a conductive material). In some embodiments, build layers are distinguishable from each other by the source of the data that is used to yield patterns of the deposits, applications, and/or etchings of material that form the respective build layers. For example, data descriptive of a structure to be formed which is derived from data extracted from different vertical levels of a data representation of the structure define different build layers of the structure. The vertical separation of successive pairs of such descriptive data may define the thickness of build layers associated with the data. As used herein, at times, “build layer” may be loosely referred simply as “layer”. In many embodiments, deposition thickness of primary structural or sacrificial materials (i.e. the thickness of any particular material after it is deposited) is generally greater than the layer thickness and a net deposit thickness is set via one or more planarization processes which may include, for example, mechanical abrasion (e.g. lapping, fly cutting, polishing, and the like) and/or chemical etching (e.g. using selective or non-selective etchants). The lower boundary and upper boundary for a build layer may be set and defined in different ways. From a design point of view they may be set based on a desired vertical resolution of the structure (which may vary with height). From a data manipulation point of view, the vertical layer boundaries may be defined as the vertical levels at which data descriptive of the structure is processed or the layer thickness may be defined as the height separating successive levels of cross-sectional data that dictate how the structure will be formed. From a fabrication point of view, depending on the exact fabrication process used, the upper and lower layer boundaries may be defined in a variety of different ways. For example by planarization levels or effective planarization levels (e.g. lapping levels, fly cutting levels, chemical mechanical polishing levels, mechanical polishing levels, vertical positions of structural and/or sacrificial materials after relatively uniform etch back following a mechanical or chemical mechanical planarization process). For example, by levels at which process steps or operations are repeated. At levels at which, at least theoretically, lateral extends of structural material can be changed to define new cross-sectional features of a structure.

[0068] “Layer thickness” is the height along the build axis between a lower boundary of a build layer and an upper boundary of that build layer.

[0069] “Planarization” is a process that tends to remove materials, above a desired plane, in a substantially non-selective manner such that all deposited materials are brought to a substantially common height or desired level (e.g. within 20%, 10%, 5%, or even 1% of a desired layer boundary level). For example, lapping removes material in a substantially non-selective manner though some amount of recession one material or another may occur (e.g. copper may recess relative to nickel). Planarization may occur primarily via mechanical means, e.g. lapping, grinding, fly cutting, milling, sanding, abrasive polishing, frictionally induced melting, other machining operations, or the like (i.e. mechanical planarization). Mechanical planarization maybe followed or proceeded by thermally induced planarization (e.g. melting) or chemically induced planarization (e.g. etching). Planarization may occur primarily via a chemical and/or electrical means (e.g. chemical etching, electrochemical etching, or the like). Planarization may occur via a simultaneous combination of mechanical and chemical etching (e.g. chemical mechanical polishing (CMP)).

[0070] “Structural material” as used herein refers to a material that remains part of the structure when put into use.

[0071] “Supplemental structural material” as used herein refers to a material that forms part of the structure when the structure is put to use but is not added as part of the build layers but instead is added to a plurality of layers simultaneously (e.g. via one or more coating operations that applies the material, selectively or in a blanket fashion, to a one or more surfaces of a desired build structure that has been released from a sacrificial material.

[0072] “Primary structural material” as used herein is a structural material that forms part of a given build layer and which is typically deposited or applied during the formation of that build layer and which makes up more than 20% of the structural material volume of the given build layer. In some embodiments, the primary structural material may be the same on each of a plurality of build layers or it may be different on different build layers. In some embodiments, a given primary structural material may be formed from two or more materials by the alloying or diffusion of two or more materials to form a single material.

[0073] “Secondary structural material” as used herein is a structural material that forms part of a given build layer and is typically deposited or applied during the formation of the given build layer but is not a primary structural material as it individually accounts for only a small volume of the structural material associated with the given layer. A secondary structural material will account for less than 20% of the volume of the structural material associated with the given
layer. In some preferred embodiments, each secondary structural material may account for less than 10%, 5%, or even 2% of the volume of the structural material associated with the given layer. Examples of secondary structural materials may include seed layer materials, adhesion layer materials, barrier layer materials (e.g., diffusion barrier material), and the like. These secondary structural materials are typically applied to form coatings having thicknesses less than 2 microns, 1 micron, 0.5 microns, or even 0.2 microns. The coatings may be applied in a conformal or directional manner (e.g., via CVD, PVD, electroless deposition, or the like). Such coatings may be applied in a blanket manner or in a selective manner. Such coatings may be applied in a planar manner (e.g., over previously planarized layers of material) as taught in U.S. patent application Ser. No. 10/607,931. In other embodiments, such coatings may be applied in a non-planar manner, for example, in openings in and over a patterned masking material that has been applied to previously planarized layers of material as taught in U.S. patent application Ser. No. 10/841,383. These referenced applications are incorporated herein by reference as if set forth in full herein.

[0074] “Functional structural material” as used herein is a structural material that would have been removed as a sacrificial material but for its actual or effective encapsulation by other structural materials. Effective encapsulation refers, for example, to the inability of an etchant to attack the functional structural material due to inaccessibility that results from a very small area of exposure and/or due to an elongated or tortuous exposure path. For example, large (10,000 μm²) but thin (e.g., less than 0.5 microns) regions of sacrificial copper sandwiched between deposits of nickel may define regions of functional structural material depending on ability of a release etchant to remove the sandwiched copper.

[0075] “Sacrificial material” is material that forms part of a build layer but is not a structural material. Sacrificial material on a given build layer is separated from structural material on that build layer after formation of that build layer is completed and more generally is removed from a plurality of layers after completion of the formation of the plurality of layers during a “release” process that removes the bulk of the sacrificial material or materials. In general sacrificial material is located on a build layer during the formation of one, two, or more subsequent build layers and is thereafter removed in a manner that does not lead to a planarized surface. Materials that are applied primarily for masking purposes, i.e., to allow subsequent selective deposition or etching of a material, e.g., photore sist that is used in forming a build layer but does not form part of the build layer) or that exist as part of a build for less than one or two complete build layer formation cycles are not considered sacrificial materials as the term is used herein but instead shall be referred as masking materials or as temporary materials. These separation processes are sometimes referred to as a release process and may or may not involve the separation of structural material from a build substrate. In many embodiments, sacrificial material within a given build layer is not removed until all build layers making up the three-dimensional structure have been formed. Of course sacrificial material may be, and typically is, removed from above the upper level of a current build layer during planarization operations during the formation of the current build layer. Sacrificial material is typically removed via a chemical etching operation but in some embodiments may be removed via a melting operation or electrochemical etching operation. In typical structures, the removal of the sacrificial material (i.e., release of the structural material from the sacrificial material) does not result in planarized surfaces but instead results in surfaces that are dictated by the boundaries of structural materials located on each build layer. Sacrificial materials are typically distinct from structural materials by having different properties therefrom (e.g., chemical etchability, hardness, melting point, etc.) but in some cases, as noted previously, what would have been a sacrificial material may become a structural material by its actual or effective encapsulation by other structural materials. Similarly, structural materials may be used to form sacrificial structures that are separated from a desired structure during a release process via the sacrificial structures being only attached to sacrificial material or potentially by dissolution of the sacrificial structures themselves using a process that is insufficient to reach structural material that is intended to form part of a desired structure. It should be understood that in some embodiments, small amounts of structural material may be removed, after or during release of sacrificial material. Such small amounts of structural material may have been inadvertently formed due to imperfections in the fabrication process or may result from the proper application of the process but may result in features that are less than optimal (e.g., layers with stairs steps in regions where smooth sloped surfaces are desired. In such cases the volume of structural material removed is typically miniscule compared to the amount that is retained and thus such removal is ignored when labeling materials as sacrificial or structural. Sacrificial materials are typically removed by a dissolution process, or the like, that destroys the geometric configuration of the sacrificial material as it existed on the build layers. In many embodiments, the sacrificial material is a conductive material such as a metal. As will be discussed hereafter, masking materials though typically sacrificial in nature are not termed sacrificial materials herein unless they meet the required definition of sacrificial material.

[0076] “Supplemental sacrificial material” as used herein refers to a material that does not form part of the structure when the structure is put to use and is not added as part of the build layers but instead is added to a plurality of layers simultaneously (e.g., via one or more coating operations that applies the material, selectively or in a blanket fashion, to one or more surfaces of a desired build structure that has been released from an initial sacrificial material. This supplemental sacrificial material will remain in place for a period of time and/or during the performance of certain post layer formation operations, e.g., to protect the structure that was released from a primary sacrificial material, but will be removed prior to putting the structure to use.

[0077] “Primary sacrificial material” as used herein is a sacrificial material that is located on a given build layer and which is typically deposited or applied during the formation of that build layer and which makes up more than 20% of the sacrificial material volume of the given build layer. In some embodiments, the primary sacrificial material may be the same on each of a plurality of build layers or may be different on different build layers. In some embodiments, a given primary sacrificial material may be formed from two or more materials by the alloying or diffusion of two or more materials to form a single material.

[0078] “Secondary sacrificial material” as used herein is a sacrificial material that is located on a given build layer and is typically deposited or applied during the formation of the build layer but is not a primary sacrificial materials as it individually accounts for only a small volume of the sacrifi-
cial material associated with the given layer. A secondary sacrificial material will account for less than 20% of the volume of the sacrificial material associated with the given layer. In some preferred embodiments, each secondary sacrificial material may account for less than 10%, 5%, or even 2% of the volume of the sacrificial material associated with the given layer. Examples of secondary structural materials may include seed layer materials, adhesion layer materials, barrier layer materials (e.g., diffusion barrier material), and the like. These secondary sacrificial materials are typically applied to form coatings having thicknesses less than 2 microns, 1 micron, 0.5 microns, or even 0.2 microns. The coatings may be applied in a conformal or directional manner (e.g., via CVD, PVD, electroleos deposition, or the like). Such coatings may be applied in a blanket manner or in a selective manner. Such coatings may be applied in a planar manner (e.g., over previously planarized layers of material) as taught in U.S. patent application Ser. No. 10/607,931. In other embodiments, such coatings may be applied in a non-planar manner, for example, in openings and in over a patterned masking material that has been applied to previously planarized layers of material as taught in U.S. patent application Ser. 10/641,383. These referenced applications are incorporated herein by reference as if set forth in full herein.

[0075] “Adhesion layer”, “seed layer”, “barrier layer”, and the like refer to coatings of material that are thin in compari-
son to the layer thickness and thus generally form secondary structural material portions or sacrificial material portions of some layers. Such coatings may be applied uniformly over a previously formed build layer, they may be applied over a portion of a previously formed build layer and over patterned structural or sacrificial material existing on a current (i.e., partially formed) build layer so that a non-planar seed layer results, or they may be selectively applied to only certain locations on a previously formed build layer. In the event such coatings are non-selectively applied, selected portions may be removed (1) prior to depositing either a sacrificial material or structural material as part of a current layer or (2) prior to beginning formation of the next layer or they may remain in place through the layer build-up process and then etched away after formation of a plurality of build layers.

[0080] “Masking material” is a material that may be used as a tool in the process of forming a build layer but does not form part of that build layer. Masking material is typically a photopolymer or photoresist material or other material that may be readily patterned. Masking material, though typically sacrificial in nature, is not a sacrificial material as the term is used herein. Masking material is typically applied to a surface during the formation of a build layer for the purpose of allowing selective deposition, etching, or other treatment and is removed either during the process of forming that build layer or immediately after the formation of that build layer.

[0081] “Multilayer structures” are structures formed from multiple build layers of deposited or applied materials.

[0082] “Multilayer three-dimensional (or 3D or 3-D) structures” are Multilayer Structures that meet at least one of two criteria: (1) the structural material portion of at least two layers of which one has structural material portions that do not overlap structural material portions of the other.

[0083] “Complex multilayer three-dimensional (or 3D or 3-D) structures” are multilayer three-dimensional structures formed from at least three layers where a line may be defined that hypothetically extends vertically through at least some portion of the build layers of the structure will extend from structural material through sacrificial material and back through structural material or will extend from sacrificial material through structural material and back through sacrificial material (these might be termed vertically complex multilayer three-dimensional structures). Alternatively, complex multilayer three-dimensional structures may be defined as multilayer three-dimensional structures formed from at least two layers where a line may be defined that hypothetically extends horizontally through at least some portion of a build layer of the structure that will extend from structural material through sacrificial material and back through structural material or will extend from sacrificial material through structural material and back through sacrificial material (these might be termed horizontally complex multilayer three-dimensional structures). Worded another way, in complex multilayer three-dimensional structures, a vertically or horizontally extending hypothetical line will extend from one or structural material or void (when the sacrificial material is removed) to the other of void or structural material and then back to structural material or void as the line is traversed along at least a portion of the line.

[0084] “Moderately complex multilayer three-dimensional (or 3D or 3-D) structures are complex multilayer 3D structures for which the alternating of void and structure or structure and void not only exists along one of a vertically or horizontally extending line but along lines extending both vertically and horizontally.

[0085] “Highly complex multilayer (or 3D or 3-D) structures are complex multilayer 3D structures for which the structure-to-void-to-structure or void-to-structure-to-void alternating occurs once along the line but occurs a plurality of times along a definable horizontally or vertically extending line.

[0086] “Up-facing feature” is an element dictated by the cross-sectional data for a given build layer “n” and a next build layer “n+1” that is to be formed from a given material that exists on the build layer “n” but does not exist on the immediately preceding build layer “n+1”. For convenience the term “up-facing feature” will apply to such features regardless of the build orientation.

[0087] “Down-facing feature” is an element dictated by the cross-sectional data for a given build layer “n” and a preceding build layer “n–1” that is to be formed from a given material that exists on build layer “n–1” but does not exist on the immediately preceding build layer “n–1”. As with up-facing features, the term “down-facing feature” shall apply to such features regardless of the actual build orientation.

[0088] “Continuing region” is the portion of a given build layer “n” that is dictated by the cross-sectional data for the given build layer “n”, a next build layer “n+1” and a preceding build layer “n–1” that is neither up-facing nor down-facing for the build layer “n”.

[0089] “Minimum feature size” refers to a necessary or desirable spacing between structural material elements on a given layer that are to remain distinct in the final device configuration. If the minimum feature size is not maintained on a given layer, the fabrication process may result in structural material inadvertently bridging the two structural elements due to masking material failure or failure to appropriately fill voids with sacrificial material during formation of the given layer such that during formation of a subsequent layer structural material inadvertently fills the void. More care during fabrication can lead to a reduction in minimum
feature size or a willingness to accept greater losses in productivity can result in a decrease in the minimum feature size. However, during fabrication for a given set of process parameters, inspection diligence, and yield (successful level of production) a minimum design feature size is set in one way or another. The above described minimum feature size may more appropriately be termed minimum feature size of sacrificial material regions. Conversely a minimum feature size for structural material regions (minimum width or length of structural material elements) may be specified. Depending on the fabrication method and order of deposition of structural material and sacrificial material, the two types of minimum feature sizes may be different. In practice, for example, using electrochemical fabrication methods and described herein, the minimum features size on a given layer may be roughly set to a value that approximates the layer thickness used to form the layer and it may be considered the same for both structural and sacrificial material widths and lengths. In some more rigorously implemented processes, examination regiments, and rework requirements, it may be set to an amount that is 80%, 50%, or even 30% of the layer thickness. Other values or methods of setting minimum feature sizes may be set.  

PACKAGING EMBODIMENTS

[0090] FIGS. 5A-5D schematically depict side views of various stages in a process for attaching an example IC to an example package where interconnects from the IC to at least one other component include vias that extend through a substrate on which electrochemically fabricated routing elements are formed.  

[0091] FIG. 5A depicts a substrate 102 for use with some embodiments of the invention. The substrate includes a plurality of conductive vias 104 through a dielectric material 106 (e.g. a ceramic, glass, or plastic material) that extend from a lower surface 108 to an upper surface 110 of the substrate. In some embodiments the vias may be uniformly spaced with a desired pattern while in other embodiments they may be spaced in an irregular pattern. In some embodiments the via may extend along straight paths perpendicular to the top and bottom surfaces while in other embodiments, the paths may form more complex patterns including merging and/or diverging configurations and/or they may not extend perpendicular to the surfaces. In some embodiments, one or both the top and bottom surfaces may not be planar and/or the surfaces may not be parallel to one another. The substrate 102 may be formed in a variety of ways such as by low temperature co-fired ceramic (LTCC) formation methods, multi-layer ceramic (MLC) formation methods, electrochemical fabrication methods, drilling vias in a dielectric material and filling the vias with conductive material, and the like.  

[0092] FIG. 5B depicts the state of the process after formation of a routing elements 122 has occurred via an electrochemical fabrication process. In some embodiments (as shown), the routing elements 122 may be partially encapsulated by a dielectric material 124. The electrochemical fabrication process, for example, may be one of those shown and described in association with FIGS. 2A-2F or 4A-4F or as described in the various other patent applications incorporated herein by reference. In particular, in some embodiments, the electrochemical fabrication process may involve the deposition of a conductive material and a dielectric material during the formation of each layer (e.g. as described in U.S. Patent Application No. 60/574,733, which was filed on May 26, 2004, by Lockard et al., and entitled “Methods for Electrochemically Fabricating Structures Using Adhered Masks, Incorporating Dielectric Sheets, and/or Seed Layers That Are Partially Removed Via Planarization”, which is incorporated herein by reference as if set forth in full). In other embodiments, each layer may be formed with a structural material (e.g. a material used in forming routing elements) and a sacrificial material (e.g. a material occupying regions that are to contain a dielectric) where after partial or complete formation of the substrate thickness, the sacrificial material may be transformed into a desired dielectric material or removed and replaced with a desired dielectric material, after which an optional planarization operation may be used to set or reset the thickness of the structure. As shown in FIG. 5B, the electrochemically fabricated structure may include various electronic components such as inductor 126 and capacitor 124. In other embodiments, other passive or active devices may be included in the structure while in still other embodiments such electronic devices need not be formed as part of, or otherwise included in, the structure. In some embodiments, added components may not be embedded in dielectric material but may instead be located within voids in the dielectric material.  

[0093] FIG. 5C shows the state of the process after an IC 132 is moved along arrow 134 and brought into contact with the electrochemically fabricated structure 120, after which it may they may be bonded or otherwise connected to one another (e.g. via flip-chip attachment). Such bonding may occur, for example, using solder bumps 136 which are located on the bottom of IC 132. In other embodiments, solder bumps may be alternatively or additionally located on selected portions of the structure 120. In still other embodiments it may be possible to use other bonding or mounting techniques, such as for example, spring contactors, in combination with retention elements such as sockets, clips, hooks, adhesive, or the like.  

[0094] FIG. 5D shows the state of the process after additional components, such as spring elements 142, have been added to the assembly. As can be seen in FIGS. 5C and 5D, various pads on the IC makes electric contact with elements 122 some of which electrically connect various portions pads of the IC to one another while others connect electric pads of the IC to the vias which in turn may electrically connect to other circuit elements (not shown). As can be seen in FIGS. 5B-5D, some routing elements may be in the form of simple conductive leads 122 while others may be in the form of shielded 122 conductive leads (e.g. coaxial elements), while still others may be in the form of waveguides (not shown), or the like. The routing elements may change dimensions, orientation, and the like for making desired electrical connections, avoiding inappropriate contact with other routing elements, enhancing electrical, thermal, and/or attributes of the package. For example, ground (GND) and voltage (VDD) connections may be made with arbitrarily wide for better current supply and lower inductance. Conductive traces in structure 120 may touch hot spots on an IC or other components to spread and/or conduct heat away.  

[0095] FIG. 6 schematically depicts a side view of two example ICs attached to and at least partially electrically interconnected to one another via an example package where at least a portion of the interconnects extend through routing elements formed via electrochemical fabrication. As shown, some routing elements conduct signals from each IC to the vias in the substrate, and/or from one IC to the other IC. The conducted signals may be shielded (e.g. via coaxial routing elements) or non-shielded, they may be power or ground
signals, data signals, clock signals, or the like. As indicated a shielded, e.g., coaxial connection, ultra-high bandwidth connection may be used between a processor IC (the left IC) and its memory IC (the right IC). Such shielded interconnect elements may provide: (1) non-dispersive signal transmission, (2) little or no cross-talk, (3) low loss (<0.5 dB/cm), (4) vastly improved routing flexibility for shortest point-to-point connections, (5) arbitrary thickness and low-inductance GNNDVYDD connections, and/or (6) routing of the main clock tree connections off the die for die size savings and power savings.

Fig. 7 schematically depicts a side view of an example IC attached to an alternative example package configuration, where the package configuration includes a conductive substrate, routing elements that provide interconnect paths from a surface of the package to the IC, and which includes passive components such as inductors and capacitors. The routing elements of the electrochemically fabricated structure 140 do not feed signals from the IC 142 to vias that extend through the substrate but instead to pads 146 located on upper surface 144 of structure 144. The pads 146 are covered with solder bumps (in this example) which may be used in establishing electrical and possibly mechanical bonding to another circuit element (not shown). In other embodiments, electrical connection may be established via other elements (e.g., wire bonding) and/or mechanical attachment may be established via other elements (e.g., adhesives, clips, sockets, or the like). The substrate in Fig. 7 is made of a solid block of conductive material which may be useful in helping conduct heat away from IC 142. In some alternative embodiments some insulated vias may pass through the substrate. In the embodiment of Fig. 7, the IC 142 is located within an indentation in the electrochemically fabricated structure so that appropriate positioning of the upper surface 144 relative to the IC 142 was obtained. In other embodiments, the IC may have an upper surface (after attachment) which is not below surface 144 but is coincident with it or which is above it.

The opening in the structure 140 into which IC 142 is placed may be formed in a variety of ways, for example, via an electrochemical fabrication process by forming routing elements from a conductive structural material, the opening 148 from a sacrificial material that is eventually removed, and the other regions from a desired dielectric material. Methods allowing such three material formation processes are set forth in a plurality of the patent applications incorporated herein by reference, for example in U.S. patent application Ser. No. 10/434,519. In other embodiments, more than one opening may exist into which a plurality of ICs or other components may be located.

In some alternatives to the embodiment of Figs. 5A-5D, 6, and 7, the electrochemically fabricated structure may be substantially formed from conductive material which is located in different regions by relative thin or narrow locations of dielectric material such that the dielectric material provides appropriate isolation and impedance characteristics but such that the structure as a whole as improved thermal conductive properties for remove heat from an IC or other electronic component that is mounted on it.

Fig. 8 schematically depicts a side view of an example IC attached to a package whose configuration is similar to that of Fig. 7 with the exception that the substrate 150 includes a passage 152 for allowing a cooling fluid to pass through the substrate as indicated by arrows 154.

Fig. 9 schematically depicts a side view of two example ICs and a package with routing element and which further includes an added packaging element that takes the form of a heat sink 160 that is located above one of the ICs and which includes a passage 162 through which a cooling liquid may flow as indicated by arrows 164.

In some alternative embodiments substrates shown in Figs. 5A-5D, Fig. 6, Fig. 7, and Fig. 9 may be removed after formation of the patterned layers, as shown in Fig. 10. As shown in Fig. 10 solder bumps may be placed on the bottom surface of the routing structure that may be used in making electrical contacts.

The packaging embodiments provided explicitly herein may be combined with the packaging embodiments provided in U.S. patent application Ser. No. 10/434,103, filed on May 7, 2003, to provide hermetically sealed packages. Such packages may protect ICs and other circuit elements from environmental damage.

In some embodiments, the packaging may include separately or integrally formed mechanically active devices (e.g., accelerometers, photonics alignment structures, pressure sensors, other sensors, actuators, and the like).

Some embodiments may employ mask based selective etching operations in conjunction with blanket deposition operations. Some embodiments may form structures on a layer-by-layer basis but deviate from a strict planar layer on planar layer build up process in favor of a process that interlacing material between the layers. Such alternating build processes are disclosed in U.S. application Ser. No. 10/434, 519, filed on May 7, 2003, entitled Methods of and Apparatus for Electrochemically Fabricating Structures Via Interfaced Layers or Via Selective Etching and Filling of Voids which is herein incorporated by reference as if set forth in full.

Some embodiments may employ diffusion bonding or the like to enhance adhesion between successive layers of material. Various teachings concerning the use of diffusion bonding in electrochemical fabrication processes are set forth in U.S. patent application Ser. No. 10/841,384 which was filed May 7, 2004 by Cohen et al. which is entitled “Method of Electrochemically Fabricating Multilayer Structures Having Improved Interlayer Adhesion” which is hereby incorporated herein by reference as if set forth in full. This application is hereby incorporated herein by reference as if set forth in full.

In some embodiments, integrated circuits may be packaged using compliant contact elements (e.g., microprobes) and as such, enhanced embodiments of the present invention may result from the combination of microprobe fabrication technology with the teachings expressly set forth herein. Teaching about microprobes and electrochemical fabrication techniques are set forth in a number of U.S. patent applications which were filed on Dec. 31, 2003. These Filings include: (1) U.S. Patent Application No. 60/533,933, by Arat et al. and which is entitled “Electrochemically Fabricated Microprobes”; (2) U.S. Patent Application No. 60/533,975, by Kim et al. and which is entitled “Microprobe Tips and Methods for Making”; (3) U.S. Patent Application No. 60/533,947, by Kumar et al. and which is entitled “Probe Arrays and Method for Making”; and (4) U.S. Patent Application No. 60/533,948, by Cohen et al. and which is entitled “Electrochemical Fabrication Method for Co-Fabricating Probes and Space Transformers”. These patent fillings are each hereby incorporated herein by reference as if set forth in full herein.

Further teachings about planarizing layers and setting layers thicknesses and the like are set forth in the following U.S. Patent Applications which were filed Dec. 31, 2003: (1) U.S. patent application No. 60/534,159 by Cohen et al. and which is entitled “Electrochemical Fabrication Methods for Producing Multilayer Structures Including the use of Diamond Machining in the Planarization of Deposits of Material” and (2) U.S. patent application No. 60/534,183 by Cohen et al. and which is entitled “Method and Apparatus for Maintaining Parallelism of Layers and/or Achieving Desired Thicknesses of Layers During the Electrochemical Fabrication of Structures”. The techniques disclosed explicitly herein may benefit by combining them with the techniques disclosed in U.S. patent application Ser. No. 11/029,220, filed Jan. 3, 2005 by Frodis et al. and entitled “Method and Apparatus for Maintaining Parallelism of Layers and/or Achieving Desired Thicknesses of Layers During the Electrochemical Fabrication of Structures”. These patent filings are each hereby incorporated herein by reference as if set forth in full herein.

Additional teachings concerning the formation of structures on dielectric substrates and/or the formation of structures that incorporate dielectric materials into the formation process and possibility into the final structures as formed are set forth in a number of patent applications: (1) U.S. Patent Application No. 60/534,184, by Cohen, which was filed on Dec. 31, 2003, and which is entitled “Electrochemical Fabrication Methods Incorporating Dielectric Materials and/or Using Dielectric Substrates”; (2) U.S. Patent Application No. 60/533,932, by Cohen, which was filed on Dec. 31, 2003, and which is entitled “Electrochemical Fabrication Methods Using Dielectric Substrates”; (3) U.S. Patent Application No. 60/554,157, by Lockard et al., which was filed on Dec. 31, 2004, and which is entitled “Electrochemical Fabrication Methods Incorporating Dielectric Materials”; (4) U.S. patent application Ser. No. 10/841,300 and 60/574,733, both by Lockard et al., filed on May 7, 2004 and May 26, 2004, respectively, and both entitled “Methods for Electrochemically Fabricating Structures Using Adhered Masks, Incorporating Dielectric Sheets, and/or Seed Layers that are Partially Removed Via Planarization”; and U.S. Patent Application No. 60/533,895, by Lembrikov et al., which was filed on Dec. 31, 2003, and which is entitled “Electrochemical Fabrication Method for Producing Multi-layer Three-Dimensional Structures on a Porous Dielectric”. The techniques disclosed explicitly herein may benefit by combining them with the techniques disclosed in U.S. patent application Ser. No. 11/029,216 filed Jan. 3, 2005 by Cohen et al. and entitled “Electrochemical Fabrication Methods Incorporating Dielectric Materials and/or Using Dielectric Substrates” and U.S. Patent Application No. 60/641,292 filed Jan. 3, 2005 by Dennis R. Smalley and entitled “Method of Forming Electrically Isolated Structures Using Thin Dielectric Coatings”. These patent filings are each hereby incorporated herein by reference as if set forth in full herein.

Many other alternative embodiments will be apparent to those of skill in the art upon reviewing the teachings herein. Further embodiments may be formed from a combination of the various teachings explicitly set forth in the body of this application. Even further embodiments may be formed by combining the teachings set forth explicitly herein with teachings set forth in the following patents and patent applications each of which is hereby incorporated herein by reference:

Various other embodiments of the present invention exist. Some embodiments may not use any blanket deposition process and/or they may not use a planarization process. Some embodiments may involve the selective deposition of a plurality of different materials on a single layer or on different layers. Some embodiments may use selective deposition processes or blanket deposition processes on some or all layers that are not electrodeposition processes. Some embodiments may, for example, use nickel, copper, gold, and/or dielectric materials as structural materials while other embodiments may use different materials. Some embodiments may remove a sacrificial material while other embodiments may not. Some embodiments may employ mask based selective etching operations in conjunction with blanket deposition operations. Some embodiments may form structures on a layer-by-layer basis but which deviate from a strict planar layer on planar layer build up process in favor of a process that interleaves material between the layers. Such alternating build processes are disclosed in U.S. application Ser. No. 10/434,519, filed on May 7, 2003, entitled Methods of and Apparatus for Electrochemically Fabricating Structures Via Interlaced Layers or Via Selective Etching and Filling of Voids which is herein incorporated by reference as if set forth in full.

Many other alternative embodiments will be apparent to those of skill in the art upon reviewing the teachings herein. Further embodiments may be formed from a combination of the various teachings explicitly set forth in the body of this application. Even further embodiments may be formed by combining the teachings set forth explicitly herein with teachings set forth in the various applications and patents referenced herein, each of which is incorporated herein by reference.

In view of the teachings herein, many further embodiments, alternatives in design and uses of the instant invention will be apparent to those of skill in the art. As such, it is not intended that the invention be limited to the particular illustrative embodiments, alternatives, and uses described above but instead that it be solely limited by the claims presented hereafter.

We claim:

1. A fabrication process for fabricating a package for holding an electronic component, comprising:
   (a) forming and adhering a layer of material to a previously formed layer and/or to a substrate, wherein the layer comprises a desired pattern of at least one material; and
   (b) repeating the forming and adhering operation of (a) a plurality of times to build up a configuration of conductive interconnect elements in a configuration of a desired package, wherein the plurality of layers are adhered to
one another and comprise at least one of (i) at least one structural material and at least one sacrificial material or (ii) at least two structural materials one of which is a conductor and one of which is a dielectric.

2. The process of claim 1 wherein the package comprises metal electrodeposited or electroless deposited on a layer by layer basis where the height of at least some layers is set by a planarization operation that planarizes an interconnect material and at least one other material.

3. The process of claim 1 wherein the package comprises vias and traces that coexist on at least some layers.

4. The process of claim 1 wherein the package comprises at least one more coaxial interconnects.

5. The process of claim 1 wherein the package comprises interconnects having traces having at least two different widths.

6. The process of claim 1 wherein the package comprises interconnects comprising vias that have at least two different widths.

7. The process of claim 1 wherein the package comprises interconnects have trace thicknesses that are at least as thick as some planarized thicknesses of a dielectric material.

8. The process of claim 1 wherein the package comprises interconnects having trace thicknesses that are at least as thick as the differential height between some interconnect traces.

9. The process of claim 1 wherein the at least one layer of the package is formed using a process comprising: patterning a first material, applying a non-planar seed layer, electrode-depositing a second material, and trimming off at least a portion of the deposited first material.

10. A fabrication process for fabricating a packaged electronic component, comprising:
    providing a substrate having conductive vias;
    forming routing elements on the substrate which have first and second ends, where at least some of the first ends are connectable to a first electronic component and at least some of the second ends connect to vias on the substrate; and
    attaching the first electronic component to at least some of the first ends.

11. A fabrication process for fabricating a packaged electronic component, comprising:
    providing a substrate;
    forming routing elements on the substrate which have first and second ends, where at least some of the first ends are connectable to a first electronic component and at least some of the second ends are connectable to a second electronic component; and
    attaching the first and second electronic components to the at least some of the first ends and second ends, respectively.

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