(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
1 May 2014 (01.05.2014)

WIPO | PCT

(10) International Publication Number
WO 2014/066421 A1

(51) International Patent Classification:
H03F 3/19 (2006.01) *H03F 1/26* (2006.01)
H03F 1/22 (2006.01) *H03F 3/24* (2006.01)
H03F 3/72 (2006.01) *H03F 3/68* (2006.01)
H03F 3/21 (2006.01)

(21) International Application Number:
PCT/US2013/066230

(22) International Filing Date:
22 October 2013 (22.10.2013)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
13/656,904 22 October 2012 (22.10.2012) US

(71) Applicant: **QUALCOMM INCORPORATED** [US/US]; Attn: International IP Administration, 5775 Morehouse Drive, San Diego, CA 92121 (US).

(72) Inventors: **XU, Rui**; 5775 Morehouse Drive, San Diego, CA 92121 (US). **CHANG, Li-Chung**; 5775 Morehouse Drive, San Diego, CA 92121 (US).

(74) Agent: **MOBARHAN, Ramin**; Attn: International IP Administration, 5775 Morehouse Drive, San Diego, CA 92121 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

(54) Title: AMPLIFIERS WITH NOISE SPLITTING

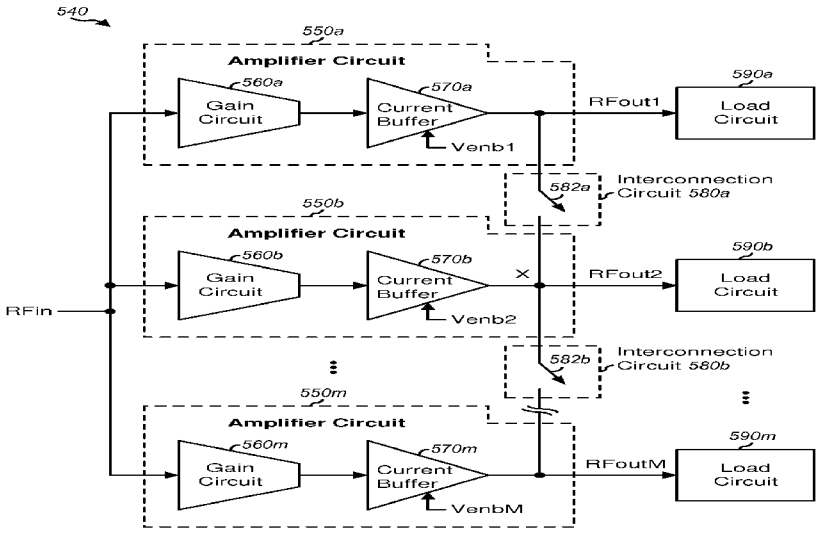

FIG. 5

(57) Abstract: Amplifiers with noise splitting to improve noise figure are disclosed. In an exemplary design, an apparatus (e.g., a wireless device, an integrated circuit, etc.) includes a plurality of amplifier circuits (550a, 550b, 550m) and at least one interconnection circuit (580a, 580b). The amplifier circuits (550a, 550b, 550m) receive an input radio frequency signal (RFin). The interconnection circuits (580a, 580b) are coupled between the plurality of amplifier circuits (550a, 550b, 550m). Each interconnection circuit (580a, 580b) is closed to short the outputs or internal nodes of two amplifier circuits coupled to that interconnection circuit (580a, 580b). The plurality of amplifier circuits (550a, 550b, 550m) may include a plurality of gain circuits (560a, 560b, 560m) coupled to a plurality of current buffers (570a, 570b, 570m), one gain circuit and one current buffer for each amplifier circuit.

WO 2014/066421 A1

AMPLIFIERS WITH NOISE SPLITTING

BACKGROUND

I. Field

[0001] The present disclosure relates generally to electronics, and more specifically to amplifiers.

II. Background

[0002] A wireless device (e.g., a cellular phone or a smartphone) in a wireless communication system may transmit and receive data for two-way communication. The wireless device may include a transmitter for data transmission and a receiver for data reception. For data transmission, the transmitter may modulate a radio frequency (RF) carrier signal with data to obtain a modulated RF signal, amplify the modulated RF signal to obtain an amplified RF signal having the proper output power level, and transmit the amplified RF signal via an antenna to a base station. For data reception, the receiver may obtain a received RF signal via the antenna and may amplify and process the received RF signal to recover data sent by the base station.

[0003] A wireless device may support carrier aggregation, which is simultaneous operation on multiple carriers. A carrier may refer to a range of frequencies used for communication and may be associated with certain characteristics. For example, a carrier may be associated with system information describing operation on the carrier. A carrier may also be referred to as a component carrier (CC), a frequency channel, a cell, etc. It is desirable to efficiently support carrier aggregation by the wireless device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIG. 1 shows a wireless device communicating with a wireless system.

[0005] FIGS. 2A to 2D show four examples of carrier aggregation (CA).

[0006] FIG. 3 shows a block diagram of the wireless device in FIG. 1.

[0007] FIG. 4 shows a single-input multiple-output (SIMO) low noise amplifier (LNA) without noise splitting.

[0008] FIG. 5 shows a SIMO LNA with noise splitting at current buffer output.

[0009] FIGS. 6A to 7C show some exemplary designs of the SIMO LNA with noise splitting at current buffer output.

[0010] FIG. 8 shows a SIMO LNA with noise splitting at gain circuit output.

[0011] FIGS. 9A to 9C show some exemplary designs of the SIMO LNA with noise splitting at gain circuit output.

[0012] FIG. 10 shows a process for performing signal amplification.

DETAILED DESCRIPTION

[0013] The detailed description set forth below is intended as a description of exemplary designs of the present disclosure and is not intended to represent the only designs in which the present disclosure can be practiced. The term "exemplary" is used herein to mean "serving as an example, instance, or illustration." Any design described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other designs. The detailed description includes specific details for the purpose of providing a thorough understanding of the exemplary designs of the present disclosure. It will be apparent to those skilled in the art that the exemplary designs described herein may be practiced without these specific details. In some instances, well-known structures and devices are shown in block diagram form in order to avoid obscuring the novelty of the exemplary designs presented herein.

[0014] Amplifier with noise splitting and having good performance and other desirable characteristics are disclosed herein. These amplifiers may include SIMO LNAs supporting simultaneous reception of multiple transmitted signals. These amplifiers may be used for various types of electronic devices such as wireless communication devices.

[0015] **FIG. 1** shows a wireless device 110 communicating with a wireless communication system 120. Wireless system 120 may be a Long Term Evolution (LTE) system, a Code Division Multiple Access (CDMA) system, a Global System for Mobile Communications (GSM) system, a wireless local area network (WLAN) system, or some other wireless system. A CDMA system may implement Wideband CDMA (WCDMA), CDMA 1X, Evolution-Data Optimized (EVDO), Time Division Synchronous CDMA (TD-SCDMA), or some other version of CDMA. For simplicity, FIG. 1 shows wireless system 120 including two base stations 130 and 132 and one system controller 140. In general, a wireless system may include any number of base stations and any set of network entities.

[0016] Wireless device 110 may also be referred to as a user equipment (UE), a mobile station, a terminal, an access terminal, a subscriber unit, a station, etc. Wireless device

110 may be a cellular phone, a smartphone, a tablet, a wireless modem, a personal digital assistant (PDA), a handheld device, a laptop computer, a smartbook, a netbook, a cordless phone, a wireless local loop (WLL) station, a Bluetooth device, etc. Wireless device 110 may communicate with wireless system 120. Wireless device 110 may also receive signals from broadcast stations (e.g., a broadcast station 134), signals from satellites (e.g., a satellite 150) in one or more global navigation satellite systems (GNSS), etc. Wireless device 110 may support one or more radio technologies for wireless communication such as LTE, WCDMA, CDMA 1X, EVDO, TD-SCDMA, GSM, 802.11, etc.

[0017] Wireless device 110 may support carrier aggregation, which is operation on multiple carriers. Carrier aggregation may also be referred to as multi-carrier operation. Wireless device 110 may be able to operate in low-band from 698 to 960 megahertz (MHz), mid-band from 1475 to 2170 MHz, and/or high-band from 2300 to 2690 and 3400 to 3800 MHz. Low-band, mid-band, and high-band refer to three groups of bands (or band groups), with each band group including a number of frequency bands (or simply, "bands"). Each band may cover up to 200 MHz and may include one or more carriers. Each carrier may cover up to 20 MHz in LTE. LTE Release 11 supports 35 bands, which are referred to as LTE/UMTS bands and are listed in 3GPP TS 36.101. Wireless device 110 may be configured with up to five carriers in one or two bands in LTE Release 11.

[0018] In general, carrier aggregation (CA) may be categorized into two types - intra-band CA and inter-band CA. Intra-band CA refers to operation on multiple carriers within the same band. Inter-band CA refers to operation on multiple carriers in different bands.

[0019] **FIG. 2A** shows an example of contiguous intra-band CA. In the example shown in FIG. 2A, wireless device 110 is configured with four contiguous carriers in one band in low-band. Wireless device 110 may send and/or receive transmissions on multiple contiguous carriers within the same band.

[0020] **FIG. 2B** shows an example of non-contiguous intra-band CA. In the example shown in FIG. 2B, wireless device 110 is configured with four non-contiguous carriers in one band in low-band. The carriers may be separated by 5 MHz, 10 MHz, or some other amount. Wireless device 110 may send and/or receive transmissions on multiple non-contiguous carriers within the same band.

[0021] **FIG. 2C** shows an example of inter-band CA in the same band group. In the example shown in FIG. 2C, wireless device 110 is configured with four carriers in two bands in low-band. Wireless device 110 may send and/or receive transmissions on multiple carriers in different bands in the same band group.

[0022] **FIG. 2D** shows an example of inter-band CA in different band groups. In the example shown in FIG. 2D, wireless device 110 is configured with four carriers in two bands in different band groups, which include two carriers in one band in low-band and two carriers in another band in mid-band. Wireless device 110 may send and/or receive transmissions on multiple carriers in different bands in different band groups.

[0023] FIGS. 2A to 2D show four examples of carrier aggregation. Carrier aggregation may also be supported for other combinations of bands and band groups.

[0024] **FIG. 3** shows a block diagram of an exemplary design of wireless device 110 in FIG. 1. In this exemplary design, wireless device 110 includes a transceiver 320 coupled to a primary antenna 310, a transceiver 322 coupled to a secondary antenna 312, and a data processor/controller 380. Transceiver 320 includes multiple (K) receivers 330pa to 330pk and multiple (K) transmitters 350pa to 350pk to support multiple frequency bands, multiple radio technologies, carrier aggregation, etc. Transceiver 322 includes L receivers 330sa to 330sl and L transmitters 350sa to 350sl to support multiple frequency bands, multiple radio technologies, carrier aggregation, receive diversity, multiple-input multiple-output (MIMO) transmission from multiple transmit antennas to multiple receive antennas, etc.

[0025] In the exemplary design shown in FIG. 3, each receiver 330 includes an LNA 340 and receive circuits 342. For data reception, antenna 310 receives signals from base stations and/or other transmitter stations and provides a received RF signal, which is routed through an antenna interface circuit 324 and presented as an input RF signal to a selected receiver. Antenna interface circuit 324 may include switches, duplexers, transmit filters, receive filters, matching circuits, etc. The description below assumes that receiver 330pa is the selected receiver. Within receiver 330pa, an LNA 340pa amplifies the input RF signal and provides an output RF signal. Receive circuits 342pa downconvert the output RF signal from RF to baseband, amplify and filter the downconverted signal, and provide an analog input signal to data processor 380. Receive circuits 342pa may include mixers, filters, amplifiers, matching circuits, an oscillator, a local oscillator (LO) generator, a phase locked loop (PLL), etc. Each

remaining receiver 330 in transceivers 320 and 322 may operate in similar manner as receiver 330pa.

[0026] In the exemplary design shown in FIG. 3, each transmitter 350 includes transmit circuits 352 and a power amplifier (PA) 354. For data transmission, data processor 380 processes (e.g., encodes and modulates) data to be transmitted and provides an analog output signal to a selected transmitter. The description below assumes that transmitter 350pa is the selected transmitter. Within transmitter 350pa, transmit circuits 352pa amplify, filter, and upconvert the analog output signal from baseband to RF and provide a modulated RF signal. Transmit circuits 352pa may include amplifiers, filters, mixers, matching circuits, an oscillator, an LO generator, a PLL, etc. A PA 354pa receives and amplifies the modulated RF signal and provides a transmit RF signal having the proper output power level. The transmit RF signal is routed through antenna interface circuit 324 and transmitted via antenna 310. Each remaining transmitter 350 in transceivers 320 and 322 may operate in similar manner as transmitter 350pa.

[0027] FIG. 3 shows an exemplary design of receiver 330 and transmitter 350. A receiver and a transmitter may also include other circuits not shown in FIG. 3, such as filters, matching circuits, etc. All or a portion of transceivers 320 and 322 may be implemented on one or more analog integrated circuits (ICs), RF ICs (RFICs), mixed-signal ICs, etc. For example, LNAs 340, and receive circuits 342 and may be implemented on one module, which may be an RFIC, etc. The circuits in transceivers 320 and 322 may also be implemented in other manners.

[0028] Data processor/controller 380 may perform various functions for wireless device 110. For example, data processor 380 may perform processing for data being received via receivers 330 and data being transmitted via transmitters 350. Controller 380 may control the operation of the various circuits within transceivers 320 and 322. A memory 382 may store program codes and data for data processor/controller 380. Data processor/controller 380 may be implemented on one or more application specific integrated circuits (ASICs) and/or other ICs.

[0029] Wireless device 110 may include one or more SIMO LNAs. A SIMO LNA includes a single input and multiple (M) outputs and can receive a single input RF signal at its input and provide up to M output RF signals from up to M outputs. A SIMO LNA may be used to simultaneously receive (i) multiple transmissions sent on multiple carriers in the same band for intra-band CA or (ii) multiple transmitted signals from different wireless systems (e.g., LTE and WCDMA).

[0030] **FIG. 4** shows a block diagram of an exemplary design of a SIMO LNA 440 without noise splitting. SIMO LNA 440 includes multiple (M) amplifier circuits 450a to 450m coupled to M load circuits 490a to 490m, respectively. The inputs of all M amplifier circuits 450a to 450m are coupled together. Each amplifier circuit 450 includes a gain circuit 460 coupled to a current buffer 470. Each amplifier circuit 450 may be enabled by turning on its current buffer 470 via a respective Venb control signal.

[0031] An input RF signal (RFin) is applied to the M amplifier circuits 450a to 450m. One or more amplifier circuits 450 may be enabled by turning on the associated current buffers 470. For example, N amplifier circuits 450 may be enabled to concurrently receive transmissions on N sets of carriers in the same band for intra-band CA, where $1 \le N \le M$. Each set of carriers may include one or more carriers. Each enabled amplifier circuit 450 may amplify the input RF signal and provides an output RF signal to its load circuit 490.

[0032] The N enabled amplifier circuits 450 in SIMO LNA 440 operate independently and have outputs that are separated from each other in order to provide isolation between different transmissions or signals being processed. Each gain circuit 460 outputs a signal current of i_s and a noise current of i_n. The noise figure (NF) of each amplifier circuit 450 is dependent on the signal current and the noise current from the associated gain circuit 460. Amplifier circuits 450 typically have worse noise figure when operating simultaneously as compare to one amplifier circuit 450 operating alone due to degradation of input matching or noise coupling between different amplifier circuits.

[0033] In an aspect of the present disclosure, a SIMO LNA with noise splitting may be used to support simultaneous reception of multiple transmissions or signals. Noise splitting refers to "splitting" of noise among multiple outputs such that each output observes less noise and can achieve a better/lower noise figure.

[0034] **FIG. 5** shows a block diagram of an exemplary design of a SIMO LNA 540 with noise splitting at current buffer output. SIMO LNA 540 may be used for one or more LNAs 340 in FIG. 3. SIMO LNA 540 includes multiple (M) amplifier circuits 550a to 550m coupled to M load circuits 590a to 590m, respectively. Each amplifier circuit 550 includes a gain circuit 560 coupled to a current buffer 570. Each amplifier circuit 550

may be enabled by turning on its current buffer 570 via a respective Venb control signal.

[0035] In the exemplary design shown in FIG. 5, SIMO LNA 540 further includes interconnection circuits 580 coupled between the outputs of amplifier circuits 550. Each interconnection circuit 580 may be implemented with a switch 582 (as shown in FIG. 5) or with some other circuit. Each switch 582 may be (i) opened to isolate the two amplifier circuits 550 coupled to the switch or (ii) closed to connect the outputs of the two amplifier circuits 550 and sum the output currents from these amplifier circuits.

[0036] In general, any number of amplifier circuits 550 and any one of amplifier circuits 550 may be enabled at any given moment. Furthermore, any number of switches 582 and any one of switches 582 may be closed at any given moment. A given amplifier circuit 550 may drive its load circuit 590 by itself. Alternatively, multiple amplifier circuits 550 may have their outputs coupled together via their closed switches 582 and may collectively drive their load circuits 590. The noise figures of amplifier circuits 550 having their outputs coupled together may be improved through noise splitting.

[0037] If all switches 582 are opened, then each amplifier circuit 550 may drive only its load circuit 590. The output current provided by each amplifier circuit 550 to its load circuit 590 may be expressed as:

$$i_m = i_{s,m} + i_{n,m} \qquad \text{Eq (1)}$$

where $i_{s,m}$ is a signal current from the m-th amplifier circuit 550,

$i_{n,m}$ is a noise current from the m-th amplifier circuit 550, and

i_m is an output current from the m-th amplifier circuit 550.

[0038] The noise power at each load circuit 590 may be expressed as:

$$P_{noise,m} \approx i_{n,m}^2 * R_{load} , \qquad \text{Eq (2)}$$

where R_{load} is an impedance of each load circuit 590, and

$P_{noise,m}$ is the noise power at the m-th load circuit 590 without noise splitting.

[0039] If all switches 582 are closed, then the outputs of all M amplifier circuits 550a to 550m are shorted together at a summing node X. In this case, the total current i_{total} at the summing node may be expressed as:

$$\begin{aligned} i_{total} &= (i_{s,1} + i_{n,1}) + (i_{s,2} + i_{n,2}) + ... + (i_{s,M} + i_{n,M}) \\ &\approx M * i_s + (i_{n,1} + i_{n,2} + ... + i_{n,M}) \end{aligned} \quad \text{Eq (3)}$$

where i_s is an average signal current from each amplifier circuit 550, and

i_{total} is a total current from all M amplifier circuits 550a to 550m.

[0040] The signal currents $i_{s,1}$ to $i_{s,M}$ from the M amplifier circuits 550a to 550m (or more specifically, from M gain circuits 560a to 560m) should be similar since they are generated based on the same input RF signal, which is applied to all M amplifier circuits 550. Hence, the total signal current may be approximately equal to $M * i_s$. The noise currents $i_{n,1}$ to $i_{n,M}$ from the M amplifier circuits 550a to 550m should be uncorrelated. Hence, the total noise current is equal to the sum of the noise currents from the M amplifier circuits 550a to 550m.

[0041] The total current at the summing node may be split and provided to the M load circuits 590a to 590m. The current received by each load circuit 590 may be expressed as:

$$i_{load} = \frac{i_{total}}{M} \approx i_d + \frac{(i_{n,1} + i_{n,2} + ... + i_{n,M})}{M}, \quad \text{Eq (4)}$$

where i_{load} is a load current provided to each load circuit 590.

[0042] The noise currents from the M amplifier circuits 550a to 550m should be uncorrelated and may add constructively or destructively. Hence, the noise power at each load circuit 590 may be expressed as:

$$P_{noise} \approx \frac{i_n^2 * R_{load}}{M}, \quad \text{Eq (5)}$$

where i_n is an average noise current from each amplifier circuit 570, and

P_{noise} is the noise power at each load circuit 590 with noise splitting.

[0043] As shown in equations (2) and (5), noise splitting may reduce the noise power at each load circuit 590 by a factor of M, which corresponds to the number of amplifier circuits 550 having their outputs shorted together. The reduction in noise power is due to the noise currents from the M amplifier circuits 550a to 550m being uncorrelated. The signal power at each load circuit 590 may be approximately the same regardless of whether or not the outputs of amplifier circuits 550 are shorted together. The constant signal power with or without noise splitting is due to the signal currents from the M amplifier circuits 550a to 550m being similar or highly correlated. The noise figure at each load circuit 590 may be improved with noise splitting since the signal power is approximately the same whereas the noise power is reduced by a factor of M with noise splitting.

[0044] SIMO LNA 540 with noise splitting at current buffer output may be implemented with various circuit architectures. Some exemplary designs of SIMO LNA 540 are described below. SIMO LNA 540 may also be implemented with transistors of various types. Some exemplary designs of SIMO LNA 540 implemented with N-channel metal oxide semiconductor (NMOS) transistors are described below.

[0045] **FIG. 6A** shows a schematic diagram of an exemplary design of a SIMO LNA 640a with separate inductive degeneration and noise splitting at current buffer output. SIMO LNA 640a is one exemplary design of SIMO LNA 540 in FIG. 5. SIMO LNA 640a includes two amplifier circuits 650a and 650b and a switch 682a. Each amplifier circuit 650 includes a gain circuit 660 and a current buffer 670. SIMO LNA 640a receives an input RF signal, which is applied to both amplifier circuits 650a and 650b. The input RF signal may include transmissions on one or two sets of carriers for carrier aggregation, with each set including one or more carriers. Alternatively, the input RF signal may include two transmitted signals (e.g., from two wireless systems) to be received simultaneously.

[0046] In the exemplary design shown in FIG. 6A, each gain circuit 660 includes a gain transistor 664 and a source degeneration inductor 666. Within gain circuit 660a, gain transistor 664a has its gate receiving the input RF signal, its source coupled to one end of inductor 666a, and its drain forming an output of gain circuit 660a. The other end of

inductor 666a is coupled to circuit ground. In the exemplary design shown in FIG. 6A, each current buffer 670 includes a cascode transistor 674. Within current buffer 670a, cascode transistor 674a has its source forming an input of current buffer 670a and being coupled to the drain of gain transistor 664a, its gate receiving a Venb1 control signal, and its drain forming an output of current buffer 670a and being coupled to a load circuit 690a. Amplifier circuit 650b includes gain transistor 664b, source degeneration inductor 666b, and cascode transistor 674b, which are coupled in similar manner as gain transistor 664a, inductor 666a, and cascode transistor 674a in amplifier circuit 650a. Gain transistors 664 and cascode transistors 674 may be implemented with NMOS transistors, as shown in FIG. 6A, or with transistors of other types.

[0047] In the exemplary design shown in FIG. 6A, switch 682a includes NMOS transistors 684a, 684b and 686. NMOS transistor 684a has its drain coupled to node A, its gate receiving a Sw control signal, and its source coupled to the drain of cascode transistor 674a, which is the output of current buffer 670a. NMOS transistor 684b has its drain coupled to node A, its gate receiving the Sw control signal, and its source coupled to the drain of cascode transistor 674b, which is the output of current buffer 670b. NMOS transistor 686 has its drain coupled to node A, its gate receiving a $\overline{Sw}$ control signal, and its source coupled to circuit ground. The $\overline{Sw}$ signal is complementary to the Sw signal. Switch 682a does not need to have a low resistance when it is closed. In particular, the on resistance of switch 682a should be low compared to the impedance of load circuit 690. Switch 682a may be closed by (i) turning on NMOS transistors 684a and 684b with a high voltage on the Sw signal and (ii) turning off NMOS transistor 686 with a low voltage on the $\overline{Sw}$ signal. Conversely, switch 682a may be opened by (i) turning off NMOS transistors 684a and 684b with a low voltage on the Sw signal and (ii) turning on NMOS transistor 686 with a high voltage on the $\overline{Sw}$ signal.

[0048] Amplifier circuits 650a and 650b may also be implemented in other manners. In another exemplary design, an amplifier circuit may include a gain transistor having its source coupled directly to circuit ground (instead of to a source degeneration inductor). In yet another exemplary design, an amplifier circuit may include two gain transistors coupled in parallel and having their gates receiving the input RF signal. A first gain transistor may have its source coupled to a source degeneration inductor, as shown in FIG. 6A. A second gain transistor may have its source coupled directly to circuit

ground. Either the first or second gain transistor may be selected depending on the received power of the input RF signal.

[0049] In the exemplary design shown in FIG. 6A, each load circuit 690 includes a transformer 692 comprising a primary coil 694 and a secondary coil 696. A coil may also be referred to as an inductor coil, a winding, a conductor, etc. Within load circuit 690a, a transformer 692a includes (i) a primary coil 694a coupled between the output of amplifier circuit 650a and a power supply (VDD) and (ii) a secondary coil 696a providing a first differential amplified RF signal to a first downconverter (not shown in FIG. 6A). Load circuit 690b includes a transformer 692b having (i) a primary coil 694b coupled between the output of amplifier circuit 650b and the VDD supply and (ii) a secondary coil 696b providing a second differential amplified RF signal to a second downconverter (not shown in FIG. 6A). Each downconverter may include two mixers to perform quadrature downconversion of an amplified RF signal from RF to baseband or an intermediate frequency.

[0050] Load circuits 690 may also be implemented in other manners. In another exemplary design, a load circuit may include an inductor and possibly a capacitor coupled between the output of an amplifier circuit and the VDD supply. In yet another exemplary design, a load circuit may include a P-channel metal oxide semiconductor (PMOS) transistor having its source coupled to the VDD supply and its drain coupled to the drain of a cascode transistor 674. The PMOS transistor may provide an active load for cascode transistor 674.

[0051] For simplicity, FIG. 6A shows SIMO LNA 640a including two amplifier circuits 650a and 650b, which are coupled to two load circuits 690a and 690b. SIMO LNA 640a may include more than two amplifier circuits 650 coupled to more than two load circuits 690.

[0052] SIMO LNA 640a may operate in a single-output mode or a multi-output mode. In the single-output mode, SIMO LNA 640a receives the input RF signal and provides one output RF signal to one load circuit 690. The single-output mode may be used to receive (i) a transmission on one carrier without carrier aggregation, or (ii) transmissions on one set of carriers among transmissions on multiple sets of carriers in different bands for inter-band CA, or (iii) a transmitted signal from one wireless system. In the multi-output mode, SIMO LNA 640a receives the input RF signal and provides two output RF signals to two load circuits 690. The multi-output mode may be used to

receive (i) transmissions on two sets of carriers for intra-band CA or (ii) two transmitted signals from two wireless systems.

[0053] **FIG. 6B** shows operation of SIMO LNA 640a in the single-output mode with RFout1 enabled. In this case, cascode transistor 674a is turned on and cascode transistor 674b is turned off. Furthermore, switch 682a is opened by turning off transistors 684a and 684b and turning on transistor 686. Amplifier circuit 650a amplifies the input RF signal and provides a first output RF signal (RFout1). Amplifier circuit 650a is isolated from amplifier circuit 650b via the opened switch 682a.

[0054] **FIG. 6C** shows operation of SIMO LNA 640a in the single-output mode with RFout2 enabled. In this case, cascode transistor 674b is turned on, cascode transistor 674a is turned off, and switch 682a is opened. Amplifier circuit 650b amplifies the input RF signal and provides a second output RF signal (RFout2). Amplifier circuit 650b is isolated from amplifier circuit 650a via the opened switch 682a.

[0055] **FIG. 6D** shows operation of SIMO LNA 640a in the multi-output mode. In this case, cascode transistors 674a and 674b are both turned on. Furthermore, switch 682a is closed by turning on transistors 684a and 684b and turning off transistor 686. Amplifier circuits 650a and 650b amplify the input RF signal, and their output currents are summed. Approximately half of the total current is provided as the RFout1 signal. The remaining current is provided as the RFout2 signal.

[0056] **FIG. 7A** shows a schematic diagram of an exemplary design of a SIMO LNA 640b with separate inductive degeneration and noise splitting at current buffer output. SIMO LNA 640b is another exemplary design of SIMO LNA 540 in FIG. 5. SIMO LNA 640b includes two amplifier circuits 650a and 650b and a switch 682b. Each amplifier circuit 650 includes (i) gain circuit 660 comprising gain transistor 664 and source degeneration inductor 666 and (ii) current buffer 670 comprising cascode transistor 674. Switch 682b includes an NMOS transistor 688 having its source coupled to the output of amplifier circuit 650a, its gate receiving a Sw control signal, and its drain coupled to the output of amplifier circuit 650b. A MOS transistor (e.g., NMOS transistor 688) may be implemented with a symmetric structure, and the source and drain of the MOS transistor may be interchangeable. SIMO LNA 640b may operate in the single-output mode or the multi-output mode, as described above for FIGS. 6B to 6D.

[0057] FIGS. 6A and 7A show two exemplary designs of a switch that may be used to short the outputs of two amplifier circuits. A switch may also be implemented in other

manners. In another exemplary design, a capacitor and/or a resistor may be coupled in series with one or more MOS transistors, and the series combination may be coupled between the outputs of two amplifier circuits. The capacitor and/or resistor may improve isolation with a tradeoff in noise figure.

[0058] **FIG. 7B** shows a schematic diagram of an exemplary design of a SIMO LNA 640c with shared inductive degeneration and noise splitting at current buffer output. SIMO LNA 640c is yet another exemplary design of SIMO LNA 540 in FIG. 5. SIMO LNA 640c includes two amplifier circuits 652a and 652b and switch 682a. Each amplifier circuit 652 includes (i) a gain circuit 662 comprising gain transistor 664 and (ii) current buffer 670 comprising cascode transistor 674. Gain transistors 664a and 664b in gain circuits 662a and 662b share a source degeneration inductor 666 having one end coupled to the sources of gain transistors 664a and 664b and the other end coupled to circuit ground. SIMO LNA 640c may operate in the single-output mode or the multi-output mode, as described above for FIGS. 6B to 6D.

[0059] **FIG. 7C** shows a schematic diagram of an exemplary design of SIMO LNA 640c with noise splitting at current buffer output and a load circuit 691 with transformer-based signal splitting. SIMO LNA 640c includes two amplifier circuits 652a and 652b sharing source degeneration inductor 666 as well as switch 682a, which are coupled as described in FIG. 7B. Load circuit 691 is coupled to amplifier circuits 652a and 652b. In the exemplary design shown in FIG. 7C, load circuit 691 comprises a transformer having a primary coil 693 and two secondary coils 695a and 695b. Primary coil 693 has one end coupled to the output of amplifier circuit 652a, the other end coupled to the output of amplifier circuit 652b, and a center tap coupled to the VDD supply. Secondary coils 695a and 695b are magnetically coupled to primary coil 693. Secondary coil 695a provides a first differential amplified RF signal to a first downconverter. Secondary coil 695b provides a second differential amplified RF signal to a second downconverter. In an exemplary design, secondary coils 695a and 695b may be symmetric with respect to each other.

[0060] **FIG. 8** shows a block diagram of an exemplary design of a SIMO LNA 840 with noise splitting at gain circuit output. SIMO LNA 840 may be used for one or more LNAs 340 in FIG. 3. SIMO LNA 840 includes multiple (M) amplifier circuits 850a to 850m, which are coupled to M load circuits 890a to 890m, respectively. Each amplifier circuit 850 includes a gain circuit 860 coupled to a current buffer 870. Each amplifier

circuit 850 may be enabled by turning on its current buffer 870 via a respective Venb control signal.

[0061] In the exemplary design shown in FIG. 8, SIMO LNA 840 further includes interconnection circuits 880 between the outputs of gain circuits 860. Interconnection circuits 880 allow the output currents from all enabled gain circuits 860 to be summed together. The total current from all enabled gain circuits 860 may then be split among current buffers 870 of all enabled amplifier circuits 850. Interconnection circuits 880 may be implemented in various manners as described below.

[0062] SIMO LNA 840 with noise splitting at gain circuit output may be implemented with various circuit architectures and various types of transistors. Some exemplary designs of SIMO LNA 840 implemented with NMOS transistors are described below.

[0063] **FIG. 9A** shows a schematic diagram of an exemplary design of a SIMO LNA 940a with separate inductive degeneration and noise splitting at gain circuit output. SIMO LNA 940a is one exemplary design of SIMO LNA 840 in FIG. 8. SIMO LNA 940a includes two amplifier circuits 950a and 950b and an interconnection circuit 980a, which is implemented with an AC coupling capacitor 982. Each amplifier circuit 950 includes (i) a gain circuit 960 comprising a gain transistor 964 and a source degeneration inductor 966 and (ii) a current buffer 970 comprising a cascode transistor 974. Capacitor 982 is coupled between the outputs of gain circuits 960a and 960b and acts to electrically short the outputs of gain circuits 960a and 960b. Since current buffers 970a and 970b can provide isolation, the outputs of gain circuits 960 may be effectively shorted together via capacitor 982 without the need to use switches. SIMO LNA 940a receives an input RF signal, which is applied to both amplifier circuits 950a and 950b. Amplifier circuits 950a and 950b provide two output RF signals RFout1 and RFout2, respectively.

[0064] FIG. 9A shows an exemplary design in which interconnection circuit 980a is implemented with capacitor 982. Capacitor 982 should be sufficiently large so that its impedance is small in comparison to the transconductance (or $1/g_m$) of cascode transistors 974. An interconnection circuit may also be implemented in other manners with other circuits.

[0065] SIMO LNA 940a may operate in a single-output mode or a multi-output mode. In the single-output mode, SIMO LNA 940a receives the input RF signal and provides one output RF signal, which may be either RFout1 or RFout2. In the multi-output

mode, SIMO LNA 940a receives the input RF signal and provides two output RF signals RFout1 and RFout2.

[0066] **FIG. 9B** shows a schematic diagram of an exemplary design of a SIMO LNA 940b with shared inductive degeneration and noise splitting at gain circuit output. SIMO LNA 940b is another exemplary design of SIMO LNA 840 in FIG. 8. SIMO LNA 940b includes two amplifier circuits 952a and 952b and interconnection circuit 980a. Each amplifier circuit 952 includes (i) a gain circuit 962 comprising gain transistor 964 and (ii) a current buffer 970 comprising cascode transistor 974. Gain transistors 964a and 964b in gain circuits 962a and 962b share a source degeneration inductor 966 having one end coupled to the sources of gain transistors 964a and 964b and the other end coupled to circuit ground. SIMO LNA 940b may operate in the single-output mode or the multi-output mode.

[0067] **FIG. 9C** shows a schematic diagram of an exemplary design of a SIMO LNA 940c with shared inductive degeneration and noise splitting at gain circuit output. SIMO LNA 940c is yet another exemplary design of SIMO LNA 840 in FIG. 8. SIMO LNA 940c includes two amplifier circuits 952a and 952b, source degeneration inductor 966, and an interconnection circuit 980b. Interconnection circuit 980b includes two cross-coupled cascode transistors 984a and 984b. Cascode transistor 984a has its source coupled to the drain of gain transistor 964a, its gate receiving a Venb12 control signal, and its drain coupled to the output of amplifier circuit 952b. Cascode transistor 984b has its source coupled to the drain of gain transistor 964b, its gate receiving a Venb21 control signal, and its drain coupled to the output of amplifier circuit 952a.

[0068] SIMO LNA 940c may operate in the single-output mode or the multi-output mode. In the single-output mode with RFout1 enabled, amplifier circuit 952a may be enabled, amplifier circuit 952b may be disabled, NMOS transistors 984a and 984b may be turned off, and amplifier circuit 952a may provide the RFout1 signal. Alternatively, amplifier circuit 952a may be enabled, gain transistor 964b and cascode transistor 984b may be enabled, cascode transistors 974b and 984a may be disabled, and amplifier circuit 952a may provide the RFout1 signal.

[0069] In the single-output mode with RFout2 enabled, amplifier circuit 952b may be enabled, amplifier circuit 952a may be disabled, NMOS transistors 984a and 984b may be turned off, and amplifier circuit 952b may provide the RFout2 signal. Alternatively, amplifier circuit 952b may be enabled, gain transistor 964a and cascode transistor 984a

may be enabled, cascode transistors 974a and 984b may be disabled, and amplifier circuit 952b may provide the RFout2 signal.

[0070] In the multi-output mode, amplifier circuits 952a and 952b may both be enabled, NMOS transistors 984a and 984b may be enabled, and amplifier circuits 952a and 952b may provide the RFout1 and RFout2 signals, respectively. In the multi-output mode, gain circuit 962a may provide half its output current to cascode transistor 974a and the other half of its output current to cascode transistor 984a. Similarly, gain circuit 962b may provide half its output current to cascode transistor 974b and the other half of its output current to cascode transistor 984b. The currents from cascode transistors 974a and 984b may be summed at the output of amplifier circuit 952a. The currents from cascode transistors 974b and 984a may be summed at the output of amplifier circuit 952b. Cascode transistors 984a and 984b effectively short the drains of gain transistors 964a and 964b together while presenting low impedance to gain transistors 964a and 964b. The noise figures of amplifier circuits 952a and 952b may be improved through noise splitting obtained by turning on cascode transistors 984a and 984b and splitting the output currents of gain transistors 964a and 964b in the multi-output mode.

[0071] FIGS. 9A and 9C show two exemplary designs of interconnection circuit 980 between gain circuits 960. An interconnection circuit between gain circuits may also be implemented in other manners. In another exemplary design, an interconnection circuit may be implemented with an NMOS transistor, which may be coupled as shown for NMOS transistor 688 in FIG. 7A. In yet another exemplary design, an interconnection circuit may be implemented with two series NMOS transistors and a shunt NMOS transistor, which may be coupled as shown for series NMOS transistors 684a and 684b and shunt NMOS transistor 686 in FIG. 6A. An interconnection circuit may be implemented in various manners and should have low impedance looking into the interconnection circuit.

[0072] FIGS. 6A to 9C shows several exemplary designs of an LNA comprising a gain transistor and a cascode transistor. In another exemplary design, an LNA may comprise a NMOS transistor and a P-channel metal oxide semiconductor (PMOS) transistor coupled in similar manner as an inverter. In yet another exemplary design, an LNA may comprise a differential pair. An LNA may also be implemented in other manners.

[0073] The SIMO LNAs with noise splitting described herein may be used for various applications. The SIMO LNAs may be used to receive transmissions on multiple carriers (e.g., in the same band) for carrier aggregation. The SIMO LNAs may also be

used to concurrently receive transmitted signals (e.g., in the same band) from multiple wireless systems (e.g., LTE and GSM, EVDO and CDMA 1X, WLAN and Bluetooth, etc.). The SIMO LNAs may also be used to concurrently receive transmissions for different services (e.g., voice and data). The SIMO LNAs may provide a single output RF signal in the single-output mode or multiple output RF signals in the multi-output mode.

[0074] The SIMO LNAs with noise splitting described herein may provide various advantages. First, these SIMO LNAs may have better noise figure due to noise splitting without sacrificing other performance metrics such as linearity. Second, the SIMO LNAs may be implemented with little additional die area and no increase in current consumption. Third, noise splitting may be applied to any circuit with two or more amplifier circuits sharing the same input RF signal.

[0075] In an exemplary design, an apparatus (e.g., a wireless device, an IC, a circuit module, etc.) may include a plurality of amplifier circuits and at least one interconnection circuit. The plurality of amplifier circuits (e.g., amplifier circuits 550a to 550m in FIG. 5 or amplifier circuits 850a to 850m in FIG. 8) may have their inputs coupled together and may receive an input RF signal. The at least one interconnection circuit (e.g., interconnection circuits 580 in FIG. 5 or interconnection circuits 880 in FIG. 8) may short at least two of the plurality of amplifier circuits coupled to the at least one interconnection circuit. Each interconnection circuit may be closed to short the outputs or internal nodes of two amplifier circuits coupled to that interconnection circuit.

[0076] In an exemplary design, the plurality of amplifier circuits may comprise a plurality of gain circuits (e.g., gain circuits 560 in FIG. 5 or gain circuits 860 in FIG. 8) and a plurality of current buffers (e.g., current buffers 570 in FIG. 5 or current buffers 870 in FIG. 7). Each amplifier circuit may include one gain circuit coupled to one current buffer. In an exemplary design, each gain circuit may comprise a gain transistor that receives the input RF signal and provides an amplified signal when the gain circuit is enabled. In an exemplary design, each current buffer may comprise a cascode transistor that receives an amplified signal from an associated gain circuit and provides an output RF signal when the current buffer is enabled.

[0077] In an exemplary design, one of the plurality of amplifier circuits may amplify the input RF signal and provide one output RF signal when this one amplifier circuit is enabled. The remaining amplifier circuits may be disabled. In an exemplary design, the

plurality of amplifier circuits may be enabled to amplify the input RF signal and provide a plurality of output RF signals. Each amplifier circuit may provide an output current comprising a portion of the current from each of the plurality of gain circuits when the plurality of amplifier circuits are enabled.

[0078] In an exemplary design, noise splitting at current buffer output may be implemented, e.g., as shown in FIG. 5. The at least one interconnection circuit may comprise at least one switch (e.g., switches 582 in FIG. 5) coupled between the outputs of the plurality of amplifier circuits. Each switch may be closed to short the outputs of two amplifier circuits coupled to that switch. The at least one interconnection circuit or switch may short the outputs of the plurality of amplifier circuits when the plurality of amplifier circuits are enabled.

[0079] In another exemplary design, noise splitting at gain circuit output may be implemented, e.g., as shown in FIG. 8. In an exemplary design, the at least one interconnection circuit may comprise at least one capacitor (e.g., capacitor 982 in FIG. 9A) coupled between the outputs of the plurality of gain circuits. Each capacitor may short the outputs of two gain circuits coupled to that capacitor. The at least one interconnection circuit may short the outputs of the plurality of gain circuits when the plurality of amplifier circuits are enabled. In another exemplary design, the at least one interconnection circuit may comprise a plurality of cascode transistors (e.g., cascode transistors 984 in FIG. 9C) coupled between the plurality of gain circuits and the plurality of current buffers. Each cascode transistor may be coupled between a gain circuit in one amplifier circuit and a current buffer in another amplifier circuit. The plurality of cascode transistors may be turned on when the plurality of amplifier circuits are enabled.

[0080] In an exemplary design, the plurality of amplifier circuits may comprise first and second amplifier circuits. The first amplifier circuit (e.g., amplifier circuit 650a in FIG. 6A) may comprise a first gain transistor (e.g., gain transistor 664a) and a first cascode transistor (e.g., cascode transistor 674a). The second amplifier circuit (e.g., amplifier circuit 650b) may comprise a second gain transistor (e.g., gain transistor 664a) and a second cascode transistor (e.g., cascode transistor 674a). In an exemplary design, a separate source degeneration inductor may be used for each gain circuit. The first amplifier circuit may comprise a first inductor (e.g., inductor 666a) coupled between the source of the first gain transistor and circuit ground. The second amplifier circuit may comprise a second inductor (e.g., inductor 666b) coupled between the source of the

second gain transistor and circuit ground. In another exemplary design, a shared source degeneration inductor (e.g., inductor 666 in FIG. 7B) may be used for the first and second gain transistors and may be coupled between the sources of these gain transistors and circuit ground.

[0081] In an exemplary design, the at least one interconnection circuit may comprise a switch (e.g., switch 682a in FIG. 6A or switch 682b in FIG. 7A) coupled between the drains of the first and second cascode transistors. The switch may be opened when only the first or second amplifier circuit is enabled and may be closed when both the first and second amplifier circuits are enabled. In an exemplary design, the switch may comprise first, second and third transistors. The first transistor (e.g., NMOS transistor 684a in FIG. 6A) may be coupled between the drain of the first cascode transistor and an intermediate node. The second transistor (e.g., NMOS transistor 684b) may be coupled between the intermediate node and the drain of the second cascode transistor. The third transistor (e.g., NMOS transistor 686) may be coupled between the intermediate node and circuit ground. In another exemplary design, the switch may comprise a transistor (e.g., NMOS transistor 688 in FIG. 7A) coupled between the drains of the first and second cascode transistors. The switch may also be implemented in other manners.

[0082] In another exemplary design, the at least one interconnection circuit may comprise a capacitor (e.g., capacitor 982 in FIG. 9A) coupled between the drains of the first and second gain transistors. The first cascode transistor may be turned on and the second cascode transistor may be turned off when the first amplifier circuit is enabled. The second cascode transistor may be turned on and the first cascode transistor may be turned off when the second amplifier circuit is enabled. The first and second cascode transistors may both be turned on when the first and second amplifier circuits are enabled.

[0083] In yet another exemplary design, the at least one interconnection circuit may comprise third and fourth cascode transistors. The third cascode transistor (e.g., cascode transistor 984a in FIG. 9C) may be coupled between the drain of the first gain transistor and the drain of the second cascode transistor. The fourth cascode transistor (e.g., cascode transistor 984b) may be coupled between the drain of the second gain transistor and the drain of the first cascode transistor. The third and fourth cascode transistors may be turned on when the first and second amplifier circuits are both enabled. Only the first cascode transistor may be turned on, or both the first and fourth cascode transistors may be turned on, when the first amplifier circuit is enabled. Only

the second cascode transistor may be turned on, or both the second and third cascode transistors may be turned on, when the second amplifier circuit is enabled.

[0084] The apparatus may include first and second load circuits coupled to the first and second amplifier circuits, respectively. In an exemplary design, the first load circuit (e.g., load circuit 690a in FIG. 6A) may comprise a first transformer (e.g., transformer 692a) coupled to the first amplifier circuit. The second load circuit (e.g., load circuit 690b) may comprise a second transformer (e.g., transformer 692b) coupled to the second amplifier circuit. The first and second load circuits may also be implemented in other manners.

[0085] **FIG. 10** shows an exemplary design of a process 1000 for performing signal amplification. Process 1000 may be performed by a wireless device or by some other entity. An input RF signal may be applied to a plurality of amplifier circuits, which may have their inputs coupled together (block 1012). At least one of the plurality of amplifier circuits may be enabled to amplify the input RF signal and provide at least one output RF signal (block 1014). The plurality of amplifier circuits may be shorted via at least one interconnection circuit when the plurality of amplifier circuits are enabled in order to perform noise splitting and improve noise figure (block 1016). Each interconnection circuit may short the outputs or internal nodes of two amplifier circuits coupled to that interconnection circuit.

[0086] In an exemplary design of block 1014, the input RF signal may be amplified with a plurality of gain circuits in the plurality of amplifier circuits. The plurality of amplifier circuits may provide output currents. The output current from each amplifier circuit may comprise a portion of the current from each of the plurality of gain circuits.

[0087] The amplifiers (e.g., SIMO LNAs) with noise splitting described herein may be implemented on an IC, an analog IC, an RFIC, a mixed-signal IC, an ASIC, a printed circuit board (PCB), an electronic device, etc. The amplifiers with noise splitting may also be fabricated with various IC process technologies such as complementary metal oxide semiconductor (CMOS), NMOS, PMOS, bipolar junction transistor (BJT), bipolar-CMOS (BiCMOS), silicon germanium (SiGe), gallium arsenide (GaAs), heterojunction bipolar transistors (HBTs), high electron mobility transistors (HEMTs), silicon-on-insulator (SOI), etc.

[0088] An apparatus implementing an amplifier with noise splitting described herein may be a stand-alone device or may be part of a larger device. A device may be (i) a stand-alone IC, (ii) a set of one or more ICs that may include memory ICs for storing

data and/or instructions, (iii) an RFIC such as an RF receiver (RFR) or an RF transmitter/receiver (RTR), (iv) an ASIC such as a mobile station modem (MSM), (v) a module that may be embedded within other devices, (vi) a receiver, cellular phone, wireless device, handset, or mobile unit, (vii) etc.

[0089] In one or more exemplary designs, the functions described may be implemented in hardware, software, firmware, or any combination thereof. If implemented in software, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. Computer-readable media includes both computer storage media and communication media including any medium that facilitates transfer of a computer program from one place to another. A storage media may be any available media that can be accessed by a computer. By way of example, and not limitation, such computer-readable media can comprise RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that can be used to carry or store desired program code in the form of instructions or data structures and that can be accessed by a computer. Also, any connection is properly termed a computer-readable medium. For example, if the software is transmitted from a website, server, or other remote source using a coaxial cable, fiber optic cable, twisted pair, digital subscriber line (DSL), or wireless technologies such as infrared, radio, and microwave, then the coaxial cable, fiber optic cable, twisted pair, DSL, or wireless technologies such as infrared, radio, and microwave are included in the definition of medium. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk and blu-ray disc where *disks* usually reproduce data magnetically, while *discs* reproduce data optically with lasers. Combinations of the above should also be included within the scope of computer-readable media.

[0090] The previous description of the disclosure is provided to enable any person skilled in the art to make or use the disclosure. Various modifications to the disclosure will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other variations without departing from the scope of the disclosure. Thus, the disclosure is not intended to be limited to the examples and designs described herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

[0091] **WHAT IS CLAIMED IS:**

CLAIMS

1. An apparatus comprising:

a plurality of amplifier circuits configured to receive an input radio frequency (RF) signal; and

at least one interconnection circuit configured to short at least two of the plurality of amplifier circuits coupled to the at least one interconnection circuit.

2. The apparatus of claim 1, the plurality of amplifier circuits comprising a plurality of gain circuits and a plurality of current buffers, one gain circuit and one current buffer for each amplifier circuit.

3. The apparatus of claim 2, each amplifier circuit configured to provide an output current comprising a portion of a current from each of the plurality of gain circuits when the plurality of amplifier circuits are enabled to amplify the input RF signal and provide a plurality of output RF signals.

4. The apparatus of claim 1, the at least one interconnection circuit configured to short outputs of the plurality of amplifier circuits when the plurality of amplifier circuits are enabled.

5. The apparatus of claim 2, the at least one interconnection circuit configured to short outputs of the plurality of gain circuits when the plurality of amplifier circuits are enabled.

6. The apparatus of claim 2, the at least one interconnection circuit comprising:

a plurality of cascode transistors coupled between the plurality of gain circuits and the plurality of current buffers, each cascode transistor being coupled between a gain circuit in one amplifier circuit and a current buffer in another amplifier circuit, the plurality of cascode transistors being turned on when the plurality of amplifier circuits are enabled.

7. The apparatus of claim 1, one of the plurality of amplifier circuits configured to amplify the input RF signal and provide an output RF signal when the one amplifier circuit is enabled and remaining ones of the plurality of amplifier circuits are disabled.

8. The apparatus of claim 1, the plurality of amplifier circuits comprising first and second amplifier circuits, the first amplifier circuit comprising a first gain transistor and a first cascode transistor, and the second amplifier circuit comprising a second gain transistor and a second cascode transistor.

9. The apparatus of claim 8, the at least one interconnection circuit comprising a switch coupled between drains of the first and second cascode transistors, the switch being opened when only the first or second amplifier circuit is enabled and being closed when both the first and second amplifier circuits are enabled.

10. The apparatus of claim 9, the switch comprising:

a first transistor coupled between a drain of the first cascode transistor and an intermediate node;

a second transistor coupled between the intermediate node and a drain of the second cascode transistor; and

a third transistor coupled between the intermediate node and circuit ground.

11. The apparatus of claim 9, the switch comprising

a transistor coupled between the drains of the first and second cascode transistors.

12. The apparatus of claim 8, the at least one interconnection circuit comprising a capacitor coupled between drains of the first and second gain transistors, the first cascode transistor being turned on and the second cascode transistor being turned off when the first amplifier circuit is enabled, the second cascode transistor being turned on and the first cascode transistor being turned off when the second amplifier circuit is enabled, and both the first and second cascode transistors being turned on when the first and second amplifier circuits are enabled.

13. The apparatus of claim 8, the at least one interconnection circuit comprising:

a third cascode transistor coupled between a drain of the first gain transistor and a drain of the second cascode transistor; and

a fourth cascode transistor coupled between a drain of the second gain transistor and a drain of the first cascode transistor, the third and fourth cascode transistors being turned on when both the first and second amplifier circuits are enabled.

14. The apparatus of claim 13, only the first cascode transistor being turned on, or both the first and fourth cascode transistors being turned on, when the first amplifier circuit is enabled.

15. The apparatus of claim 8, further comprising:

an inductor coupled between sources of the first and second gain transistors and circuit ground.

16. The apparatus of claim 8, further comprising:

a first load circuit comprising a first transformer coupled to the first amplifier circuit; and

a second load circuit comprising a second transformer coupled to the second amplifier circuit.

17. A method comprising:

applying an input radio frequency (RF) signal to a plurality of amplifier circuits;

enabling at least one of the plurality of amplifier circuits to amplify the input RF signal and provide at least one output RF signal; and

shorting the plurality of amplifier circuits when the plurality of amplifier circuits are enabled.

18. The method of claim 17, further comprising:

amplifying the input RF signal with a plurality of gain circuits in the plurality of amplifier circuits; and

providing output currents from the plurality of amplifier circuits, an output current from each amplifier circuit comprising a portion of a current from each of the plurality of gain circuits.

19. An apparatus comprising:

a plurality of amplifying means configured to receive an input radio frequency (RF) signal; and

at least one interconnection means configured to short at least two of the plurality of amplifying means coupled to the at least one interconnection means.

20. The apparatus of claim 19, the plurality of amplifying means comprising:

a plurality of gain means configured to amplify the input RF signal; and

a plurality of buffer means coupled to the plurality of gain means, each amplifying means configured to provide an output current comprising a portion of a current from each of the plurality of gain means when the plurality of amplifying means are enabled.

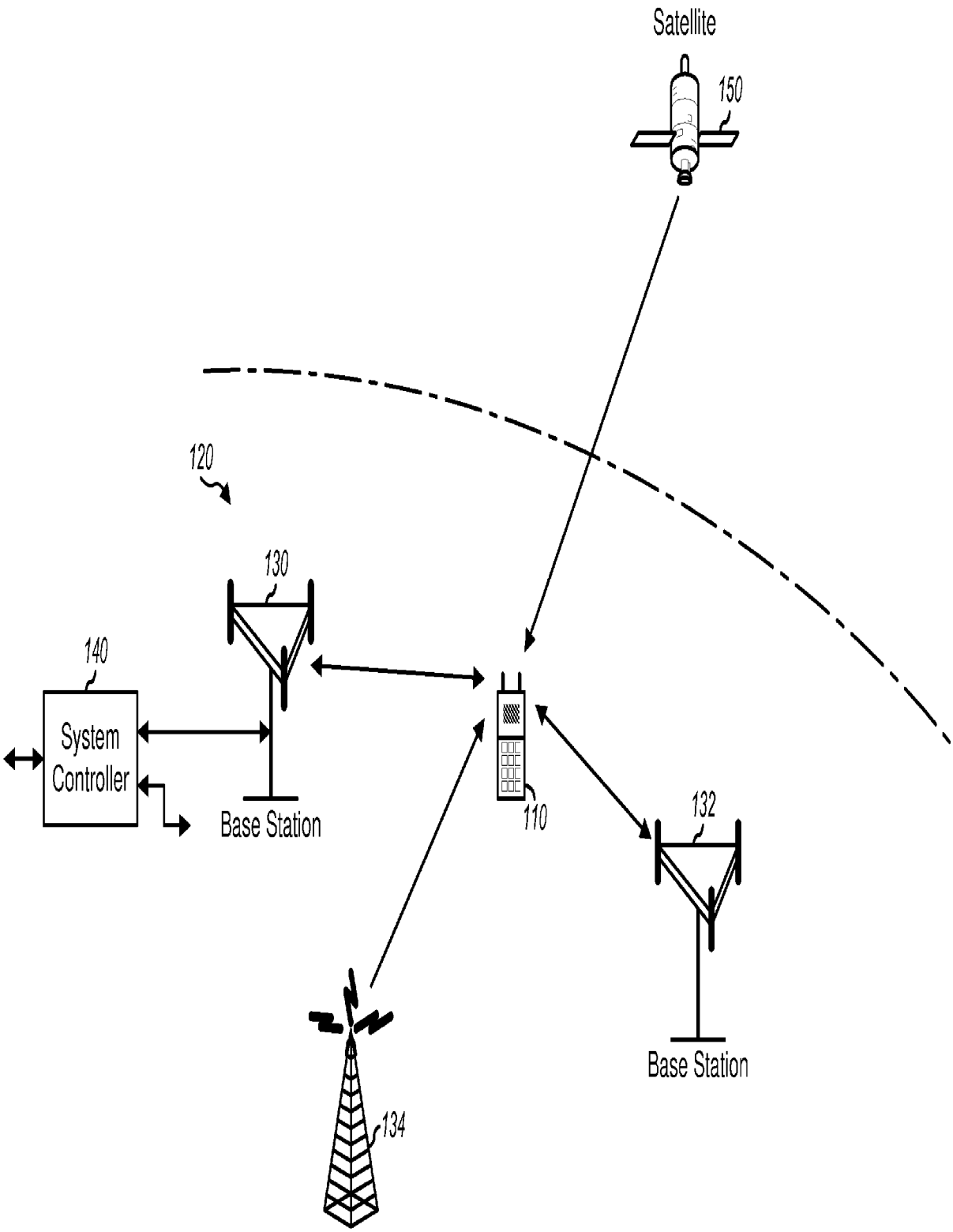
Satellite
150
120
130
140
System Controller
Base Station
110
132
Base Station
134

FIG. 1

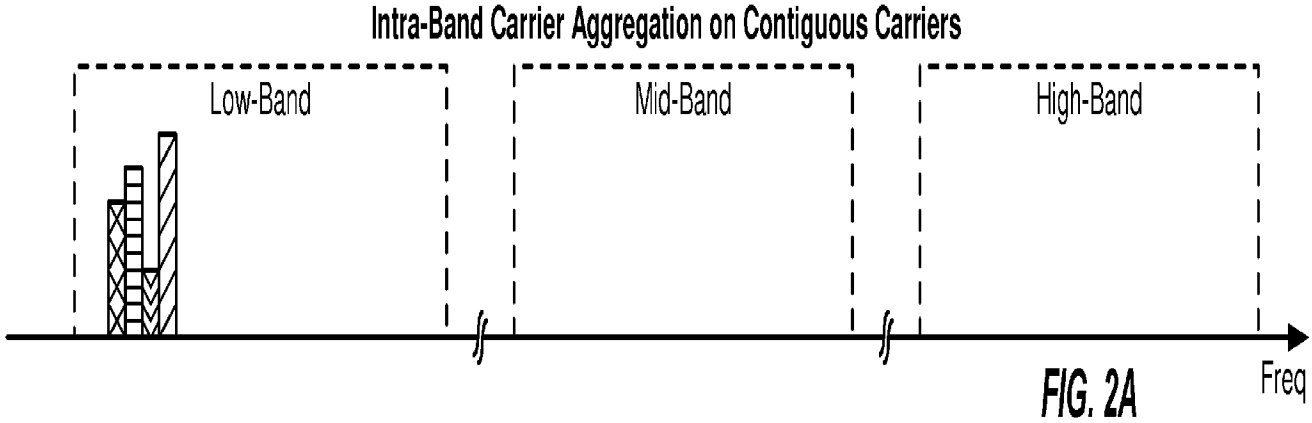

FIG. 2A

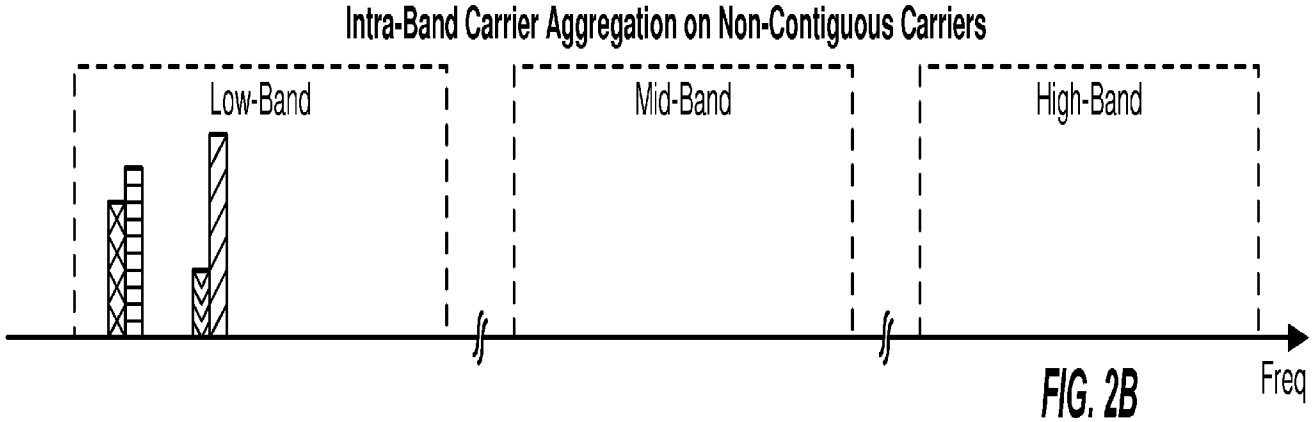

FIG. 2B

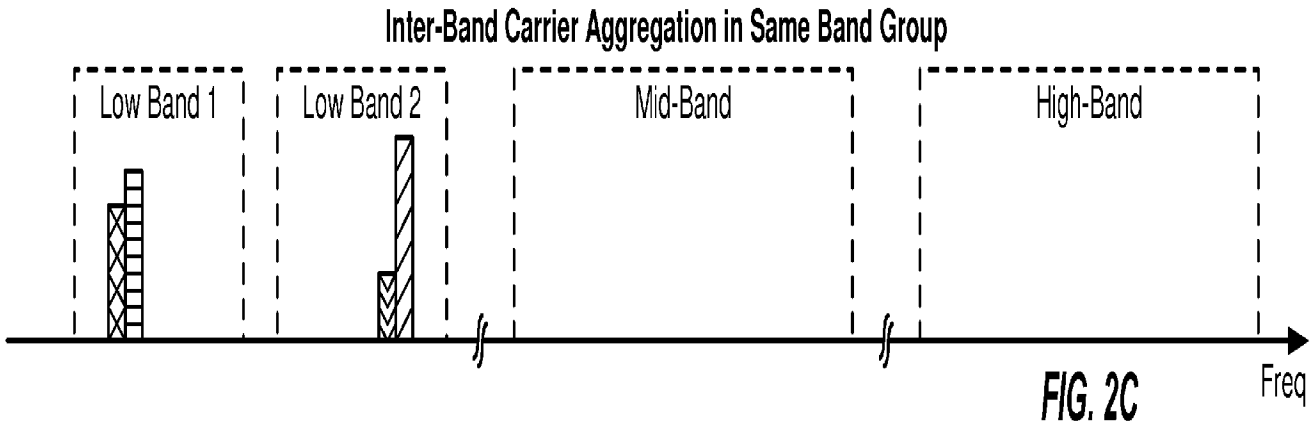

FIG. 2C

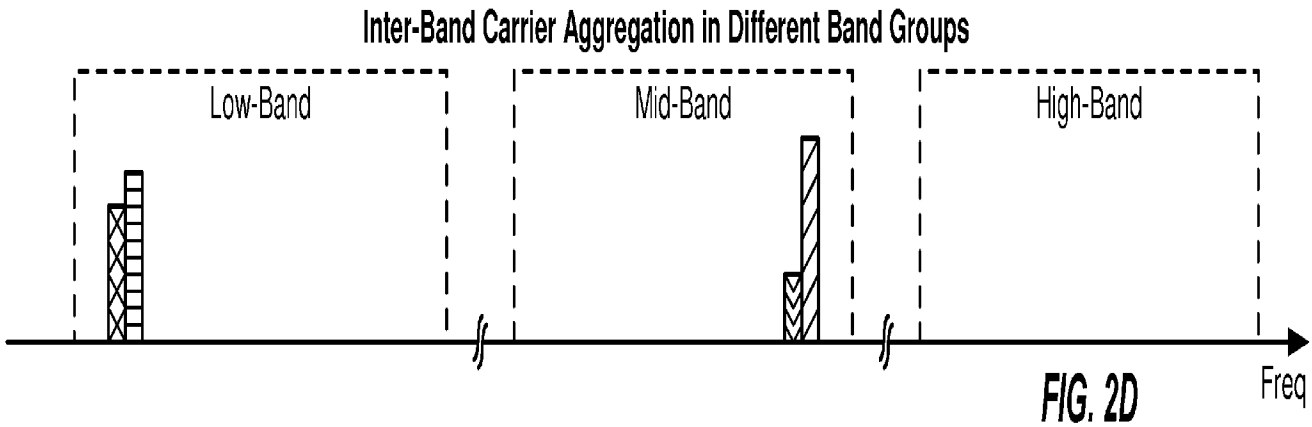

FIG. 2D

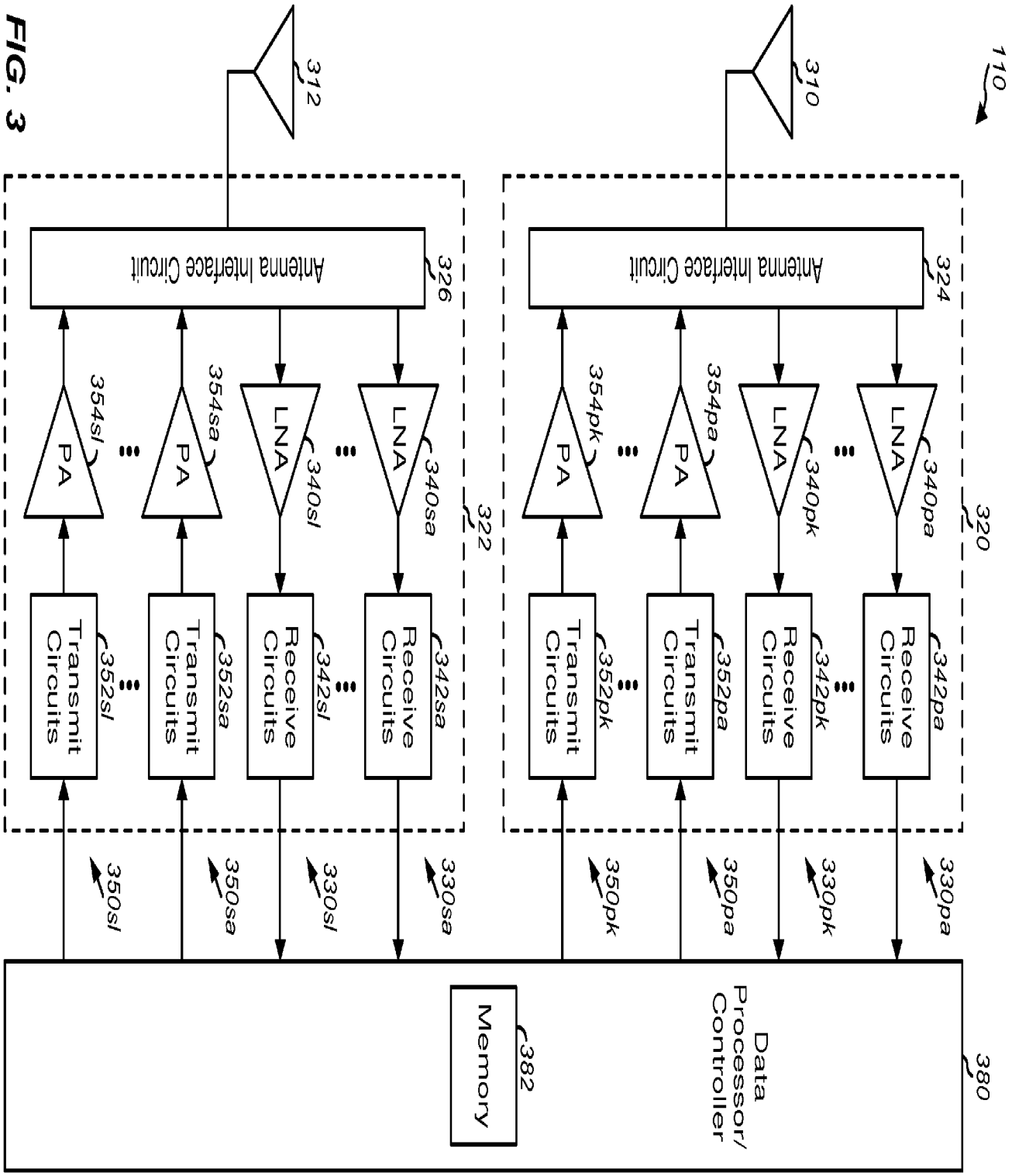
110
310
312
320
322
324
326
Antenna Interface Circuit
Antenna Interface Circuit
LNA
340pa
340pk
340sa
340sl
PA
354pk
354pa
354sa
354sl
Receive Circuits
342pa
342pk
342sa
342sl
Transmit Circuits
352pk
352pa
352sa
352sl
330pa
330pk
330sa
330sl
350pk
350pa
350sa
350sl
Data Processor/ Controller
380
Memory
382

FIG. 3

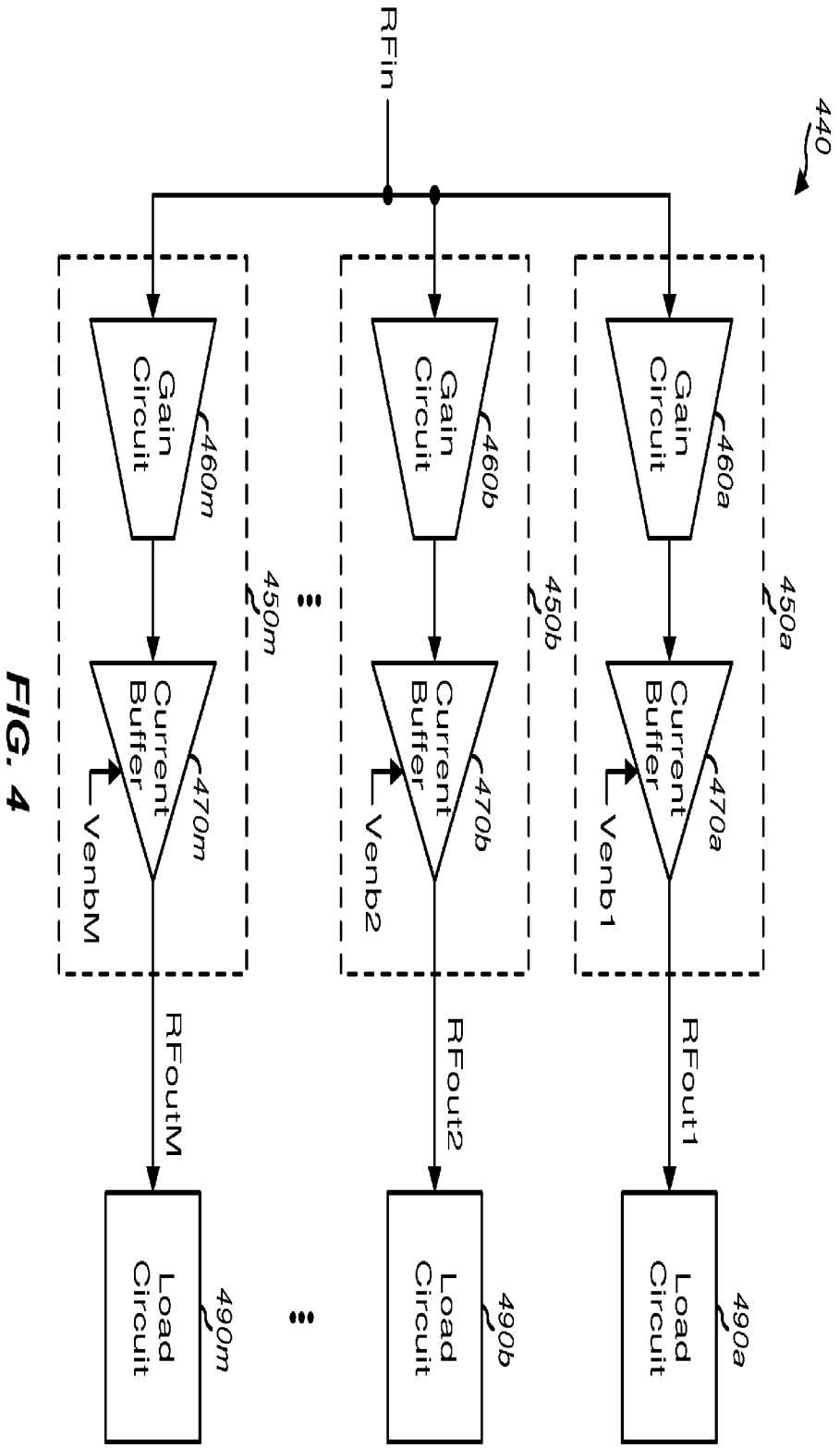
440
RFin
450a
450b
450m
Gain Circuit
460a
460b
460m
Current Buffer
470a
470b
470m
Venb1
Venb2
VenbM
RFout1
RFout2
RFoutM
Load Circuit
490a
490b
490m

FIG. 4

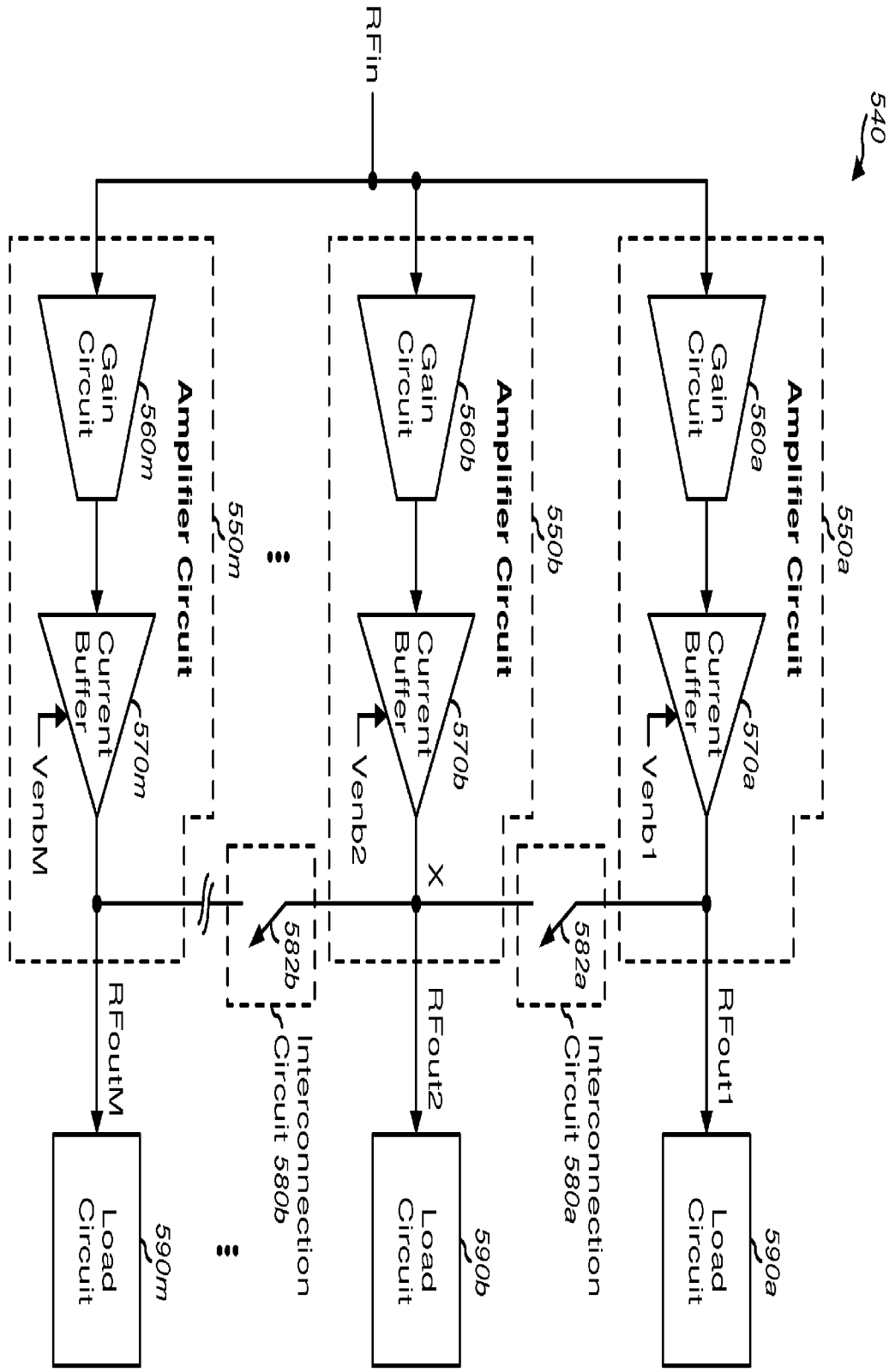
540
RFin
Amplifier Circuit
550a
Gain Circuit
560a
Current Buffer
570a
Venb1
Amplifier Circuit
550b
Gain Circuit
560b
Current Buffer
570b
Venb2
X
Amplifier Circuit
550m
Gain Circuit
560m
Current Buffer
570m
VenbM
582a
582b
Interconnection Circuit 580a
Interconnection Circuit 580b
RFout1
RFout2
RFoutM
Load Circuit
590a
Load Circuit
590b
Load Circuit
590m

FIG. 5

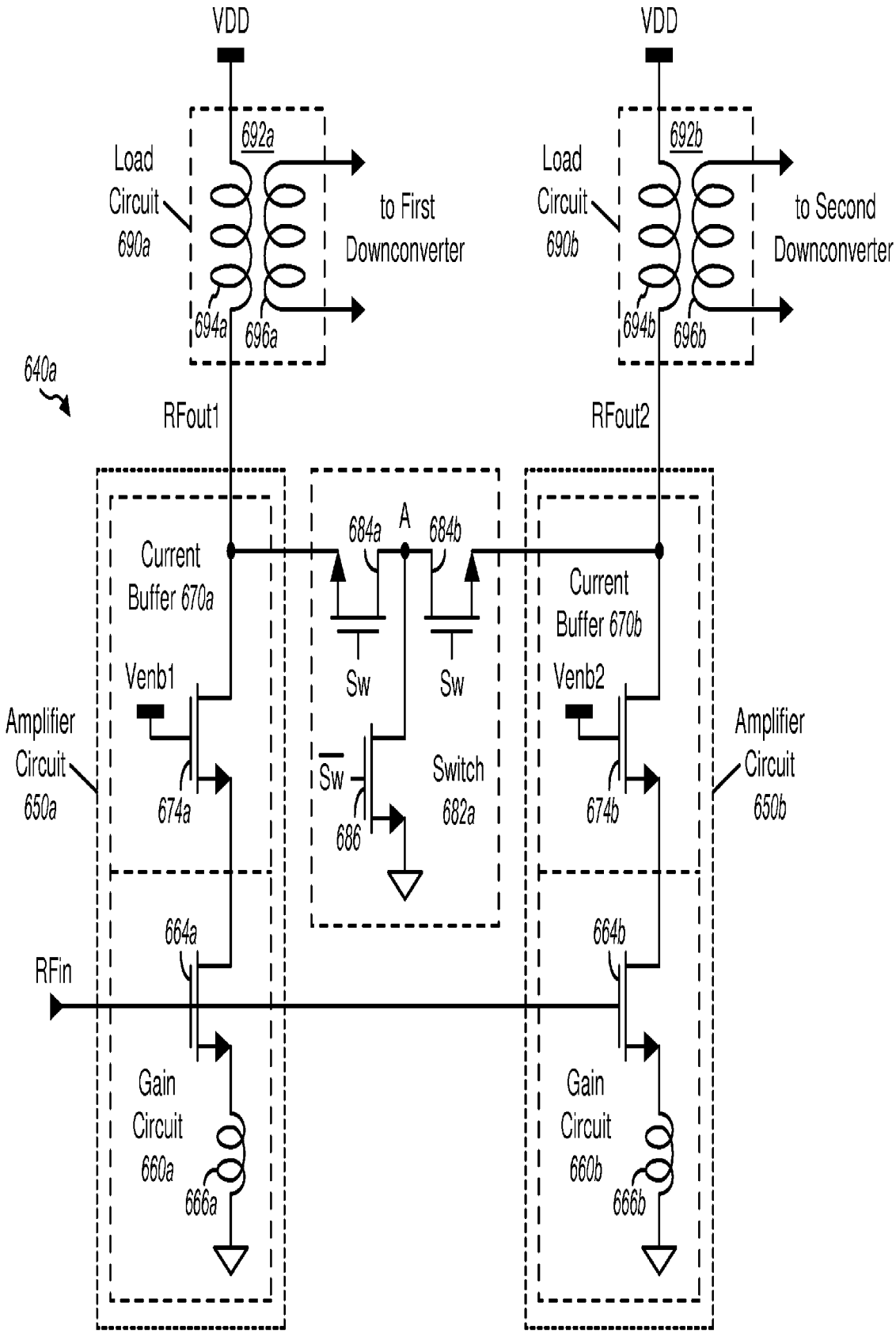
VDD
VDD
692a
692b
Load Circuit 690a
Load Circuit 690b
to First Downconverter
to Second Downconverter
694a
696a
694b
696b
640a
RFout1
RFout2
684a
A
684b
Current Buffer 670a
Current Buffer 670b
Venb1
Venb2
Sw
Sw
Sw
Switch 682a
686
Amplifier Circuit 650a
Amplifier Circuit 650b
674a
674b
664a
664b
RFin
Gain Circuit 660a
Gain Circuit 660b
666a
666b

FIG. 6A

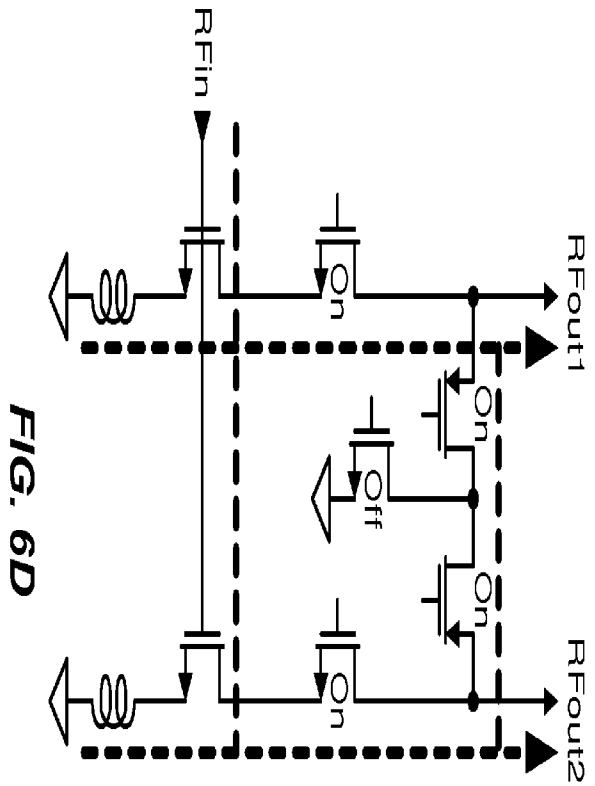

FIG. 6D

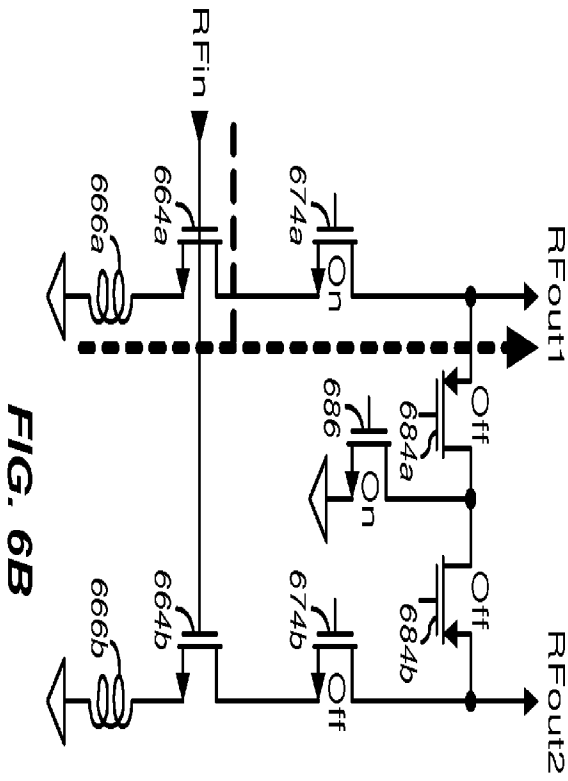

FIG. 6B

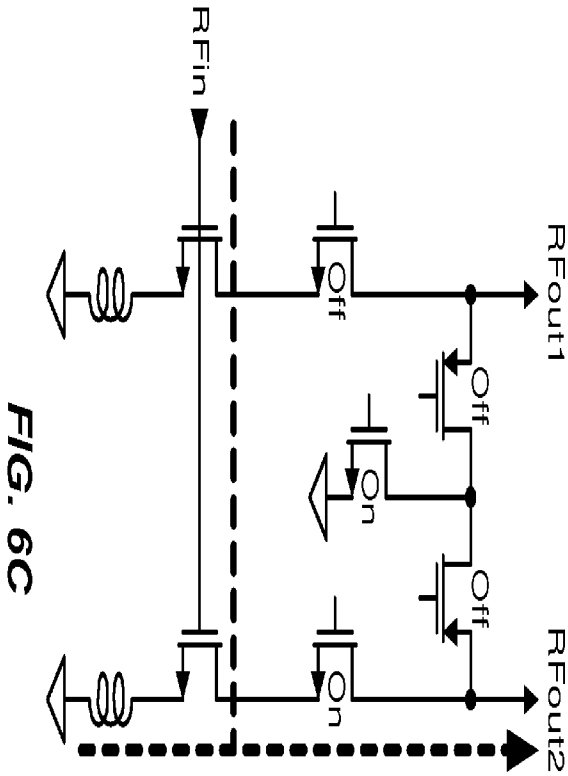

FIG. 6C

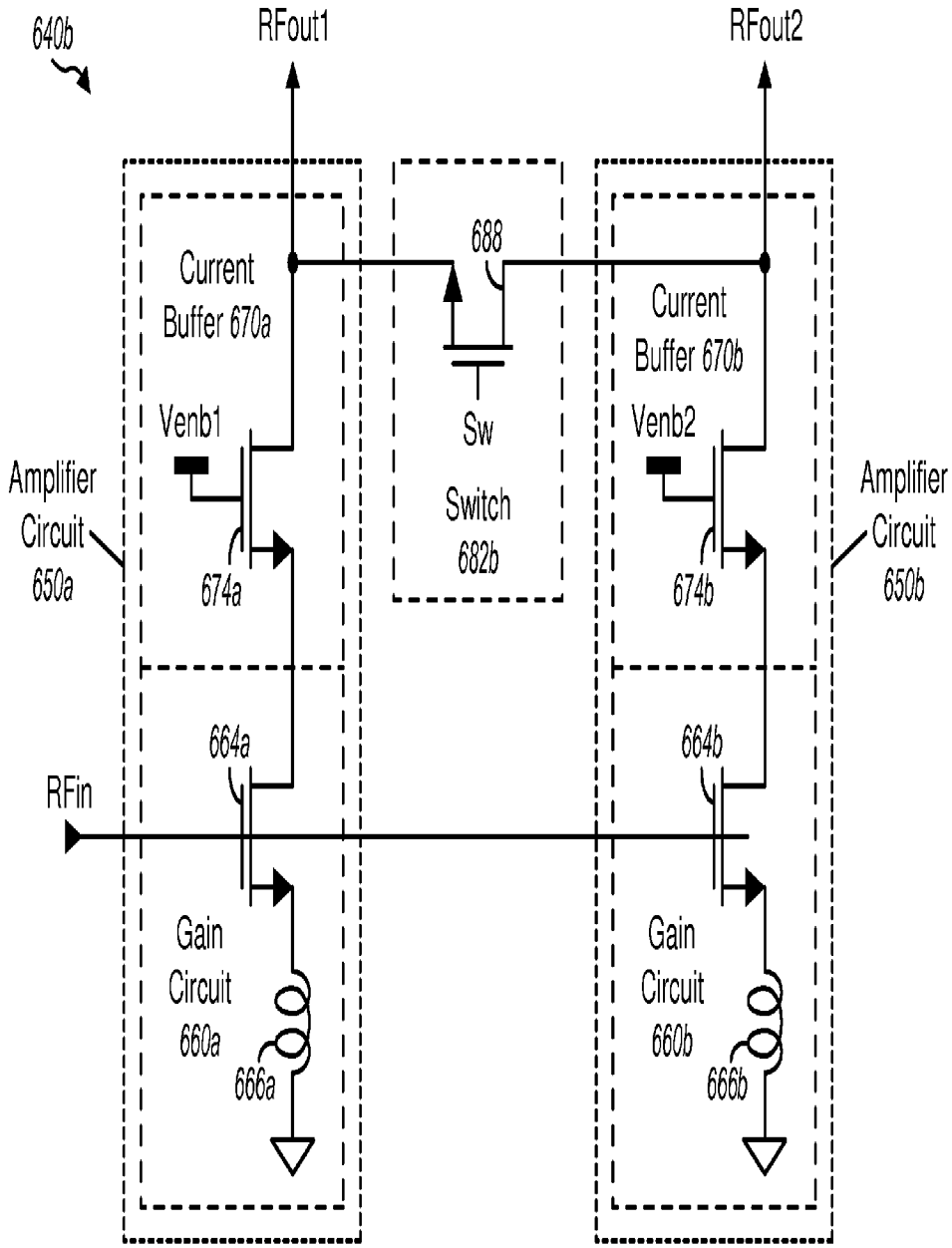
640b
RFout1
RFout2
688
Current
Buffer 670a
Current
Buffer 670b
Venb1
Venb2
Sw
Switch
682b
Amplifier
Circuit
650a
Amplifier
Circuit
650b
674a
674b
664a
664b
RFin
Gain
Circuit
660a
Gain
Circuit
660b
666a
666b

FIG. 7A

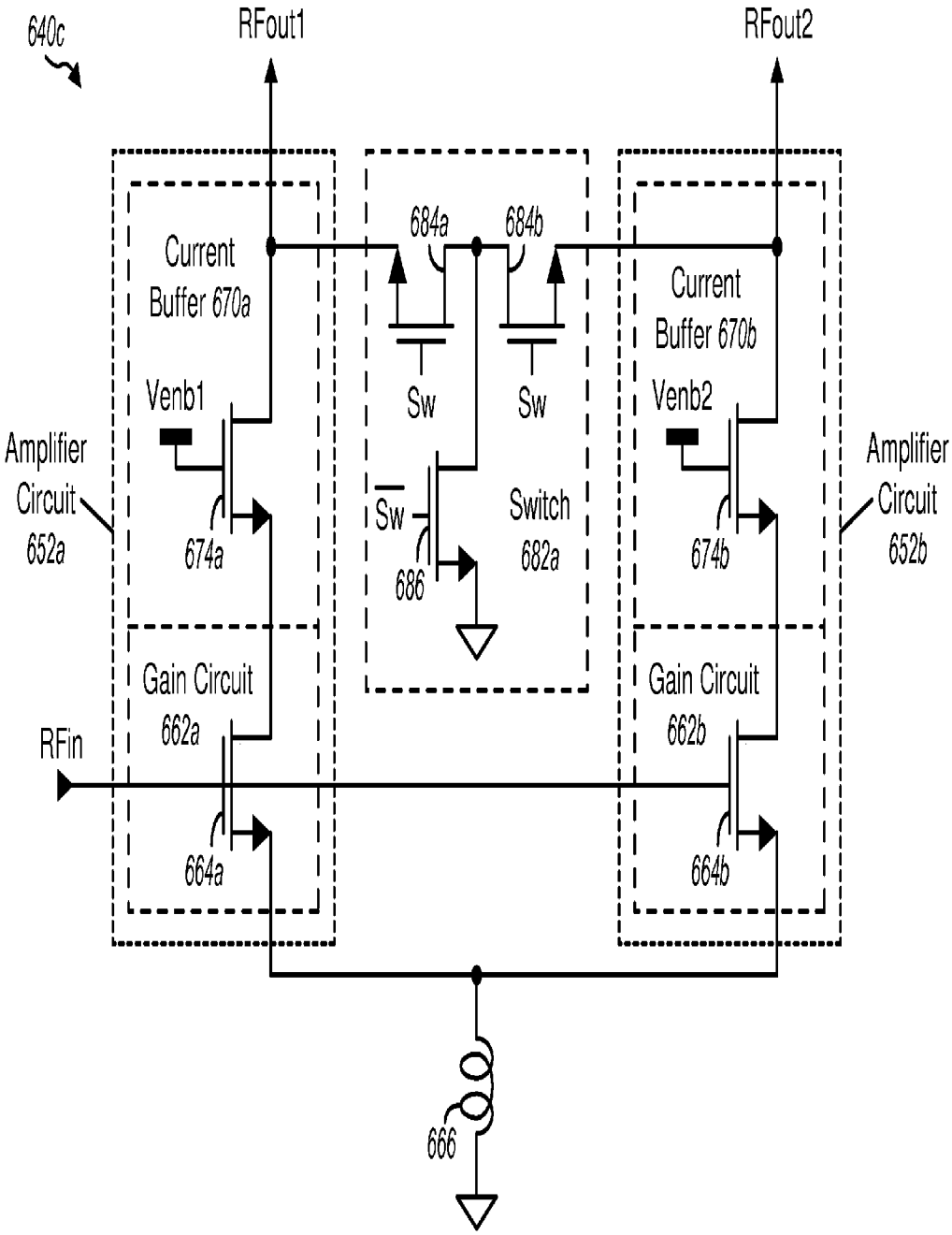
640c
RFout1
RFout2
684a
684b
Current
Buffer 670a
Current
Buffer 670b
Venb1
Venb2
Sw
Sw
Amplifier
Circuit
652a
Sw
Switch
682a
686
674a
674b
Amplifier
Circuit
652b
Gain Circuit
662a
Gain Circuit
662b
RFin
664a
664b
666

FIG. 7B

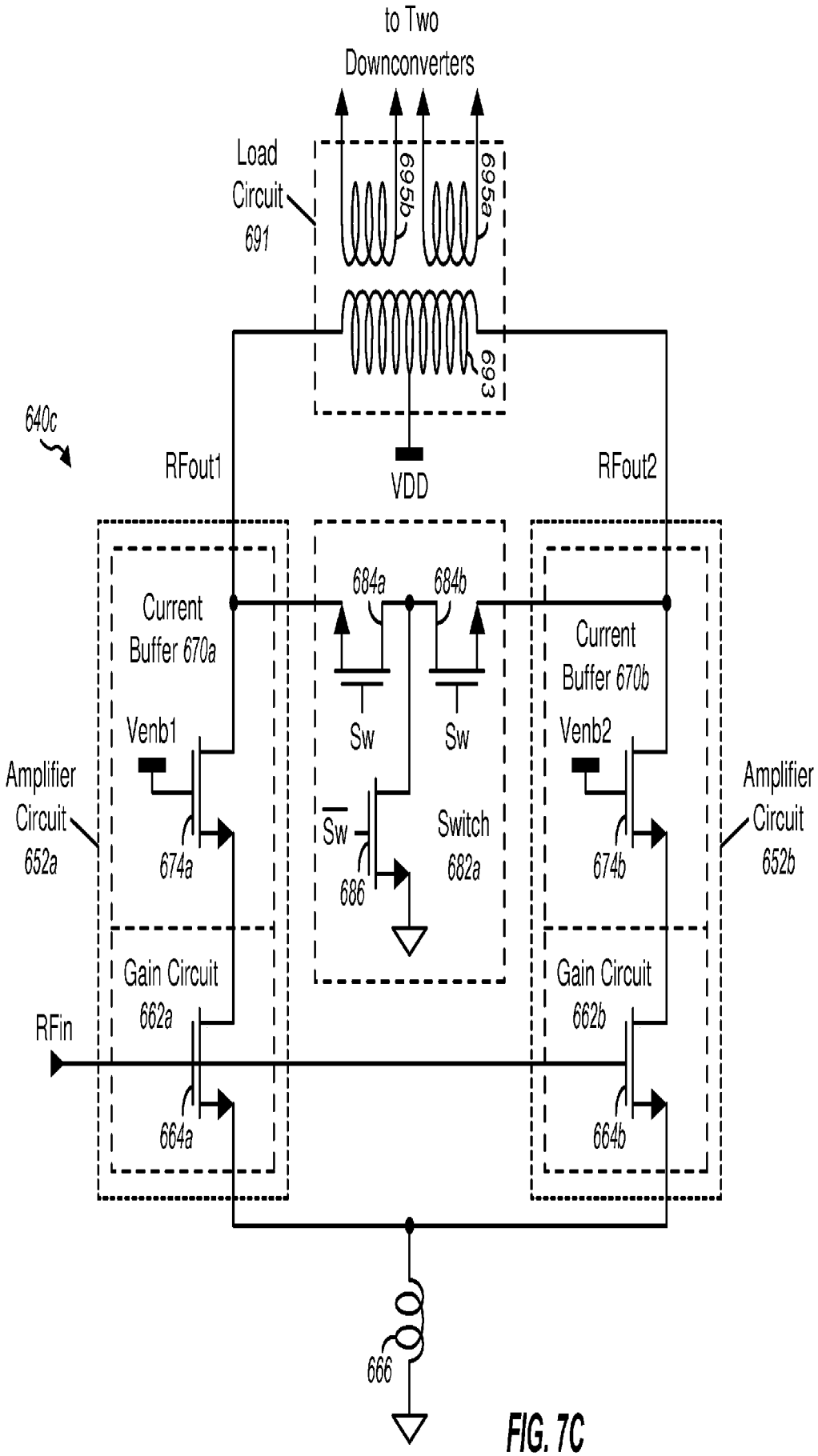
to Two
Downconverters
Load
Circuit
691
695b
695a
693
640c
RFout1
VDD
RFout2
684a
684b
Current
Buffer 670a
Current
Buffer 670b
Venb1
Venb2
Sw
Sw
Amplifier
Circuit
652a
Amplifier
Circuit
652b
Sw
Switch
682a
686
674a
674b
Gain Circuit
662a
Gain Circuit
662b
RFin
664a
664b
666

FIG. 7C

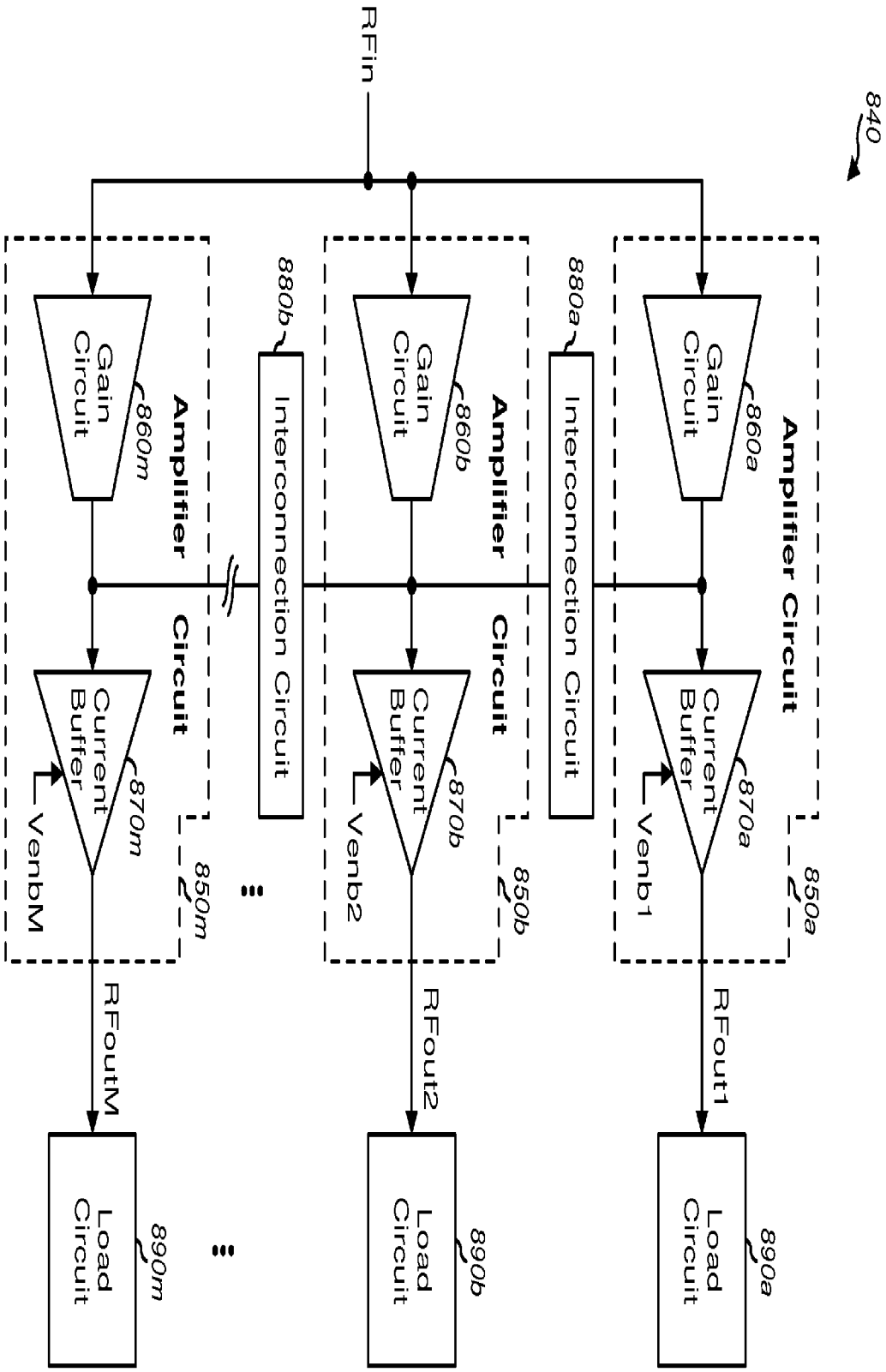
840
RFin
Amplifier Circuit
850a
Gain Circuit
860a
Current Buffer
870a
Venb1
RFout1
Load Circuit
890a
880a
Interconnection Circuit
Amplifier Circuit
850b
Gain Circuit
860b
Current Buffer
870b
Venb2
RFout2
Load Circuit
890b
880b
Interconnection Circuit
Amplifier Circuit
850m
Gain Circuit
860m
Current Buffer
870m
VenbM
RFoutM
Load Circuit
890m

FIG. 8

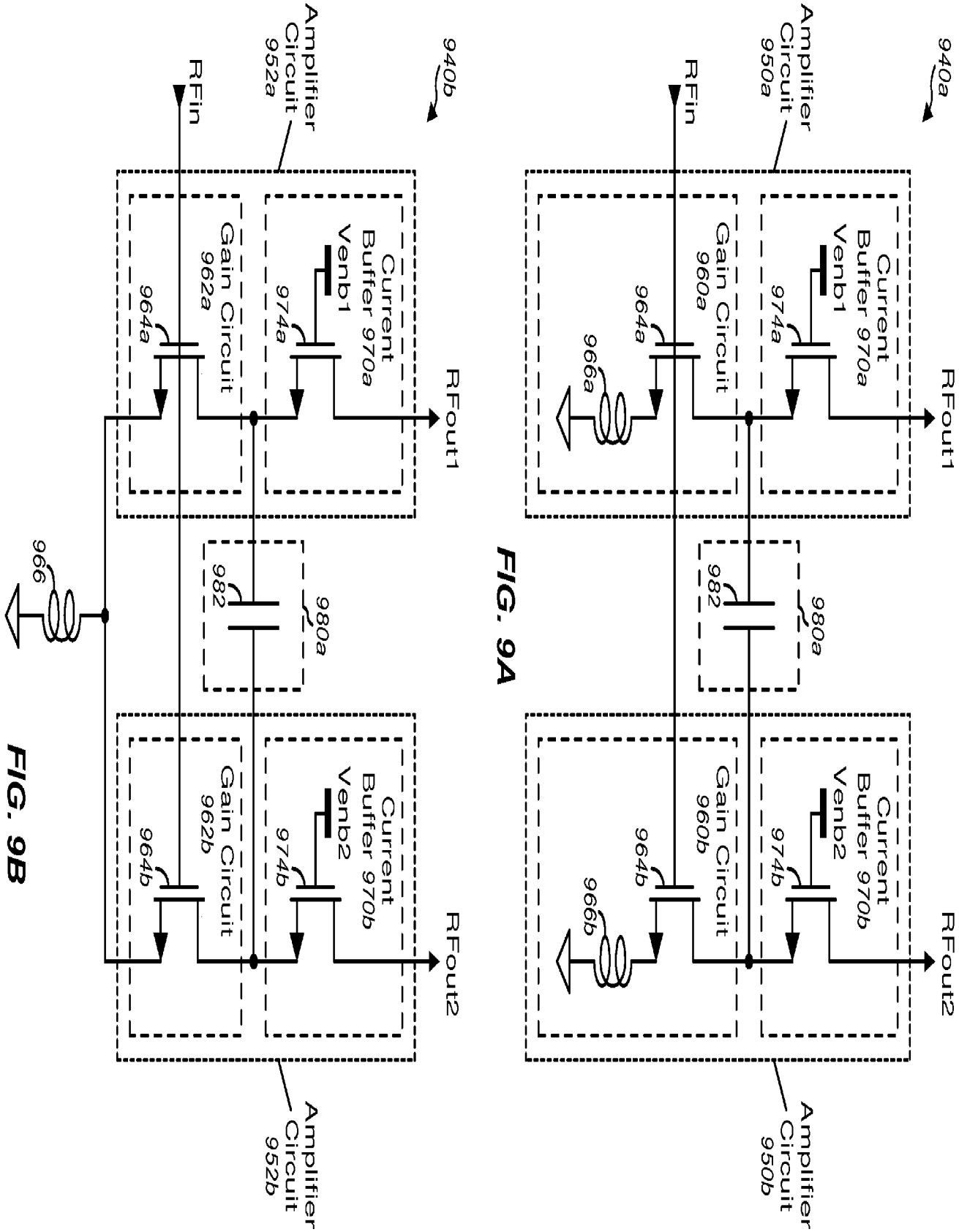
940a
Amplifier Circuit 950a
RFin
Current Buffer 970a
Venb1
974a
Gain Circuit 960a
964a
966a
RFout1
980a
982
Current Buffer 970b
Venb2
974b
Gain Circuit 960b
964b
966b
RFout2
Amplifier Circuit 950b

FIG. 9A

940b
Amplifier Circuit 952a
RFin
Current Buffer 970a
Venb1
974a
Gain Circuit 962a
964a
RFout1
966
980a
982
Current Buffer 970b
Venb2
974b
Gain Circuit 962b
964b
RFout2
Amplifier Circuit 952b

FIG. 9B

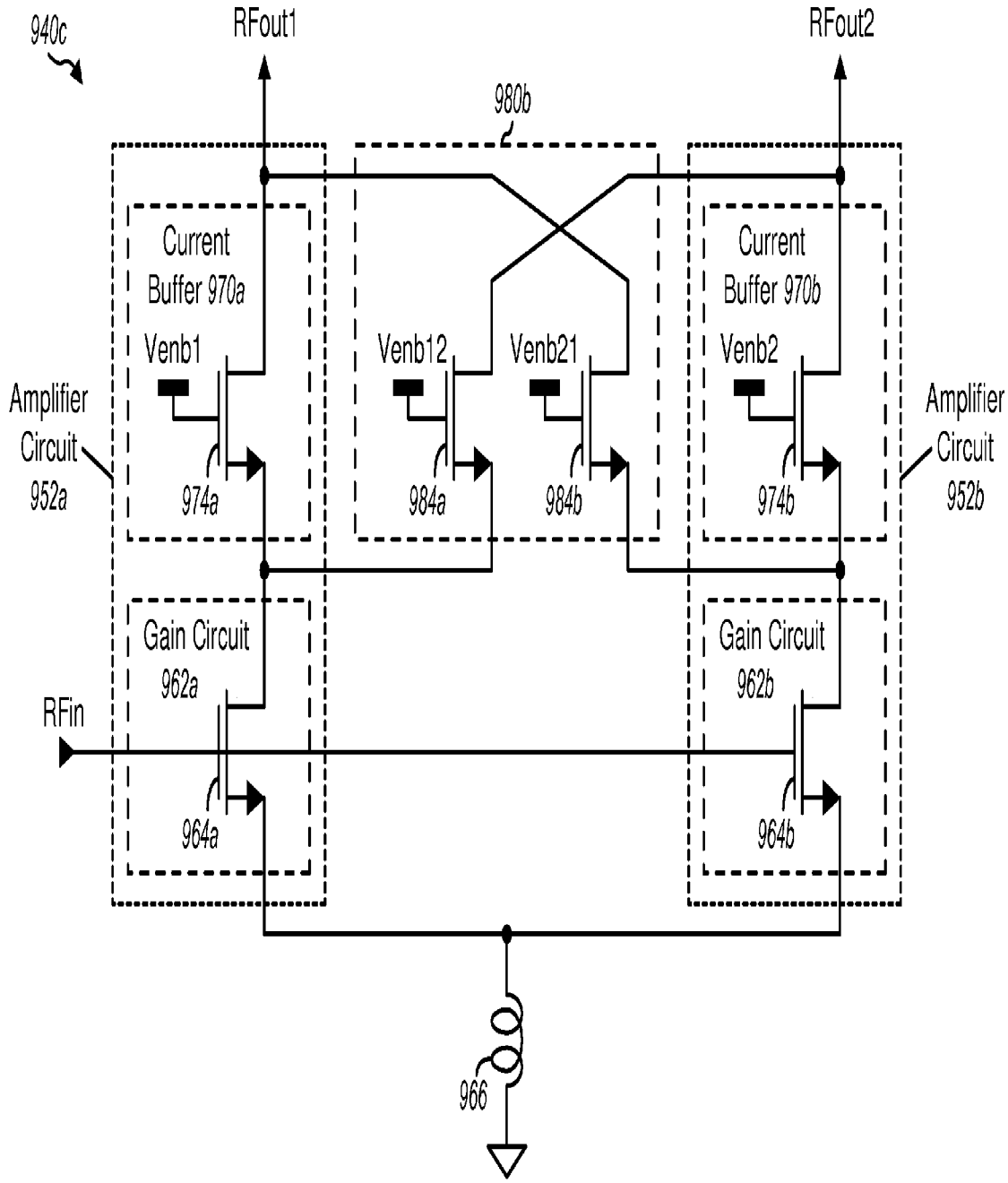
940c
RFout1
RFout2
980b
Current
Buffer 970a
Current
Buffer 970b
Venb1
Venb12
Venb21
Venb2
Amplifier
Circuit
952a
Amplifier
Circuit
952b
974a
984a
984b
974b
Gain Circuit
962a
Gain Circuit
962b
RFin
964a
964b
966

FIG. 9C

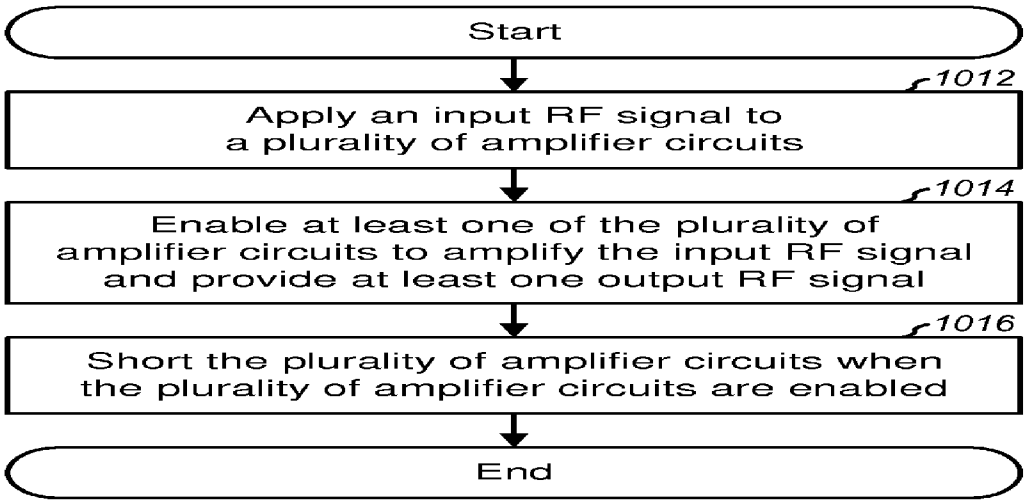
Start
1000
1012
Apply an input RF signal to a plurality of amplifier circuits
1014
Enable at least one of the plurality of amplifier circuits to amplify the input RF signal and provide at least one output RF signal
1016
Short the plurality of amplifier circuits when the plurality of amplifier circuits are enabled
End

FIG. 10

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/066230

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03F3/19 H03F1/22 H03F3/72 H03F3/21 H03F1/26
H03F3/24 H03F3/68
ADD.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F H03G H04B H03H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010/237945 A1 (CASSIA MARCO [US] ET AL) 23 September 2010 (2010-09-23)	1-12, 15-20
A	paragraphs [0004] - [0005], [0032] - [0055]; figures 3,4,5	13,14
X	WO 2011/019850 A1 (QUALCOMM INC [US]; LEE HANIL [US]; CHANG LI-CHUNG [US]) 17 February 2011 (2011-02-17)	1-12, 15-20
A	paragraphs [0047] - [0064]; figures 6,7,8	13,14
X	WO 2008/103757 A1 (QUALCOMM INC [US]; KIM TAE WOOK [US]; KLEMENS GUY [US]; BARNETT KENNET) 28 August 2008 (2008-08-28)	1-12, 15-20
A	paragraphs [0062] - [0099]; figures 6,7,8A,9,10	13,14
A	US 2004/113746 A1 (BRINDLE CHRISTOPHER N [US]) 17 June 2004 (2004-06-17) paragraphs [0007] - [0008]; figure 2	9-11

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 November 2013	03/12/2013

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Fedi, Giulio

3

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2013/066230

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2010237945 A1	23-09-2010	CN 102356542 A	15-02-2012
		EP 2409399 A1	25-01-2012
		JP 2012521670 A	13-09-2012
		KR 20110128355 A	29-11-2011
		TW 201103252 A	16-01-2011
		US 2010237945 A1	23-09-2010
		WO 2010108039 A1	23-09-2010
WO 2011019850 A1	17-02-2011	US 2011037518 A1	17-02-2011
		WO 2011019850 A1	17-02-2011
WO 2008103757 A1	28-08-2008	EP 2122826 A1	25-11-2009
		JP 5226702 B2	03-07-2013
		JP 2010519857 A	03-06-2010
		JP 2012151864 A	09-08-2012
		TW 200845568 A	16-11-2008
		US 2008204148 A1	28-08-2008
		US 2012274403 A1	01-11-2012
		WO 2008103757 A1	28-08-2008
US 2004113746 A1	17-06-2004	AU 2003299635 A1	22-07-2004
		EP 1573918 A1	14-09-2005
		JP 2006511179 A	30-03-2006
		US 2004113746 A1	17-06-2004
		US 2007247211 A1	25-10-2007
		WO 2004059842 A1	15-07-2004