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(54) **PHASE DIFFERENCE MAGNIFIER**

PHASENDIFFERENZVERGRÖSSERER

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- **PATENT ABSTRACTS OF JAPAN vol. 1996, no. 10, 31 October 1996 (1996-10-31) -& JP 08 146056 A (AKAI ELECTRIC CO LTD), 7 June 1996 (1996-06-07)**

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Description

FIELD OF THE INVENTION

[0001] The present invention relates to the field of signal processing, and more particularly to detecting and magnifying a phase difference between signals.

BACKGROUND OF THE INVENTION

[0002] In modern electronic devices, it is often necessary to transfer data between circuits in different digital clock domains. Although in many cases the clocks in the different domains are entirely unrelated, occasionally the clocks are generated from a common base clock or otherwise have a frequency relationship that may be used to time the transfer of data. In such cases, it is often critical to accurately align the phases of the clocks to provide deterministic timing relationships for data transfer. Unfortunately, accurate phase alignment is difficult in high frequency systems, because even very small sources of timing offset tend to produce proportionally large phase errors.

[0003] Patent Abstracts of Japan vol, 1996 no. 10, 31 October 1996 and JP-08146056-A disclose a controller which detects a phase difference between two signals with a slight phase difference to control equipment according to the phase difference. A phase difference detection circuit inputs the two signals and amplifies the phase difference. A waveform conversion circuit converts the signals with the amplified phase difference into square wave signals. A microcomputer inputs the square wave signals and outputs signals to two input ports of equipment to be controlled by the amplified phase difference.

[0004] Figure 1 is a diagram of a prior art memory system 10 that includes phase alignment logic for maintaining phase alignment between a host clock 16 (HCLK) and a memory clock 17 (MEMCLK). A reference clock generator 12 generates a reference clock 15 and outputs the reference clock 15 to a memory controller 25 and to a memory clock generator 14. The memory clock generator 14 includes a frequency multiplier circuit 21 that multiplies the reference clock 15 to produce a raw memory clock 13. The raw memory clock 13 is forwarded to a phase adjusting circuit 22 which incrementally adjusts the phase of the raw memory clock 13 to produce the memory clock 17. The memory clock 17 is output from the memory clock generator 14 by an output buffer 23 and supplied to a memory array 19 and to the memory controller 25.

[0005] The memory controller 25 receives the reference clock 15 and uses it to generate the host clock 16. The memory controller 25 includes host-side control logic 27 which is clocked by the host clock 16 and memory-side control logic 29 which is clocked by the memory clock 17. The host-side control logic 27 responds to memory access requests received from external agents by issuing commands to the memory-side control logic 29 to read and write the memory array 19. The memory-side control logic 29 responds to the commands from the host-side control logic 27 by issuing read and write commands to the memory array 19 via memory interface 42. Data to be written to the memory array 19 is supplied by external agents and forwarded by the host-side control logic 27 to the memory-side control logic 29, which in turn transfers the data to the memory array. Data read from the memory array 19 is forwarded by the memory-side control logic 29 to the host-side control logic 27 which in turn transfers the data to a requesting agent. The memory-side control logic 29 also includes a buffer 40 and dividing circuit 41 for generating a divided version of the memory clock 43. Because the divided version of the memory clock 43 is further divided by other circuitry in the memory controller, clock signal 43 is referred to as a partially divided memory clock 43 (PD MEMCLK).

[0006] The memory controller 25 also includes gear ratio logic 31 which includes respective dividers 34 and 36 to divide the host clock 16 and the partially divided memory clock 43 into respective clock signals that have a common frequency, called a beat frequency. The divided host clock 46 (HCDIV) and the divided memory clock 47 (MCDIV) are supplied to the phase adjuster 22 in the memory clock generator 14. The phase adjuster 22 reacts to the divided clock signals 46, 47 by detecting which of the clock signals 46, 47 leads the other and incrementally advancing or retarding the phase of the memory clock 17 accordingly. Using the phase difference between the divided clock signals 46, 47 as feedback, the phase adjuster 22 ideally drives the phase difference between the host clock 16 and the memory clock 17 to zero.

[0007] As mentioned above, accurate clock phase alignment becomes difficult in high frequency systems, because even very small sources of timing offset tend to produce proportionally large phase errors. In the prior-art system of Figure 1, for example, the memory clock generator 14 is typically implemented as a discrete integrated circuit (IC), rather than being integrated with the memory controller 25 on a single IC. Consequently, signal paths from the dividing circuits 34, 36 to the memory clock generator 14 are relatively long and output buffers 37, 38 are typically required to drive the divided clock signals 46, 47 off-chip to the memory clock generator 14. Routing delays in the signal paths from the dividers 34, 36 to the output buffers 37, 38 to the memory clock generator 14 usually must be closely matched, because any offset in these delays tends to produce a corresponding offset between the host clock 16 and the memory clock 17. This imposes significant constraints on the layout of the memory controller IC and on the board-level layout of the signal traces used to carry the divided clock signals 46, 47. Further, the output buffers 37, 38 typically require separate, quiet ground and power supplies to avoid introducing switching noise from adjacent interfaces. Otherwise, the divided clock signals 46, 47 supplied to the

phase adjuster 22 may have jitter contributing to the uncertainty of the phase alignment between the memory clock 17 and the host clock 16. Unfortunately, providing a separate power and ground supply requires two additional pins on the memory controller IC, often a scarce and valuable resource. Thus, the need to provide closely matched routing delays and quiet power and ground add to the complexity and expense of memory controller and board-level design. On the other hand, timing offset in the divided clock signals 46, 47 due to lack of care in signal routing or insufficient noise suppression may result in unacceptably small timing margins in the interface between the host clock and memory clock domains.

SUMMARY OF THE INVENTION

[0008] According to a first aspect of the invention there is provided a method of indicating a phase difference as claimed in claim 1. According to a second aspect of the invention there is provided an apparatus to indicate a phase difference as claimed in claim 6.

[0009] Other features and advantages of the invention will be apparent from the accompanying drawings and from the detailed description that follows below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings in which like references indicate similar elements and in which:

Figure 1 is a block diagram of a prior art circuit for phase aligning a pair of clocks;

Figure 2 is a block diagram of a circuit for phase aligning a pair of clocks according to one embodiment;

Figure 3 is a block diagram of a phase shift magnifier according to one embodiment;

Figure 4 is a waveform diagram that illustrates the operation of the phase shift magnifier of Figure 3;

Figure 5 is a block diagram of a phase shift magnifier according to an alternate embodiment; and

Figure 6 is a diagram illustrating exemplary alternate configurations of delay elements.

DETAILED DESCRIPTION

[0011] A circuit for aligning clock signals and other phase-alignable signals is disclosed in various embodiments. A phase shift magnifier is used to detect a phase difference between input clock signals and to indicate the phase difference by outputting clock signals having a phase difference that is magnified relative to the phase difference between the input clock signals. Because the phase difference between the output clock signals is magnified, signal path layout constraints and noise suppression requirements may be relaxed without introducing an undesirable phase - offset between the clocks sought to be aligned. This and other intended advantages will be apparent from the following description.

[0012] Figure 2 is a diagram of a memory system 50 that includes phase alignment logic according to an embodiment of the present invention. The memory system 50 includes a reference clock generator 12, memory clock generator 14 and memory array 19 that each function generally as described above in reference to Figure 1. The memory system 50 also includes a memory controller 53 having host-side control logic 27 and memory side control logic 29 that also each function generally as described above in reference to Figure 1. In one embodiment, the host clock 16 is generated from the reference clock 15, by clock insertion fogic 49 within the memory controller 53. The clock insertion logic 49 generates the host clock 16 by advancing the phase of the reference clock 15 (e.g., using a phase-locked loop circuit) to cancel delay caused by insertion of the reference clock 15 into the memory controller 53. In alternate embodiments, the host clock 16 may have a different phase relationship to the reference clock 15. Also, in alternate embodiments, subdivided versions of the reference clock 15 (e.g., REFCLK/2) may be supplied to the memory clock generator 14 instead of the reference clock 15 itself.

[0013] The memory controller 53 also includes gear ratio logic 51 that has been modified to include a phase difference magnifier 55. The phase difference magnifier 55 receives the divided host clock signal 46 (HCDIV) and the divided memory clock signal 47 (MCDIV) from respective dividing circuits 34, 36 and in response, generates a host clock feedback signal 56 (HCFB) and a memory clock feedback signal 57 (MCFB) that have a magnified phase difference relative to the phase difference between the divided host clock and divided memory clock signals 46, 47. The host clock feedback and memory clock feedback signals 56, 57 are output to the phase adjuster 22 in the memory clock generator by respective output buffers 37 and 38.

[0014] Because the phase difference magnifier 55 is positioned electrically and physically near the dividing circuits 34 and 36, the phase difference magnifier 55 receives the divided host clock and divided memory clock signals 46, 47 before they experience significant routing delays. As discussed below, the phase difference magnifier 55 includes phase detection circuitry for detecting the phase difference between the divided clock signals 46, 47 at this early stage. This is in contrast to prior art techniques in which the divided host clock signals 46, 47 are routed through the output buffers 37, 38 and onto external signal traces before their phase difference is detected by the phase adjusting circuit 22. Further, because the phase difference between the clock feedback signals 56, 57 is magnified relative to the phase difference between the divided clock signals 46, 47, substantially larger phase errors caused by noise and routing delays can be tolerated. Consequently, board and component level layout constraints can be significantly relaxed and the

output buffers 37, 38 can be powered using existing on-chip power and ground sources instead of requiring dedicated power and ground pins. Thus, by detecting the phase difference between the divided clock signals 46, 47 at an early stage and by magnifying the phase difference to provide greater noise and routing delay tolerance, accurate phase alignment can be achieved using a less expensive and less constrained design.

[0015] Figure 3 is a block diagram of a phase difference magnifier 55 according to one embodiment. The phase difference magnifier 55 includes a Reset/Set (R/S) flip-flop 67 that functions as a phase detector and that operates according to a truth table 70. Referring to the truth table 70, if a rising edge is detected on the divided memory clock signal (MCDIV) while the divided host clock signal (HCDIV) is low (shown in the truth table as HCDIV=0, MCDIV=1), then a signal called H_LATE will be driven high by NAND gate 59. In response to the high H_LATE signal and the high MCDIV signal, the NAND gate 60 will drive low a signal called M_LATE. Thus, when the MCDIV signal leads the HCDIV signal, M_LATE is driven low and H_LATE is driven high. On the other hand, if the HCDIV signal leads the MCDIV signal, M_LATE is driven high (indicating that MCDIV lags HCDIV) and H_LATE is driven low. After both HCDIV and MCDIV reach a high state, the R/S flip-flop retains the M_LATE and H_LATE signals in respective states that were determined by the low to high transition of the trailing input signal. MCDIV or HCDIV. This is shown in the truth table 70 by the entry indicating that M_LATE_{N+1} maintains the preceding state of M_LATE (i.e., M_LATE_N) while both HCDIV and MCDIV are high. During the time that MCDIV and HCDIV are both low, referred to herein as a "reset period", M_LATE and H_LATE are both reset to a high state. In one embodiment. H_LATE is not used outside the R/S flip-flop, but M_LATE and H_LATE are both coupled to respective output buffers 61. 62 so that balanced load impedances are presented to the logic gates 59, 60.

[0016] In the embodiment shown in Figure 3, HCDIV is input to a delay element Delay1 to generate a delayed version of the HCDIV signal called D1. D1 is used to gate a D flip-flop 64 that receives M_LATE as an input. In this arrangement, the D flip-flop 64 samples M_LATE a predetermined time after each risthg edge of HCDIV and outputs the sampled value as a select signal called SET_LATE. As discussed below, the predetermined delay introduced by the delay element Delay1 is chosen to provide time for any extended metastable state of the R/S flip-flop 67 to be resolved.

[0017] The delayed HCDIV signal. D1, is further delayed by another delay element Delay2 to produce signal D2, and the signal D2 is further delayed by another delay element Delay3 to produce signal D3. Because the D2 and D3 signals have a fixed, predetermined phase difference (i.e., equal to the delay introduced by element Delay3), they can be used to express the phase difference detected between the divided clock signals HCDIV and MCDIV. Depending on the state of the SEL_LATE signal, one of the D2 and D3 signals is selected to be the memory clock feedback signal 57 (MCFB) and the other of the D2 and D3 signals is selected to be the host clock feedback signal 56 (HCFB). Multiplexers 66 and 68 are provided for this purpose, with each of the multiplexers 66, 68 selecting an opposite one of D2 and D3 for a given state of the SEL_LATE signal. For example, if SEL_LATE is high, indicating that the host clock leads the memory clock, then SEL_LATE causes multiplexer 68 to select D2 to be the host clock feedback signal 56 and SEL_LATE causes multiplexer 66 to select D3 to be the memory clock feedback signal 57. Because the phase difference between the divided clock signals HCDN and MCDIV will tend to be much smaller than the predetermined phase difference between the D2 and D3 signals (due to the closed-loop phase adjustment tending toward a zero phase difference), the effect of outputting the D2 and D3 signals to represent the phase difference between the divided clock signals 46, 47 is to magnify the phase difference in the representative feedback signals 56, 57 and therefore to make the phase difference more impervious to transient events (e.g., noise) and systematic inaccuracies (e.g., unequal routing delays).

[0018] Still referring to Fig. 3, note that, because SEL_LATE is generated in response to a rising edge transition of D 1 which necessarily precedes a rising edge transition of D2 or D3, the inputs to the multiplexers 66 and 68 will be low during any transition of the SEL_LATE signal. This prevents a glitch in the HCFB and MCFB signals 53, 56 that might otherwise be caused by simultaneous transitioning of the SEL_LATE signal and an input to the multiplexers 66, 68.

[0019] A number of changes may be made to the phase difference magnifier 55 of Figure 3 without departing from the scope of the present invention. For example, other phase detection circuits may be used instead of the R/S flip-flop 67 including, but not limited to, cross-coupled D flip-flops, cross-coupled R/S flip-flops and other sense and hold circuits. Further, the R/S flip-flop itself may be implemented differently (e.g., using NOR gates instead of NAND gates). Also, in other embodiments, other types of storage elements may be used in place of the D flip-flop 64. Also, the Delay2 and Delay3 elements may be clocked by a clock that is not derived from the divided host clock 46. For example, delayed versions of the host clock itself (e.g., signal 16 of Figure 2), instead of the divided host clock 46, could be output by the phase difference magnifier 55. Also, the divided memory clock 47, or the memory clock itself (e.g., signal 17 of Figure 2) could be used in an alternate embodiment. Further, as discussed below in reference to Figure 6, different delay element configurations may be used instead of the configuration shown in Figure 3. Other implementation details may also be changed without departing from the scope of the present invention.

[0020] Figure 4 is a timing diagram that illustrates the operation of a phase difference magnifier according to the embodiment shown in Figure 3. In a first cycle (Cycle

1) of the divided host and memory clocks (HCDIV and MCDIV), HCDIV leads MCDIV. Consequently, M_LATE is driven high and sampled a short time later at the rising edge 81 of signal D1 to cause the SEL_LATE signal to become high. Because SEL_LATE is high, the D2 signal is selected to be HCFB output and the more delayed D3 signal is selected to be the MCFB output. Thus, while there is only a relatively small phase difference 91 between HCDIV and MCDIV, the phase difference is effectively magnified in the output to the phase adjuster as shown by the phase difference 101 by which MCFB lags HCFB.

[0021] Still referring to the first cycle of the MCDIV and HCDIV signals shown in Figure 4, for a brief time MCDIV remains high after HCDN has transitioned to a low level. Because of this input state, the M_LATE signal briefly goes low and then returns to a high level when MCDIV goes low. This is shown by arrow 111. Because the sample time established by the rising edge 81 of D1 occurs well before the brief low state 111 of M_LATE, the low state 111 of M_LATE caused by the phase offset between the trailing edges of HCDIV and MCDIV does not affect the SEL_LATE signal.

[0022] In cycle two (Cycle2) of the HCDIV and MCDIV signals, HCDIV continues to lead MCDIV, but now by a smaller margin. This is expected because, in response to detecting that MCFB lags HCFB, the phase adjusting circuit in the memory clock generator has incrementally advanced the phase of the memory clock signal (e.g., by slightly shortening the time period of a cycle of the memory clock signal). Because HCDIV continues to lead MCDIV in cycle two, the M_LATE signal is driven high and sampled at the rising edge 83 of D1 to also drive the SEL_LATE signal high. Because SEL_LATE is high, the more delayed of the D2 and D3 signals (i.e., D3) is again output to be the MCFB signal, while the more advanced of the D2 and D3 signals (i.e., D2) is output to be the HCFB signal. Thus, while the phase difference 93 between the MCDIV and HCDIV signals has become even smaller, HCFB still leads MCFB by the same magnified phase difference 103 as in the previous cycle.

[0023] In cycle three (Cycle3) of the HCDIV and MCDIV signals, MCDIV has been advanced so that it now slightly leads the HCDIV signal. Consequently, the M_LATE signal goes low at the rising edge of MCDIV and remains low at least until it is sampled at the rising edge 85 of D1 to generate a low SEL_LATE signal. Because the SEL_LATE signal is low, the more advanced of the D2 and D3 signals (i.e., D2) is selected to be the MCFB signal and the more delayed of the D2 and D3 signals (i.e., D3) is selected to be the HCFB signal. Thus, MCFB now leads HCFB, but the same magnified phase difference 105 still appears between the MCFB and HCFB signals, despite the relatively small phase difference 95 between the MCDIV and HCDIV signals.

[0024] In cycle four (Cycle4) of the HCDIV and MCDIV signals, the MCDIV signal has been slightly retarded such that the MCDIV and HCDIV signals are almost perfectly in phase. The simultaneous (or near simultaneous) low to high transitions of the HCDIV and MCDIV signals gives rise to a metastable state in the R/S flip-flop of the phase difference magnifier. The metastable state is essentially a race condition in the two NAND gates that form the R/S flip-flop to determine which will eventually go high and which will go low (the outputs of both NAND gates cannot remain in the same state when both the HCDIV and MCDIV inputs are high). Until the race condition is resolved, the H_LATE and M_LATE signals are driven to voltage levels somewhere between a valid logic high and a valid logic low. The metastable state is illustrated by the shaded area 112 of the M_LATE signal in Figure 4. If the metastable state is not resolved by the time M_LATE is sampled at the rising edge of D1, an incorrect state of M_LATE may be captured in the D flip-flop that outputs SEL_LATE. In other words, an incorrect or even invalid SEL_LATE signal may be output to the multiplexers used to route the D2 and D3 signals to the phase adjuster. In one embodiment, this condition is prevented (at least within practical mean failure times), by using high gain amplifiers in the NAND gates (or other logic elements) that make up the R/S flip flop and also by providing a delay element Delay 1 that delays the rising edge of D 1 for a time considerably longer than the metastable state can reasonably be expected to last. Further, the output buffers (elements 61 and 62 of Figure 3) in the R/S flip-flop may be designed to have a hysteresis or a predetermined transition threshold (e.g., as in a Schmidt trigger device) such that a metastable signal level at the buffer input will not change the buffer output.

[0025] Still referring to cycle four, the metastable state is eventually resolved in favor of the HCDIV signal so that M_LATE is driven high. The M_LATE signal is sampled a brief time later to drive the SEL_LATE signal high and thereby to output D2 as HCFB and D3 as MCFB so that MCFB lags HCFB by the predetermined phase difference between D2 and D3.

[0026] Figure 5 is a block diagram of an alternate embodiment of a phase difference magnifier 75. The phase difference magnifier 75 includes a Reset/Set (R/S) flip-flop 67, a D flip-flop 64 and a delay element Delay 1, each of which functions generally as described in reference to Figure 3 to produce a SEL_LATE signal. In the embodiment of Figure 5, the SEL_LATE signal is driven high when the HCDIV signal leads the MCDIV signal, and the SEL_LATE signal is driven low when the MCDIV signal leads the HCDIV signal. As shown, a signal D2 is output by the Delay2 element and provided to a first input of a dual-input multiplexer 66. The D2 signal is also supplied to a delay element Delay3 which outputs a D3 signal. The D3 signal is output to be the host clock feedback signal, HCFB, and is also supplied to a Delay4 element which outputs a D4 signal to the other input of the multiplexer 66. The SEL_LATE is used to select which of the D2 and D4 signals is output by the multiplexer to be the memory clock feedback signal, MCFB. If SEL_LATE is high (indicating that MCDIV lags HCDIV), the D4 signal

is selected to be the MCFB signal. If SEL_LATE is low (indicating that MCDIV leads HCDIV), the D2 signal is selected to be the MCFB signal. By using delay elements Delay3 and Delay4 that each introduce a delay time, TDLY, the effect of selecting either the D2 or D4 signal is to select a signal that lags D3 by time TDLY (i.e., D4) or to select a signal that leads D3 by time TDLY (i.e., D2) as shown by the waveform diagram 71 in Figure 5. Thus, in contrast to the phase difference magnifier 55 of Figure 3, in which D3 and D4 signals are alternately selected to be the HCFB and MCFB outputs, depending on the state of SEL_LATE, in the phase difference magnifier 75 of Figure 5, a predetermined signal (e.g., D3) is output as the HCFB signal, and the SEL_LATE signal is used to select between signals that lead or lag the HCFB signal by a predetermined time. In an alternate embodiment, the D3 signal may be output as the MCFB signal and the SEL_LATE signal may be used to select between a leading and lagging signal to be the HCFB output. Also, a signal other than HCDIV may be used as the base clock source for the MCFB and HCFB output signals. Further, although the time delays introduced by the Delay3 and Delay4 elements have been described as being equal, unequal time delays may be used in an alternate embodiment. Also, it may be desirable to introduce an additional delay element between the Delay2 element and the multiplexer to provide time for the output of the D flip-flop to stabilize. These and other implementation details may be changed without departing from the spirit and scope of the present invention.

[0027] Figure 6 illustrates alternate delay circuits 121, 123 that may be used in the phase difference magnifier of Figure 5. The delay circuit 121, referred to as a cumulative delay circuit, is essentially the arrangement shown in Figure 5, except that a generalized clock, REFCLK, is used to clock the circuit. REFCLK may be the divided host clock HCDIV in a particular embodiment. In the cumulative delay circuit 121, the signal D3 is generated from REFCLK by applying the cumulative delays in elements Delay2 and Delay3. Similarly, the signal D4 is generated from REFCLK by applying the cumulative delays in elements Delay2, Delay3 and Delay4. In the delay circuit 123, referred to as a non-cumulative delay circuit, elements Delay5 and Delay6 are used to produce the D3 and D4 signals, respectively, directly from REFCLK. By choosing delay element Delay5 to produce essentially the same delay as elements Delay2 and Delay3 combined, and by choosing delay element Delay6 to produce essentially the same delay as elements Delay2, Delay3 and Delay4 combined, the non-cumulative delay circuit 123 provides essentially the same functionality as the cumulative delay circuit 121. A non-cumulative delay circuit design may likewise be used instead of the cumulative delay configuration of elements Delay3 and Delay4 in the phase difference magnifier 55 of Figure 3. Delay elements may be implemented using passive circuit components or any number of well known transistor-based circuits (e.g., a concatenation of buffer amplifiers, with the delay being determined by the number of stages).

[0028] Although the embodiments herein relate to aligning clocks in different clock domains of a memory system, application of the present invention is not so limited. The present invention may be applied in any circumstance where it is desirable to align the phase of two or more signals.

[0029] In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made to the specific exemplary embodiments without departing from the broader scope of the invention as set forth in the appended claims. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

Claims

1. A method of indicating a phase difference between a first input signal (46) and a second input signal (47), the method comprising:

   generating a first delayed signal (D2) by delaying a reference signal by a first predetermined time;
   generating a second delayed signal (D3;D4) by delaying the reference signal by a second predetermined time, the second predetermined time being longer than the first predetermined time;
   detecting which of the first and second input signals leads the other;
   outputting the first delayed signal (D2) to represent the first input signal and outputting a signal that lags the first delayed signal by a third predetermined time to represent the second input signal, if the first input signal leads the second input signal; and
   outputting the second delayed signal (D3;D4) to represent the first input signal and outputting a signal that leads the second delayed signal by a fourth predetermined time to represent the second input signal, if the second input signal leads the first input signal.

2. The method of claim 1 wherein the reference signal is the first input signal (46).

3. The method of claim 1 wherein outputting the first delayed signal (D2) and a signal that lags the first delayed signal comprises outputting the first delayed signal (D2) to represent the first input signal and outputting the second delayed signal (D3) to represent the second input signal, the third predetermined time being the difference between the first predetermined time and the second predetermined time.

4. The method of claim 3 wherein outputting the second delayed signal (D3) and a signal that leads the second delayed signal comprises outputting the second delayed signal (D3) to represent the first input signal and outputting the first delayed signal (D2) to represent the second input signal, the fourth predetermined time being the difference between the first predetennined time and the second predetermined time.

5. The method of claim 1 further comprising:

generating a third delayed signal (D3) that lags the reference signal by a fifth predetermined time, the fifth predetermined time being greater than the first predetermined time and less than the second predetermined time; and
outputting the third delayed signal (D3) to represent the second input signal, the third predetermined time being the difference between the first predetermined time and the fifth predetermined time, and the fourth predetermined time being the difference between the second predetermined time and the fifth predetermined time.

6. An apparatus (55) to indicate a phase difference between a first input signal (46) and a second input signal (47), the apparatus comprising:

a phase detector (67) to detect which of the first and second input signals leads the other and to output a select signal having a first state if the first input signal leads the second input signal and a second state if the second input signal leads the first input signal;
a first delay circuit element (DELAY 2) having an input to receive a first reference signal and an output to output a first delayed signal (D2) that lags the first reference signal by a first predetermined time;
a second delay circuit element (DELAY 3; DELAY 4) having an input to receive a second reference signal and an output to output a second delayed signal (D3;D4) that lags the second reference signal by a second predetermined time;
a first multiplexer (66) that includes a control input coupled to receive the select signal (SEL-LATE) from the phase detector (67) and first and second data inputs respectively coupled to receive the first and second delayed signals from the first and second delay circuit elements, the first multiplexer outputting the first delayed signal (D2) if the select signal is in the first state and outputting the second delayed signal (D3; D4) if the select signal is in the second state; and an output signal path to output a signal (HCFB) that lags the first delayed signal (D2) when the select signal is in the first state and that leads the second delayed signal (D3; D4) when the select signal is in the second state.

7. The apparatus of claim 6 further comprising a third delay circuit element (DELAY 3) having an input to receive a third reference signal and an output to output a third delayed signal (D3) that lags the first delayed signal (D2) by a third predetermined time and that leads the second delayed signal (D4) by a fourth predetermined time, and wherein the output signal path is coupled to the third delay circuit to output the third delayed signal.

8. The system of claim 7 wherein the second reference signal is the third delayed signal (D3).

9. The system of claim 7 wherein the third reference signal is the first delayed signal (D2).

10. The system of claim 6 further comprising a second multiplexer (68) that includes a control input coupled to receive the select signal (SEL-LATE) from the phase detector (67), first and second data inputs respectively coupled to receive the first and second delayed signals (D2,D3) from the first and second delay circuit elements, and an output coupled to the output signal path, the second multiplexer (68) outputting the second delayed signal (D3) on the output signal path if the select signal is in the first state and outputting the first delayed signal (D2) on the output signal path if the select signal is in the second state.

Patentansprüche

1. Verfahren zum Anzeigen einer Phasendifferenz zwischen einem ersten Eingangssignal (46) und einem zweiten Eingangssignal (47), wobei das Verfahren folgendes umfasst:

das Erzeugen eines ersten verzögerten Signals (D2), indem ein erstes Referenzsignal um einen vorbestimmten Zeitraum verzögert wird;
das Erzeugen eines zweiten verzögerten Signals (D3; D4), indem das Referenzsignal um einen zweiten vorbestimmten Zeitraum verzögert wird, wobei der zweite vorbestimmte Zeitraum länger ist als der erste vorbestimmte Zeitraum;
das Detektieren, welches der ersten und zweiten Eingangssignale in Bezug auf das andere voreilt;
das Ausgeben des ersten verzögerten Signals (D2), so dass es das erste Eingangssignal darstellt, und das Ausgaben eines Signals, das dem ersten verzögerten Signal um einen dritten vorbestimmten Zeitraum nacheilt, so dass es das zweite Eingangssignal darstellt, wenn das erste

Eingangssignal in Bezug auf das zweite Eingangssignal voreilt; und
das Ausgeben des zweiten verzögerten Signals (D3; D4), so dass es das erste Eingangssignal darstellt, und das Ausgaben eines Signals, das in Bezug auf das zweite verzögerte Signal um einen vierten vorbestimmten Zeitraum voreilt, so dass es das zweite Eingangssignal darstellt, wenn das zweite Eingangssignal in Bezug auf das erste Eingangssignal voreilt.

2. Verfahren nach Anspruch 1, wobei es sich bei dem Referenzsignal um das erste Eingangssignal (46) handelt.

3. Verfahren nach Anspruch 1, wobei das Ausgeben des ersten verzögerten Signals (D2) und eines Signals, das dem ersten verzögerten Signal nacheilt, das Ausgeben des ersten verzögerten Signals (D2) umfasst, so dass das erste Eingangssignal dargestellt wird, und das Ausgaben des zweiten verzögerten Signals (D3), so dass das zweite Eingangssignal dargestellt wird, wobei der dritte vorbestimmte Zeitraum die Differenz zwischen dem ersten vorbestimmten Zeitraum und dem zweiten vorbestimmten Zeitraum entspricht.

4. Verfahren nach Anspruch 3, wobei das Ausgeben des zweiten verzögerten Signals und eines Signals, das dem zweiten verzögerten Signal voreilt, das Ausgeben des zweiten verzögerten Signals umfasst, um das erste Eingangssignal darzustellen, und das Ausgeben des ersten verzögerten Signals, um das zweite Eingangssignals darzustellen, wobei der vierte vorbestimmte Zeitraum die Differenz zwischen dem ersten vorbestimmten Zeitraum und dem zweiten vorbestimmten Zeitraum darstellt.

5. Verfahren nach Anspruch 1, wobei dieses ferner folgendes umfasst:

das Erzeugen eines dritten verzögerten Signals (D3), das dem Referenzsignal um einen fünften vorbestimmten Zeitraum nacheilt, wobei der fünfte vorbestimmte Zeitraum größer ist als der erste vorbestimmte Zeitraum und kleiner als der zweite vorbestimmte Zeitraum; und
das Ausgeben des dritten verzögerten Signals, um das zweite Eingangssignal darzustellen, wobei der dritte vorbestimmte Zeitraum die Differenz zwischen dem ersten vorbestimmten Zeitraum und dem fünften vorbestimmten Zeitraum darstellt, und wobei der vierte vorbestimmte Zeitraum die Differenz zwischen dem zweiten vorbestimmten Zeitraum und dem fünften vorbestimmten Zeitraum darstellt.

6. Vorrichtung (55) zum Anzeigen einer Phasendifferenz zwischen einem ersten Eingangssignal (46) und einem zweiten Eingangssignal (47), wobei die Vorrichtung folgendes umfasst:

einen Phasendetektor (67) zum Detektieren, welches der ersten und zweiten Eingangssignale in Bezug auf das andere voreilt, und zum Ausgeben eines Auswahlsignals mit einem ersten Zustand, wenn das erste Eingangssignal in Bezug auf das andere in Bezug auf das zweite Eingangssignal voreilt, und mit einem zweiten Zustand, wenn das zweite Eingangssignal in Bezug auf das erste Eingangssignal voreilt;
ein erstes Verzögerungsschaltungselement (DELAY 2) mit einem Eingang für den Empfang eines ersten Referenzsignals und einem Ausgang zum Ausgeben eines ersten verzögerten Signals (D2), das hinter dem ersten Referenzsignal um einen ersten vorbestimmten Zeitraum nacheilt;
ein zweites Verzögerungsschaltungselement (DELAY 3; DELAY 4) mit einem Eingang für den Empfang eines zweiten Referenzsignals und einem Ausgang zum Ausgeben eines zweiten verzögerten Signals (D3; D4), das hinter dem zweiten Referenzsignal um einen zweiten vorbestimmten Zeitraum nacheilt;
einen ersten Multiplexer (66), der einen Steuereingang aufweist, der so gekoppelt ist, dass er das Auswahlsignal (SEL-LATE) von dem Phasendetektor (67) empfängt, und wobei die ersten und zweiten Dateneingänge entsprechend so gekoppelt sind, dass sie die ersten und zweiten verzögerten Signale von den ersten und zweiten Verzögerungsschaltungselementen empfangen, wobei der erste Multiplexer das erste verzögerte Signal (D2) ausgibt, wenn sich das Auswahlsignal in dem ersten Zustand befindet, und wobei das zweite verzögerte Signal (D3; D4) ausgegeben wird, wenn sich das Auswahlsignal in dem zweiten Zustand befindet; und mit einem Ausgangssignalpfad zur Ausgabe eines Signals (HCFB), das dem ersten verzögerten Signal (D2) nacheilt, wenn sich das Auswahlsignal in dem ersten Zustand befindet, und welches dem zweiten verzögerten Signal (D3; D4) voreilt, wenn sich das Auswahlsignal in dem zweiten Zustand befindet.

7. Vorrichtung nach Anspruch 6, wobei diese ferner ein drittes Verzögerungsschaltungselement (DELAY 3) umfasst, mit einem Eingang für den Empfang eines dritten Referenzsignals und mit einem Ausgang zum Ausgeben eines dritten verzögerten Signals (D3), das in Bezug auf das erste verzögerte Signal (D2) um einen dritten vorbestimmten Zeitraum nacheilt und das in Bezug auf das zweite verzögerte Signal (D4) um einen vierten vorbestimmten Zeitraum vor-

eilt, und wobei der Ausgangssignalpfad mit der dritten Verzögerungsschaltung gekoppelt ist, um das dritte verzögerte Signal auszugeben.

8. System nach Anspruch 7, wobei das zweite Referenzsignal das dritte verzögerte Signal (D3) darstellt.

9. System nach Anspruch 7, wobei das dritte Referenzsignal das erste verzögerte Signal (D2) darstellt.

10. System nach Anspruch 6, wobei dieses ferner einen zweiten Multiplexer (68) umfasst, der einen Steuereingang aufweist, um das Auswahlsignal (SEL-LATE) von dem Phasendetektor (67) zu empfangen, wobei erste und zweite Dateneingänge entsprechend so gekoppelt sind, dass sie die ersten und zweiten verzögerten Signale (D2; D3) von den ersten und zweiten Verzögerungsschaltungselementen empfangen, und mit einem Ausgang, der mit dem Ausgangssignalpfad gekoppelt ist, wobei der zweite Multiplexer (68) das zweite verzögerte Signal (D3) auf dem Ausgangssignalpfad ausgibt, wenn sich das Auswahlsignal in dem ersten Zustand befindet, und wobei er das erste verzögerte Signal (D2) auf dem Ausgangssignalpfad ausgibt, wenn sich das Auswahlsignal in dem zweiten Zustand befindet.

Revendications

1. Procédé d'indication d'une différence de phase entre un premier signal d'entrée (46) et un second signal d'entrée (47), le procédé comprenant les étapes consistant à :

générer un premier signal retardé (D2) en retardant un signal de référence par un premier temps prédéterminé ;
générer un second signal retardé (D3 ; D4) en retardant le signal de référence par un second temps prédéterminé, le second temps prédéterminé étant plus long que le premier temps prédéterminé;
détecter lequel des premier et second signaux d'entrée devance l'autre ;
émettre le premier signal retardé (D2) pour représenter le premier signal d'entrée et émettre un signal qui retarde le premier signal retardé par un troisième temps prédéterminé pour représenter le second signal d'entrée, si le premier signal d'entrée devance le second signal d'entrée ; et
émettre le second signal retardé (D3 ; D4) pour représenter le premier signal d'entrée et émettre un signal qui devance le second signal retardé par un quatrième temps prédéterminé pour représenter le second signal d'entrée, si le second signal d'entrée devance le premier signal d'entrée.

2. Procédé selon la revendication 1, dans lequel le signal de référence est le premier signal d'entrée (46).

3. Procédé selon la revendication 1, dans lequel l'émission du premier signal retardé (D2) et d'un signal qui retarde le premier signal retardé comprend l'étape consistant à émettre le premier signal retardé (D2) pour représenter le premier signal d'entrée et émettre le second signal retardé (D3) pour représenter le second signal d'entrée, le troisième temps prédéterminé étant la différence entre le premier temps prédéterminé et le second temps prédéterminé.

4. Procédé selon la revendication 3, dans lequel l'émission du second signal retardé (D3) et d'un signal qui devance le second signal retardé comprend l'étape consistant à émettre le second signal retardé (D3) pour représenter le premier signal d'entrée et à émettre le premier signal retardé (D2) pour représenter le second signal d'entrée, le quatrième temps prédéterminé étant la différence entre le premier temps prédéterminé et le second temps prédéterminé.

5. Procédé selon la revendication 1, comprenant en outre les étapes consistant à :

générer un troisième signal retardé (D3) qui retarde le signal de référence par un cinquième temps prédéterminé, le cinquième temps prédéterminé étant supérieur au premier temps prédéterminé et inférieur au second temps prédéterminé ; et
émettre le troisième signal retardé (D3) pour représenter le second signal d'entrée, le troisième temps prédéterminé étant la différence entre le premier temps prédéterminé et le cinquième temps prédéterminé, et le quatrième temps prédéterminé étant la différence entre le second temps prédéterminé et le cinquième temps prédéterminé.

6. Appareil (55) pour indiquer une différence de phase entre un premier signal d'entrée (46) et un second signal d'entrée (47), l'appareil comprenant :

un détecteur de phase (67) pour détecter lequel des premier et second signaux d'entrée devance l'autre et pour émettre un signal de sélection ayant un premier état si le premier signal d'entrée devance le second signal d'entrée et un second état si le second signal d'entrée devance le premier signal d'entrée ;
un premier élément de circuit de retard (DELAY 2) ayant une entrée pour recevoir un premier signal de référence et une sortie pour émettre

un premier signal retardé (D2) qui retarde le premier signal de référence par un premier temps prédéterminé ;
un second élément de circuit de retard (DELAY 3 ; DELAY 4) ayant une entrée pour recevoir un second signal de référence et une sortie pour émettre un second signal retardé (D3 ; D4) qui retarde le second signal de référence par un second temps prédéterminé ;
un premier multiplexeur (66) qui comprend une entrée de commande couplée pour recevoir le signal de sélection (SEL-LATE) du détecteur de phase (67) et les première et seconde entrées de données respectivement couplées pour recevoir les premier et second signaux retardés des premier et second éléments de circuit de retard, le premier multiplexeur émettant le premier signal retardé (D2) si le signal de sélection est dans le premier état et émettant le second signal retardé (D3 ; D4) si le signal de sélection est dans le second état ; et un chemin de signal de sortie pour émettre un signal (HCFB) qui retarde le premier signal retardé (D2) lorsque le signal de sélection est dans le premier état et qui devance le second signal retardé (D3 ; D4) lorsque le signal de sélection est dans le second état.

7. Appareil selon la revendication 6, comprenant en outre un troisième élément de circuit de retard (DELAY 3) ayant une entrée pour recevoir un troisième signal de référence et une sortie pour émettre un troisième signal retardé (D3) qui retarde le premier signal retardé (D2) par un troisième temps prédéterminé et qui devance le second signal retardé (D4) par un quatrième temps prédéterminé, et dans lequel le chemin de signal de sortie est couplé au troisième circuit de retard pour émettre le troisième signal retardé.

8. Système selon la revendication 7, dans lequel le second signal de référence est le troisième signal retardé (D3).

9. Système selon la revendication 7, dans lequel le troisième signal de référence est le premier signal retardé (D2).

10. Système selon la revendication 6 comprenant en outre un second multiplexeur (68) qui comprend une entrée de commande couplée pour recevoir le signal de sélection (SEL-LATE) du détecteur de phase (67), des première et seconde entrées de données couplées pour recevoir les premier et second signaux retardés (D2 ; D3) des premier et second éléments de circuit de retard, et une sortie couplée au chemin de signal de sortie, le second multiplexeur (68) émettant le second signal retardé (D3) sur le chemin de signal de sortie si le signal de sélection est dans le premier état et émettant le premier signal retardé (D2) sur le chemin de signal de sortie si le signal de sélection est dans le second état.

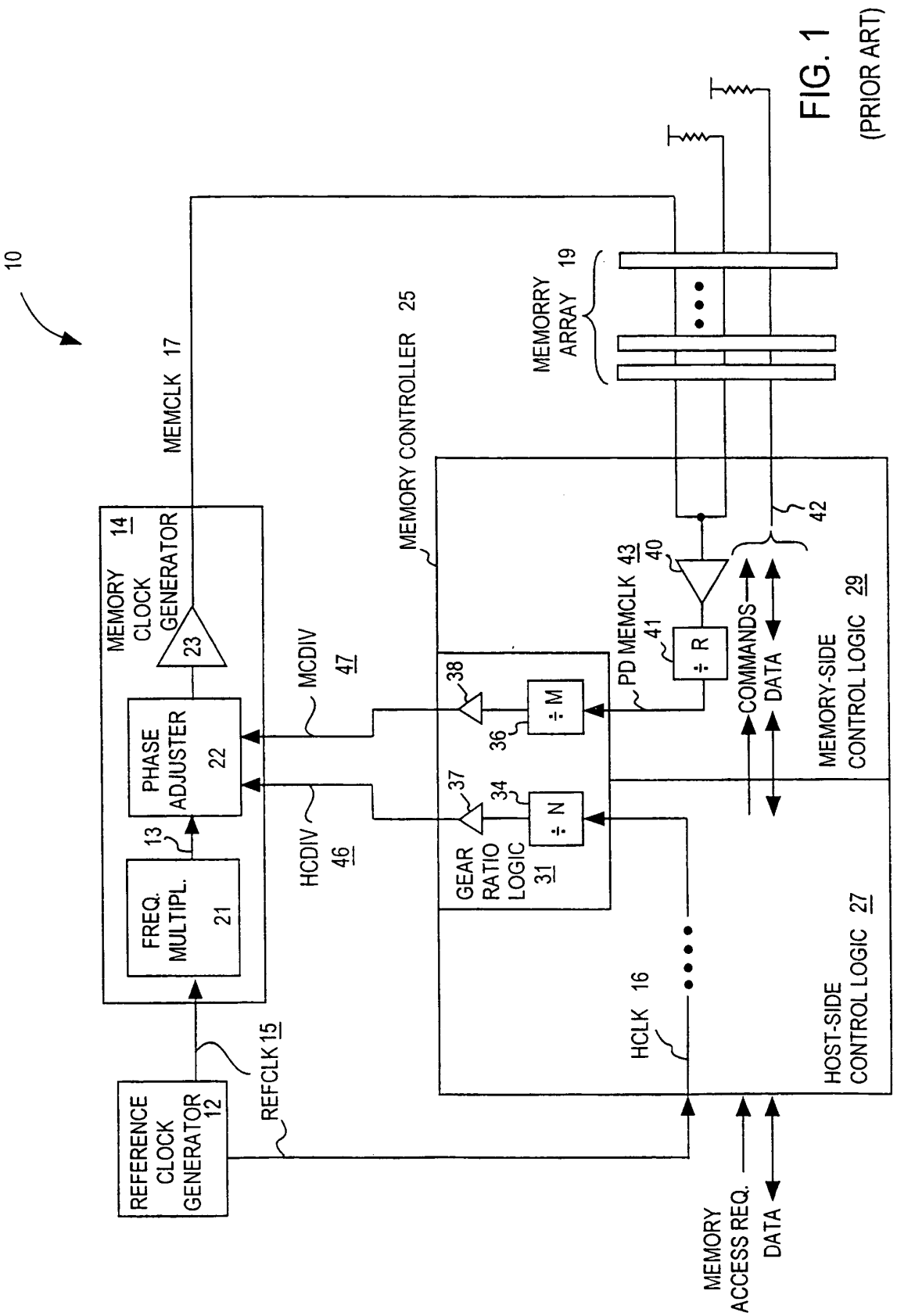

FIG. 1
(PRIOR ART)

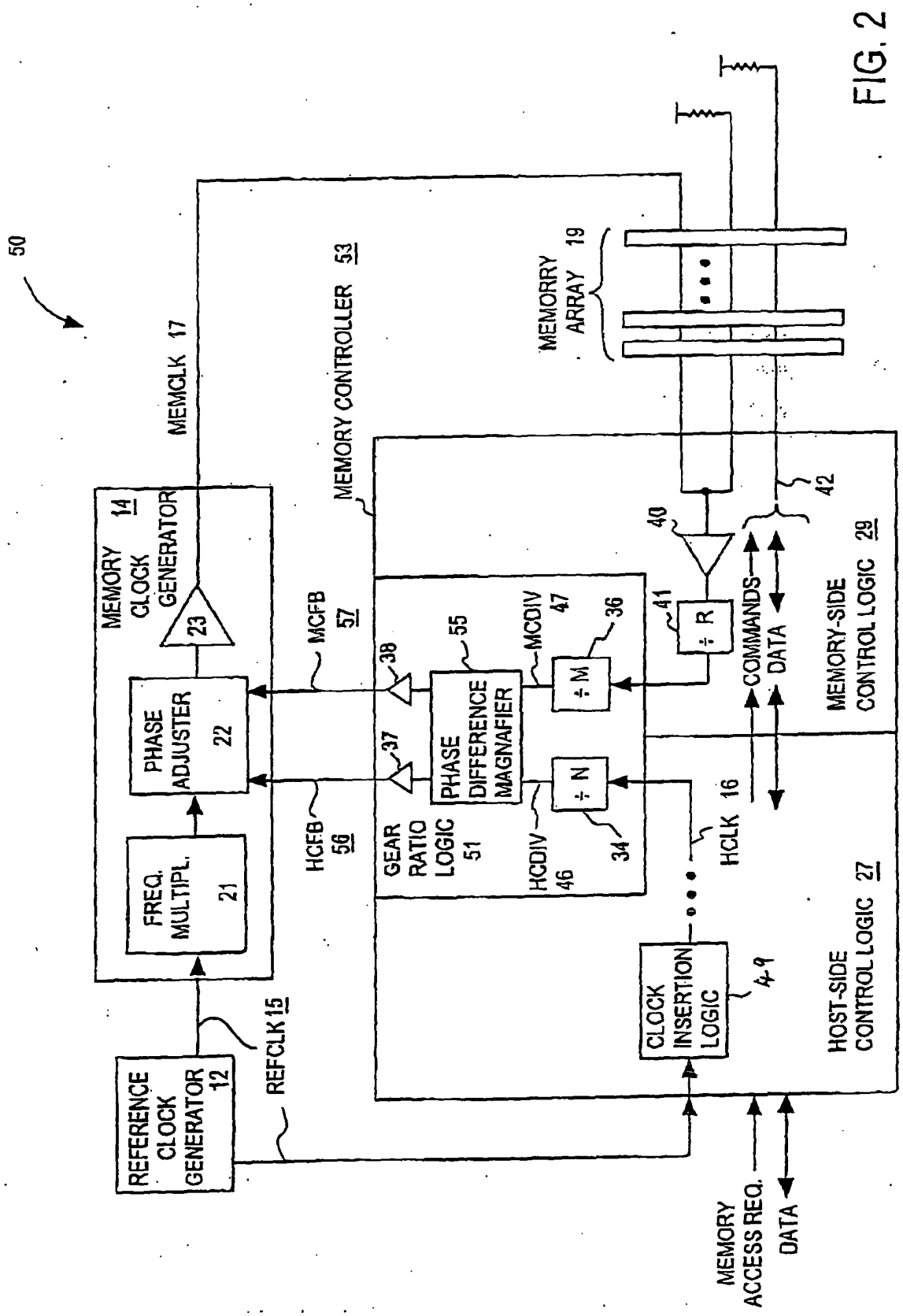
50
MEMCLK 17
MEMORY CONTROLLER 53
MEMORY ARRAY 19
MEMORY CLOCK GENERATOR 14
23
PHASE ADJUSTER 22
FREQ. MULTIPL. 21
REFERENCE CLOCK GENERATOR 12
REFCLK 15
MCFB 57
HCFB 56
38
37
PHASE DIFFERENCE MAGNAFIER 55
MCDIV 47
HCDIV 46
GEAR RATIO LOGIC 51
÷ M
÷ N
36
34
÷ R
41
40
42
COMMANDS
DATA
MEMORY-SIDE CONTROL LOGIC 29
HCLK 16
CLOCK INSERTION LOGIC 49
HOST-SIDE CONTROL LOGIC 27
MEMORY ACCESS REQ.
DATA

FIG. 2

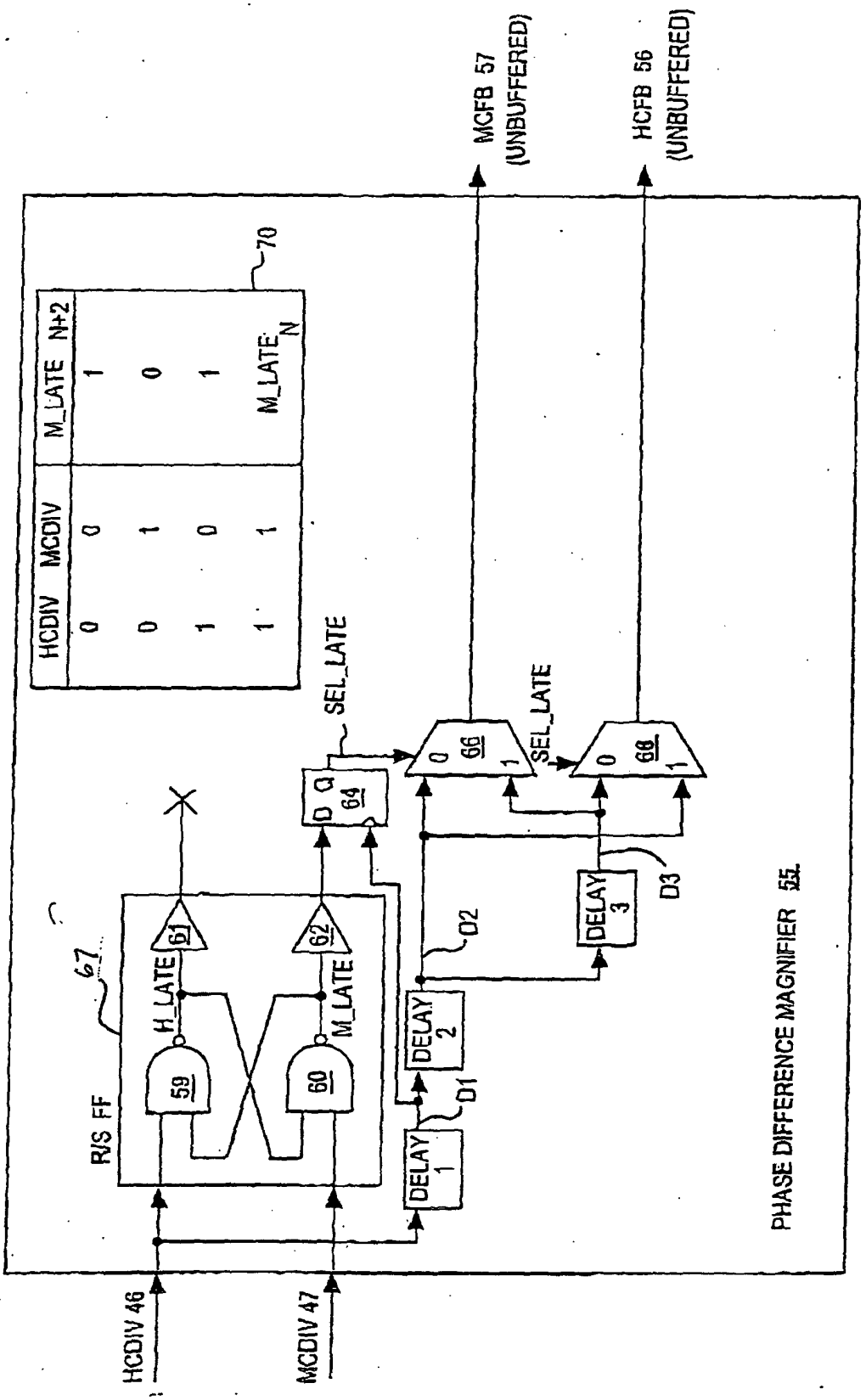
MCFB 57 (UNBUFFERED)
HCFB 56 (UNBUFFERED)
70
HCDIV MCDIV M_LATE N+2
0 0 1
0 1 0
1 0 1
1 1 M_LATE N
SEL_LATE
D Q 64
0 66 1
SEL_LATE
0 68 1
67
R/S FF
H_LATE 61
M_LATE 62
59
60
DELAY 1
DELAY 2
DELAY 3
D1
D2
D3
HCDIV 46
MCDIV 47
PHASE DIFFERENCE MAGNIFIER 55

FIG. 3

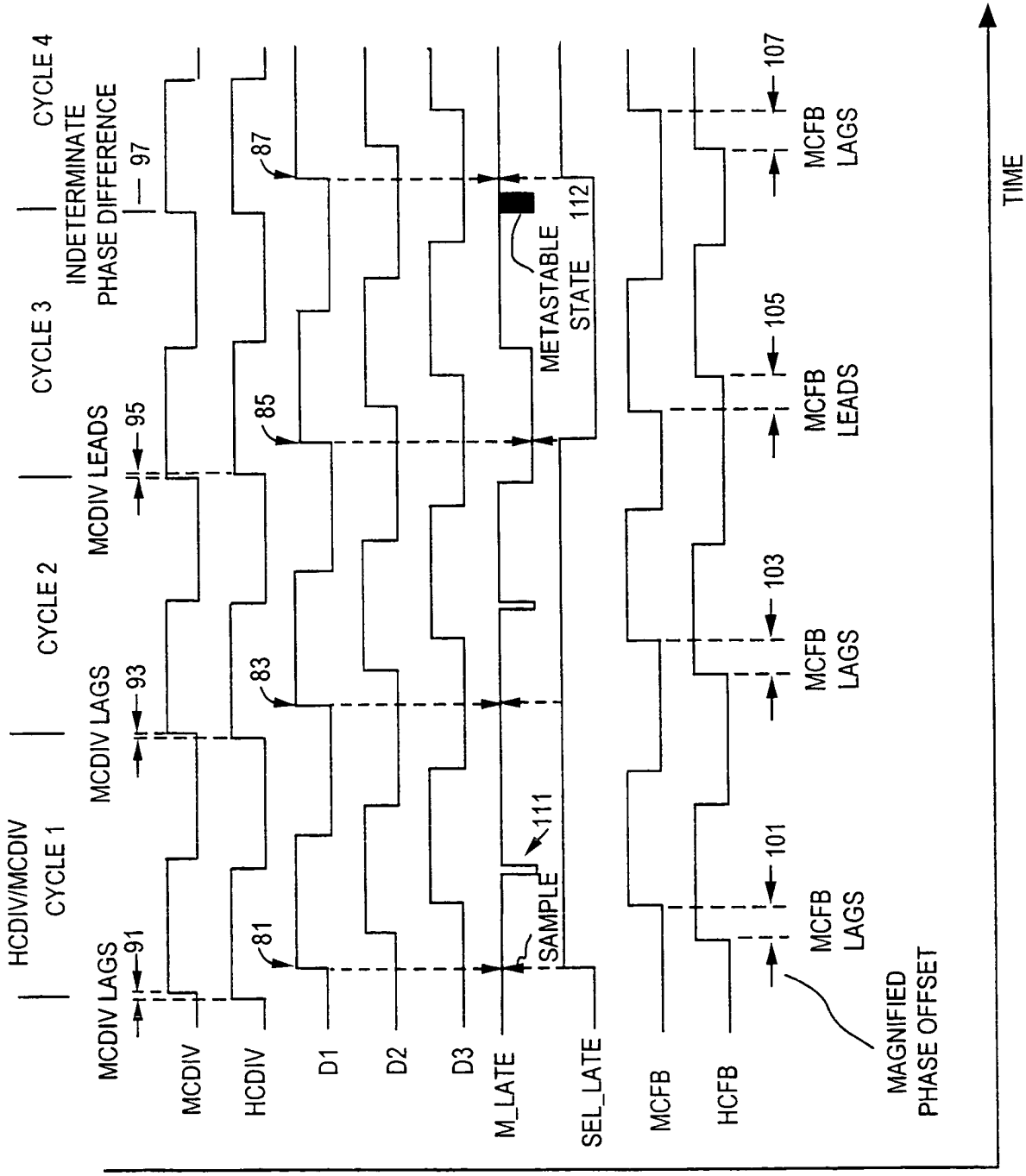
HCDIV/MCDIV
CYCLE 1
CYCLE 2
CYCLE 3
CYCLE 4
MCDIV LAGS
91
MCDIV LAGS
93
MCDIV LEADS
95
INDETERMINATE
PHASE DIFFERENCE
97
MCDIV
HCDIV
D1
D2
D3
M_LATE
SEL_LATE
MCFB
HCFB
81
83
85
87
SAMPLE
111
METASTABLE
STATE
112
101
103
105
107
MCFB
LAGS
MCFB
LAGS
MCFB
LEADS
MCFB
LAGS
MAGNIFIED
PHASE OFFSET
TIME

FIG. 4

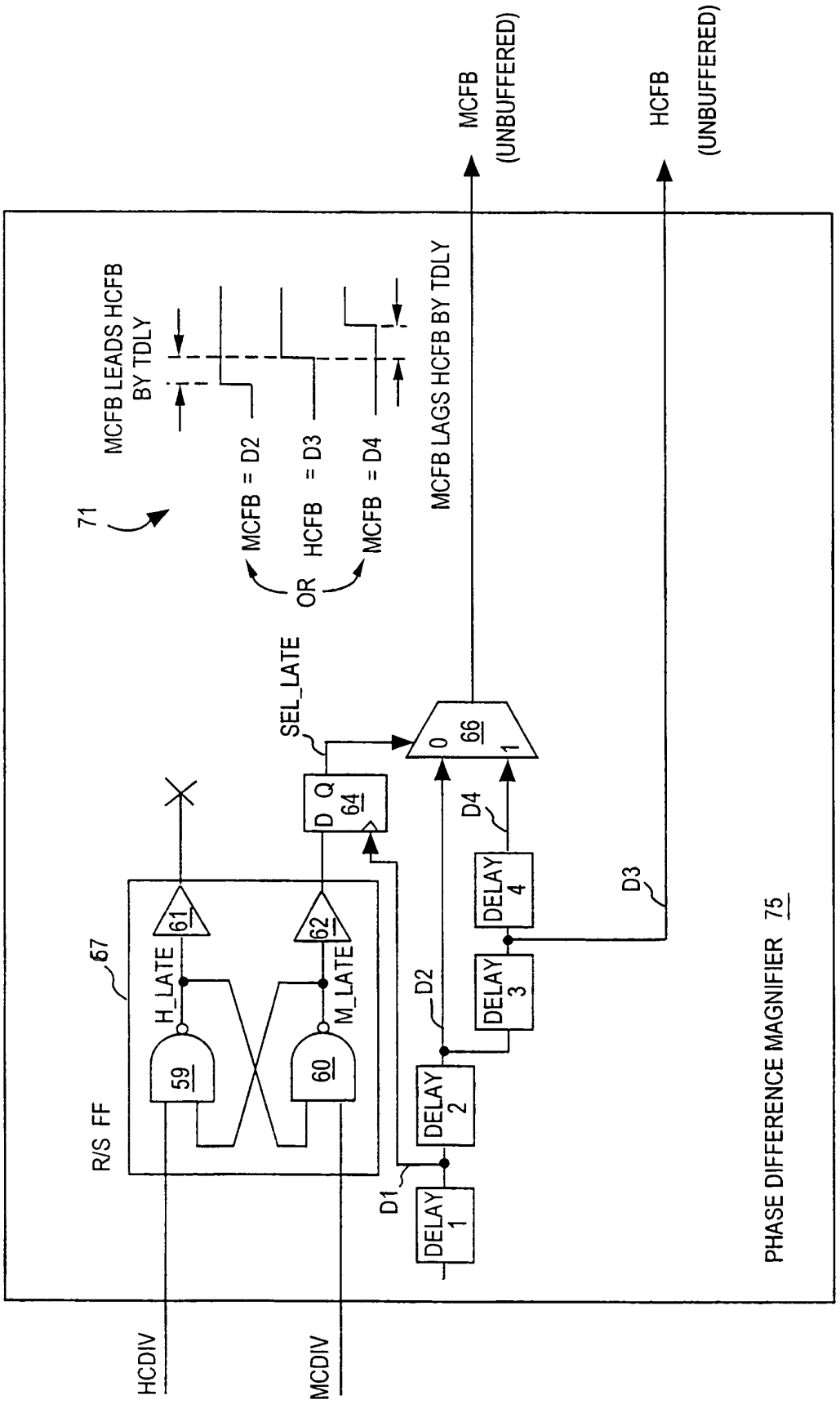
MCFB (UNBUFFERED)
HCFB (UNBUFFERED)
MCFB LEADS HCFB BY TDLY
MCFB LAGS HCFB BY TDLY
71
MCFB = D2
OR
HCFB = D3
MCFB = D4
SEL_LATE
D Q
64
0
66
1
D4
D3
DELAY 4
DELAY 3
D2
DELAY 2
D1
DELAY 1
67
R/S FF
H_LATE
M_LATE
61
62
59
60
HCDIV
MCDIV
PHASE DIFFERENCE MAGNIFIER 75

FIG.5

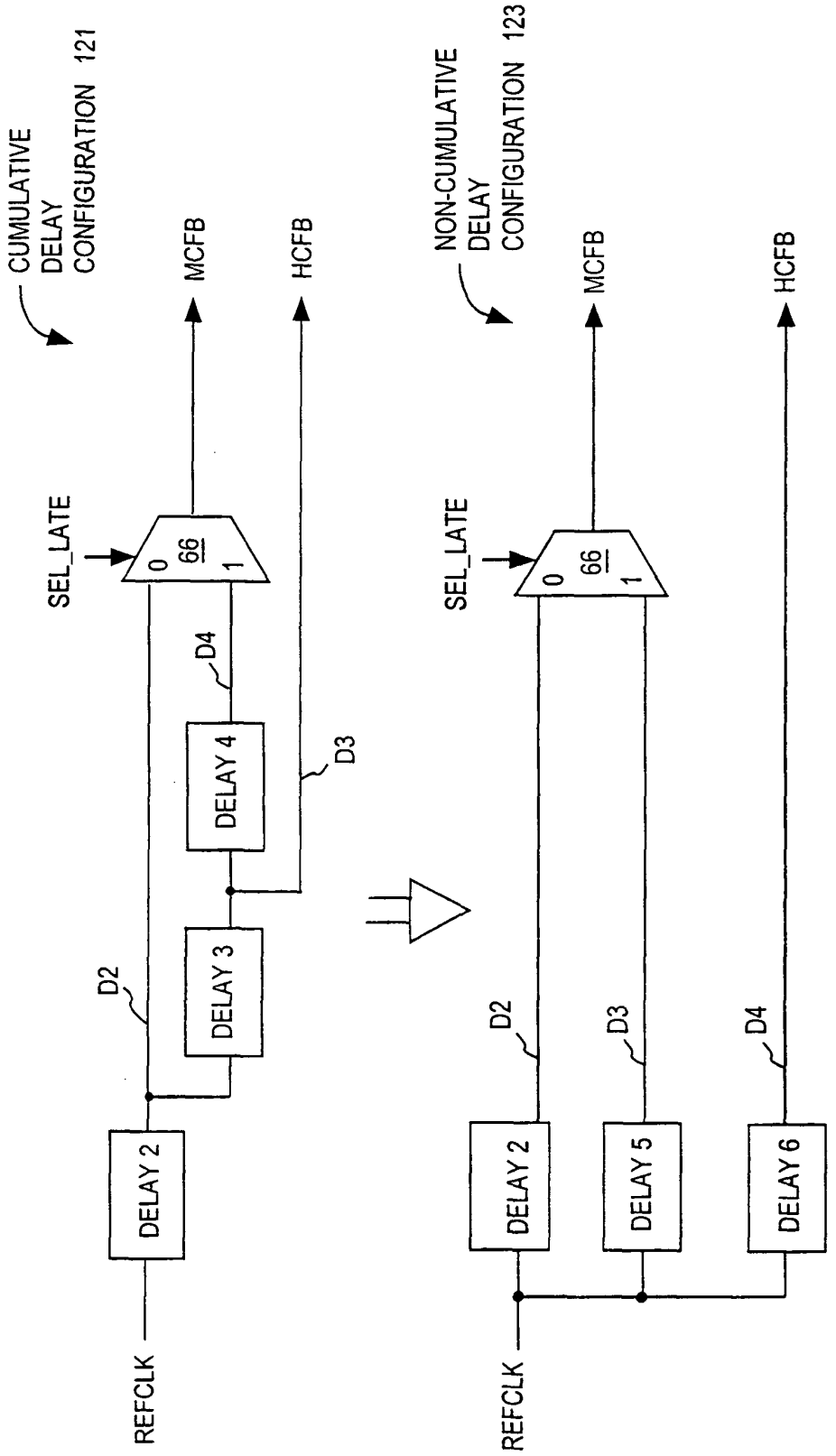
CUMULATIVE
DELAY
CONFIGURATION 121
SEL_LATE
0
66
1
MCFB
HCFB
D4
D3
D2
DELAY 4
DELAY 3
DELAY 2
REFCLK
NON-CUMULATIVE
DELAY
CONFIGURATION 123
SEL_LATE
0
66
1
MCFB
HCFB
D2
D3
D4
DELAY 2
DELAY 5
DELAY 6
REFCLK

FIG. 6