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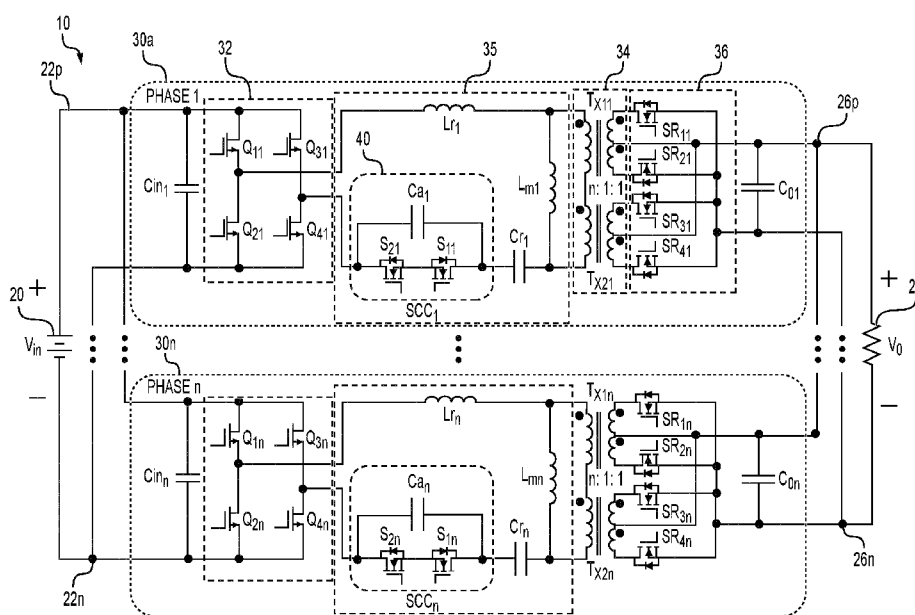


FIG. 1

(57) **Abstract:** A method for controlling a switch-controlled capacitor (SCC) in a resonant power converter includes: detecting a first zero crossing of a current through the SCC; determining a first predetermined time having elapsed after the first zero crossing; changing, after the first predetermined time after the first zero crossing, a switch of the SCC from a conducting state to a non-conducting state; detecting a second zero crossing of the current through the SCC; determining a second predetermined time having elapsed after the second zero crossing; and changing, after the second predetermined time after the second zero crossing, the switch of the SCC from the non-conducting state to the conducting state.



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SWITCH-CONTROLLED CAPACITOR WITH ASYMMETRICAL OPERATION

FIELD

The present disclosure relates generally to switch-controlled capacitors, such as those used in multi-phase inductor-inductor-capacitor (LLC) type power converters.

BACKGROUND

With advancements of power conversion technology and power electronics devices, high efficiency and high power density become a major challenge for front-end DC-DC converters. LLC resonant converter has been widely accepted in recent years by providing both high efficiency and high power density for numerous applications, such as servers, flat panel TVs, and LED lighting.

Increasing load demands call for high-power converters. For example, high power electronic converters may be used in Electric Vehicles (EVs) for charging a high-capacity high voltage battery (such as a battery with a nominal voltage of 250 V - 450 V) as well as a low voltage battery (such as a battery with a nominal voltage of 10 V - 16 V) that are installed on a typical EV. The high voltage battery may provide power to drive electric traction motors that move the vehicle. The high voltage battery may also be used to charge the low voltage battery that supplies numerous auxiliary loads of the EV. Hence, a high-power DC-DC converter with a wide input and output voltage range is needed to maintain the state of charge of the low voltage battery. The charging requirements for a low voltage battery charger can easily exceed two-hundred amperes (A), which can be challenging for a single-phase converter design. Multi-phase converters may be employed in this application for distributing current stress.

Resonant converters, such as inductor-inductor-capacitor (LLC) type resonant power converters, are used in various isolated DC-DC conversion applications due to their soft-

switching performance and ability to achieve high conversion efficiencies. They can achieve high conversion efficiencies at high power densities while dealing with minimal concern for low electromagnetic interferences. A major limitation of resonant converters is high component stress and conduction loss at high current applications. Hence, multi-phase resonant converters are commonly employed for high power and high current applications. The voltage gain of a resonant converter is highly sensitive to the impedance of the resonant tank and hence any small tolerance in the resonant tank components may cause severe load balancing between the paralleled resonant converters. Therefore, various different solutions for current sharing have been developed. There are two main methods for current sharing. One method uses passive current sharing, with no control on the current performance over the operating range. The other method uses active current sharing, which can actively control the current sharing for different operating conditions.

Various passive impedance matching (PIM) methods and automatic current sharing approaches have been developed for LLC resonant converters. PIM is an attractive approach as often no extra active or passive elements and/or control methods are required. However, the current balancing performance will deteriorate with large tolerances in resonant elements. Moreover, phase shedding may be employed in multiphase converters for light-load efficiency improvement, and it is not possible to be realized this with most of the passive current balancing approaches. A double-phase half-bridge LLC converter has been developed for EV application. The voltage gain difference between the phases is adjusted by using different switching frequencies for each phase, which prevents interleaving. An interleaved LLC converter may take advantage of phase shift control for controlling the voltage gain for current sharing purposes. The method can only be applied in a full-bridge topology, and it is not good for large tolerances as it introduces too much current stress due to large phase shifts for current balancing. A two-phase interleaved LLC converter utilizing duty-cycle adjustment of a higher current carrying phase to do the current balancing has been developed. The duty cycle in this converter control method cannot be reduced much without compromising efficiency. Although in all these active current sharing methods only new control methods are needed, each has its limitations and they are not so effective for wide input voltage range operation.

In some designs, current sharing between phases of a multiphase resonant converter may use a Switch-Controlled Capacitor (SCC) or a Switch-Controlled Inductor (SCI) in series with the resonant tank capacitor or inductor, respectively, to slightly alter the resonant tank impedance in order to compensate the voltage gain. This approach provides a precise current sharing between paralleled phases that can be applied to any number of phases with either half-bridge or full-bridge topology. The main limitation of this method is the additional component cost for each SCC/SCI circuit and the complexity of the current sharing control, which both are reliant on the number of paralleled phases. It should be mentioned that the additional circuitry does not add any switching losses to the original converter and there are only extra conduction losses via the added switching devices, which is not significant considering the rating of the switch. In one design, a full-wave SCC has been implemented in a three-phase LLC converter for wide input/output voltage applications.

SUMMARY

The present disclosure provides a method for controlling a switch-controlled capacitor (SCC) in a resonant power converter. The method includes: detecting a first zero crossing of a current through the SCC; determining a first predetermined time having elapsed after the first zero crossing; changing, after the first predetermined time after the first zero crossing, a switch of the SCC from a conducting state to a non-conducting state; detecting a second zero crossing of the current through the SCC; determining a second predetermined time having elapsed after the second zero crossing; and changing, after the second predetermined time after the second zero crossing, the switch of the SCC from the non-conducting state to the conducting state. The second predetermined time is different from the first predetermined time.

The present disclosure also provides a system for a resonant power converter. having. The system includes a switch-controlled capacitor (SCC). The SCC includes a capacitor and at least one switch configured to selectively conduct current to bypass the capacitor. The system also includes a controller. The controller is configured to: detect a first zero crossing of a current through the SCC; determine a first predetermined time having elapsed after the first zero crossing; change, after the first predetermined time after the

first zero crossing, the at least one switch from a conducting state to a non-conducting state; detect a second zero crossing of the current through the SCC; determine a second predetermined time having elapsed after the second zero crossing; and change, after the second predetermined time after the second zero crossing, the at least one switch from the non-conducting state to the conducting state. The second predetermined time is different from the first predetermined time.

BRIEF DESCRIPTION OF THE DRAWINGS

Further details, features and advantages of designs of the invention result from the following description of embodiment examples in reference to the associated drawings.

FIG. 1 shows a schematic diagram of a multi-phase LLC power converter with switch-controlled capacitors (SCC) in each of two phases;

FIG. 2 shows a controller for an LLC power converter, in accordance with some embodiments of the present disclosure;

FIG. 3 shows a schematic diagram of a full-wave SCC;

FIG. 4 shows a graph with plots of voltages and currents in the full-wave SCC circuit over a common time scale;

FIG. 5 shows a graph with plots of voltages and currents in the full-wave SCC circuit over a common time scale and with modified turn-on time, in accordance with some embodiments of the present disclosure;

FIG. 6 shows a graph with plots of voltages and currents in an LCC converter with an SCC, over a common time scale, in accordance with some embodiments of the present disclosure;

FIG. 7 shows a graph with plots of voltages and currents in an LCC converter with an SCC, over a common time scale, in accordance with some embodiments of the present disclosure;

FIG. 8 shows a graph with plots of voltages and currents in an LCC converter with an SCC, over a common time scale, in accordance with some embodiments of the present disclosure;

FIG. 9 shows a graph with plots of voltages and currents in an LCC converter with an SCC, over a common time scale, in accordance with some embodiments of the present disclosure;

FIG. 10 shows a graph with plots of voltages and currents in an LCC converter with an SCC, over a common time scale, in accordance with some embodiments of the present disclosure; and

FIG. 11 shows a flow chart of steps in a method for controlling a switch-controlled capacitor (SCC) in a resonant power converter, in accordance with some embodiments of the present disclosure.

DETAILED DESCRIPTION

Referring to the drawings, the present invention will be described in detail in view of following embodiments.

FIG. 1 shows a schematic diagram of a multi-phase LLC converter 10 with full-wave switch-controlled capacitor (SCC) and two transformers on each phase for high current applications. The main idea is to be able to tune the impedance of each LLC tank by modulating the resonant capacitance of each phase to compensate for the impedance mismatch caused by component tolerances. While the mentioned method is quite effective in balancing the three-phase current sharing, the design and control implementation are complex. Half-wave SCC have been implemented in an interleaved two-phase LCLC resonant converter for data center applications with a wide input voltage range. The SCC circuit has been used in both phases as because of component tolerances the voltage

gain of one phase is larger than the other one at minimum input voltage condition and it is vice versa at the maximum input voltage condition.

As shown in FIG. 1, a multi-phase LLC converter 10 may receive DC power from a DC source 20, such as a battery, and having an input voltage V_{in} via input conductors 22p, 22n. The multi-phase LLC converter 10 may supply output power to a load 24 via output conductors 26p, 26n. The output power may be supplied at an output voltage V_o , which may be higher than or lower than the input voltage V_{in} . The multi-phase LLC converter 10 includes a plurality of LLC phases 30a, 30n connected in parallel. The multi-phase LLC converter 10 of FIG. 1 includes two of the LLC phases 30a, 30n. However, a multi-phase LLC converter may include any number n of the LLC phases 30a, 30n, where n is a number greater than 1. Each of the LLC phases 30a, 30n may have a similar or identical construction. For the simplicity of the description, only one of the LLC phases 30a, 30n is described herein. The LLC phases 30a, 30n include a first LLC phase 30a, which may also be called Phase 1.

The first LLC phase 30a includes an input capacitor C_{in1} connected across the input conductors 22p, 22n. The first LLC phase 30a also includes an inverter stage 32 having a plurality of switching transistors Q_{11} , Q_{21} , Q_{31} , Q_{41} that function to switch an input power at an operating frequency to generate a switched power that approximates an alternating current (AC) waveform. The first LLC phase 30a also includes a transformer 34. The transformer 34 may include two or more transformers which may include series-connected primary windings for enhanced current carrying capability. The transformer 34 may have a 1:1 winding ratio and may provide electrical isolation between the input conductors 22p, 22n and the output conductors 26p, 26n. However, other configurations may be used, and the transformer 34 may have a different winding ratio to provide a step-up or a step-down conversion.

The first LLC phase 30a also includes a resonant tank 35 which includes a resonant inductor L_{r1} , a SCC circuit 40, a series capacitor C_{r1} , and a parallel inductance L_{m1} . In some embodiments, the parallel inductance L_{m1} is a physical device. Alternatively or additionally, the parallel inductance L_{m1} may represent inductance characteristics of the transformer 34. The SCC circuit 40 and the series capacitor C_{r1} are connected in series, with

the series combination of the SCC circuit 40 and the series capacitor C_{r1} together providing a resonant capacitance C_{r1} .

The SCC circuit 40 includes a switched capacitance C_{a1} connected in parallel with one or more switches S_{11} , S_{21} . The two or more switches S_{11} , S_{21} may include field-effect transistors (FETs), as shown in FIG. 1. However, other types of switching devices may be used, such as junction transistors. The two or more switches may be arranged to form a full-wave switch configured to selectively conduct current in either of two opposite polarities to bypass the switched capacitance C_{a1} . For example, the FETs may be arranged as shown in FIG. 1, in a back-to-back configuration, with each of their source terminals connected to a common node.

The first LLC phase 30a also includes a rectifier stage 36 connected to a secondary side of the transformer 34, opposite from the resonant tank 35 and configured to rectify AC power therefrom and to provide the DC output power on the output conductors 26p, 26n. The rectifier stage 36 may be configured as a synchronous rectifier including a plurality of transistors SR_{11} , SR_{21} , SR_{31} , SR_{41} . However, the rectifier stage 36 may have a different configuration and/or arrangement. The first LLC phase 30a also includes an output capacitor C_{o1} connected across the output conductors 26p, 26n to smooth ripples in the DC output power generated by the rectifier stage 36.

The present disclosure provides a system and method to tune the impedance of each resonant tank 35 by modulating the resonant capacitance of each phase to compensate for the impedance mismatch caused by component tolerances. In order to avoid MOSFET body diode conduction over the SCC operation, the gate signals in the full-wave SCC circuit 40 may be synchronized with the resonant current to reduce the conduction time.

The present disclosure provides a modified driving signal for the SCC MOSFET driving to avoid body diode conduction. In a wide input/output voltage design, the resonant converter tends to operate in a wide switching frequency range to achieve voltage regulation. At switching frequencies far away from the resonant frequency and with heavy load conditions the SCC capacitor voltage is not symmetrical anymore and hence a symmetrical SCC driving signal will not completely avoid body diode conduction. In this disclosure, an

adaptive asymmetrical SCC driving scheme is proposed to completely avoid body diode conduction. Hence, it is possible to reduce the conduction loss and improve the conversion efficiency.

FIG. 2 shows a controller 100 for the multi-phase LLC power converter 10. The controller 100 may control operation of the SCC circuits 40. For example, the controller 100 may generate gate driver signals for controlling conduction of one or more switches S_{11} , S_{21} in one or more of the SCC circuits 40. In some embodiments, the controller 100 may control other functions and/or components within the multi-phase LLC power converter 10, such as the inverter 32 and/or the rectifier stage 36. The controller 100 includes a processor 102 coupled to a storage memory 104. The storage memory 104 includes instruction storage 106 storing instructions, such as program code for execution by the processor 102. The storage memory 104 also includes data storage 108 for holding data for use by the processor 102. The data storage 108 may record, for example, values of the parameters measured by one or more sensors and/or the outcome of functions calculated by the processor 102.

Asymmetric Driving Signal for Switch-Controlled Capacitor (SCC)

The SCC circuit is shown in FIG. 3 and its operation is illustrated in FIG. 4. FIG. 3 shows the structure of the SCC circuit 40, which is configured as a full wave device, operable to switch current in either of two opposite directions, and which includes a switched capacitor C_a in parallel with the two MOSFETs SC1, SC2.

FIG. 4 is a graph 200 showing plots of voltages and currents in an LLC power converter over a common time scale. Graph 200 includes plot 202 having line 204 showing current I_{AB} , plot 206 having line 208 showing gate voltage V_{gs1} of SCC switch SC1, and plot 210 having line 212 showing gate voltage V_{gs2} of SCC switch SC2. The gate voltages V_{gs1} , V_{gs2} are driven between a high, or asserted state to cause the corresponding SCC switch SC1, SC2 to be in a conductive state (which may also be called “on”), and a low, or de-asserted state to cause the corresponding SCC switch SC1, SC2 to be in a non-conductive state (which may also be called “off”). Graph 200 also includes plot 214 having line

216 showing current I_{Ca} into the switched capacitor C_a , and plot 218 having line 219 showing voltage V_{Ca} across the switched capacitor C_a .

Assuming a sinusoidal current I_{AB} is passing through the SCC circuit from node A to node B as shown in FIG. 4, the current zero-crossing points are at angles $0, \pi, 2\pi, \dots$ etc. For a positive half cycle, S_1 is turned OFF at an angle of $2n\pi + \alpha$. After S_1 is turned OFF, the current flows from A to B via C_a and charges the capacitor until the next current zero-crossing point at $(2n+1)\pi$. Then, the current reverse direction, and begins to discharge the switched capacitor C_a . After the switched capacitor C_a is fully discharged, the negative current is about to flow from B to A via the body diode of S_1 . To prevent its body diode from conducting, S is turned ON. It remains ON for the rest of the cycle and turns OFF again at angle $(2n+2)\pi + \alpha$. Following the same procedure, S_2 controls the negative half cycle.

The SCC has an equivalent capacitance C_{SCC} , where the switch capacitor C_a is modulated by angle α , and can be expressed as equation (1):

$$C_{SCC} = \frac{C_a}{2 - \frac{(2\alpha - \sin(2\alpha))}{\pi}} \quad (1)$$

where C_a is the SCC capacitor. The equivalent resonant capacitance C_{r_eq} can be expressed as:

$$C_{r_eq} = \frac{C_{SCC}C_r}{C_{SCC} + C_r} \quad (2)$$

where C_r is the series resonant capacitor. Based on the above two equations, the equivalent resonant capacitance can be rewritten as:

$$C_{r_eq} = \frac{\pi C_a C_r}{\pi C_a + 2\pi C_r - 2\alpha C_r + C_r \sin(2\alpha)} \quad (3)$$

With the angle α varying from $\pi/2$ to π , the equivalent resonant capacitance C_{r_eq} changes from the minimum to the maximum. In extreme cases, when $\alpha = \pi/2$, current I_{AB} will flow

through C_a and bypass SCC MOSFETs. Thus, the equivalent resonant capacitance is at the minimum value which is equal to C_r and C_a connected in series. When $\alpha = \pi$, current I_{AB} will flow through SCC MOSFETs and bypass capacitor C_a , which makes the equivalent resonant capacitance toward its maximum value C_r . To have a continuous SCC operation and for safety reasons, a minimum and maximum operating angle is considered in practice.

There are three main operating stages in the resonant tank operation, the P stage which refers to the positive cycle power delivery, the N stage which refers to the negative cycle power delivery and the O stage which refers to the cut OFF stage where all the output rectifiers are OFF and no power is delivered to the load. When the resonant converter is operating far away from the resonant frequency while operating at heavy loads, the resonant capacitor voltage is not completely sinusoidal. The latter makes the SCC capacitor voltage asymmetrical leading to the SCC capacitor voltage dropping to zero earlier than expected and then as the drive signal of the SCC MOSFET is late its body diode starts to conduct. This problem is more pronounced in the below resonant operation region when the operation mode includes the O stage like PO and PON modes.

FIG. 5 shows a second graph 220 showing plots of voltages and currents in an LLC power converter over a common time scale. The second graph 220 includes plot 222 having line 224 showing current I_{AB} , plot 226 having line 228 showing gate voltage V_{gs1} of SCC switch SC1, and plot 230 having line 232 showing gate voltage V_{gs2} of SCC switch SC2. The gate voltages V_{gs1} , V_{gs2} are driven between a high, or asserted state to cause the corresponding SCC switch SC1, SC2 to be in a conductive state (which may also be called "on"), and a low, or de-asserted state to cause the corresponding SCC switch SC1, SC2 to be in a non-conductive state (which may also be called "off"). The second graph 220 also includes plot 234 having line 236 showing current I_{Ca} into the switched capacitor C_a , and plot 238 having line 239 showing voltage V_{Ca} across the switched capacitor C_a .

FIG. 5 illustrates the heavy load condition operation at frequencies far away from the resonant frequency. The resonant capacitor voltage and hence SCC capacitor voltage are asymmetrical around the resonant current zero-crossing points which can be observed in the bottom row of FIG. 5. To avoid MOSFET body diode conduction in both positive and

negative half-cycles. The rising edge of the driving signal of both SCC MOSFETs needs to be modified as illustrated in FIG. 5. The gray areas are showing body diode conduction time for respective MOSFETs if a symmetrical gate drive signal is used.

A computer simulation is done based on a 4 kW designed two-phase LLC converter with the SCC circuit. The operating range is from 280 V to 460 V and 14 V rated output voltage at 280 A output current.

FIG. 6 shows a third graph 240 with a plots 242, 246, 250, 254, 258 of voltages and currents in an LCC converter with an SCC circuit 40, over a common time scale. FIG. 6 illustrates steady-state simulation results with $V_{in}=260$ V, $V_o=14$ V at $I_o=100$ A. The third graph 240 includes a plot 242 with a line 244 showing current $I(L_r)$ through the resonant inductor L_r . The third graph 240 also includes a plot 246 with a line 248 showing a gate voltage (i.e. a control voltage) V_{g_SCC1} of a first switch in the SCC circuit 40. The third graph 240 also includes a plot 250 with a line 252 showing a gate voltage (i.e. a control voltage) V_{g_SCC2} of a second switch in the SCC circuit 40. The third graph 240 also includes a plot 254 with a line 256 showing an SCC capacitor voltage V_{Ca} across the switched capacitor C_a in the SCC circuit 40. The third graph 240 also includes a plot 258 with a line 259 showing a resonant capacitor voltage V_{Cr} across the series resonant capacitor C_r in the resonant tank 35.

The third graph 240 of FIG. 6 shows that the SCC capacitor voltage V_{Ca} drops to zero, and then the SCC MOSFETs (i.e. the switches S_{11} , S_{21} in the SCC circuit 40) are turned ON. Hence, the body diode of the SCC MOSFETs is conducted for a short time of 80 ns. In this condition, the resonant capacitor voltage is more sinusoidal.

FIG. 7 shows a fourth graph 260 with a plots 262, 266, 270, 274, 278 of voltages and currents in an LCC converter with an SCC circuit 40, over a common time scale. FIG. 7 illustrates the steady-state results of the same input and output voltage condition as shown in FIG. 6, but operated at 280 A rated current. The fourth graph 260 includes a plot 262 with a line 264 showing current $I(L_r)$ through the resonant inductor L_r . The fourth graph 260 also includes a plot 266 with a line 268 showing a gate voltage (i.e. a control voltage) V_{g_SCC1} of a first switch in the SCC circuit 40. The fourth graph 260 also includes a plot

270 with a line 272 showing a gate voltage (i.e. a control voltage) V_{g_SCC2} of a second switch in the SCC circuit 40. The fourth graph 260 also includes a plot 274 with a line 276 showing an SCC capacitor voltage V_{Ca} across the switched capacitor C_a in the SCC circuit 40. The fourth graph 260 also includes a plot 278 with a line 279 showing a resonant capacitor voltage V_{Cr} across the series resonant capacitor C_r in the resonant tank 35.

The fourth graph 260 of FIG. 7 shows the resonant capacitor voltage V_{Cr} in this condition is not completely sinusoidal which is why there is a phase shift in the SCC voltage making it asymmetrical. FIG. 7 shows that the body diode conduction is much longer in heavy load conditions and for a same voltage gain.

FIG. 8 shows a fifth graph 280 with a plots 282, 286, 290, 294, 298 of voltages and currents in an LCC converter with an SCC circuit 40, over a common time scale. FIG. 8 illustrates steady-state simulation results with $V_{in}=320$ V, $V_o=14$ V at $I_o=280$ A. The fifth graph 280 includes a plot 282 with a line 284 showing current $I(L_r)$ through the resonant inductor L_r . The fifth graph 280 also includes a plot 286 with a line 288 showing a gate voltage (i.e. a control voltage) V_{g_SCC1} of a first switch in the SCC circuit 40. The fifth graph 280 also includes a plot 290 with a line 292 showing a gate voltage (i.e. a control voltage) V_{g_SCC2} of a second switch in the SCC circuit 40. The fifth graph 280 also includes a plot 294 with a line 296 showing an SCC capacitor voltage V_{Ca} across the switched capacitor C_a in the SCC circuit 40. The fifth graph 280 also includes a plot 298 with a line 299 showing a resonant capacitor voltage V_{Cr} across the series resonant capacitor C_r in the resonant tank 35.

The fifth graph 280 of FIG. 8 shows that body diode conduction for this case is about 290 ns, which is considerably large.

FIG. 9 shows a sixth graph 300 with a plots 302, 306, 310, 314, 318 of voltages and currents in an LCC converter with an SCC circuit 40, over a common time scale. FIG. 9 illustrates the steady-state simulation results with $V_{in}=380$ V, $V_o=14$ V at $I_o=300$ A. The sixth graph 300 includes a plot 302 with a line 304 showing current $I(L_r)$ through the resonant inductor L_r . The sixth graph 300 also includes a plot 306 with a line 308 showing a gate voltage (i.e. a control voltage) V_{g_SCC1} of a first switch in the SCC circuit 40. The

sixth graph 300 also includes a plot 310 with a line 312 showing a gate voltage (i.e. a control voltage) V_{g_SCC2} of a second switch in the SCC circuit 40. The sixth graph 300 also includes a plot 314 with a line 316 showing an SCC capacitor voltage V_{Ca} across the switched capacitor C_a in the SCC circuit 40. The sixth graph 300 also includes a plot 318 with a line 319 showing a resonant capacitor voltage V_{Cr} across the series resonant capacitor C_r in the resonant tank 35.

The sixth graph 300 of FIG. 9 shows that the resonant capacitor voltage V_{Cr} becomes more sinusoidal, and hence the asymmetrical SCC capacitor voltage V_{Ca} become less severe as the switching frequency approaches the resonant frequency.

FIG. 10 shows a seventh graph 320 with a plots 322, 326, 330, 334, 338 of voltages and currents in an LCC converter with an SCC circuit 40, over a common time scale. FIG. 10 illustrates the steady-state simulation results with $V_{in}=460$ V, $V_o=14$ V at $I_o=280$ A. The seventh graph 320 includes a plot 322 with a line 324 showing current $I(L_r)$ through the resonant inductor L_r . The seventh graph 320 also includes a plot 326 with a line 328 showing a gate voltage (i.e. a control voltage) V_{g_SCC1} of a first switch in the SCC circuit 40. The seventh graph 320 also includes a plot 330 with a line 332 showing a gate voltage (i.e. a control voltage) V_{g_SCC2} of a second switch in the SCC circuit 40. The seventh graph 320 also includes a plot 334 with a line 336 showing an SCC capacitor voltage V_{Ca} across the switched capacitor C_a in the SCC circuit 40. The seventh graph 320 also includes a plot 338 with a line 339 showing a resonant capacitor voltage V_{Cr} across the series resonant capacitor C_r in the resonant tank 35.

The seventh graph 320 of FIG. 10 shows that operating near the resonant frequency, even with rated power, does not cause severe asymmetry of the SCC capacitor voltage V_{Ca} , as the resonant capacitor voltage V_{Cr} approximates a sinusoidal shape near the resonant frequency.

In order to avoid SCC MOSFET body diode conduction, an adaptive rising edge compensation is proposed to adjust the turn ON instant of the SCC MOSFETs based on the operating condition. A 3D look-up table may be used based on the switching frequency and load level to implement the adjusted rising edge for the gate of the SCC MOSFETs.

A method 400 for controlling a switch-controlled capacitor (SCC) in a resonant power converter is shown in the flow chart of FIG. 11. The method 400 can be performed by a control unit, such as the controller 100. In some embodiments, the method 400 may include the processor 102 executing instructions, which may be retrieved from the instruction storage 106, in order to cause the processor 102 to perform functions or steps of the method 400. As can be appreciated in light of the disclosure, the order of operation within the method is not limited to the sequential execution as illustrated in FIG. 11, but may be performed in one or more varying orders as applicable and in accordance with the present disclosure.

The method 400 includes detecting a first zero crossing of a current through the SCC at step 402. In some embodiments, the first zero crossing represents the current through the SCC (i.e. current I_{AB}) transitioning from a negative value to a positive value. For example, the processor 102 and/or other hardware and/or software may be configured to determine the first zero crossing of the current I_{AB} as shown by line 204 of FIG. 4, where the first zero crossing happens at time 0.

The method 400 also includes determining, at step 404, a first predetermined time having elapsed after the first zero crossing. For example, the the processor 102 and/or other hardware and/or software may be configured to wait for the first predetermined time after the first zero crossing. The first predetermined time may be shown as the first delay time α as shown on FIG. 4.

The method 400 also includes changing, at step 406, after the first predetermined time after the first zero crossing, a switch of the SCC from a conducting state to a non-conducting state. For example, the processor 102 and/or other hardware and/or software may be configured to de-assert a gate control signal after the first delay time α , as shown by the falling-edge of line 228 of plot 226 on FIG. 4.

The method 400 also includes detecting a second zero crossing of the current through the SCC at step 408. In some embodiments, the second zero crossing represents the current through the SCC (i.e. current I_{AB}) transitioning from a positive value to a negative value. For example, the processor 102 and/or other hardware and/or software may be configured

to determine the second zero crossing of the current I_{AB} as shown by line 204 of FIG. 4, where the first zero crossing happens at time π .

The method 400 also includes determining, at step 410, a second predetermined time having elapsed after the second zero crossing. For example, the the processor 102 and/or other hardware and/or software may be configured to wait for the second predetermined time after the second zero crossing. The second predetermined time may be shown as the second delay time β , as shown on FIG. 4.

The method 400 also includes changing, at step 412, after the second predetermined time after the second zero crossing, the switch of the SCC from the non-conducting state to the conducting state. For example, the processor 102 and/or other hardware and/or software may be configured to assert the gate control signal after the second delay time β , as shown by the rising-edge of line 228 of plot 226 on FIG. 4.

The second predetermined time may be different from the first predetermined time. For example, as illustrated on FIG. 4, the second predetermined time may be shorter than the first predetermined time.

In some embodiments similar control techniques and timing may be used for each of the two switches of the SCC circuit 40, as shown by plots 226 and 230, which respectively show the gate voltage V_{gs1} of SCC switch SC1, and the gate voltage V_{gs2} of SCC switch SC2. These gate voltages V_{gs1} V_{gs2} represent control signals that control conduction of the respective switches SC1, SC2 in the SCC circuit 40.

The system, methods and/or processes described above, and steps thereof, may be realized in hardware, software or any combination of hardware and software suitable for a particular application. The hardware may include a general purpose computer and/or dedicated computing device or specific computing device or particular aspect or component of a specific computing device. The processes may be realized in one or more microprocessors, microcontrollers, embedded microcontrollers, programmable digital signal processors or other programmable device, along with internal and/or external memory. The processes may also, or alternatively, be embodied in an application specific integrated

circuit, a programmable gate array, programmable array logic, or any other device or combination of devices that may be configured to process electronic signals. It will further be appreciated that one or more of the processes may be realized as a computer executable code capable of being executed on a machine readable medium.

The computer executable code may be created using a structured programming language such as C, an object oriented programming language such as C++, or any other high-level or low-level programming language (including assembly languages, hardware description languages, and database programming languages and technologies) that may be stored, compiled or interpreted to run on one of the above devices as well as heterogeneous combinations of processors processor architectures, or combinations of different hardware and software, or any other machine capable of executing program instructions.

Thus, in one aspect, each method described above and combinations thereof may be embodied in computer executable code that, when executing on one or more computing devices performs the steps thereof. In another aspect, the methods may be embodied in systems that perform the steps thereof, and may be distributed across devices in a number of ways, or all of the functionality may be integrated into a dedicated, standalone device or other hardware. In another aspect, the means for performing the steps associated with the processes described above may include any of the hardware and/or software described above. All such permutations and combinations are intended to fall within the scope of the present disclosure.

The foregoing description is not intended to be exhaustive or to limit the disclosure. Individual elements or features of a particular embodiment are generally not limited to that particular embodiment, but, where applicable, are interchangeable and can be used in a selected embodiment, even if not specifically shown or described. The same may also be varied in many ways. Such variations are not to be regarded as a departure from the disclosure, and all such modifications are intended to be included within the scope of the disclosure.

CLAIMS

1. A method for controlling a switch-controlled capacitor (SCC) in a resonant power converter, comprising:

detecting a first zero crossing of a current through the SCC;

determining a first predetermined time having elapsed after the first zero crossing;

changing, after the first predetermined time after the first zero crossing, a switch of the SCC from a conducting state to a non-conducting state;

detecting a second zero crossing of the current through the SCC;

determining a second predetermined time having elapsed after the second zero crossing; and

changing, after the second predetermined time after the second zero crossing, the switch of the SCC from the non-conducting state to the conducting state,

wherein the second predetermined time is different from the first predetermined time.

2. The method of Claim 1, wherein one of the first zero crossing and the second zero crossing represents the current through the SCC transitioning from a negative value to a positive value; and

wherein another one of the first zero crossing and the second zero crossing represents the current through the SCC transitioning from the positive value to the negative value.

3. The method of Claim 2, wherein the first zero crossing represents the current through the SCC transitioning from a negative value to a positive value, and the second zero crossing represents the current through the SCC transitioning from the positive value to the negative value.

4. The method of Claim 1, wherein the SCC is configured as a full-wave SCC circuit including a switched capacitor and a full-wave switch including the switch of the SCC and configured to selectively conduct current in either of two opposite directions to bypass the switched capacitor.

5. The method of Claim 4, wherein the full-wave switch includes a first switch configured to selectively conduct the current in a first direction, and the switch of the SCC includes a second switch configured to selectively conduct the current in a second direction opposite the first direction, and

wherein the switch of the SCC is one of the first switch or the second switch.

6. The method of Claim 5, wherein the switch of the SCC is the first switch, and the method further comprises:

determining the first predetermined time having elapsed after the second zero crossing;

changing, after the first predetermined time after the second zero crossing, the second switch of the SCC from a conducting state to a non-conducting state;

determining the second predetermined time having elapsed after the first zero crossing; and

changing, after the second predetermined time after the first zero crossing, the second switch of the SCC from the non-conducting state to the conducting state.

7. The method of Claim 1, further comprising determining at least one of the first predetermined time or the second predetermined time as a function of at least one of a switching frequency or a load level of the resonant power converter.

8. The method of Claim 7, wherein the at least one of the first predetermined time or the second predetermined time includes the second predetermined time.

9. The method of Claim 7, wherein determining the at least one of the first predetermined time or the second predetermined time includes determining the at least one of the first predetermined time or the second predetermined time as a function of both of the switching frequency and the load level of the resonant power converter.

10. The method of Claim 9, wherein determining the at least one of the first predetermined time or the second predetermined time as a function of both of the switching frequency and the load level of the resonant power converter includes using a 3-dimensional (3D) look-up table to determine the at least one of the first predetermined time or the second predetermined time.

11. A system for a resonant power converter, comprising:
a switch-controlled capacitor (SCC) including a capacitor and at least one switch configured to selectively conduct current to bypass the capacitor; and

a controller configured to:

- detect a first zero crossing of a current through the SCC;

- determine a first predetermined time having elapsed after the first zero crossing;

- change, after the first predetermined time after the first zero crossing, the at least one switch from a conducting state to a non-conducting state;

- detect a second zero crossing of the current through the SCC;

- determine a second predetermined time having elapsed after the second zero crossing; and

- change, after the second predetermined time after the second zero crossing, the at least one switch from the non-conducting state to the conducting state; and

wherein the second predetermined time is different from the first predetermined time.

12. The system of Claim 11, wherein one of the first zero crossing and the second zero crossing represents the current through the SCC transitioning from a negative value to a positive value; and

wherein another one of the first zero crossing and the second zero crossing represents the current through the SCC transitioning from the positive value to the negative value.

13. The system of Claim 12, wherein the first zero crossing represents the current through the SCC transitioning from a negative value to a positive value, and the second zero crossing represents the current through the SCC transitioning from the positive value to the negative value.

14. The system of Claim 11, wherein the at least one switch includes a full-wave switch configured to selectively conduct current in either of two opposite directions to bypass the capacitor.

15. The system of Claim 14, wherein the full-wave switch includes a first switch configured to selectively conduct the current in a first direction, and a second switch configured to selectively conduct the current in a second direction opposite the first direction.

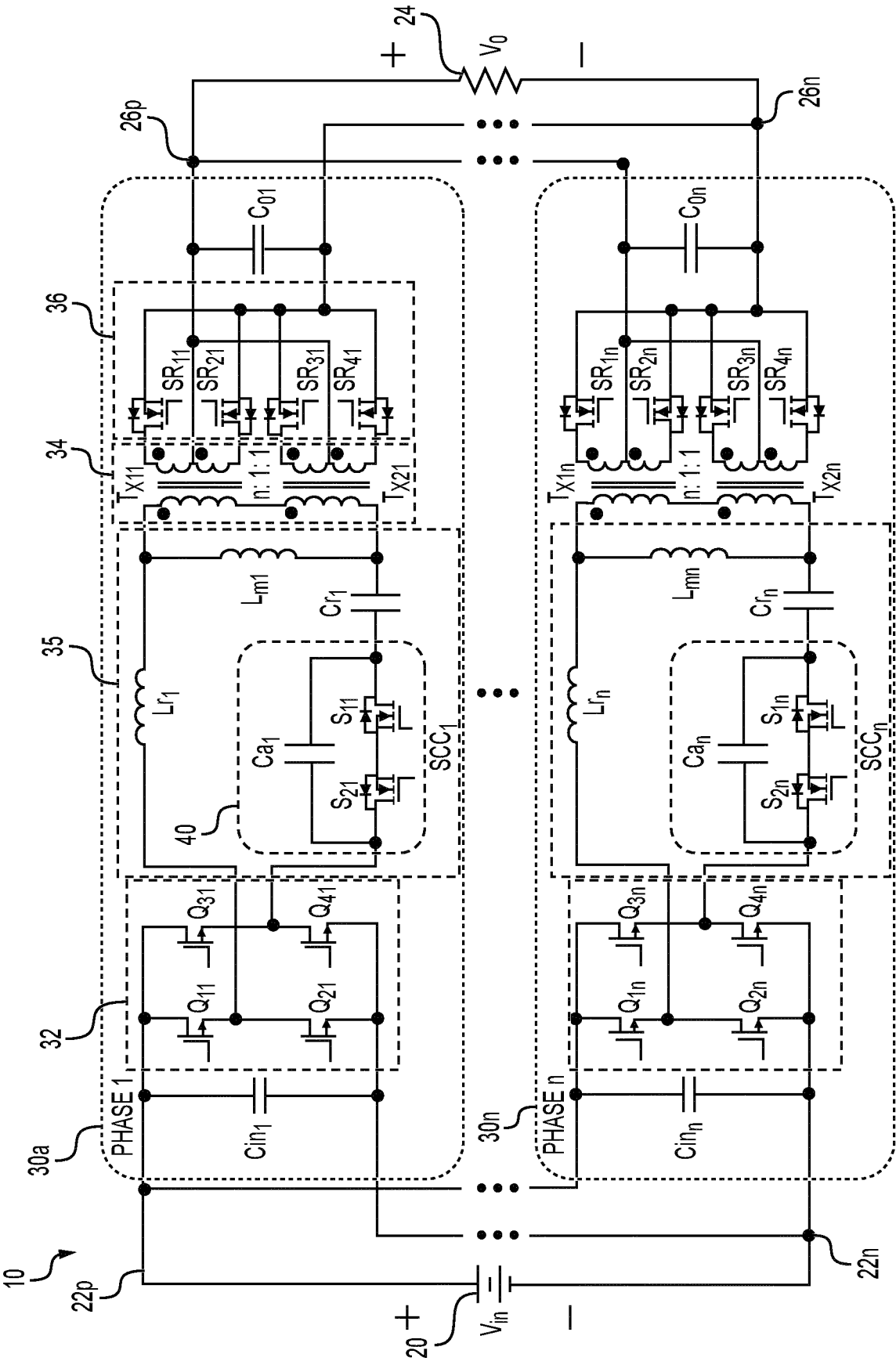


FIG. 1

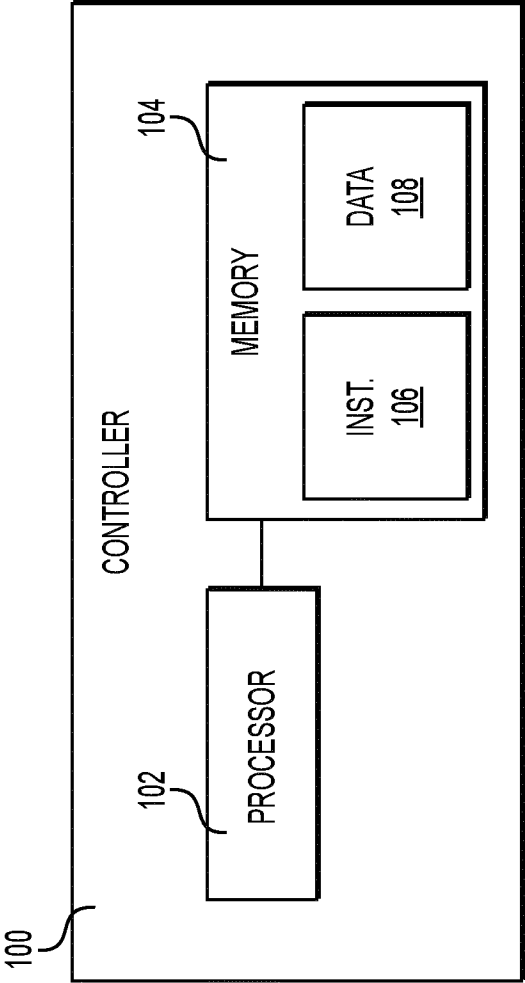


FIG. 2

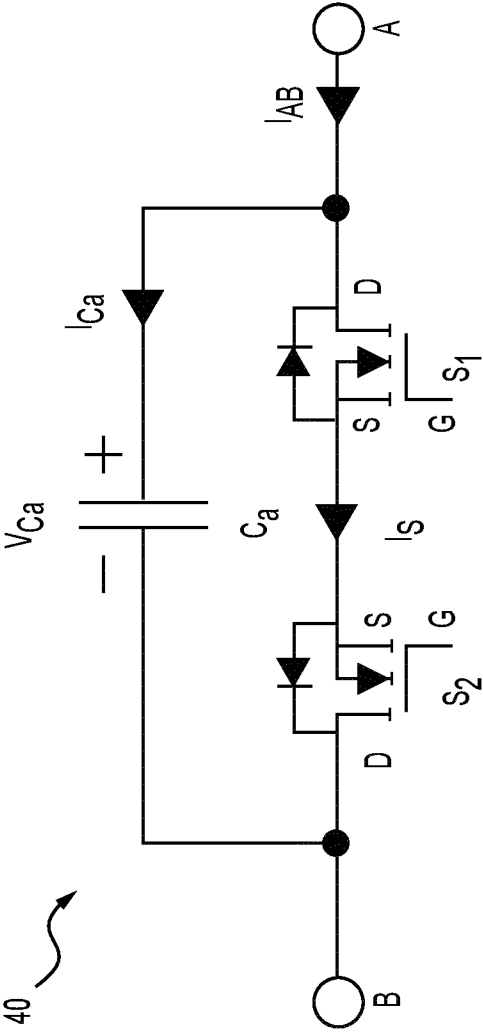


FIG. 3

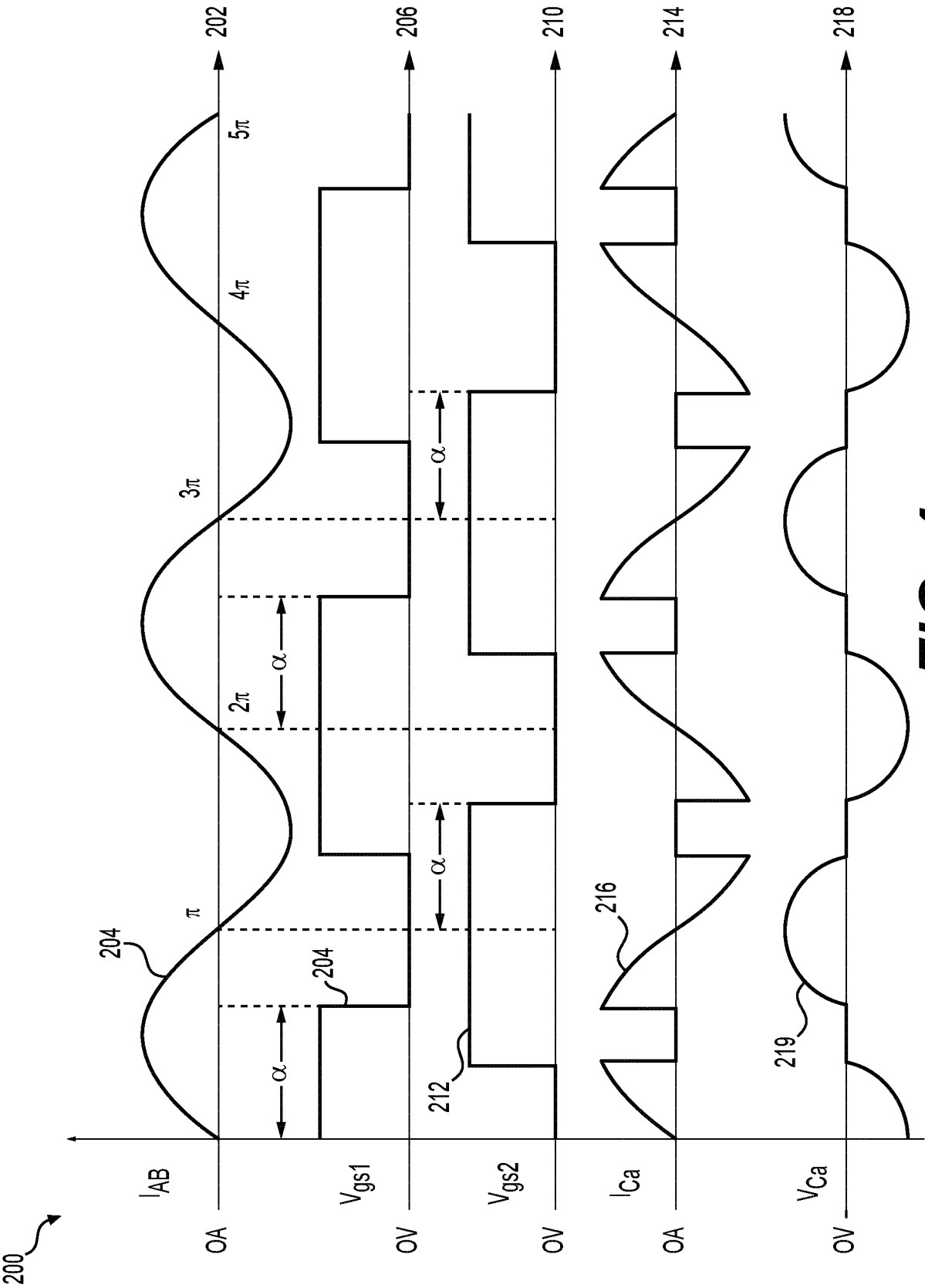


FIG. 4

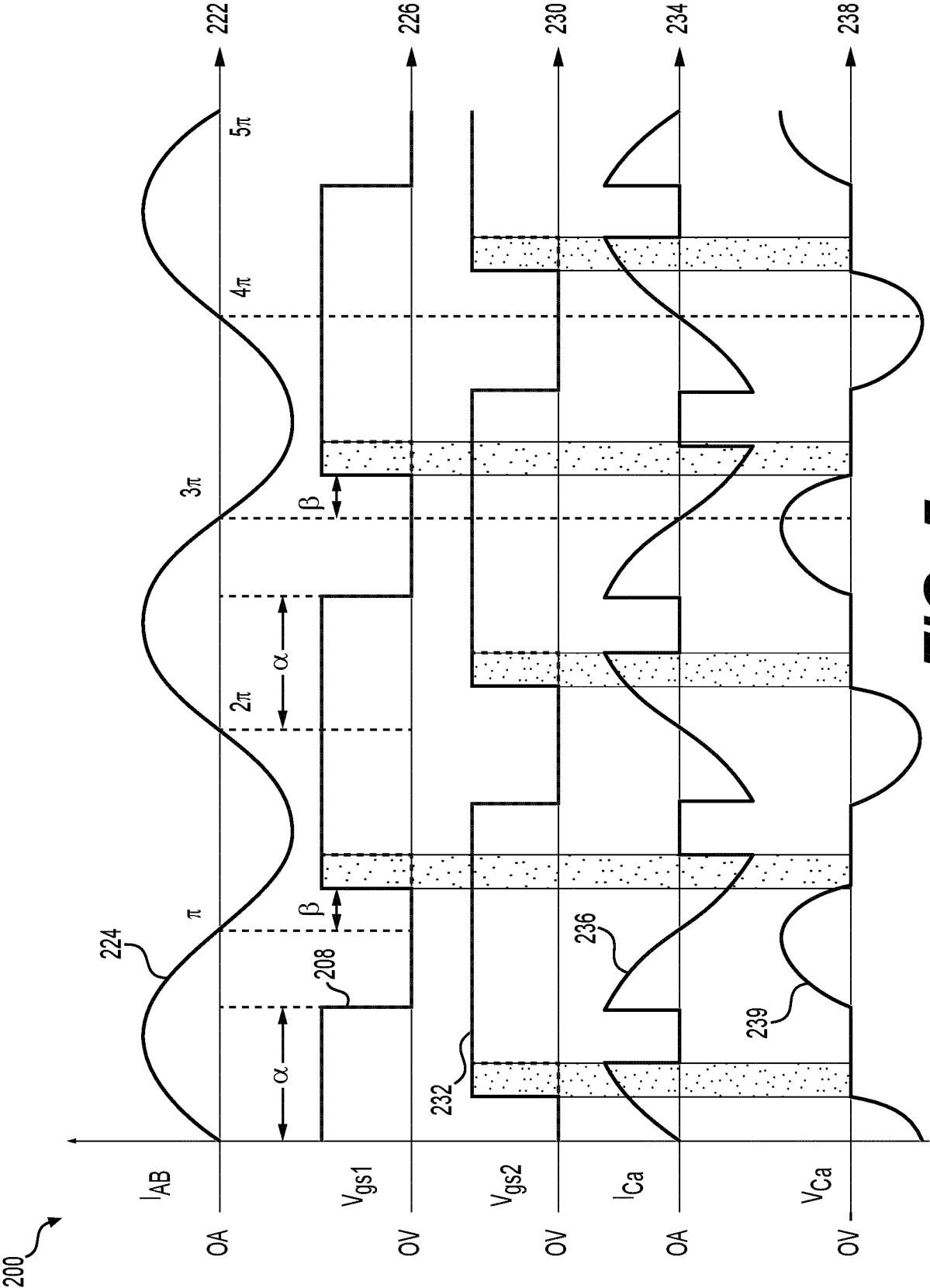


FIG. 5

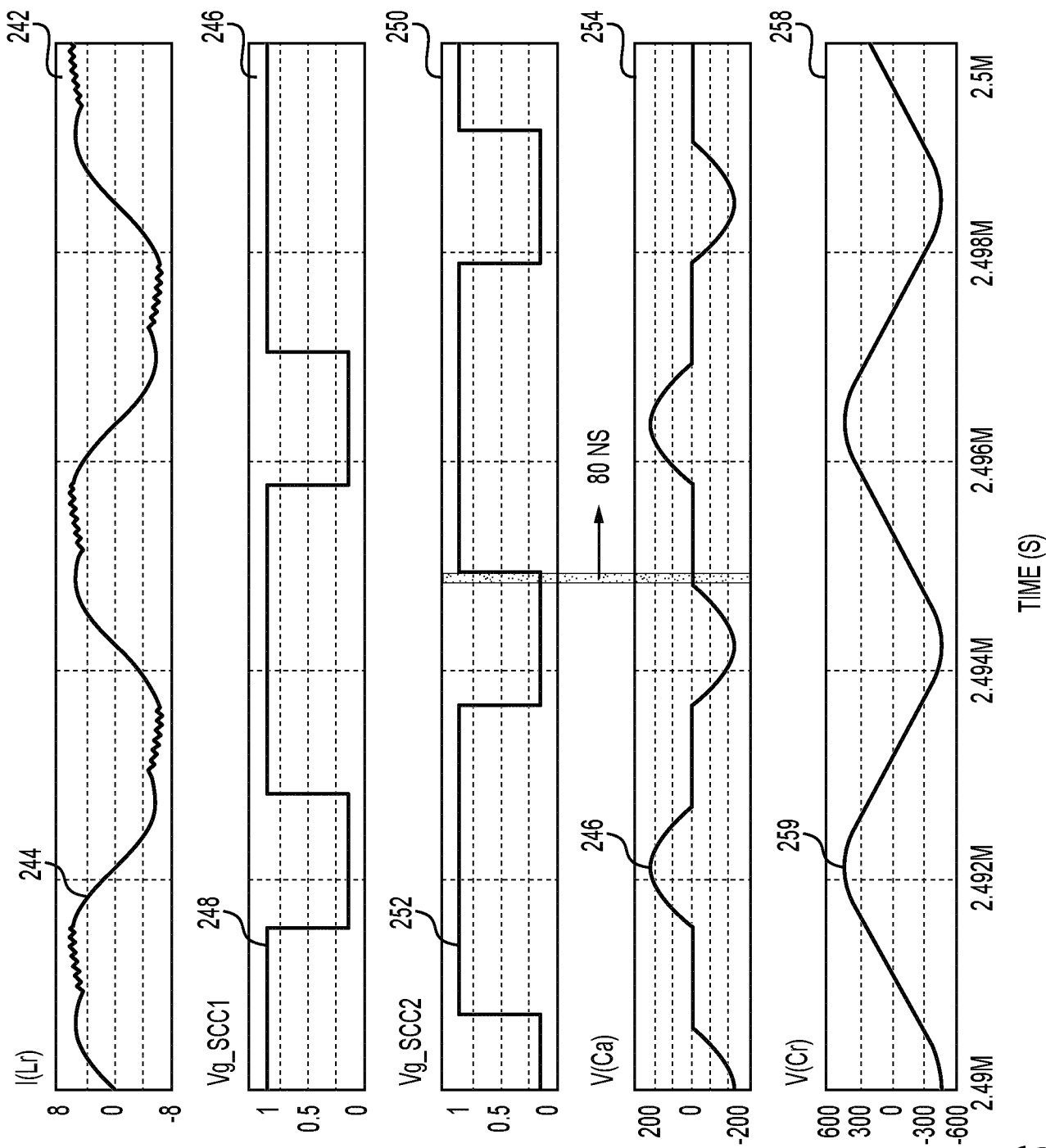


FIG. 6

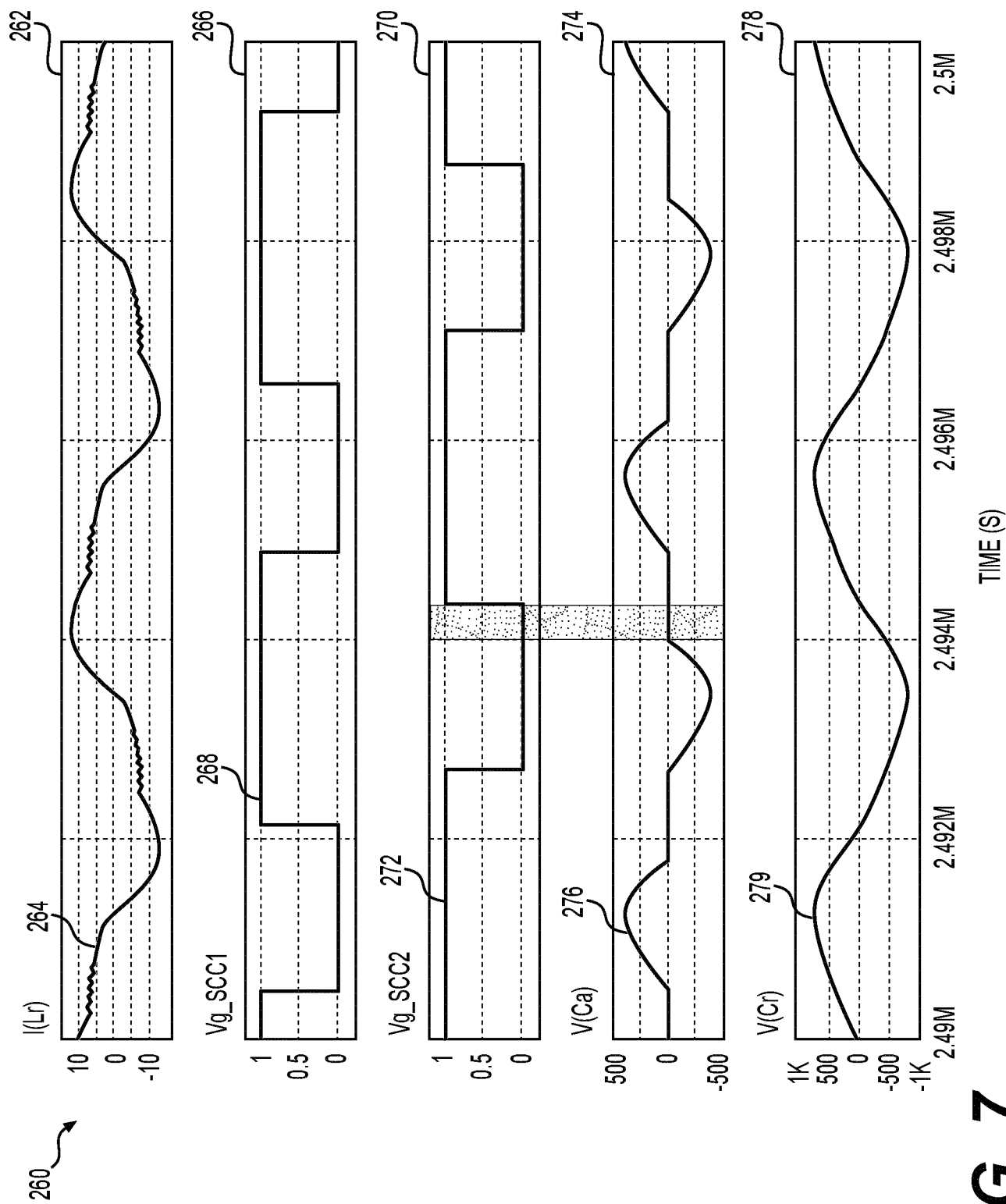


FIG. 7

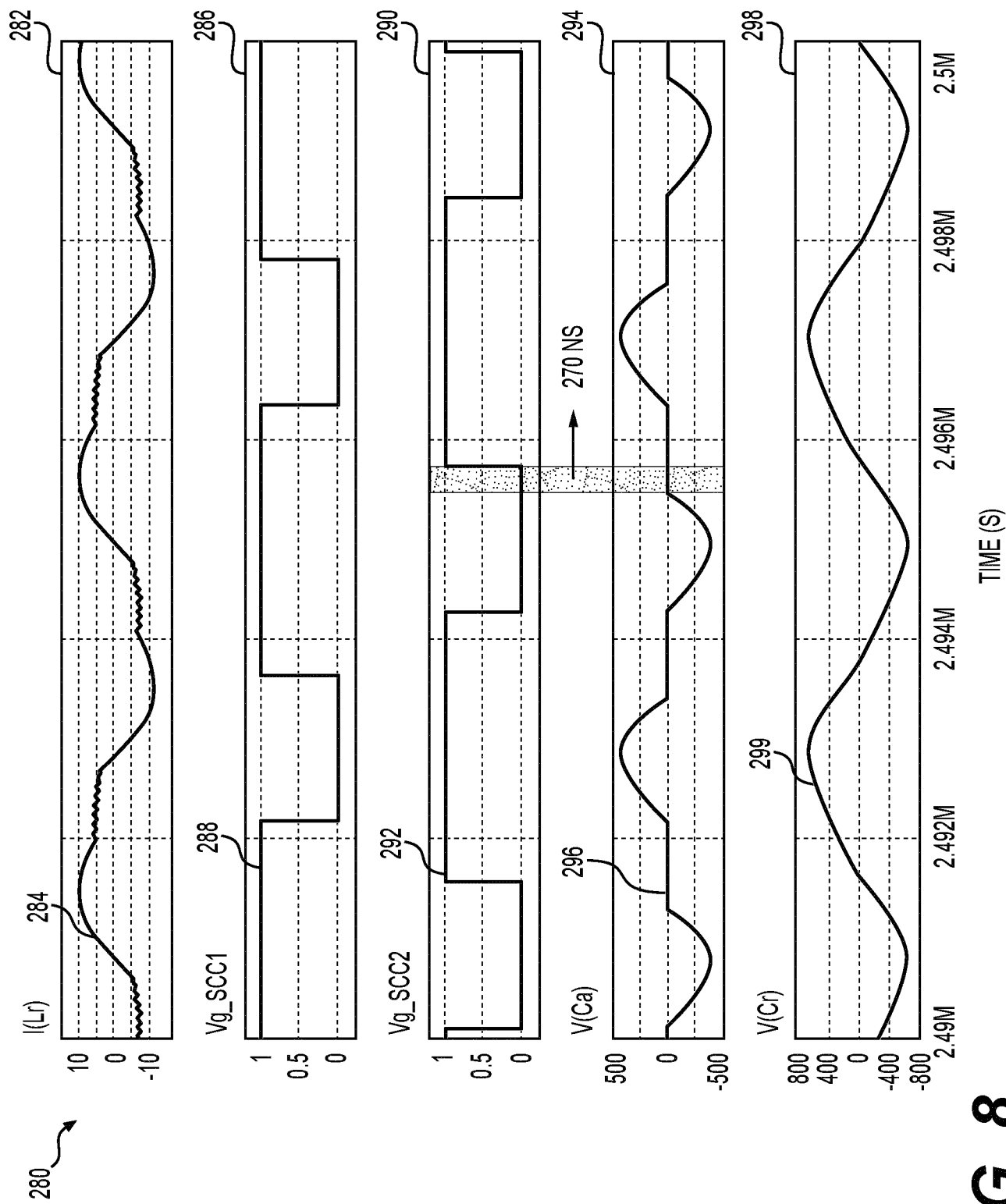


FIG. 8

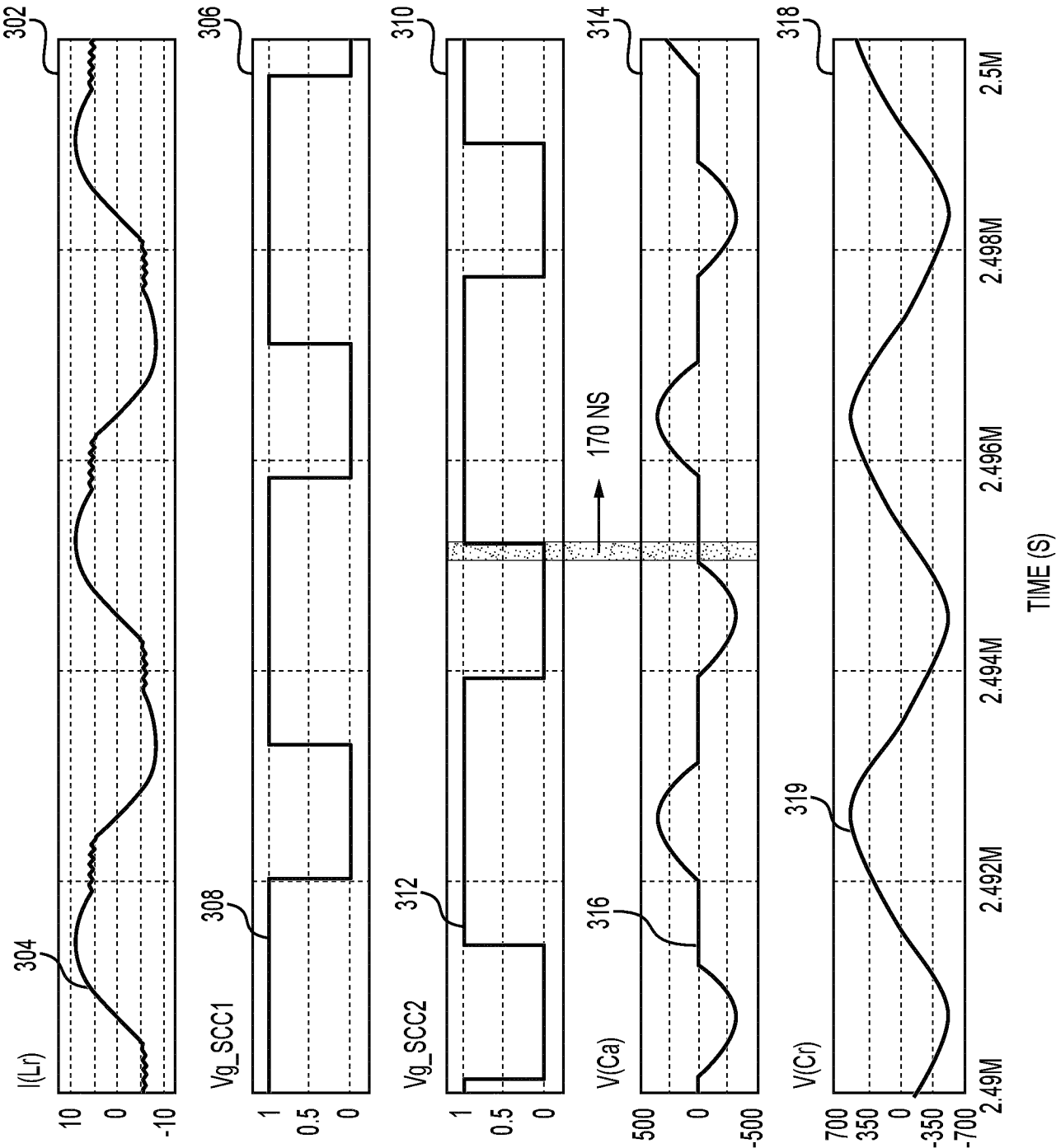


FIG. 9

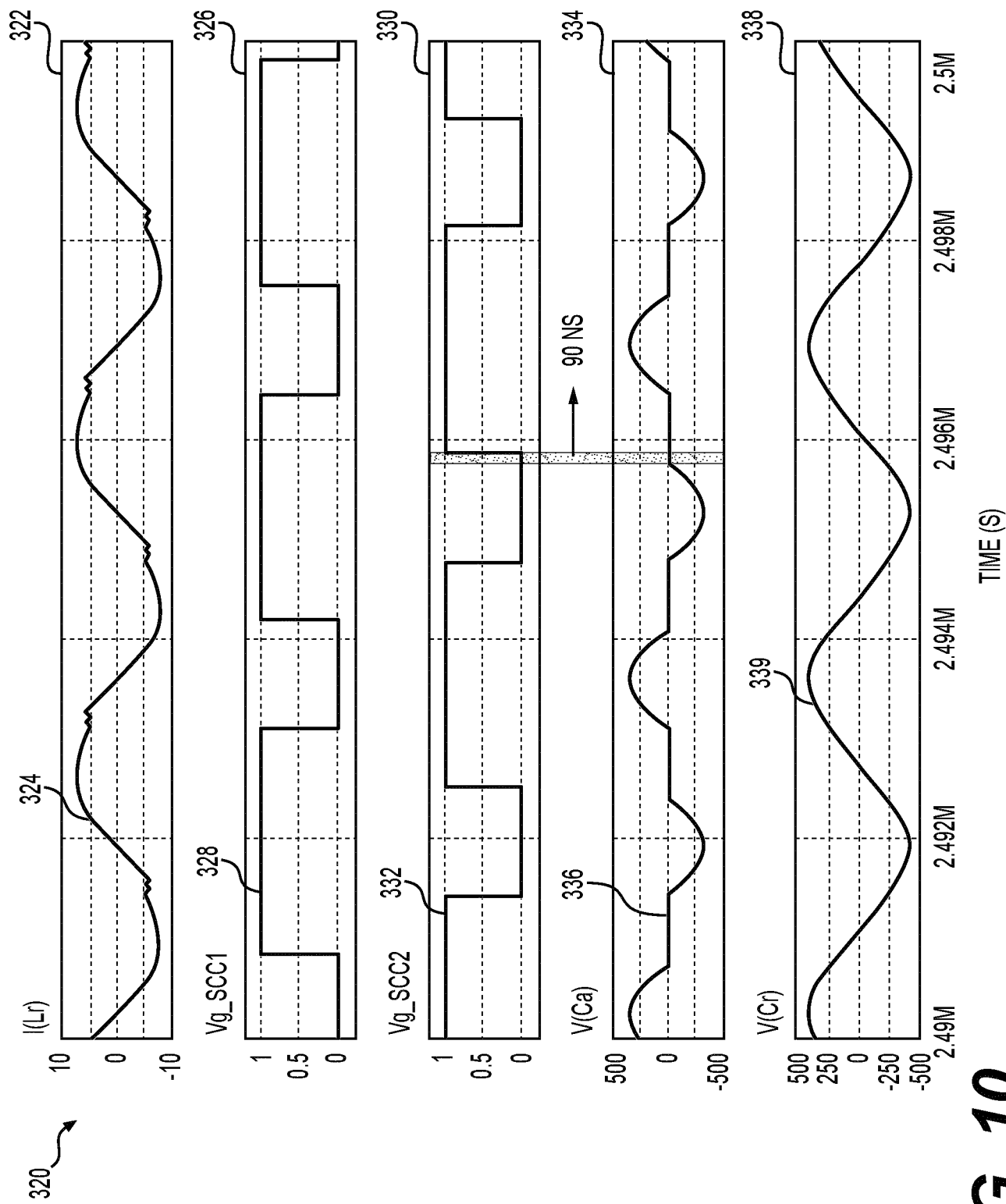


FIG. 10

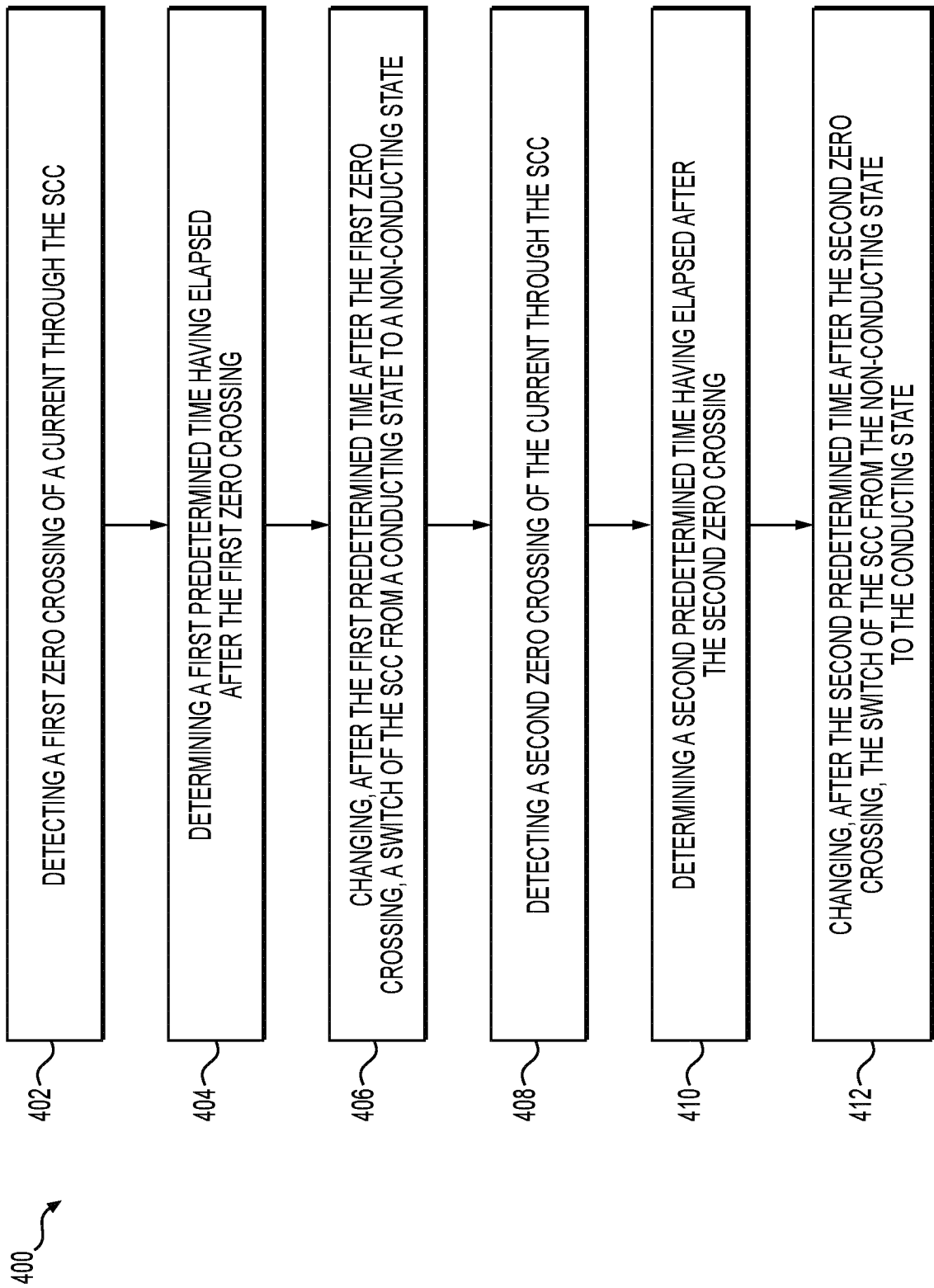


FIG. 11

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2023/069577

A. CLASSIFICATION OF SUBJECT MATTER		
INV.	H02M3/00	H02M7/48
	H02M3/335	H02M3/337
	H02M1/00	
ADD.		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) H02M		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EPO-Internal		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2022/103081 A1 (SHENG BO [CA] ET AL) 31 March 2022 (2022-03-31) paragraphs [0044], [0058]; figures 3-6, 8-11 ----- -/--	1-15
☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents : "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance;; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 9 October 2023		Date of mailing of the international search report 17/10/2023
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016		Authorized officer Kanelis, Konstantin

INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2023/069577

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	ZHOU XIANG ET AL: "A High-Efficiency High-Power-Density On-Board Low-Voltage DC-DC Converter for Electric Vehicles Application", IEEE TRANSACTIONS ON POWER ELECTRONICS, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, USA, vol. 36, no. 11, 30 April 2021 (2021-04-30), pages 12781-12794, XP011869781, ISSN: 0885-8993, DOI: 10.1109/TPEL.2021.3076773 [retrieved on 2021-07-26] abstract; figures 4,6,16,17 -----	1-15
X	LUO ZHICHAO ET AL: "A Self-Tuning LCC/LCC System Based on Switch-Controlled Capacitors for Constant-Power Wireless Electric Vehicle Charging", IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE SERVICE CENTER, PISCATAWAY, NJ, USA, vol. 70, no. 1, 28 February 2022 (2022-02-28), pages 709-720, XP011918222, ISSN: 0278-0046, DOI: 10.1109/TIE.2022.3153812 [retrieved on 2022-03-01] abstract; figures 1,7 -----	1-15

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2023/069577

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2022103081 A1	31-03-2022	CA 3125295 A1	30-07-2020
		CN 113330673 A	31-08-2021
		EP 3884574 A1	29-09-2021
		KR 20210117319 A	28-09-2021
		US 2022103081 A1	31-03-2022
		WO 2020154588 A1	30-07-2020
