(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
8 November 2007 (08.11.2007)

PCT

(10) International Publication Number
WO 2007/124769 A1

(51) International Patent Classification:
*H01L 23/31* (2006.01)

(21) International Application Number:
PCT/EP2006/003997

(22) International Filing Date: 28 April 2006 (28.04.2006)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant *(for all designated States except US)*: **TELEFONAKTIEBOLAGET LM ERICSSON (PUBL)** [SE/SE]; S-164 83 Stockholm (SE).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **LIGANDER, Per** [SE/SE]; Blåsutgatan 17, S-414 56 Göteborg (SE).

(74) Agent: **ALBIHNS GÖTEBORG AB**; Box 142, S-401 22 Göteborg (SE).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

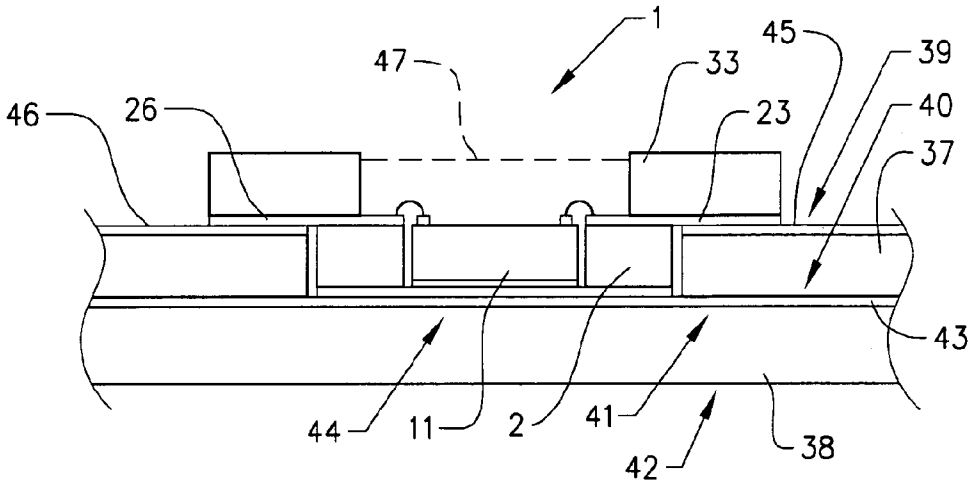
(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

**Declaration under Rule 4.17:**
— *of inventorship (Rule 4.17(iv))*

**Published:**
— *with international search report*

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

(54) **Title:** A MICROWAVE CHIP SUPPORTING STRUCTURE




(57) **Abstract:** The present invention relates to a microwave chip supporting structure (1, 1', 1") comprising a first microwave laminate layer (2, 49), with a first side (3, 50) and a second side (4, 51), and an outer limit (6, 7, 8, 9; 53, 54, 55, 56). At least one conductor (21, 22, 23, 24, 25, 26; 60, 61, 62, 63, 64, 65) is formed on said first side (3, 50), extending towards said outer limit (6, 7, 8, 9; 53, 54, 55, 56). The microwave chip supporting structure (1, 1', 1") further comprises a second microwave laminate layer (33, 33'; 57), with a first side (34, 58) and a second side (35, 59), the second side (35, 59) of the second laminate layer (33, 33', 57) being fixed to at least a part of the first side (3, 50) of the first laminate layer (2, 49). The first laminate layer (2, 49) and/or the second laminate layer (33, 33'; 57) comprises at least one recess (10, 36, 66) arranged for receiving a microwave chip (11, 67) intended to be connected to said conductor (21, 22, 23, 24, 25, 26; 60, 61, 62, 63, 64, 65). The second laminate layer (33, 57) extends outside the outer limit (6, 7, 8, 9; 53, 54, 55, 56) of the first laminate layer (2, 49), said conductors (21, 22, 23, 24, 25, 26; 60, 61, 62, 63, 64, 65) continuing on the second side (35, 59) of the second laminate layer (33, 57) without contacting the first laminate layer (2, 49).

WO 2007/124769 A1

TITLE

A microwave chip supporting structure

TECHNICAL FIELD

The present invention relates to a microwave chip supporting structure comprising a first microwave laminate layer, with a first side and a second side, the first microwave laminate layer having an outer limit, where further at least one conductor is formed on the first side of the first laminate layer, said conductor extending towards the outer limit of the first laminate layer.

BACKGROUND

In microwave technology, it has become technically feasible to integrate circuits in commercial packages for volume manufacturing and sale. Previously it was necessary to design a layout and mount discrete components on that layout, where a matching procedure often was necessary afterwards in order to tune the circuit. These packaged integrated microwave circuits thus make microwave design easier and cheaper than before.

A number of such packages have been developed during the last years. A package normally comprises a circuit with etched components on a silicon substrate, constituting a microwave chip. A package normally further comprises a carrier, for example in the form of a microwave laminate, to which the chip is fixed. The chip comprises connecting points, which are connected to connecting points on the laminate by means of bonding, using very thin gold wires. The laminate communicates its connecting points via a plurality of connectors, accessible for a user. The laminate and its chip are normally provided with a protective covering, for example an epoxy resin, a plastic cover shell, or both.

One such type of package is the so-called BGA (Ball Grid Array) package, which is an encapsulated circuit with a more or less complete MxN array of

connectors on its lower side, constituting a so-called footprint. The connectors are in the form of balls which stands out a certain distance from the package. A circuit board on which the package is to be mounted has a corresponding soldering pattern comprising corresponding soldering pads, matching the footprint - one pad for each ball-shaped connector on the package. An adhesive soldering paste is dispensed on each pad. The package is placed on the circuit board in such a way that the ball-shaped connectors contact the desired corresponding soldering pads. Then the circuit board is gently heated in such a way that the balls and the soldering paste melts, followed by cooling, where the pads and the connectors now are soldered together.

The solder joint more or less preserves its spherical shape, creating a stand-off between the package and the circuit board. This is, however, disadvantageous at higher frequencies, since this stand-off constitutes an inductance which is difficult to predict with sufficient accuracy.

Another type of package is called QFN (Quad Flat No lead) which is rectangular with connectors arranged at all four sides. The connectors do not extend out from the outline of the package, but extend at least partly along the lower side of the package. The chip is glued to a laminate, and its connecting points are connected to connecting points on the laminate by means of bonding, using very thin gold wires. The connecting points on the laminate are in turn connected to the connectors of the package by means of via holes that extend from the top of the laminate where its bond-connected connecting point is positioned, to the lower side of the laminate, where the connector is positioned.

This configuration is, however, disadvantageous since there are two inductances present for each connection; the bond wire and the via. The higher frequency, the more problematic do these inductances become for designing an accurate, repeatable construction.

One other type of package is called flip-chip, and comprises a chip of BGA type, but much more miniaturized. The chip is soldered as an ordinary BGA package to a laminate in order to constitute either a BGA package or a QFN package.

If it is a BGA package, there are problems with stand-off distances for the ball connectors at the chip as well as at the lower side of the laminate. There are also vias connecting between connecting points on the upper side of the laminate, and the ball connectors on the lower side of the laminate.

If it is a QFN package, there are problems with stand-off distances for the ball connectors at the chip and those vias connecting between connecting points on the upper side of the laminate, and the connectors on the lower side of the laminate.

As described in US 6011692, which is considered as closest prior art, a chip is bonded to connectors at a supporting element into which the chip is fastened. The bottom of the chip rests on a conductive foil. The supporting element is lowered into a recess in a circuit board with a ground plane. In the recess, the dielectrica of the circuit board is completely removed, allowing the lowered supporting element to rest on the conducting foil constituting the ground plane of the circuit board. In this way, the ground of the chip is easily connected to the circuit board ground. The connectors of the supporting element are connected to conductors at the circuit board via conductors, soldered or glued in place.

Although the known device functions in a satisfactory manner, there are certain aspects which can be improved, for example:

- A glue or solder has to be applied to the conductors on the supporting structure, and may interfere with the chip and/or bond wires.

- The transmission lines are broken by solder or glue joints at two places after the bond wires

- When mounting the supporting structure with its chip, the circuit board has to be brought through two runs in a pick-n-place machine and solder dispenser.

- The bond wires are unprotected if no lid is positioned over the supporting structure

- Should a lid be placed over the supporting structure, the lid will be in contact with the conductors

SUMMARY

It is an aim of the present invention to present a microwave chip supporting structure adapted for microwave frequencies, which microwave package overcomes the above disadvantages.

This aim is achieved by means of a microwave chip supporting structure as mentioned in the introduction, where furthermore the microwave chip supporting structure comprises a second microwave laminate layer, with a first side and a second side, the second laminate layer being fixed to the first laminate layer in such a way that the second side of the second laminate layer faces at least a part of the first side of the first laminate layer. The first laminate layer and/or the second laminate layer comprises at least one recess arranged for receiving a microwave chip intended to be connected to said conductor. The second laminate layer further extends outside the outer limit of the first laminate layer, said conductors continuing on the second side of the second laminate layer without contacting the first laminate layer.

Preferred embodiments are disclosed in the dependent claims.

Several advantages are achieved by means of the present invention, for example:

- no glue or solder has to be applied to the conductors on the supporting structure,

- the transmission lines are unbroken, and
- only one run in a pick-n-place machine and solder dispenser is necessary.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will now be described more in detail with reference to the appended drawing, where

Figure 1 shows a top view of a first embodiment of the present invention;

Figure 2 shows a section of the first embodiment of the present invention;

Figure 3 shows a section of the first embodiment of the present invention;

Figure 4 shows a section of a variety of the first embodiment of the present invention;

Figure 5 shows a section of a second embodiment of the present invention;

Figure 6 shows a top view of a third embodiment of the present invention; and

Figure 7 shows a section of the third embodiment of the present invention.

DETAILED DESCRIPTION

In Figure 1 and Figure 2, illustrating a first embodiment, a microwave chip supporting structure 1 is shown. Said supporting structure 1 comprises a first microwave laminate layer 2, for example a PTFE-based laminate, with a first side 3 and a second side 4, where a copper ground plane 5 is fixed to the second side 4. The first laminate layer 2 is limited by a first edge 6, a second edge 7, a third edge 8 and a fourth edge 9, the first laminate layer 2 being essentially rectangular. A first recess 10 is formed in the first laminate layer

2, where the first recess 10 is formed in such a way that a part of the copper ground plane 5 is forming an accessible surface, against which a microwave chip 11 is fixed by means of, for example, soldering or gluing. Such a chip 11 is normally constituted by a circuit with etched components on a silicon substrate. The chip 11 has a top side 12 and a bottom side 13, the bottom side 13 facing the ground plane. In that way, the chip's ground may be directly connected to the ground plane 5, since the chip's bottom side 13 has at least one ground connection 14. The chip 11 and the microwave chip supporting structure 1 together form a microwave package.

The chip 11 has connections 15, 16, 17, 18, 19, 20 on its top side 12, which connections 15, 16, 17, 18, 19, 20 are brought into contact with conductors 21, 22, 23, 24, 25, 26 formed on the first side 3 of the first laminate layer 2 by means of corresponding bonding wires 27, 28, 29, 30, 31, 32. The conductors 21, 22, 23, 24, 25, 26 extend towards the four edges 6, 7, 8, 9 of the first laminate layer 2.

According to the present invention, the supporting structure 1 further comprises a second microwave laminate layer 33, for example a PTFE-based laminate, with a first side 34 and a second side 35. The second laminate layer 33 is fixed to the first laminate layer 2 in such a way that the second side 35 of the second laminate layer 33 faces the first side 3 of the first laminate layer 2. The conductors 21, 22, 23, 24, 25, 26 are thus positioned between the first laminate layer 2 and the second laminate layer 33. A second recess 36 is formed in the second laminate layer 33, having essentially the same position as the first recess 10, but being larger in order to allow the bond wires 27, 28, 29, 30, 31, 32 to be connected to the conductors 21, 22, 23, 24, 25, 26.

The second laminate layer 33 further extends outside the four edges 6, 7, 8, 9 of the first laminate 2, the conductors 21, 22, 23, 24, 25, 26 continuing out from the first laminate layer 2 and continuing on the second side 35 of the

second laminate layer 33. The second laminate 33 layer thus carries the conductors 21, 22, 23, 24, 25, 26 out from the first laminate layer 2.

As shown in Figure 3, a first PCB (printed circuit board) 37 and a second PCB 38 is shown. The first PCB 37 has a first side 39 and a second side 40, and the second PCB 38 has a first side 41 and a second side 42. The first PCB 37 and the second PCB 38 are attached to each other in such a way that the second side 40 of the first PCB 37 and the first side 41 of the second PCB 41 face each other with a PCB ground plane 43 positioned between. In the first PCB 37, a third recess 44 is formed in such a way that a part of the PCB ground plane 43 is forming an accessible surface, against which the supporting structure 1 is fixed by means of, for example, soldering or gluing.

The first PCB 37 has a thickness that essentially is the same as the thickness of the first laminate layer 2, resulting in that the conductors 21, 22, 23, 24, 25, 26, when carried only by the second laminate 33, will rest on corresponding PCB conductors 45, 46. The connections between the conductors 21, 22, 23, 24, 25, 26 on the second laminate 33 and the PCB conductors 45, 46 are achieved by means of for example soldering or gluing.

In this way, each conducting path is only broken by one solder or glue joint after the respective bond wire 27, 28, 29, 30, 31, 32.

The chip 11 is now surrounded by the second laminate layer 33, which offers a protection for the chip 11. In order to achieve a more rigid protection of the chip, the second recess 36, formed in the second laminate layer 33, may be filled with a protective filler substance 47, such a s for example epoxy. Other examples of the protective filler substance 47 are a gel or a silicone compound.

According to a variety of the first embodiment, as shown in Figure 4, a cover 48 is placed on the first side 34 of the second laminate layer 33, covering the chip 11 without interfering with any conductors 23, 26. The cover 48 may for example be made in plastic, metal or a combination of both. The cover 48

may of course be combined with a protective filler substance as disclosed with reference to Figure 3. The shape of the cover 48 may vary, it may for example be arched or be constituted by a flat lid lying directly on the first side 34 of the second microwave laminate layer 33.

According to a second embodiment of the present invention, with reference to Figure 5, showing a microwave chip supporting structure 1', the second laminate layer 33' is not provided with a recess, but covers the chip 11. In this second embodiment, there are no bond wires, but the second laminate layer 33' carries the conductors 23, 26 partly into the first recess 10, enabling them to achieve a direct contact with the chip connections 17, 20, thus dispensing with the need for bond wires. In this way, the second laminate layer functions as:

- a first connecting means, between the chip connections and the conductors on the first side of the first laminate,
- a second connecting means, between the conductors on the first side of the first laminate and the PCB connections, and
- a cover for the chip.

The second embodiment corresponds to the first embodiment regarding all other features, and may of course be attached to a PCB in the same way as described for the first embodiment.

In Figure 6 and Figure 7, illustrating a third embodiment, a microwave chip supporting structure 1'' is shown. Said supporting structure 1'' comprises a first microwave laminate layer 49, for example a PTFE-based laminate, with a first side 50 and a second side 51, where a copper ground plane 52 is fixed to the second side 51. The first laminate layer 49 is limited by a first edge 53, a second edge 54, a third edge 55 and a fourth edge 56, the first laminate layer 49 being essentially rectangular.

The supporting structure 1" further comprises a second microwave laminate layer 57, for example a PTFE-based laminate, with a first side 58 and a second side 59. The second laminate layer 57 is fixed to the first laminate layer 49 in such a way that the second side 59 of the second laminate layer 57 faces the first side 50 of the first laminate layer 49. Conductors 60, 61, 62, 63, 64, 65 are formed between the first laminate layer 49 and the second laminate layer 57 in a similar way as described for the previous embodiments. The conductors 60, 61, 62, 63, 64, 65 are of the type CPW (co-planar waveguide), i.e. the conductors are surrounded by their corresponding ground plane G, separated from the ground plane by a small gap, in a way well known to the person skilled in the art.

A recess 66 is formed in the second laminate layer 57, being of such a form that a microwave chip 67 fits in the recess 66, the chip 67 having a top side 68 and a bottom side 69. The chip 67 is arranged to rest on the first side 50 of the first laminate layer 49 in such a way that connections 70, 71, 72, 73, 74, 75 on the bottom side 69 of the chip 67 are brought into contact with the conductors 60, 61, 62, 63, 64, 65 formed on the first side 50 of the first laminate layer 49.

The connections between conductors 60, 61, 62, 63, 64, 65 and the chip connections 70, 71, 72, 73, 74, 75 are in the form of ball connectors B which stand out a certain distance from the package. An adhesive soldering paste is dispensed on an appropriate spot at each conductor 60, 61, 62, 63, 64, 65 before the chip 67 is fitted in place. Then the circuit board is gently heated in such a way that the balls B and the soldering paste melts, followed by cooling, where the conductors 60, 61, 62, 63, 64, 65 and the chip connections 70, 71, 72, 73, 74, 75 now are soldered together.

The second laminate layer 57 further extends outside the four edges 53, 54, 55, 56 of the first laminate 49, the conductors 60, 61, 62, 63, 64, 65 continuing out from the first laminate layer 49 and continuing on the second side 59 of the second laminate layer 57. The second laminate 57 layer thus

carries the conductors 60, 61, 62, 63, 64, 65 out from the first laminate layer 49 in the same way as described for the previous embodiments.

The supporting structure 1'' according to the third embodiment may thus be attached to a PCB in the same way as described for the previous embodiments. The copper ground plane 52 may be used for soldering the supporting structure 1'' to the appropriate PCB, but is not necessary for any electric functions. If the supporting structure 1'' is glued to the appropriate PCB instead, the copper ground plane 52 may be omitted.

The ball connectors B of the third embodiment may be exchanged with any type of convenient connection means, for example gluing with conducting glue, the main idea of the third embodiment is to present a supporting structure 1'' to which it is possible to connect a chip 67 having both signal and ground connections on the same side of the chip 67, in this case the bottom side 69, allowing it to be connected to CPW conductors.

The recess 66 may be filled with a protective filler substance and/or covered with a protective cover as described for the first embodiment.

The invention is not limited to the embodiments described, but may vary freely within the scope of the appended claims. For example, the conductors 21, 22, 23, 24, 25, 26; 60, 61, 62, 63, 64, 65 on the first laminate layer 2; 49 extend towards at least one of the edges 6, 7, 8, 9; 53, 54, 55, 56 of the first laminate layer 2; 49. The second laminate layer 33, 33'; 57 extends a certain distance outside the at least one edge 6, 7, 8, 9; 53, 54, 55, 56 of the first laminate layer 2; 49, the conductors 21, 22, 23, 24, 25, 26; 60, 61, 62, 63, 64, 65 continuing out from the first laminate layer 2; 49 and continuing on the second side 35; 59 of the second laminate layer 33, 33'; 57. The second laminate layer 33, 33'; 57 preferably only extends outside those edges 6, 7, 8, 9; 53, 54, 55, 56 of the first laminate layer 2; 49 towards which the conductors 21, 22, 23, 24, 25, 26; 60, 61, 62, 63, 64, 65 of the first laminate layer 2; 49 extend.

The number of conductors on the first laminate layer 2; 49 is at least one.

The second laminate layer 33, 33'; 57 thus extends outside at least one edge 6, 7, 8, 9; 53, 54, 55, 56 of the first laminate layer 2; 49. The length of the extension, or extensions, should be appropriate to fulfil its connecting function.

The widths of the conductors should be adapted to achieve optimal performance, usually by adapting them to the characteristic impedance of the system. Such an adaptation must take into account whether the conductors run as microstrip, i.e. essentially on a supporting dielectric structure without any dielectrica on the other side, or as stripline, i.e. squeezed between two supporting structures. The same is valid if the conductors run in a CPW configuration.

The materials may also be chosen conveniently depending on performance and cost requirements, the materials mentioned herein are only mentioned as an example. The laminate layer may for example be formed using ceramics instead of PTFE. Furthermore, the copper ground planes may for example be formed in any suitable conducting material, for example gold.

The ground planes may furthermore be omitted if suitable, for example if other ground connections are available.

The shapes of the materials and the recesses may also vary in any way, the recess may be oval or circular, if that is more convenient due to manufacturing or chip structure. The edges 6, 7, 8, 9; 53, 54, 55, 56 may be arranged in any way, the function of the edges is to define an outer limit of the first laminate layer 2; 49.

The conductors on the PCB may be in the form of CPW for all embodiments.

CLAIMS

1. A microwave chip supporting structure (1, 1', 1") comprising a first microwave laminate layer (2, 49), with a first side (3, 50) and a second side (4, 51), the first microwave laminate layer (2, 49) having an outer limit (6, 7, 8, 9; 53, 54, 55, 56), where further at least one conductor (21, 22, 23, 24, 25, 26; 60, 61, 62, 63, 64, 65) is formed on the first side (3, 50) of the first laminate layer (2, 49), said conductor (21, 22, 23, 24, 25, 26; 60, 61, 62, 63, 64, 65) extending towards the outer limit (6, 7, 8, 9; 53, 54, 55, 56) of the first laminate layer (2, 49), characterized in that the microwave chip supporting structure (1, 1', 1") further comprises a second microwave laminate layer (33, 33'; 57), with a first side (34, 58) and a second side (35, 59), the second laminate layer (33, 33'; 57) being fixed to the first laminate layer (2, 49) in such a way that the second side (35, 59) of the second laminate layer (33, 33', 57) faces at least a part of the first side (3, 50) of the first laminate layer (2, 49), the first laminate layer (2, 49) and/or the second laminate layer (33, 33'; 57) comprising at least one recess (10, 36, 66) arranged for receiving a microwave chip (11, 67) intended to be connected to said conductor (21, 22, 23, 24, 25, 26; 60, 61, 62, 63, 64, 65), where the second laminate layer (33, 33'; 57) further extends outside the outer limit (6, 7, 8, 9; 53, 54, 55, 56) of the first laminate layer (2, 49), said conductors (21, 22, 23, 24, 25, 26; 60, 61, 62, 63, 64, 65) continuing on the second side (35, 59) of the second laminate layer (33, 57) without contacting the first laminate layer (2, 49).

2. A microwave chip supporting structure (1, 1') according to claim 1, characterized in that the first laminate layer (2) has a first recess (10), into which the microwave chip (11, 67) is inserted, the microwave chip (11, 67) having a top side (12) and a bottom side (13), the bottom side (13) facing an electrically conducting ground plane (5) that is fixed to the second side (4) of the first laminate layer (2), and the top side (12) being equipped with chip connections (15, 16, 17, 18, 19, 20), which chip connections (15,

16, 17, 18, 19, 20) are brought into contact with said conductors (21, 22, 23, 24, 25, 26).

3. A microwave chip supporting structure (1, 1') according to claim 2, characterized in that said bottom side (13) has at least one ground connection (14) which is electrically connected to said ground plane (5).

4. A microwave chip supporting structure (1) according to any one of the claims 2 or 3, characterized in that the second laminate layer (33) has a second recess (36), having essentially the same position as the first recess (10), but being larger, allowing the chip connections (15, 16, 17, 18, 19, 20) to be brought into contact with said conductors (21, 22, 23, 24, 25, 26) by means of bond wires (27, 28, 29, 30, 31, 32).

5. A microwave chip supporting structure (1) according to claim 4, characterized in that the second recess (36) is filled with a protective filler substance (47).

6. A microwave chip supporting structure (1) according to any one of the claims 4 or 5, characterized in that a cover (48) is placed on the first side (34) of the second laminate layer (33), covering the chip (11).

7. A microwave chip supporting structure (1') according to any one of the claims 2 or 3, characterized in that the second laminate layer (33') covers the microwave chip (11), carrying the conductors (21, 22, 23, 24, 25, 26) partly into the first recess 10, enabling them to achieve a direct contact with the chip connections (15, 16, 17, 18, 19, 20).

8. A microwave chip supporting structure (1") according to claim 1, characterized in that the second laminate layer (57) has a recess (66) arranged to receive the microwave chip (67), the microwave chip (67) having a top side (68) and a bottom side (69), where the chip (67) is arranged to rest on the first side (50) of the first laminate layer (49) in such a

way that connections (70, 71, 72, 73, 74, 75) on the bottom side (69) of the chip (67) are brought into contact with the conductors (60, 61, 62, 63, 64, 65) formed on the first side (50) of the first laminate layer (49).

9. A microwave chip supporting structure (1") according to claim 8, characterized in that the connections between conductors (60, 61, 62, 63, 64, 65) and the chip connections (70, 71, 72, 73, 74, 75) are in the form of ball connectors (B).

10. A microwave chip supporting structure (1") according to any one of the claims 8 or 9, characterized in that the recess (66) is filled with a protective filler substance.

11. A microwave chip supporting structure (1") according to any one of the claims 8-10, characterized in that a cover is placed on the first side (58) of the second laminate layer (59), covering the microwave chip (67).

12. A microwave chip supporting structure (1, 1', 1") according to any one of the previous claims, characterized in that it is arranged for being placed in a recess (44) formed in a first PCB (Printed Circuit Board) (37), the first PCB (37) being attached to a second PCB (38) in such a way that a second side (40) of the first PCB (37) and a first side (41) of the second PCB (41) face each other with a PCB ground plane (43) positioned between them.

13. A microwave chip supporting structure (1, 1', 1") according to claim 12, characterized in that that a part of the PCB ground plane (43) is forming an accessible surface via the recess (44), against which the supporting structure (1, 1', 1"') may be fixed.

14. A microwave chip supporting structure (1, 1', 1") according to any one of the claims 12 or 13, characterized in that the first PCB (37) has a thickness that essentially is the same as the thickness of the first

laminate layer (2, 49), resulting in that said conductors (21, 22, 23, 24, 25, 26; 60, 61, 62, 63, 64, 65), when carried only by the second laminate layer (33, 33'; 57), will rest on corresponding PCB conductors (45, 46), enabling an electrical connection between said conductors (21, 22, 23, 24, 25, 26; 60, 61, 62, 63, 64, 65) on the second laminate 33 and the PCB conductors (45, 46).

15. A microwave chip supporting structure (1, 1', 1") according to any one of the claims 12-14, characterized in that the PCB conductors (45, 46) are in the form of CPW (Co-Planar Waveguide).

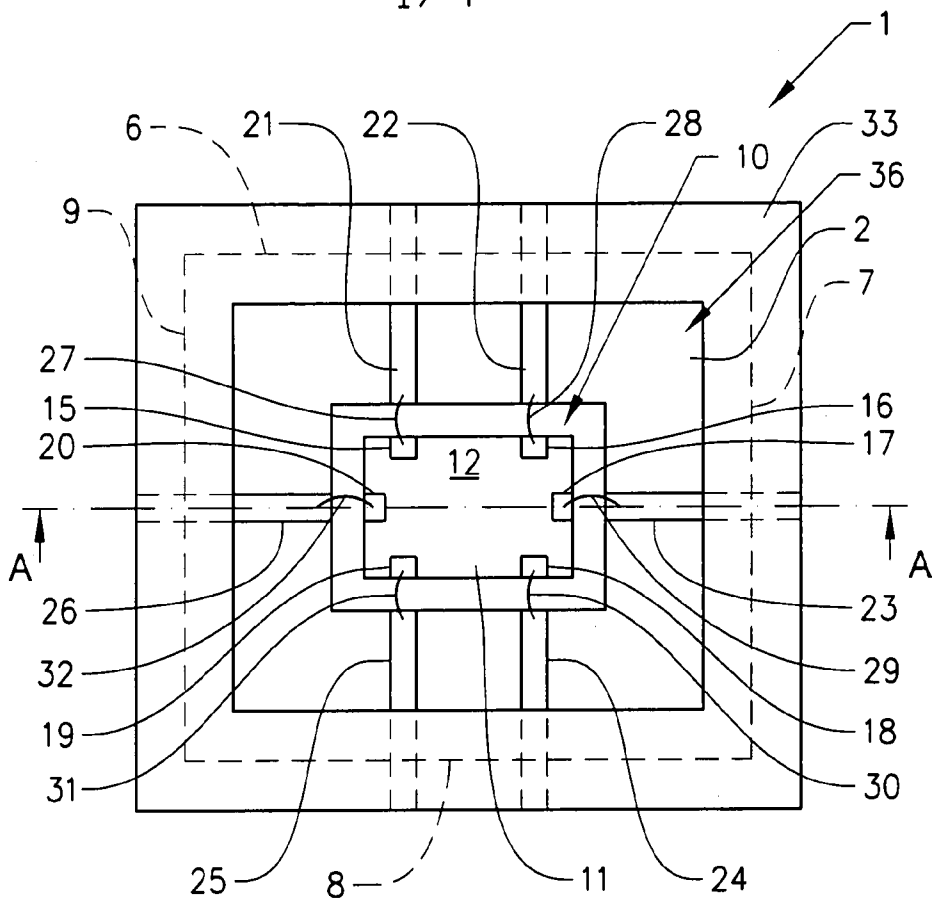
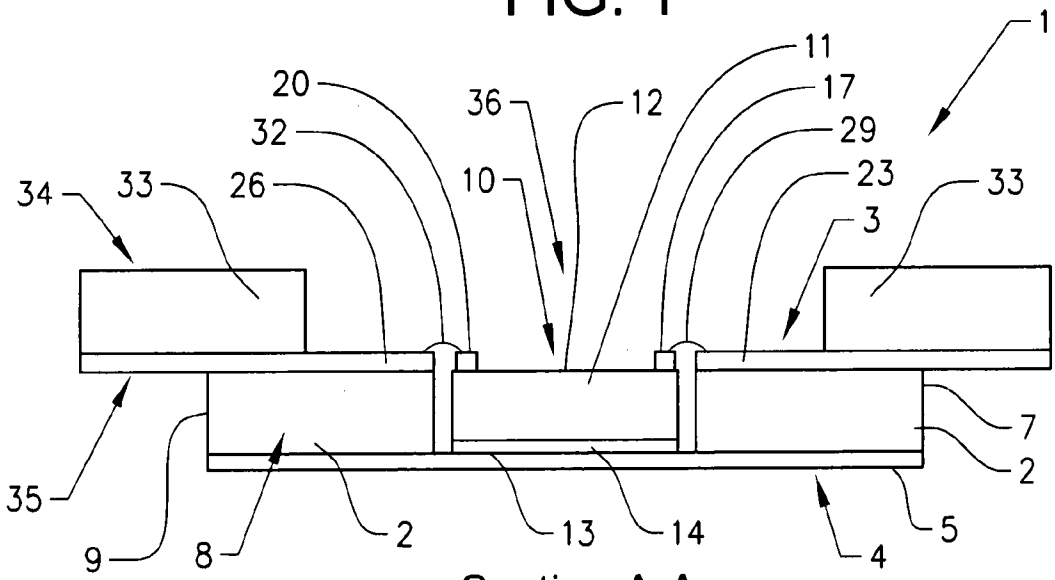



FIG. 1




Section A-A

FIG. 2

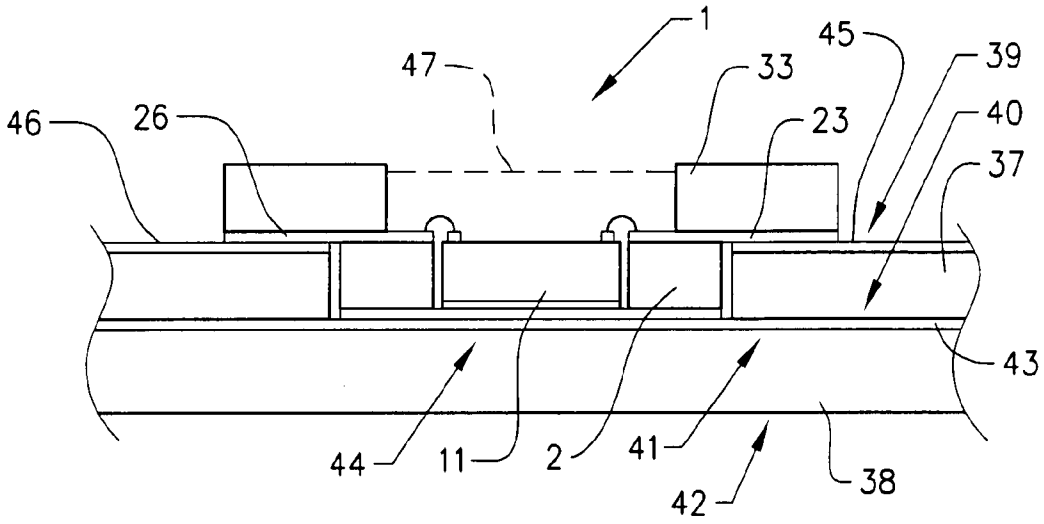



FIG. 3

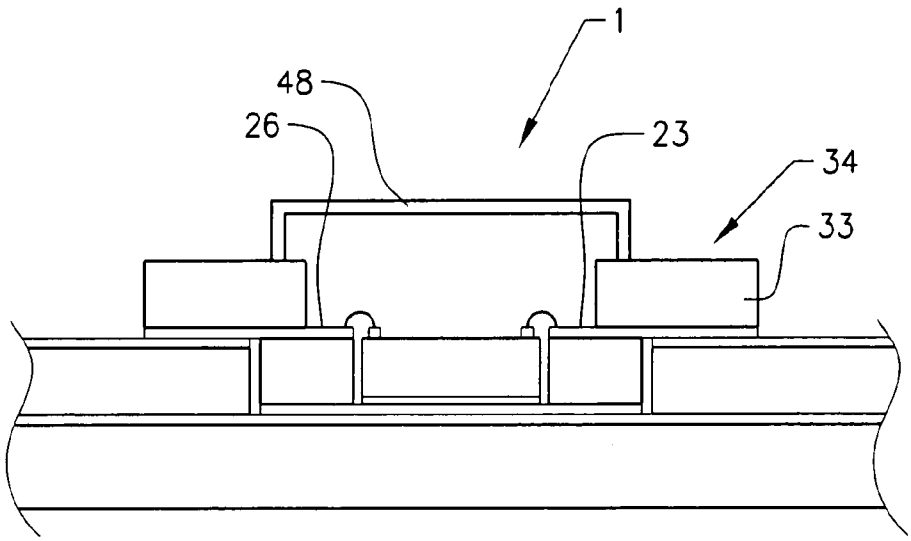



FIG. 4

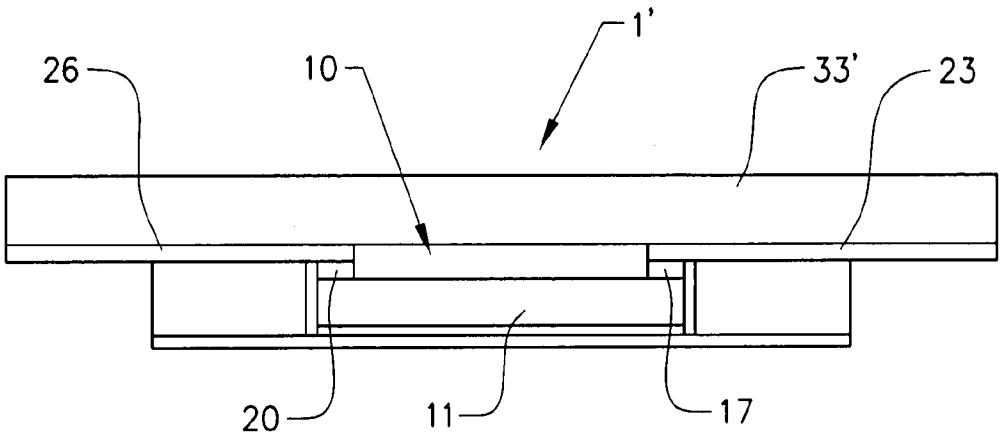

1'
26
10
33'
23
20
11
17

FIG. 5

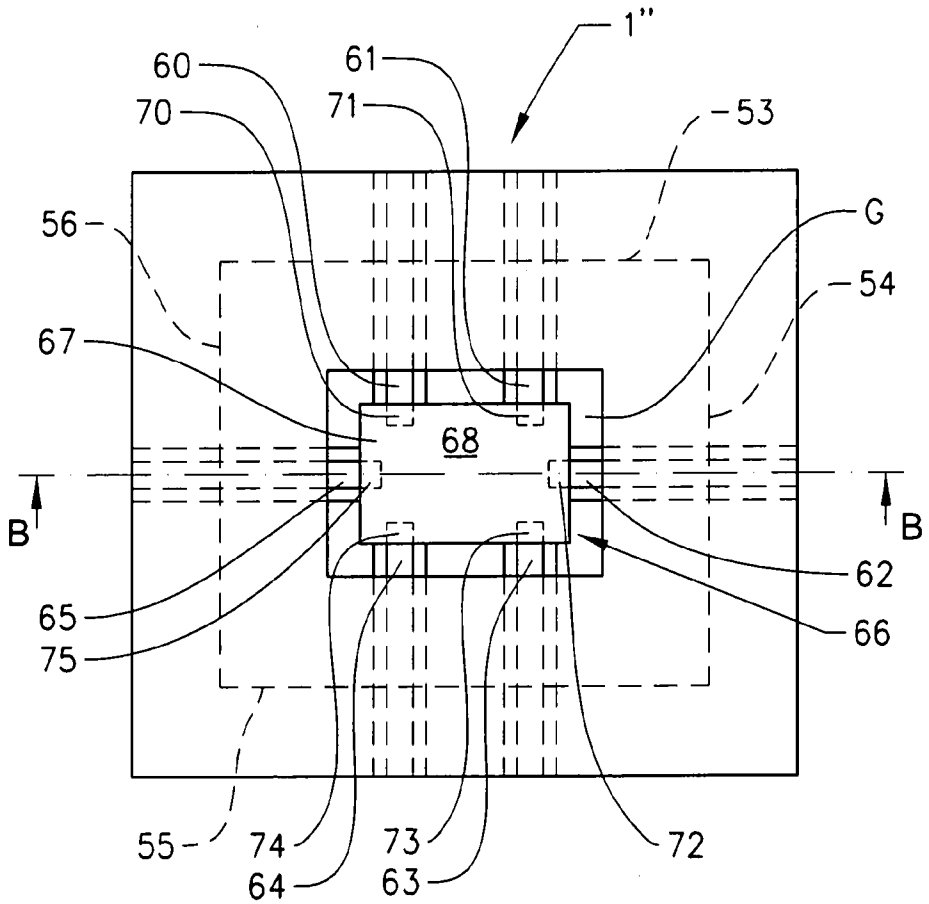
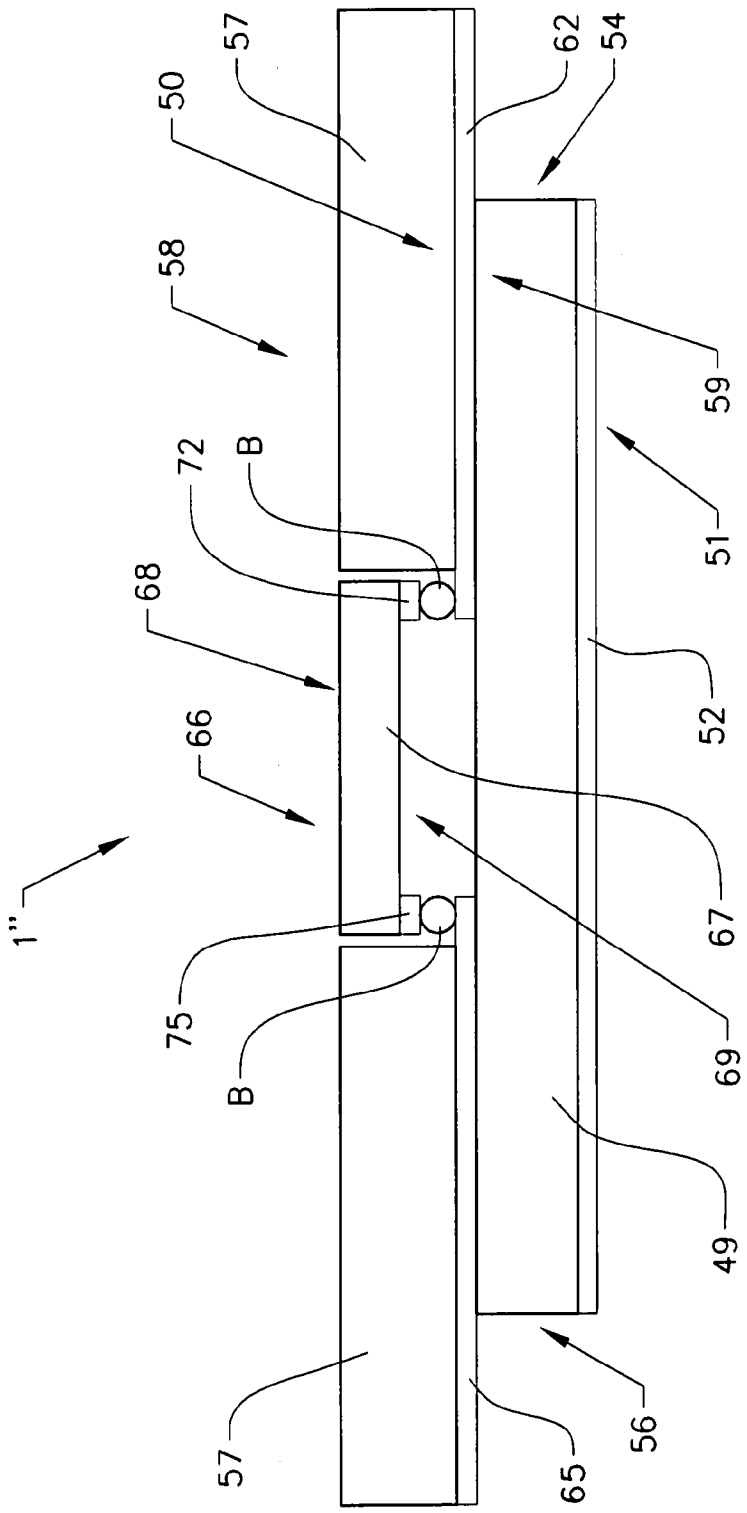

1''
60
61
70
71
53
56
G
54
67
68
B
B
62
65
66
75
55
74
73
72
64
63

FIG. 6




Section B-B

FIG. 7

# INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2006/003997

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L23/31

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X<br>Y | US 2003/150641 A1 (KINAYMAN NOYAN ET AL)<br>14 August 2003 (2003-08-14)<br>paragraph [0044] - paragraph [0052];<br>figure 1 | 1-11<br>12-15 |
| Y | WO 97/34247 A (PAV CARD GMBH; WILM, ROBERT) 18 September 1997 (1997-09-18)<br>page 19, line 27 - page 21, line 28;<br>figures 2-4 | 12-15 |
| A | US 5 578 796 A (BHATT ET AL)<br>26 November 1996 (1996-11-26)<br>column 3, line 40 - column 8, line 9;<br>figure 8 | 12-15 |

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 19 September 2006 | 28/09/2006 |

| Name and mailing address of the ISA/ | Authorized officer |
|---|---|
| European Patent Office, P.B. 5818 Patentlaan 2<br>NL – 2280 HV Rijswijk<br>Tel. (+31–70) 340–2040, Tx. 31 651 epo nl,<br>Fax: (+31–70) 340–3016 | Stirn, Jean-Pierre |

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2006/003997

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
|---|---|---|---|
| US 2003150641 A1 | 14-08-2003 | AU 2003209137 A1 | 04-09-2003 |
| | | WO 03069695 A2 | 21-08-2003 |
| WO 9734247 A | 18-09-1997 | AU 2155697 A | 01-10-1997 |
| | | EP 0976104 A2 | 02-02-2000 |
| US 5578796 A | 26-11-1996 | CN 1132463 A | 02-10-1996 |
| | | CN 1262596 A | 09-08-2000 |
| | | US 5542175 A | 06-08-1996 |