

[72] Inventor **Hachiro Omote**
Osaka, Japan
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[73] Assignee **Matsushita Electrical Industrial Co., Ltd.**
Kadoma-shi, Osaka, Japan

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Primary Examiner—Stanley D. Miller, Jr.
Attorney—Stevens, Davis, Miller and Mosher

[54] **ELECTRICAL RING COUNTER CIRCUIT**
4 Claims, 12 Drawing Figs.

[52] U.S. Cl. 307/223,
307/289, 328/43, 328/205
[51] Int. Cl. H03k 21/00,
H03k 23/08, H03k 3/26
[50] Field of Search 307/289,
223; 328/205, 43

ABSTRACT: A tristable circuit of which the main components are three transistors and three diodes, wherein the conduction of the transistors is switched by applying a trigger pulse thereto so that when one of the transistors is rendered conductive, the other two transistors are rendered nonconductive.

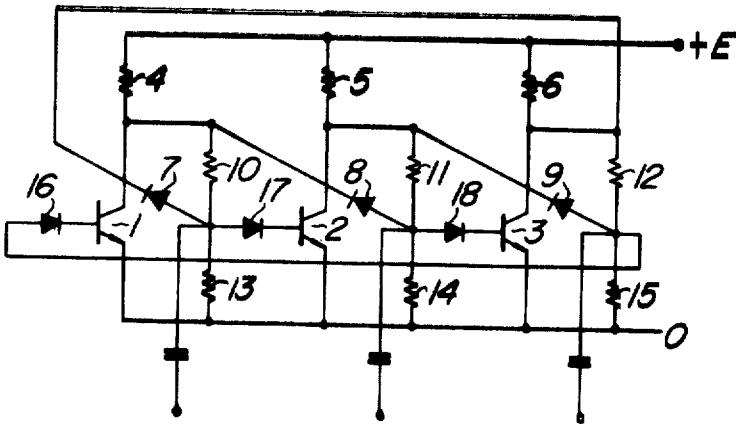


FIG. 1 PRIOR ART

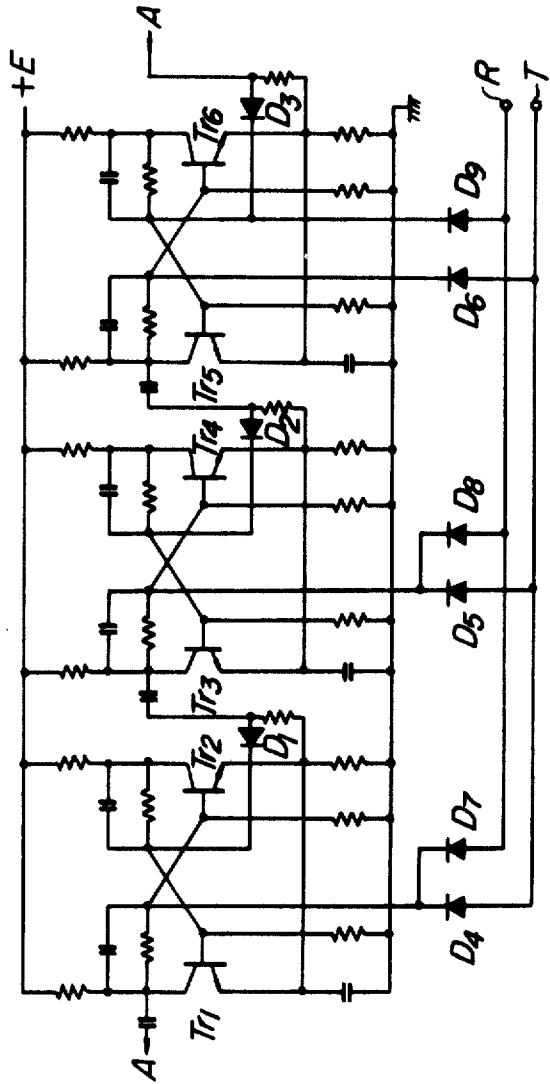


FIG. 2

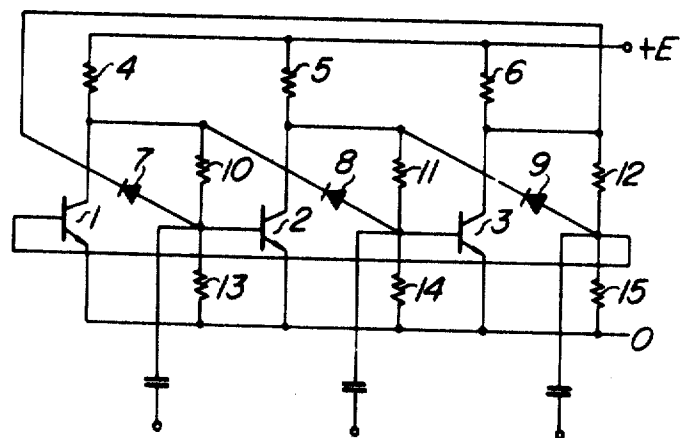


FIG. 3

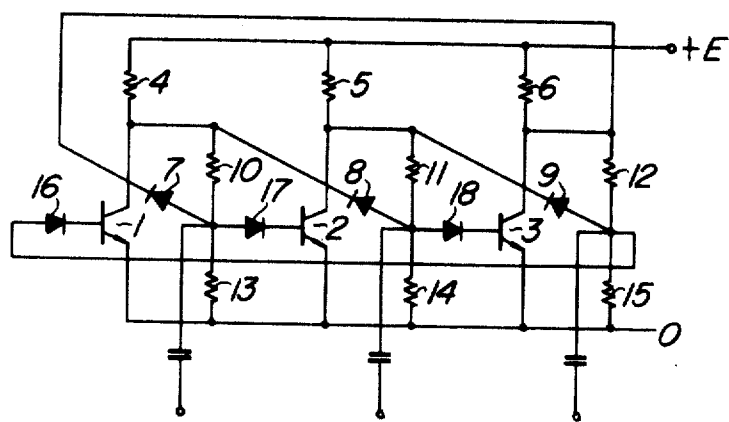


FIG. 4

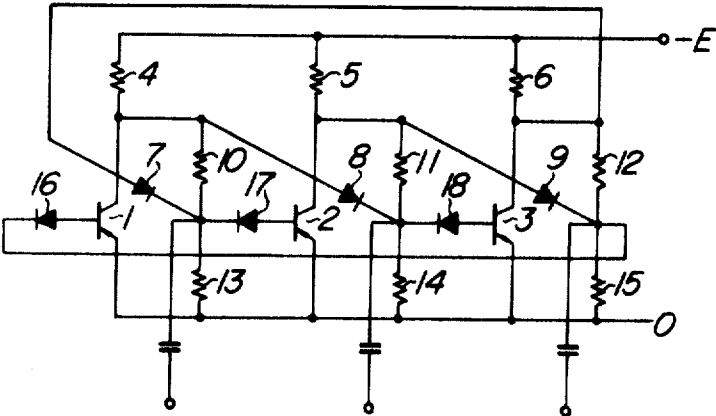
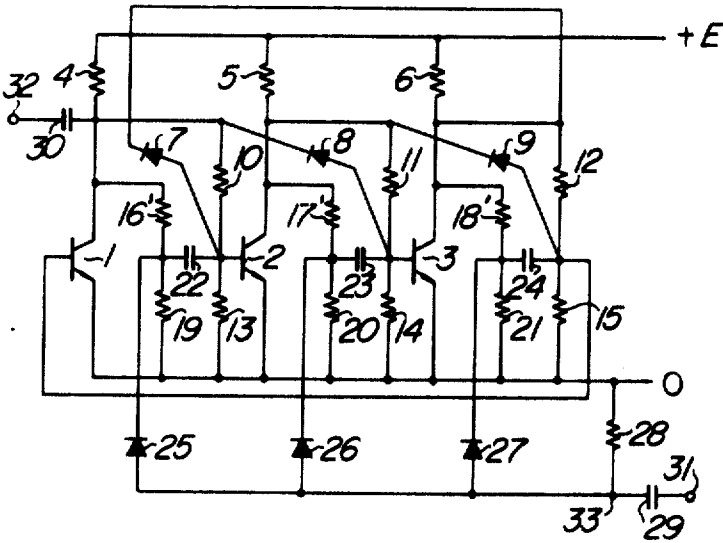


FIG. 5



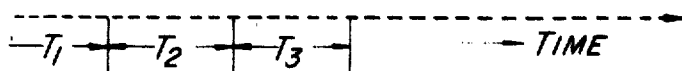
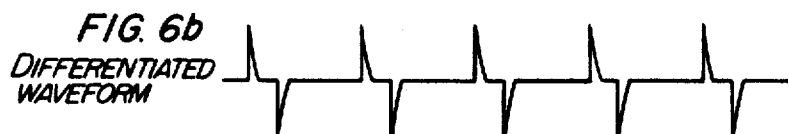
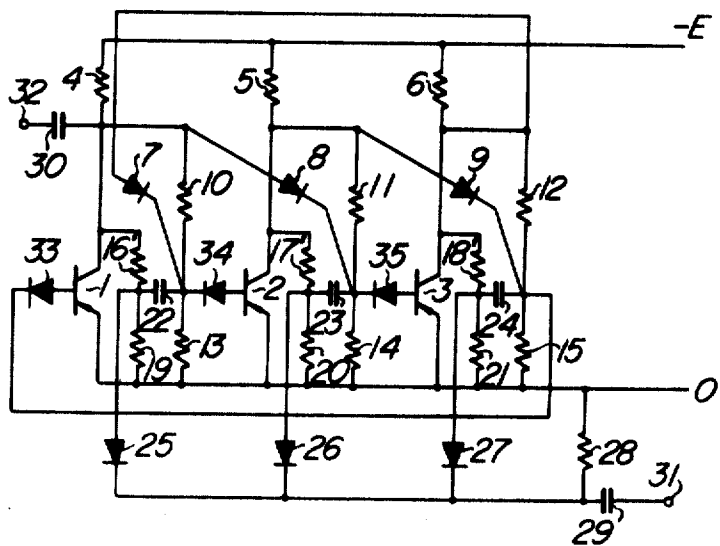


FIG. 7



ELECTRICAL RING COUNTER CIRCUIT

This invention relates to a tristable circuit using transistors.

The conventional tristable circuit is constructed in the form of a ring-counter by the use of three pairs of bistable circuits. Disadvantageously, however, such conventional circuit arrangement is complicated because six transistors are needed.

Accordingly, it is a primary object of the present invention to provide a tristable circuit of simplified construction, which is formed by the use of three transistors constituting the main components thereof.

Another object of the present invention is to provide a tristable circuit using three silicon transistors.

Another object of the present invention is to provide a tristable circuit using germanium transistors.

Still another object of the present invention is to provide a frequency divider circuit adapted for dividing a frequency by a factor of three and constituted by the tristable circuit embodying the present invention.

A further object of the present invention is to provide such frequency divider circuit using silicon transistors.

A still further object of the present invention is to provide such frequency divider circuit using germanium transistors.

Other objects, features and advantages of the present invention will become apparent from the following description taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a circuit diagram showing the conventional tristable circuit;

FIG. 2 is a circuit diagram showing the tristable circuit according to an embodiment of the present invention;

FIGS. 3 and 4 are circuit diagrams showing the tristable circuits according to second and third embodiments of the present invention, respectively;

FIG. 5 is a circuit diagram showing the tristable circuit according to a fourth embodiment of the present invention;

FIGS. 6a to 6f show waveforms useful for explaining the circuit shown in FIG. 5; and

FIG. 7 is a circuit diagram showing the tristable circuit according to a fifth embodiment of the present invention.

Conventionally, for tristable operation, use was made of a ring-counter constituted by three bistable multivibrators. Such ring-counter is well known in the art, an example of which is shown in FIG. 1.

Referring to FIG. 1, transistors Tr_1 and Tr_2 , Tr_3 and Tr_4 , and Tr_5 and Tr_6 constitute three bistable multivibrators respectively, which are connected in cascade with each other. Application of a reset input to a reset input terminal R renders the transistors Tr_2 , Tr_4 and Tr_6 conductive and the transistors Tr_1 , Tr_3 and Tr_5 nonconductive. In such state, when a positive trigger pulse is imparted to a trigger input terminal T, it is applied to the transistors Tr_2 , Tr_4 and Tr_6 through diodes D_4 , D_5 and D_6 respectively, so that the transistor Tr_6 is reversed or turned on since it was in the nonconducting state while the transistors Tr_2 and Tr_4 are not reversed since they were already in the conducting state. Thus, the bistable multivibrator constituted by the transistors Tr_5 and Tr_6 is reversed so that the transistor Tr_5 is reversed so that there occurs at the collector thereof a positive output which is in turn supplied to the transistor Tr_3 through the diode D_2 to thereby turn on this transistor. At this point, since the transistor Tr_3 is switched from "off" to "on", a negative output occurs at the collector thereof, but it is prevented from passing to the transistor Tr_1 by the diode D_1 . Thus, the circuit is switched from a first stable state to a second stable state by being supplied with the trigger pulse, and then it is made to assume a third stable state by the next trigger pulse. Upon arrival of a further trigger pulse, the circuit is returned to the first stable state. In this way, the tristable operation is performed.

However, the foregoing circuit arrangement is disadvantageous in that it is complicated due to the fact that six transistors and a considerable number of other circuit ele-

ments are required for the tristable operation. Furthermore, there are other circuit arrangements of prior art in which three transistors are employed to obtain the desired stable states; in these arrangements, however, two of the three transistors are turned on and the remaining one transistor is cut off. According to the present invention, only one of the three transistors is turned on thereby reducing the power requirement of the circuit, which makes the present invention distinct from and superior to such prior art devices as mentioned above.

The present invention is intended to provide a simplified tristable circuit. Referring to FIG. 2, there is shown the tristable circuit according to a first embodiment of the present invention wherein use is made of NPN silicon transistors. First of all, description will be made of the circuit arrangement shown in FIG. 2. In this Figure, the reference numerals 1, 2 and 3 represent NPN silicon transistors respectively, which are connected in cascade with each other, and 7, 8 and 9 diodes of which the forward voltage is sufficiently low (for example, germanium diodes) respectively. The reference numerals 4, 5 and 6 denote collector loads for the transistors 1, 2 and 3, respectively, and 10, 11, 12, 13, 14 and 15 voltage dividing resistors for dividing the collector voltages of the transistors 1, 2 and 3 and supplying the divided voltages to the bases of the next stage transistors, with the connection point between the resistors 10 and 13, that between the resistors 11 and 14 and that between the resistors 12 and 15 being connected with the bases of the transistors 2, 3 and 1 respectively. The diodes 7, 8 and 9 are connected between the collector of the transistor 3 and the base of the transistor 2, between the collector of the transistor 1 and the base of the transistor 3 and between the collector of the transistor 2 and the base of the transistor 1 respectively, with the cathodes coupled to the collectors and the anodes to the bases.

The operation of the foregoing circuit arrangement will be described below. Assume now that the transistor 2 is in the "on" state. Then the collector voltage of the transistor 2 is equal to the collector saturation voltage thereof (represented by $V_{CE(SAT)}$). This collector voltage is divided by the resistors 11 and 14 and then imparted to the base of the transistor 3. If the divided voltage is lower than the base-emitter cutoff voltage (represented by $V_{BE(CUT)}$) of the transistor 3, then the latter remains nonconductive. In this case, the collector voltage of the transistor 3 becomes equal to +E, and a positive potential appears at the connection point between the resistors 12 and 15 and hence at the base of the transistor 1. In case this positive potential is higher than $V_{BE(CUT)}$, the transistor 1 tends to be rendered conductive. In the circuit arrangement of the present invention, however, the connection point between the resistors 12 and 15 is connected with the collector of the conducting transistor 2 through the diode 9, so that the latter is made conductive to thereby decrease the voltage at the connection point between the resistors 12 and 15. In this case, the voltage at this connection point becomes equal to the sum of the collector saturation voltage $V_{CE(SAT)}$ and the forward voltage (represented by V_F) of the diode 9. By making the voltage lower than $V_{BE(CUT)}$, the transistor 1 is rendered nonconductive. Thus, the collector voltage of the transistor 1 becomes equal to +E, and therefore a positive potential appears at the connection point between the resistors 10 and 13 so that the transistor remains conductive. At this point, the diode 7 remains nonconductive having no effect on the operation because it has the cathode thereof connected with the collector of the transistor 3 which is now in the nonconductive state. This is also true of the diode 8.

In the above-described manner, the first stable state is maintained. In accordance with the present invention, the resistors 4, 5 and 6 are selected so as to have an equal resistance value (R_1), and so are the resistors 10, 11, 12 (R_2) and the resistors 13, 14, 15 (R_3). By applying a positive pulse to the base of the transistor 3 by a suitable method, the transistor 3 is rendered conductive, so that by a similar operation, the transistor 2 is turned off. Consequently, the circuit is caused to assume a second stable state. By imparting a subsequent positive pulse

to the base of the transistor 1, the latter is made conductive, so that by the similar operation the transistors 2 and 3 are rendered nonconductive. As a result, the circuit is made to assume a third stable state. In this way, it is possible to attain the three stable states.

When the symbols referred to here above are used, the conditions for the aforementioned tristable operations are given by

$$\frac{R_3 \cdot E}{R_1 + R_2 + R_3} > V_{BE(CUT)} > \frac{R_3 \cdot V_{CE(SAT)}}{R_2 + R_3}$$

$$V_{CE(SAT)} + V_F < V_{BE(CUT)}$$

In practice, the collector voltage $V_{CE(SAT)}$ of the silicon transistor is about 0.2 v., the base-emitter cutoff voltage $V_{BE(CUT)}$ is about 0.7 v., and the forward voltage V_F of the germanium diode is about 0.2 v. Thus, by suitably selecting the resistance values R_1 , R_2 and R_3 , the foregoing conditions can be sufficiently satisfied.

On the other hand, in case use is made of germanium transistors of which the collector saturation voltage $V_{CE(SAT)}$ is about 0.1 v. and the base-emitter cutoff voltage $V_{BE(CUT)}$ about 0.2 v., it is impossible to meet the above conditions. Therefore, the tristable operation cannot be performed. In accordance with the present invention, however, it is possible to perform the tristable operation even by using germanium transistors, examples of the circuit arrangement being shown in FIGS. 3 and 4.

FIG. 3 shows the case where use is made of NPN germanium transistors, and FIG. 4 shows the case where use is made of PNP ones. Description will first be made of the circuit arrangement shown in FIG. 3.

Elements indicated by 1 to 15 in FIG. 3 correspond to those in FIG. 1, and therefore further description thereof will be omitted. The reference numerals 16, 17 and 18 represent diodes having a high forward voltage (represented by V_{FH}) (for example, silicon diodes), with the anodes being connected with the connection point between the voltage dividing resistors 12 and 15 that between 10 and 13 and that between 11 and 14 and the cathodes being connected in series with the bases of the transistors 1, 2 and 3, respectively.

The conditions for the tristable operation of this circuit are given by

$$\frac{R_3 \cdot E}{R_1 + R_2 + R_3} > V_{BE(CUT)} + V_{FH} > \frac{R_3 \cdot V_{CE(SAT)}}{R_2 + R_3}$$

$$V_{CE(SAT)} + V_F < V_{BE(CUT)} + V_{FH}$$

Such conditions can be met by using as the diodes 16, 17 and 18 silicon diodes of which the forward voltage is about 0.6 V. In case such conditions cannot be satisfied (for example, in the case where use is made of germanium diodes of which the forward voltage is about 0.2 v.), then a plurality of diodes should be connected in series with each other. By doing so, it is possible to satisfy the conditions described above.

The circuit arrangement of FIG. 4 wherein PNP germanium transistors are used is similar to that of FIG. 3, except that the direction of the current flow in the former are opposite to those in the latter so that the directions of the connections between the diodes 7, 8, 9 and 16, 17, 18 are reversed. Thus, it is possible to construct a tristable circuit by the use of three germanium transistors, which is greatly simplified in arrangement as compared with a ring counter, so that the manufacturing cost and the number of steps can be reduced.

Description will now be made of a circuit which is adapted to divide the frequency of an input trigger pulse by a factor of three by using the circuit shown in FIG. 2. FIG. 5 shows an example of such circuit. Parts of FIG. 5 corresponding to those of FIG. 1 are indicated by similar reference numerals, and further description thereof will be omitted. An output terminal 32 is taken from the collector of the transistor 1 through a capacitor 30. A diode 25 has the cathode thereof connected with the base of the transistor 2 through a capacitor 22, and

the connection point between the diode 25 and the capacitor 22 is connected with the collector of the transistor 1 through a resistor 16' and also connected with an earth terminal through a resistor 19. Similar networks are established also with respect to the bases of the transistors 3 and 1 by the use of the diodes 26 and 27 capacitors 23 and 24 and resistors 17', 20, 18' and 21. The anodes of the aforementioned diodes 25, 26 and 27 are connected with each other and coupled to the trigger pulse input terminal 31 through a differentiating circuit constituted by a resistor 28 and a capacitor 29.

Description will next be made of the operation of this circuit.

Assume now that the transistor 2 is in the "on" state (during a period T_1 in FIG. 6). Then, the collector voltage of the transistor 6 becomes equal to the collector saturation voltage thereof. This voltage is divided by the resistors 11 and 14 and then applied to the base of the transistor 3. However, if the divided voltage applied to the transistor 3 is lower than the base-emitter cutoff voltage thereof, then the transistor 3 remains nonconductive so that the collector voltage thereof becomes equal to a DC voltage E. Thus, the connection point between the resistors 12 and 15 assumes a high potential so that the transistor 1 tends to be turned on. In this case, however, since the connection point between the resistors 12 and 15 is connected with the collector of the conducting transistor 2 through the diode 9, the latter is made conductive so that the voltage at the connection point between the resistors 12 and 15 becomes equal to the sum of the collector saturation voltage and the forward voltage of the diode 9. If this sum voltage is lower than the base-emitter cutoff voltage of the transistor 1, then the latter is turned off. Consequently, the collector voltage of the transistor 1 becomes equal to E, and thus the transistor 2 remains conductive. Practically, the collector saturation voltage of the transistor is about 0.2 v., the base-emitter cutoff voltage is about 0.7 v., and the forward voltage of the germanium diode is about 0.2 v., as described above. Thus, the aforementioned operation can be performed.

When a trigger pulse as shown in FIG. 6a is applied to terminal 31, a waveform differentiated by the resistor 28 and 29 such as shown in FIG. 6b occurs at the connection point between the capacitor 29 and the resistor 28, and only positive pulses (FIG. 6c) tend to be imparted to the bases of the transistors 1, 2 and 3 through diodes 25, 26 and 27 and thence through the capacitors 22, 23 and 24. At this point, however, the transistor 1 is maintained in the "off" state so that the connection point between the resistors 16' and 19 assumes a positive potential, and the transistor 3 is also maintained in the "off" state so that the connection point between the resistors 18' and 21 assumes a positive potential. Thus, the diodes 25 and 27 are rendered nonconductive. Therefore, the pulse is prevented from passing to the bases of the transistors 1 and 2. On the other hand, the transistor 2 is in the "on" state so that the potential at the connection point between the resistors 17 and 20 is substantially zero so that the pulse is imparted to the base of the transistor 3 through the diode 26. Thus, the transistor 3 is rendered conductive, while the transistors 1 and 2 remain nonconductive, as is the case with the aforementioned operation. When a further pulse is applied (period T_2 in FIG. 6), it is prevented from passing to the transistors 2 and 3 since the diodes 25 and 26 are nonconductive, but it is imparted only to the transistor 1 through the diode 27 to render the transistor 1 conductive so that a stable state is maintained (period T_3 in FIG. 6). This relationship is shown in FIGS. 6d to 6f.

As will be appreciated from the foregoing, the transistor to be rendered conductive is sequentially switched every time a trigger pulse arrives. Thus, at the output terminal 32, a change in the collector voltage of the transistor 1 occurs at a frequency which is one-third of that of the input trigger pulse.

FIG. 5 shows the case where use is made of NPN silicon transistors. The present circuitry can be realized also by using PNP silicon transistors only if the sum of the collector saturation voltage of the transistor and the forward voltage of the

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diode is lower than the base-emitter cutoff voltage of the transistor. In this case, it goes without saying that the directions of application of the DC voltage and the connection of the diodes 7, 8, 9, 25, 26 and 27 are reversed.

In the case where use is made of germanium transistors, there is no possibility that the sum of the collector saturation voltage of the transistor and the forward voltage of the diode becomes lower than the base-emitter cutoff voltage of the transistor since it is usual that the collector saturation voltage of the germanium transistor is about 0.1 v. and the base-emitter cutoff voltage thereof is about 0.2 v. Therefore, it is usually impossible to achieve a circuit capable of dividing a frequency by a factor of three. However, by connecting in series diodes such for example as silicon diodes 33, 34 and 35, having a high forward voltage, with the bases of the transistors 1, 2 and 3 respectively, it is possible to perform the operation for dividing a frequency by a factor of three.

In accordance with the present invention, therefore, either silicon transistors or germanium transistors may be utilized for the circuit capable of dividing a frequency by a factor of three. The present invention is advantageous in that use may be made of germanium transistors. Furthermore, the circuit arrangement embodying this invention can be simplified since it is composed of only three transistors and nine diodes, and yet there is provided no time-constant circuit, the frequency dividing operation can be stabilized.

I claim:

1. An electrical ring-counter circuit comprising three transistors whose emitters are grounded and whose collectors are connected to a DC source through respective resistors, three voltage dividing network means disposed between said collectors of said transistors and ground respectively, three diodes each of which is connected between a voltage dividing point of one of said voltage dividing network means and the collector of a transistor in a stage preceding that which includes the transistor to whose collector said one voltage dividing network means is connected, and further three diodes each of which is connected between a voltage dividing point of one of said voltage dividing network means and a base of a transistor in a stage succeeding that which includes the

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transistor to whose collector said one voltage dividing network means is connected, thereby adding a voltage to a cutoff voltage between the base and emitter of said transistors.

2. An electrical ring-counter circuit comprising three transistors whose emitters are grounded and whose collectors are connected to a DC source through respective resistors, three first voltage dividing network means disposed between said collectors of said transistors and ground respectively, a voltage dividing point of each one of said first voltage dividing network means being directly connected to a base of a transistor in a stage succeeding that which includes the transistor to whose collector said one of said first voltage dividing network means is connected, three second voltage dividing network means disposed in parallel with said three first voltage dividing network means respectively, three capacitors connected between respective voltage dividing points of said first and second voltage dividing network means, three first diodes each of which is disposed between each one of said voltage dividing points of said first voltage dividing network means and the collector of a transistor in a stage succeeding that which includes the transistor whose base is connected to said one of said voltage dividing points of said first voltage dividing network means, three second diodes which are connected to said voltage dividing points of said second voltage dividing network means respectively at one terminal of each of said three second diodes and are connected to a common junction point at the other terminal of each thereof, and a differentiating circuit disposed between said common junction point of the terminals of said three second diodes and an input terminal for receiving trigger pulses.

3. An electrical ring-counter circuit according to claim 2, wherein said three transistors are silicon transistors.

4. An electrical ring-counter circuit according to claim 2, wherein said three transistors are germanium transistors and said voltage dividing point of each one of said first voltage dividing network means is connected to the base of said transistor through each one of three third diodes, instead of being directly connected thereto, thereby adding a voltage to a cutoff voltage between the base and emitter of said transistor.

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,593,034 Dated July 13, 1971

Inventor(s) Hachiro OMOTE

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Instead of "Matsushita Electrical Industrial Co., Ltd.", the Assignee should read MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.

Signed and sealed this 13th day of June 1972.

(SEAL)
Attest:

EDWARD M. FLETCHER, JR.
Attesting Officer

ROBERT GOTTSCHALK
Commissioner of Patents