SYSTEM AND METHOD OF SAMPLING A SIGNAL HAVING A PLURALITY OF IDENTICALLY SHAPED PULSES

Abstract: A system and a method of sampling a signal having a plurality of identically shaped pulses, the pulses being spaced apart from each other in an equidistant manner. The method includes sampling the signal at a plurality of sampling points, wherein the sampling points are spaced apart from each other in an equidistant manner, and the distance between neighbouring sampling points is chosen such that a) it is larger than the distance between respective rising edges of neighbouring pulses, and b) only pulses are sampled at each of a plurality of successive sampling points.
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TECHNICAL FIELD

[0001] Various embodiments relate generally to a system and a method of sampling a signal having a plurality of identically shaped pulses.

BACKGROUND

[0002] Analog-to-digital converters (ADCs) have been generally implemented in many high speed applications such as high performance digital communication system and high quality video system. The rapid development of the high speed applications requires ADCs having a higher operating speed, lower power consumption and smaller die area. As the sampling rate of ADCs increases, high speed application circuits having a faster settling time (i.e. the time required for the circuits to reach a steady state) is desirable. However, a faster settling time may increase the current required by the high speed application circuits to drive the parasitic capacitance load and hence may result in an increase of power consumption of the high speed application circuits.

[0003] In impulse ultra wideband (UWB) systems, the signals comprise narrow pulses transmitted at a fixed periodic repetition frequency (PRF). Due to the impulse nature of the signal, the bandwidth of the signal is generally very wide (e.g. about 500MHz). Thus, a very high sampling rate is required to be able to sample the pulses at the Nyquist rate. Depending on the pulse width and PRF, the pulses may only be
transmitted for a short duration compared to the duration of the whole signal. In this case, it may be highly inefficient to sample the whole signal.

[0004] One conventional way to overcome the problem of a high sampling rate is to use a time-interleaved method which routes the signal to be sampled into two or more parallel signal sampling paths, wherein each path is processed at a slower frequency (compared to the sampling frequency used by a system having only one signal sampling path) with a fixed phase offset, and wherein the two or more parallel paths are subsequently summed up. This may achieve a sampling rate of \( N \) times the clock frequency, where \( N \) is the number of parallel stages. However, the phase offset of the time-interleaved method needs to be very precise and the power consumption is \( N \) times the power consumption of the system having only one signal sampling path.

[0005] Figure 1 shows a typical pulse signal 100 of an impulse radio ultra wideband (IR-UWB) system in a time domain. The signal 100 has a plurality of identically shaped pulses 102. The signal 100 has a periodic repetition frequency (PRF) of about 10MHz (i.e. a pulse repetition rate (PRT) of about 100ns). The triangular pulses 102 have a pulse width (T_pulse) of about 10ns. Thus, 90ns of the PRT of the signal 100 will be "empty" in the time domain. In order to adequately sample the pulses 102, the signal 100 is sampled at about 1GHz. Such a high frequency sampling rate may result in high power consumption. Figure 2 shows the signal 100 in a frequency domain. It can be derived from Figure 2 that the bandwidth of the signal 100 is about 200MHz. To sample the signal 100, the sampling rate must be more than twice the bandwidth of the signal 100. Thus, the sampling rate should be more than 400MHz even in the frequency domain.
Figure 3 shows a schematic block diagram of a conventional system 300 used for sampling the signal 100 of Figure 1. The conventional system 300 includes a high speed clock generator 302 and a high speed analog-to-digital converter (ADC) 304. The high speed clock generator 302 has an output terminal 306. The high speed ADC 304 has a first input terminal 308, a second input terminal 310, a third input terminal 312, a first output terminal 314 and a second output terminal 316. The output terminal 306 of the high speed clock generator 302 is coupled to the third input terminal 312 of the high speed ADC 304. The high speed clock generator 302 sends a sampling clock signal to the high speed ADC 304 via the output terminal 306. The high speed ADC 304 receives the sampling clock signal via the third input terminal 312. The high speed ADC 304 receives an input signal e.g. via the first input terminal 308 and the second input terminal 310, and samples the input signal based on the received sampling clock signal. Similarly, the high speed clock generator 302 and the high speed analog-to-digital converter (ADC) 304 may have a high sampling rate which may result in high power consumption.

SUMMARY

According to one embodiment of the present invention, a method of sampling a signal having a plurality of identically shaped pulses, the pulses being spaced apart from each other in an equidistant manner, is provided. The method includes sampling the signal at a plurality of sampling points, wherein the sampling points are spaced apart from each other in an equidistant manner, and the distance between neighbouring sampling points is chosen such that a) it is larger than the distance between respective raising edges of neighbouring pulses, and b) only pulses are sampled at each of a plurality
of successive sampling points. The distance between respective raising edges of
neighbouring pulses corresponds to the periodic repetitive time (PRT) of the signal. The
distance between neighbouring sampling points corresponds to the sampling period
($T_{samp}$) based on which the signal is sampled. Since the sampling period of the signal is
larger than the periodic repetitive time of the signal, the signal can be sampled at a
sampling frequency which is lower than a periodic repetitive frequency of the signal. Due
to the lower sampling frequency, power consumption may be reduced.

[0008] In one embodiment, a first sampling point of the plurality of successive
sampling points coincides with a rising edge of a pulse of the signal. One effect of this
embodiment is that the first sampling point of the plurality of successive sampling points
can be located within the pulse of the signal.

[0009] In one embodiment, the first sampling point of the plurality of successive
sampling points is located after the rising edge of a pulse of the signal. One effect of this
embodiment is that the first sampling point of the plurality of successive sampling points
can be located within the pulse of the signal.

[0010] In one embodiment, the number of sampling points of the plurality of
successive sampling points is set according to a predetermined sampling resolution of the
pulses of the signal.

[0011] In one embodiment, the distance between neighbouring sampling points is set
using the formula: $[\text{distance} = \text{distance between respective raising edges of neighbouring
pulses} + \text{time value}]$, wherein the time value is determined by dividing a pulse width of a
pulse of the signal by the set number of successive sampling points.
In one embodiment, the number of sampling points of the plurality of successive sampling points is equal to or larger than 2.

In one embodiment, the number of sampling points of the plurality of successive sampling points ranges between 2 and 10.

In one embodiment, the number of sampling points of the plurality of successive sampling points is greater than 10.

In one embodiment, the signal is a ranging signal or a communication signal.

In one embodiment, the method further includes reconstructing a waveform of the pulses based on samples obtained at the plurality of successive sampling points.

In one embodiment, the reconstructed waveform of the signal includes a bandwidth which is given by:

\[ BW_{\text{original}} \times \frac{(PRF - F_{\text{sample}})}{PRF}, \]

wherein \( BW_{\text{original}} \) is an original bandwidth of the signal, \( PRF \) represents a periodic repetitive frequency of the signal, and \( F_{\text{sample}} \) is a sampling frequency of the signal. The bandwidth of the reconstructed waveform of the signal may be smaller than the original bandwidth of the signal. Although the bandwidth of the reconstructed waveform of the signal is smaller than the original bandwidth of the signal, the shape of the signal can be preserved.

According to another embodiment of the present invention, a system for sampling a signal having a plurality of identically shaped pulses, the pulses being spaced apart from each other in an equidistant manner, is provided. The system includes an analog to digital converter configured to receive the signal and to sample the signal at a plurality of sampling points, wherein the sampling points are spaced apart from each
other in an equidistant manner, and the distance between neighbouring sampling points is chosen such that a) it is larger than the distance between respective raising edges of neighbouring pulses, and b) only pulses are sampled at each of a plurality of successive sampling points. The system uses a single analog to digital converter to sample the signal. Thus, the system may require a smaller area and may consume less power as compared to the conventional systems.

[0019] In one embodiment, the system further includes a clock generating unit configured to generate a plurality of clock signals; a pulse detecting unit coupled to the analog to digital converter and being configured to detect the plurality of pulses of the signal; and a clock selecting unit coupled to the clock generating unit and the pulse detecting unit; wherein upon detection of the plurality of pulses of the signal, the pulse detecting unit is configured to activate the clock selecting unit to select a sampling clock signal from the plurality of clock signals generated by the clock generating unit. Power consumption of the system may be reduced by activating the clock selecting unit only after the pulse detecting unit detects a plurality of pulses of the signal.

[0020] In one embodiment, the analog to digital converter is coupled to the clock selecting unit and is configured to receive the selected sampling clock signal from the clock selecting unit, and to sample the signal based on the received sampling clock signal.

[0021] In one embodiment, the clock signals generated by the clock generating unit differ from each other regarding their phase.
BRIEF DESCRIPTION OF THE DRAWINGS

[0022] In the drawings, like reference characters generally refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the principles of the invention. In the following description, various embodiments of the invention are described with reference to the following drawings, in which:

[0023] Figure 1 shows a typical pulse signal which may be sampled by an impulse radio ultra wideband (IR-UWB) system in a time domain.

[0024] Figure 2 shows the pulse signal of Figure 1 in a frequency domain.

[0025] Figure 3 shows a schematic block diagram of a conventional system used for sampling the pulse signal of Figure 1.

[0026] Figure 4 shows a schematic block diagram of a system for sampling a signal having a plurality of identically shaped pulses according to one embodiment of the present invention.

[0027] Figure 5 shows a schematic block diagram of a clock generating unit usable within a system according to one embodiment of the present invention.

[0028] Figure 6 shows different phases of a reference clock signal which may be used for sampling by a system according to one embodiment of the present invention.

[0029] Figure 7 shows a schematic block diagram of a clock selecting unit usable within a system according to one embodiment of the present invention.

[0030] Figure 8 shows a timing diagram usable for sampling by a system according to one embodiment of the present invention.
Figure 9 shows a signal sampled at a plurality of sampling points which may be sampled by a system according to one embodiment of the present invention.

Figure 10 shows a waveform of a signal in the time domain which may be reconstructed by a system according to one embodiment of the present invention.

Figure 11 shows a waveform of a signal in the frequency domain which may be reconstructed by a system according to one embodiment of the present invention.

Figure 12 shows a flowchart of a method of sampling a signal having a plurality of identically shaped pulses according to one embodiment of the present invention.

DETAILED DESCRIPTION

Embodiments of a system and a method of sampling a signal having a plurality of identically shaped pulses will be described in detail below with reference to the accompanying figures. It will be appreciated that the embodiments described below can be modified in various aspects without changing the essence of the invention.

Figure 4 shows a schematic block diagram of a system 400 for sampling a signal having a plurality of identically shaped pulses (like the signal shown in Figure 1) according to one embodiment of the present invention. The system 400 includes an analog to digital converter (ADC) 402, a pulse detecting unit 404, a clock selecting unit 406 and a clock generating unit 408. In one embodiment, the ADC 402 may be a differential ADC. The ADC 402 may also be a slow speed ADC. The ADC 402 has a first input terminal 410, a second input terminal 412 and a third input terminal 414. The ADC 402 also has a first output terminal 416 and a second output terminal 418.
In one embodiment, the pulse detecting unit 404 may be a comparator. The pulse detecting unit 404 has a first input terminal 420, a second input terminal 422 and an output terminal 424. The clock selecting unit 406 has a first input terminal 426, a plurality of second input terminals 428 and an output terminal 430. The clock generating unit 408 has a plurality of output terminals 432.

The first input terminal 410 and the second input terminal 412 of the ADC 402 are coupled to the first input terminal 420 and the second input terminal 422 of the pulse detecting unit 404, respectively. The third input terminal 414 of the ADC 402 is coupled to the output terminal 430 of the clock selecting unit 406. The output terminal 424 of the pulse detecting unit 404 is coupled to the first input terminal 426 of the clock selecting unit 406. The plurality of second input terminals 428 of the clock selecting unit 406 are coupled to the plurality of output terminals 432 of the clock generating unit 408.

Figure 5 shows a schematic block diagram of a possible embodiment of the clock generating unit 408. In this embodiment, the clock generating unit 408 includes a plurality of delay cells 502. For illustration purposes, only 16 delay cells 502 are shown in Figure 5. The number of delay cells 502 may be different in other embodiments. The number of delay cells 502 may be dependent on the number of clock phases to be generated by the clock generating unit 408. The plurality of delay cells 502 are arranged in series. The plurality of delay cells 502 may be a ring oscillator. The clock generating unit 408 also includes a phase detector and low pass filter 504. An input terminal 506 of the first delay cell 502 of the series of delay cells 502 and an output terminal 508 of the last delay cell 502 of the series of delay cells 502 are coupled to the phase detector and
low pass filter 504. In one embodiment, the clock generating unit 408 may be a low
frequency delay locked loop (DLL).

[0040] An external reference clock signal (clk-ref) having a desired frequency may
be inputted to the clock generating unit 408. That is, the reference clock signal (clk-ref)
may be received by the input terminal 506 of the first delay cell 502. In this case, the
plurality of delay cells 502 generate multiple phases (e.g. 16 phases) of the reference
clock signal (clk-ref). The numbers of phases of the reference clock signal (clk-ref)
generated may be different in other embodiments. For example, 32 phases of the
reference clock signal (clk-ref) may be generated. When a higher number of phases of the
reference clock signal (clk-ref) is generated, power consumption of the system 400 may
be further reduced. The phase detector and low pass filter 504 inputs a control voltage
signal (V) into the plurality of delay cells 502. The control voltage signal (V) may allow
the phase detector and low pass filter 504 and the plurality of delay cells 502 to form a
closed loop. The phase detector and low pass filter 504 together with the plurality of
delay cells 502 forms a closed loop to lock the frequency and the phase of the reference
clock signal (clk-ref). The control voltage signal (V) may be a variable voltage which
ensures that the multiple phases $\phi_1$ to $\phi_{16}$ of the reference clock signal (clk-ref) generated
by the plurality of delay cells 502 are equally spaced apart. That is, the phase difference
between two consecutive phases (e.g. $\phi_3$ and $\phi_4$) is the same. The clock generating unit
408 outputs the multiple phases $\phi_1$ to $\phi_{16}$ of the reference clock signal (clk-ref) via the
plurality of output terminals 432. Figure 6 shows the different phases $\phi_1$ to $\phi_{16}$ of the
reference clock signal (clk-ref) generated by the plurality of delay cells 502.
Figure 7 shows a schematic block diagram of a possible embodiment of the clock selecting unit 406. In this embodiment, the clock selecting unit 406 includes a clock comparing logic 702 and a plurality of multiplexer switches S1 to S16. The clock comparing logic 702 has a plurality of input terminals 704 and a plurality of output terminals 706. Each of the plurality of output terminals 706 of the clock comparing logic 702 is coupled to a corresponding switch S1 to S16. The switches S1 to S16 of the clock selecting unit 406 are controlled by control signals C1 to C16 sent from the output terminals 706 of the clock comparing logic 702 respectively.

The clock selecting unit 406 receives the plurality of clock phases $\phi_1$ to $\phi_{16}$ from the clock generating unit 408 (see Figure 4) via the plurality of input terminals 428. The plurality of clock phases $\phi_1$ to $\phi_{16}$ is then sent to the plurality of input terminals 704 of the clock comparing logic 702. The plurality of clock phases $\phi_i$ to $\phi_{16}$ is also sent to the respective multiplexer switches S1 to S16. The clock comparing logic 702 receives an output signal ($P_{\text{output}}$) from the pulse detecting unit 406 (see Figure 4) via the input terminal 426. The clock comparing logic 702 then compares the output signal ($P_{\text{output}}$) with each of the plurality of clock phases $\phi_i$ to $\phi_{16}$.

In one embodiment, the clock selecting unit 406 may select one of the clock phases $\phi_1$ to $\phi_{16}$ that has a rising edge which coincides with a rising edge of the output signal ($P_{\text{output}}$) from the pulse detecting unit 406 to be a sampling signal. In another embodiment, the clock selecting unit 406 may determine one of the clock phases $\phi_i$ to $\phi_{16}$ that has a rising edge which is after the rising edge of the output signal ($P_{\text{output}}$) from the pulse detecting unit 406. For example, the clock selecting unit 406 may determine one of the clock phases $\phi_1$ to $\phi_{16}$ that has a rising edge which is after and closest to the rising
edge of the output signal \((P_{out})\) from the pulse detecting unit 406. The clock selecting unit 406 may select a clock phase \((\phi_1 \text{ to } \phi_{16})\) before the clock phase \((\phi_1 \text{ to } \phi_{16})\), which is determined to have a rising edge which is after and closest to the rising edge of the output signal \((P_{out})\), to be a sampling signal. For example, the clock selecting unit 406 may select the clock phase \((\phi_1 \text{ to } \phi_{16})\) that has a rising edge which is before and closest to the rising edge of the output signal \((P_{out})\) to be the sampling signal. If the clock phase \(\phi_3\) is determined to be the clock phase that has a rising edge which is after and closest to the rising edge of the output signal \((P_{out})\), the clock selecting unit 406 may select the clock phase \((e.g. \phi_1, \phi_2)\) that has a rising edge which is before the rising edge of the clock phase \(\phi_3\) to be the sampling signal. In one embodiment, the clock selecting unit 406 may select the clock phase \(\phi_2\) that has a rising edge which is before and closest to the rising edge of the clock phase \(\phi_3\) to be the sampling signal. The selected sampling signal \(\phi_2\) may have a rising edge which is before or before and closest to the rising edge of the output signal \((P_{out})\).

[0044] Selecting a clock phase that has a rising edge which is before the rising edge of the output signal \((P_{out})\) to be the sampling signal may ensure that a sufficient number of successive sampling points (to the effect of an entire pulse of a signal being sampled) is obtained for reconstructing a waveform of the pulse of the signal. The shape of the pulses may be sampled over the entire width of the pulse with a constant sampling resolution, meaning that no area of the pulse remains unsampled. To ensure that the selected sampling signal does not have a rising edge which is very much in front of the rising edge of the output signal \((P_{out})\), it may be preferable to select a clock phase that has a rising edge which is before and closest to the rising edge of the output signal.
The two embodiments described above may apply for ideal situations where the rising edge of the output signal ($P_{\text{output}}$) coincides with a rising edge of a pulse of a signal to be sampled.

However, the rising edge of the output signal ($P_{\text{output}}$) may not coincide with the rising edge of the pulse of the signal to be sampled. In such events, the clock selecting unit 406 may select a clock phase ($\phi_1$ to $\phi_{16}$) that has a rising edge which is before or before and closest to both the rising edge of the output signal ($P_{\text{output}}$) and the rising edge of the pulse of the signal to be sampled to be the sampling signal.

For example, if the clock selecting unit 406 selects the clock phase $\phi_2$, the clock comparing logic 702 sends a control signal $C_2$ to the switch $S_2$ which corresponds to the selected clock phase $\phi_2$ to turn on the switch $S_2$. The clock selecting unit 406 then outputs the selected clock phase $\phi_2$ via the output terminal 430.

Details of the operation of the system 400 are described in the following and with reference to Figures 4, 8 and 9. Figure 8 shows a timing diagram 800 of the system.

A first pulse 801 of a reset signal 802 may be generated by e.g. a baseband of a receiver (not shown) to set an output signal (e.g. $P_{\text{output}}$ of Figure 7) 804 of the pulse detecting unit 404 to 'Low' or 'O'. This may set the pulse detecting unit 404 to a detection mode to detect pulses. A signal 806 to be sampled having a plurality of identically shaped pulses 808 is inputted into the first input terminal 410 of the ADC 402. In one embodiment, the signal 806 may be similar to the signal 100 of Figure 1. The signal 806 may be a communication signal or a ranging signal. The pulses 808 of the
signal 806 are spaced apart from each other in an equidistant manner. The pulses 808 are triangular. The shapes of the pulses 808 may be different in other embodiments.

[0049] Since the first input terminal 420 of the pulse detecting unit 404 is coupled to the first input terminal 410 of the ADC 402, the pulse detecting unit 404 can detect the plurality of identically shaped pulses 808 of the signal 806. Thus, the signal 806 is also inputted into the first input terminal 420 of the pulse detecting unit 404. The signal inputted into the second terminal 412 of the ADC 402 and the second terminal 422 of the pulse detecting unit 404 is a differential signal of the signal 806 inputted into the first input terminal 410 of the ADC 402 and the first input terminal 420 of the pulse detecting unit 404. The pulse detecting unit 404 compares a voltage of the pulses 808 of the signal 806 and a reference voltage. The reference voltage may be either generated internally by the pulse detecting unit 404 or inputted externally. If the voltage of the pulses 808 of the signal 806 is higher than the reference voltage, the pulse detecting unit 404 outputs an output signal 804 of 'high' or '1'. A rising edge 805 of the output signal 804 is formed by the output signal 804 changing from 'Low' or '0' to 'high' or '1'. Upon detection of the plurality of pulses 808 of the signal 806 (i.e. with the pulse detecting unit 404 outputting a 'high' or '1' output 804), the pulse detecting unit 404 activates the clock selecting unit 406 by outputting a 'high' or '1' output 804 to the clock selecting unit 406.

[0050] At the same time, the clock generating unit 408 generates a plurality of clock signals. As explained above with Figure 5, the clock signals generated by the clock generating unit 408 differ from each other only regarding their phase. In one embodiment, the clock generating unit 408 may generate e.g. 32 clock signals having different phases. The number of clock signals having different phases may vary in
different embodiments. The clock generating unit 408 transmits the plurality of clock signals to the clock selecting unit 406 via the plurality of output terminals 432.

[0051] The clock selecting unit 406 receives the plurality of clock signals from the clock generating unit 408 via the plurality of second input terminals 428. The clock selecting unit 406 selects a sampling clock signal 810 from the plurality of clock signals generated by the clock generating unit 408.

[0052] In one embodiment, the clock selecting unit 406 may select a sampling clock signal 810 that has a rising edge which coincides with the rising edge 805 of the output signal 804 of the pulse detecting unit 404. In another embodiment, the clock selecting unit 406 may determine a clock signal that has a rising edge which is after the rising edge 805 of the output signal 804 of the pulse detecting unit 404. For example, the clock selecting unit 406 may determine a clock signal (e.g. φ₃) that has a rising edge which is after and closest to the rising edge 805 of the output signal 804 of the pulse detecting unit 404. The clock selecting unit 406 may select a clock signal (e.g. φ₁, φ₂) that has a rising edge which is before or before and closest to the rising edge of the clock signal (φ₃) to be a sampling clock signal 810. For example, the clock selecting unit 406 may select the clock signal (e.g. φ₂) that has a rising edge which is before or before and closest to the rising edge 805 of the output signal 804 of the pulse detecting unit 404 to be the sampling clock signal 810. Selecting a clock signal that has a rising edge which is before the rising edge 805 of the output signal 804 of the pulse detecting unit 404 to be the sampling clock signal 810 may ensure that a sufficient number of successive sampling points (to the effect of an entire pulse 808 of the signal 806 being sampled) is obtained for reconstructing a waveform of the pulse 808 of the signal 806. The shape of the pulses 808
may be sampled over the entire width of the pulse 808 with a constant sampling resolution, meaning that no area of the pulse 808 remains unsampled. To ensure that the selected sampling clock signal 810 does not have a rising edge which is very much in front of the rising edge 805 of the output signal 804, it may be preferable to select a clock signal that has a rising edge which is before and closest to the rising edge 805 of the output signal 804. The two embodiments described above may apply for ideal situations where the rising edge 805 of the output signal 804 coincides with a rising edge of the pulse 808 of the signal 806.

As described above, the pulse detecting unit 404 compares the voltage of the pulses 808 of the signal 806 and the reference voltage. Once the voltage of the pulses 808 of the signal 806 is determined to be higher than the reference voltage, the pulse detecting unit 404 outputs an output signal 804 of 'high' or '1' with a delay. Due to the finite threshold level (e.g. comparison of the voltage of the pulses 808 of the signal 806 with the reference voltage) and the internal delay of the pulse detecting unit 404, the rising edge 805 of the output signal 804 may not coincide with the rising edge of the pulse 808 of the signal 806. For example, the rising edge 805 of the output signal 804 may coincide with the peak of the pulse 808 of the signal 806, as shown in Figure 8. Thus, the selected sampling clock signal 810 may have a rising edge which is after the rising edge of the pulse 808 of the signal 806. In such events, a certain portion of the pulse 808 (e.g. the first half of the pulse 808) may not be sampled.

Therefore, it is preferable that the clock selecting unit 406 selects a clock signal that has a rising edge which is before or before and closest to both the rising edge 805 of the output signal 804 and the rising edge of the pulse 808 of the signal 806 to be
the sampling clock signal 810. The clock selecting unit 406 may determine a clock signal (e.g. \( \phi_3 \)) that has a rising edge which coincides with or is after or is after and closest to the rising edge 805 of the output signal 804 of the pulse detecting unit 404. The clock selecting unit 406 may first select a clock signal (e.g. \( \phi_2 \)) that has a rising edge which is before or before and closest to the rising edge 805 of the output signal 804. The clock selecting unit 406 may then select a sampling clock signal (e.g. \( \phi_1 \)) that has a rising edge which is before or before and closest to the rising edge of the pulse 808 of the signal 806 based on the first selected clock signal (\( \phi_2 \)) by a total constant delay resulted from the finite threshold level and the internal delay of the pulse detecting unit 404.

[0055] However, if the selected sampling clock signal 810 has a rising edge which is very much in front of the rising edge of the pulse 808 of the signal 806, a number of successive sampling points (e.g. 5 out of 10 sampling points) may fall outside the pulse 808 (e.g. the area in front of the pulse 808) and only e.g. the first half of the pulse 808 may be sampled. If the selected sampling clock signal 810 has a rising edge which is very much later than the rising edge of the pulse 808 of the signal 806, only e.g. the second half of the pulse 808 may be sampled. A 'high' pulse of the reset signal 802 may be generated to end the sampling process if two or more successive '0's are detected (i.e. two or more successive sampling points fall outside the pulse 808). This may prevent an "erroneous" sampling process. Under normal circumstances, this may ensure that the signal 806 has ended, and that the sampling process only stops after the signal 806 has ended.

[0056] The clock selecting unit 406 transmits the selected sampling clock signal 810 to the ADC 402 via the output terminal 430. The ADC 402 receives the selected sampling
clock signal 810 from the clock selecting unit 406 via the third input terminal 414. The ADC 402 is turned on at the time of receiving the first rising edge of the selected sampling clock signal 810 from the clock selecting unit 406.

[0057] The ADC 402 samples the signal 806 based on the received sampling clock signal 810. The ADC 402 samples the signal 806 at a plurality of sampling points 902, as shown in Figure 9. In one embodiment, a first sampling point 902 of the plurality of successive sampling points 902 coincides with a rising edge 904 of a pulse 808 of the signal 806. In another embodiment, the first sampling point 902 of the plurality of successive sampling points 902 is located after the rising edge 904 of a pulse 808 of the signal 806. It may be understood by a skilled person that the position of the first sampling point 902 within a pulse 808 of the signal 806 is dependent on the selected sampling clock signal 810 (i.e. whether the selected sampling clock signal 810 coincides with or is before a rising edge of the pulse 808 of the signal 806). In one embodiment, the positions of the plurality of sampling points 902 coincide with respective rising edges of the selected sampling clock signal 810.

[0058] The number (N) of sampling points 902 of the plurality of successive sampling points 902 is set according to a predetermined sampling resolution of the pulses 808 of the signal 806. The number (N) of sampling points 902 of the plurality of successive sampling points 902 may also vary depending on the applications. In one embodiment, the number (N) of sampling points of the plurality of successive sampling points is equal to or larger than 2. In another embodiment, the number (N) of sampling points of the plurality of successive sampling points ranges between 2 and 10. In a further
embodiment, the number (N) of sampling points of the plurality of successive sampling points is greater than 10.

[0059] The plurality of successive sampling points 902 refer to consecutive sampling points 902 that are located within a pulse 808 of the signal 806. That means no sampling point 902 of the plurality of successive sampling points 902 is located "outside" a pulse 808 of the signal 806 (i.e. no sampling point 902 is located in the "empty" part of the signal 806). For example, as shown in Figure 8, 11 successive sampling points are used to sample respective pulses 808 of the signal 806. Assuming that the sampling of the signal 806 does not stop after the 11th sampling point, the subsequent (12th) sampling point will be located "outside" a pulse 808 of the signal 806. The 12th sampling point will not be considered as a sampling point belonging to the plurality of successive sampling points 902. The 11 successive sampling points when superimposed onto a single pulse 808 of the signal 806 may achieve an effect of an entire pulse 808 of the signal 806 being sampled.

[0060] The sampling points 902 are spaced apart from each other in an equidistant manner. The distance d1 between neighbouring sampling points 902 is chosen such that the distance d1 between neighbouring sampling points 902 is larger than the distance d2 between respective rising edges 904 of neighbouring pulses 808, and only pulses 808 are sampled at each of a plurality of successive sampling points 902. This means that no sampling point is located "outside" a pulse, i.e. no sampling point is located in the "empty" part of the signal 806. The distance d1 between neighbouring sampling points 902 corresponds to the sampling period (T_{sample}) based on which the signal 806 is
sampled. The distance \( d_2 \) between respective rising edges 904 of neighbouring pulses 808 corresponds to the periodic repetitive time (PRT) of the signal 806.

[0061] The distance \( d_1 \) between neighbouring sampling points 902 is set using the formula:

\[
\text{distance} = \text{distance between respective raising edges} \ 904 \ \text{of neighbouring pulses} \ 808 \ + \ \text{time value},
\]

(which is: \( d_1 = d_2 + A_t \))

wherein the time value (\( A_t \)) is determined by dividing a pulse width (\( T_{\text{pulse}} \)) of a pulse 808 of the signal 806 by the set number (N) of successive sampling points 902.

[0062] Assume that the periodic repetitive time (PRT) of the signal 806, which is also the distance \( d_2 \) between respective rising edges 904 of neighbouring pulses 808, is about 100ns. A periodic repetitive frequency (PRF) of the signal 806, which is a reciprocal of the periodic repetitive time (PRT) of the signal 806, is about 10MHz. The time value (\( A_t \)) is assumed to be about 1ns. Therefore, the sampling period (\( T_{\text{sampl}} \)), which is the distance \( d_1 \) between neighbouring sampling points 902, can be about 101ns. A sampling frequency (\( F_{\text{sampl}} \)), which is a reciprocal of the sampling period (\( T_{\text{sampl}} \)), can be about 9.901MHz.

[0063] The signal 806 can be sampled at the sampling frequency which is lower than the periodic repetitive frequency (PRF) of the signal 806. The signal 806 can be sampled at a sampling rate lower than the Nyquist rate (e.g. about 1GHz as described above with Figures 1 and 2). Due to the lower sampling rate, power consumption may be reduced. Since the sampling period is larger than the periodic repetitive time (PRT) of the signal 806, a longer settling time (i.e. the time required after the signal is sampled for the ADC
402 to reach a steady state) can be provided for the ADC 402. This may also reduce power consumption.

[0064] After obtaining the set number (N) of successive sampling points 902, the ADC 402 reconstructs a waveform 812 (see Figure 8) of the pulses 808 based on samples obtained at the plurality of successive sampling points 902. Since the sampling rate is lower than a periodic repetitive frequency (PRF) of the signal and the Nyquist rate, the waveform 812 of the signal 806 can be reconstructed at a slower rate compared to e.g. rates of the conventional sampling methods.

[0065] A second pulse 803 of the reset signal 802 is generated by e.g. the baseband of the receiver to set the output of the pulse detecting unit 404 to 'Low' or '0' after the set number (N) of successive sampling points 902 are obtained. The pulse detecting unit 404 may be set to a detection mode to detect new incoming pulses. The pulse detecting unit 404 sends a 'Low' or '0' output to the clock selecting unit 406 to turn off the clock selecting unit 406. As such, no sampling clock signal is sent from the clock selecting unit 406 to the ADC 402. The ADC 402 is thus turned off until new incoming pulses are detected by the pulse detecting unit 404 and a new sampling clock signal is received by the ADC 402. Power consumption can be reduced by turning on the clock selecting unit 406 and the ADC 402 when pulses are detected and turning off the clock selecting unit 406 and the ADC 402 when no pulses are detected.

[0066] Figure 10 shows a more detailed diagram of the reconstructed waveform 812 of the signal 806 in the time domain. Figure 11 shows the reconstructed waveform 812 of the signal 806 in the frequency domain. The reconstructed waveform 812 of the signal 806 has a bandwidth which is given by:
wherein \( BW_{\text{original}} \) is an original bandwidth of the signal, PRF represents the periodic repetitive frequency of the signal, and \( F_{\text{sampling}} \) is the sampling frequency of the signal.

[0067] Assuming that \( BW_{\text{original}} \) of the signal 806 is about 200MHz (as described above with Figure 2) and considering that PRF is about 10MHz and \( F_{\text{sampling}} \) is about 9.901MHz, the bandwidth of the reconstructed waveform 812 of the signal 806 is about 1.98MHz.

[0068] Although the bandwidth of the reconstructed waveform 812 of the signal 806 is lower than the original bandwidth of the signal 806, the shape of the signal 806 is preserved. Further, \( F_{\text{sampling}} \) is much smaller than the original bandwidth of the signal 806 (compared to conventional methods having a sampling frequency which is more than twice the original bandwidth of the signal).

[0069] Figure 12 shows a flowchart 1200 of a method of sampling a signal having a plurality of identically shaped pulses. The pulses may be spaced apart from each other in an equidistant manner. At 1202, the signal may be sampled at a plurality of sampling points. The sampling points are spaced apart from each other in an equidistant manner, and the distance between neighbouring sampling points is chosen such that it is larger than the distance between respective rising edges of neighbouring pulses, and only pulses are sampled at each of a plurality of successive sampling points. At 1204, a waveform of the pulses may be reconstructed based on samples obtained at the plurality of successive sampling points.

[0070] The above described method may provide a simple and low cost method to reduce the sampling rate for sampling a signal having a plurality of identically shaped
pulses. The above described method may be applicable for impulse wideband radio where the interval between pulses of a signal is longer than a pulse width of the pulses. The above described method may be used to sample IR-UWB signals or radar signals. Further, the above described system 400 may provide a simple architecture which requires a single ADC and a smaller area for sampling a signal having a plurality of identically shaped pulses. Power consumption of circuits having the above described system 400 may be reduced. Capacitance load at an input of a circuit having the above described system 400 may be reduced.

[0071] While embodiments of the invention have been particularly shown and described with reference to specific embodiments, it should be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention as defined by the appended claims. The scope of the invention is thus indicated by the appended claims and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced.
What is claimed is:

1. A method of sampling a signal having a plurality of identically shaped pulses, the pulses being spaced apart from each other in an equidistant manner, the method comprising sampling the signal at a plurality of sampling points, wherein:
   - the sampling points are spaced apart from each other in an equidistant manner,
   - the distance between neighbouring sampling points is chosen such that
     a) it is larger than the distance between respective rising edges of neighbouring pulses, and
     b) only pulses are sampled at each of a plurality of successive sampling points.

2. The method of claim 1,

   wherein a first sampling point of the plurality of successive sampling points coincides with a rising edge of a pulse of the signal.

3. The method of claim 1,

   wherein the first sampling point of the plurality of successive sampling points is located after the rising edge of a pulse of the signal.

4. The method of any one of claims 1 to 3,
wherein the number of sampling points of the plurality of successive sampling points is set according to a predetermined sampling resolution of the pulses of the signal.

5. The method of claim 4,

wherein the distance between neighbouring sampling points is set using the formula: [distance = distance between respective raising edges of neighbouring pulses + time value], wherein the time value is determined by dividing a pulse width of a pulse of the signal by the set number of successive sampling points.

6. The method of claims 5 or 6,

wherein the number of sampling points of the plurality of successive sampling points is equal to or larger than 2.

7. The method of claim 6,

wherein the number of sampling points of the plurality of successive sampling points ranges between 2 and 10.

8. The method of claim 6,

wherein the number of sampling points of the plurality of successive sampling points is greater than 10.

9. The method of any one of claims 1 to 8,

wherein the signal is a ranging signal or a communication signal.
10. The method of any one of claims 1 to 9, further comprising reconstructing a waveform of the pulses based on samples obtained at the plurality of successive sampling points.

11. The method of claim 10, wherein the reconstructed waveform of the signal comprises a bandwidth which is given by:

\[ \text{BW}_{\text{original}} \times \frac{(\text{PRF} - \text{F}_{\text{sampling}})}{\text{PRF}}, \]

wherein \( \text{BW}_{\text{original}} \) is an original bandwidth of the signal, PRF represents a periodic repetitive frequency of the signal, and \( \text{F}_{\text{sampling}} \) is a sampling frequency of the signal.

12. A system for sampling a signal having a plurality of identically shaped pulses, the pulses being spaced apart from each other in an equidistant manner, the system comprising:

an analog to digital converter configured to receive the signal and to sample the signal at a plurality of sampling points, wherein:

- the sampling points are spaced apart from each other in an equidistant manner,
- the distance between neighbouring sampling points is chosen such that
  a) it is larger than the distance between respective raising edges of neighbouring pulses, and
  b) only pulses are sampled at each of a plurality of successive sampling points.
13. The system of claim 12, further comprising:
   a clock generating unit configured to generate a plurality of clock signals;
   a pulse detecting unit coupled to the analog to digital converter and being
   configured to detect the plurality of pulses of the signal; and
   a clock selecting unit coupled to the clock generating unit and the pulse detecting
   unit;
   wherein upon detection of the plurality of pulses of the signal, the pulse detecting
   unit is configured to activate the clock selecting unit, and the clock selecting unit is
   configured to select a sampling clock signal from the plurality of clock signals generated
   by the clock generating unit.

14. The system of claim 13,
   wherein the analog to digital converter is coupled to the clock selecting unit and is
   configured to receive the selected sampling clock signal from the clock selecting unit,
   and to sample the signal based on the received sampling clock signal.

15. The system of claims 13 or 14,
   wherein the clock signals generated by the clock generating unit differ from each
   other regarding their phase.
Figure 1
Figure 2

PRF = 10 MHz

BW signal = 200 MHz
Figure 3
Figure 8
Figure 10
\[ \text{Fsampling} = 9.901 \text{MHz} \]

\[ \text{BW}_{\text{reconstructed}} = 1.98 \text{MHz} \]

\[ \text{Fsampling} \ll \text{BW}_{\text{signal}} \]

**Figure 11**
Sampling the signal at a plurality of sampling points

Reconstructing a waveform of the pulses based on samples obtained at the plurality of successive sampling points

Figure 12
INTERNATIONAL SEARCH REPORT

PCT/SG20 10/000 184

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl.
H03K 5/13 (2006.0) H03K 5/135 (2006.0) H03L 7/00 (2006.0)

According to International Patent Classification (IPC) or to both national classification and IPC

B. MINIMUM DATA SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
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<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
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<td>US 4344705 A (KOMPA et al.) 17 August 1982 (col.2 lines 50-5, col.5 line 64-col.6 line 6, Figs. 2, 5)</td>
<td>1-3, 9, 12</td>
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<td>Y</td>
<td>US 6229570 B1 (BUGWADIA et al.) 08 May 2001 (col.2 line 62-col.3 line 18, col.9 lines 55-64, claim 1)</td>
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<td>US 4672639 A (TANABE et al.) 09 June 1987 (col.3 line 15-col.4 line 9, col.8 lines 53-68, Figs. 1, 2, 12)</td>
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