US 20190158135A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2019/0158135 A1**

Ling et al. (43) **Pub. Date: May 23, 2019**

(54) **PHASE NOISE SUPPRESSION**

(71) Applicant: **Maxlinear, Inc.**, Carlsbad, CA (US)

(72) Inventors: **Curtis Ling**, Carlsbad, CA (US); **Sheng Ye**, Carlsbad, CA (US)

(21) Appl. No.: **16/255,881**

(22) Filed: **Jan. 24, 2019**

Related U.S. Application Data

(63) Continuation of application No. 14/918,793, filed on Oct. 21, 2015, now Pat. No. 10,211,868.

(60) Provisional application No. 62/066,591, filed on Oct. 21, 2014.

Publication Classification

(51) **Int. Cl.**

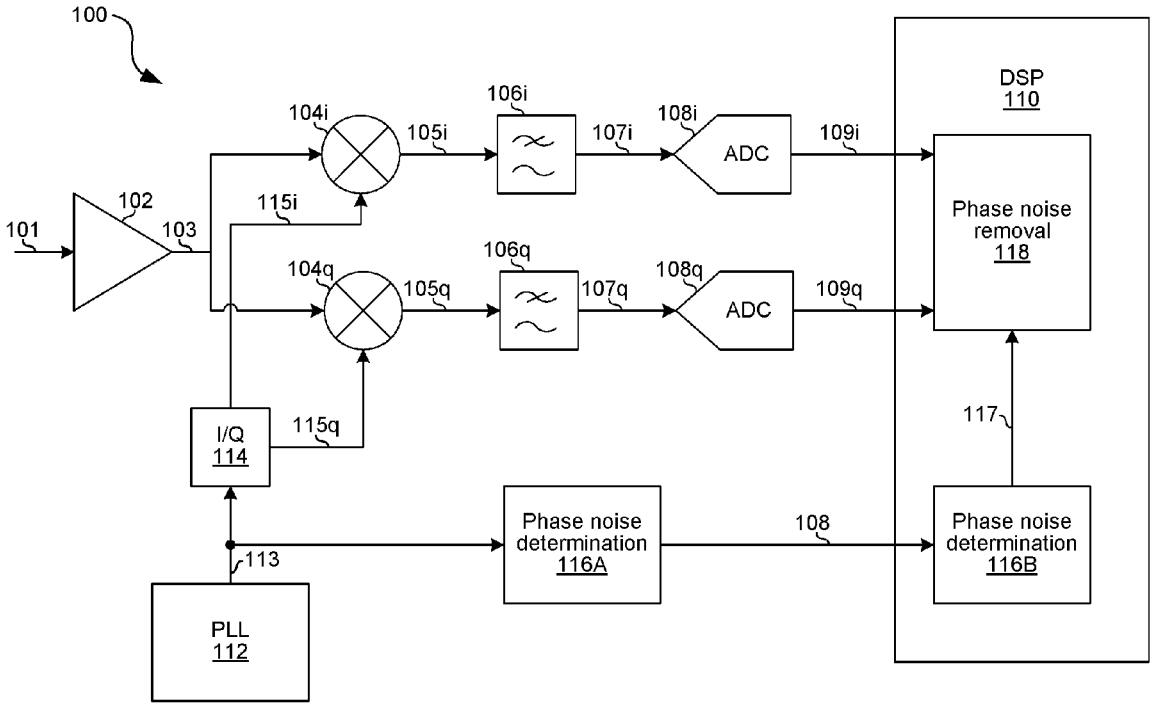
H04B 1/30	(2006.01)
H03F 3/24	(2006.01)
H04B 1/00	(2006.01)

(52) **U.S. Cl.**

CPC ***H04B 1/30*** (2013.01); *H04B 2001/0408* (2013.01); ***H04B 1/0007*** (2013.01); ***H03F 3/24*** (2013.01)

(57) **ABSTRACT**

A transceiver comprises local oscillator circuitry, phase noise determination circuitry, mixing circuitry, and digital signal processing circuitry. The local oscillator circuitry is operable to generate a local oscillator signal. The phase noise determination circuitry is operable to introduce a frequency-dependent phase shift to the local oscillator signal to generate a phase-shifted version of the local oscillator signal. The mixing circuitry is operable to mix the local oscillator signal and the phase-shifted version of the local oscillator to generate a baseband signal having an amplitude proportional to a phase difference between the local oscillator signal and the phase-shifted version of the local oscillator signal. The digital signal processing circuity is operable to process the baseband signal to determine a phase error of the local oscillator signal, and perform signal compensation based on the determined phase error.



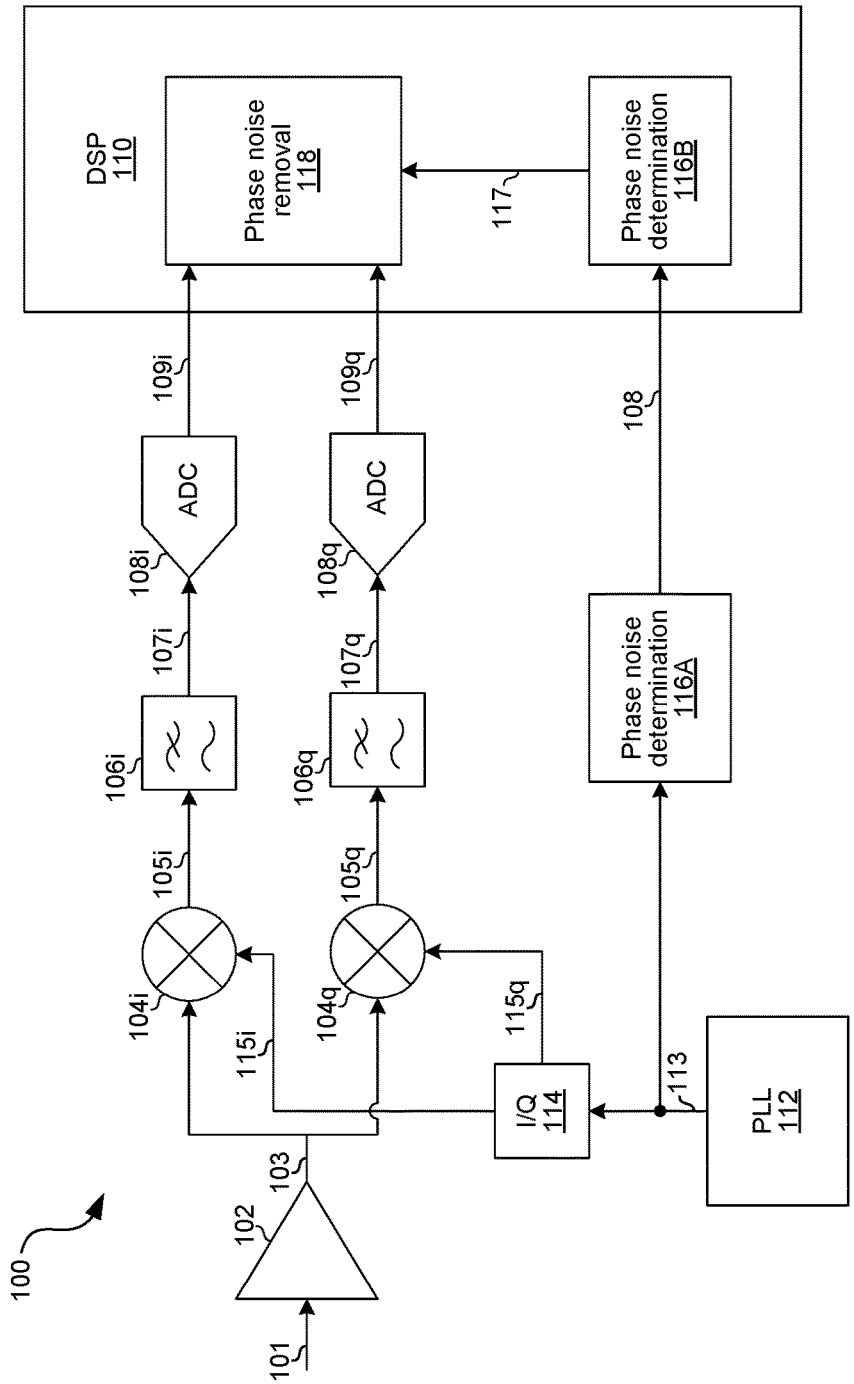

DSP
110
Phase noise
removal
118
Phase noise
determination
116B
117
109i
109q
108
ADC
ADC
108i
108q
107i
107q
Phase noise
determination
116A
106i
106q
105i
105q
104i
104q
115i
115q
I/Q
114
PLL
112
113
103
102
101
100

FIG. 1A

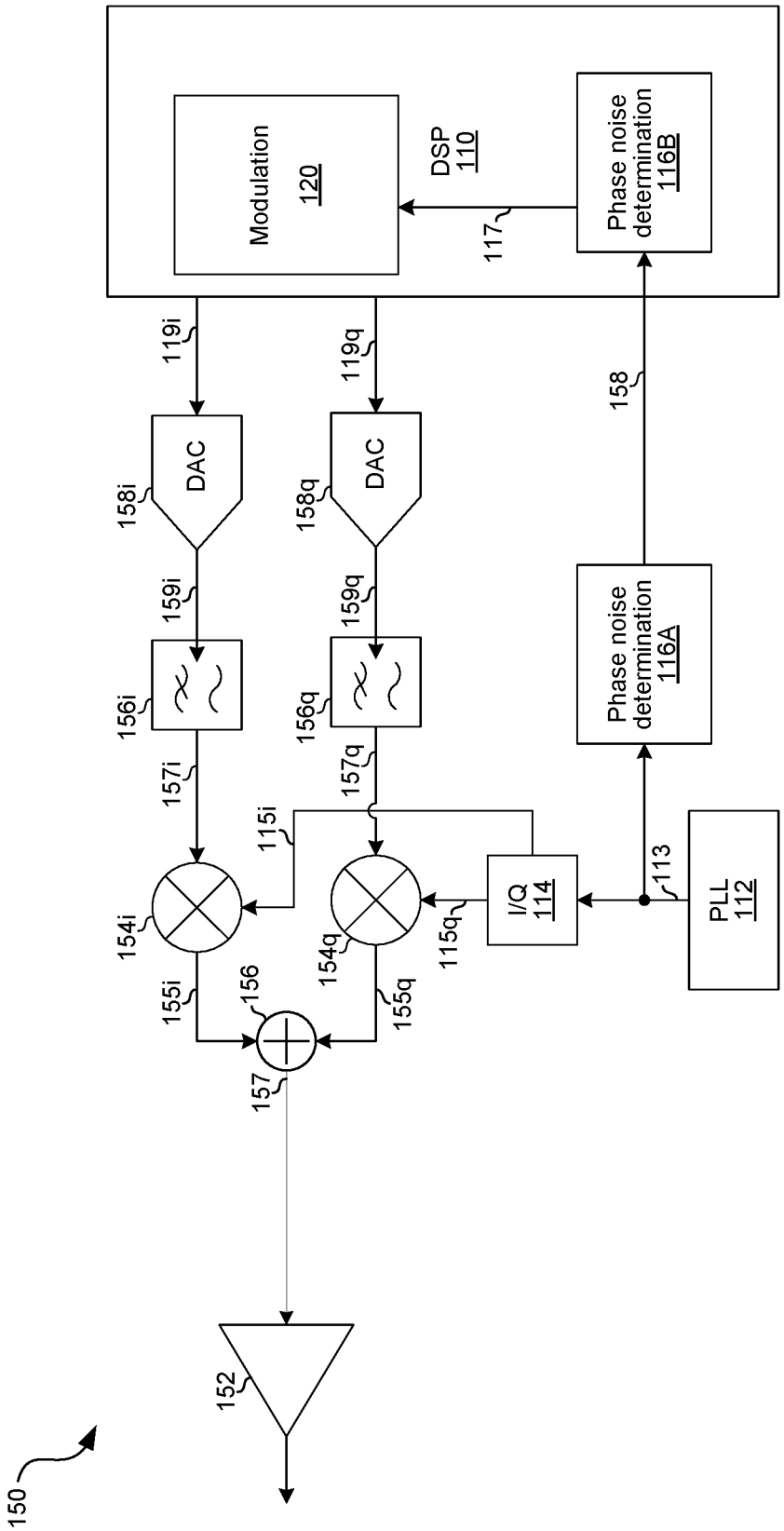

Modulation
120
DSP
110
Phase noise
determination
116B
117
119i
119q
158
DAC
DAC
158i
158q
159i
159q
Phase noise
determination
116A
156i
156q
157i
157q
115i
113
PLL
112
I/Q
114
115q
154i
154q
155i
156
155q
157
152
150

FIG. 1B

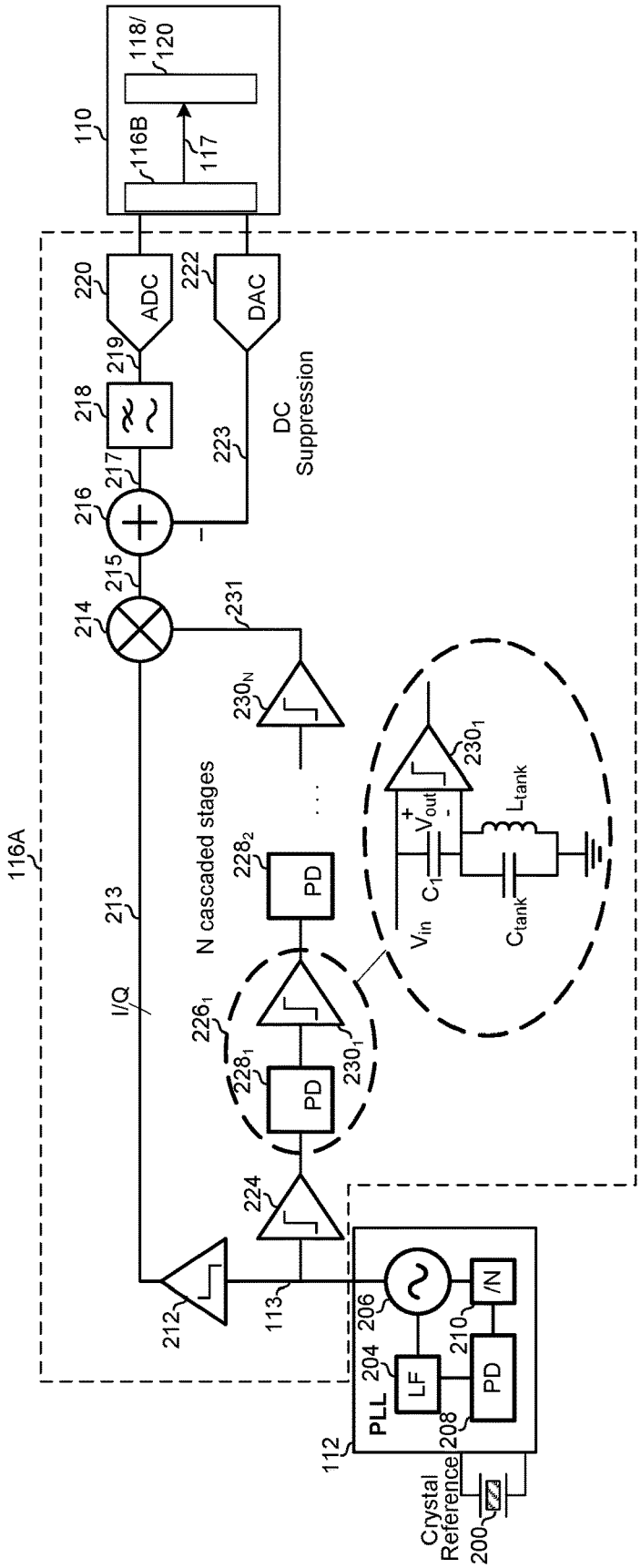

110
118/
120
116B
117
220
ADC
222
DAC
219
218
223
DC
Suppression
217
216
215
214
231
230N
230₁
Vout
Ltank
C1
Vin
Ctank
116A
213
N cascaded stages
228₂
PD
I/Q
226₁
228₁
PD
230₁
224
212
113
206
/N
210
PLL
204
LF
PD
208
112
Crystal
Reference
200

FIG. 2

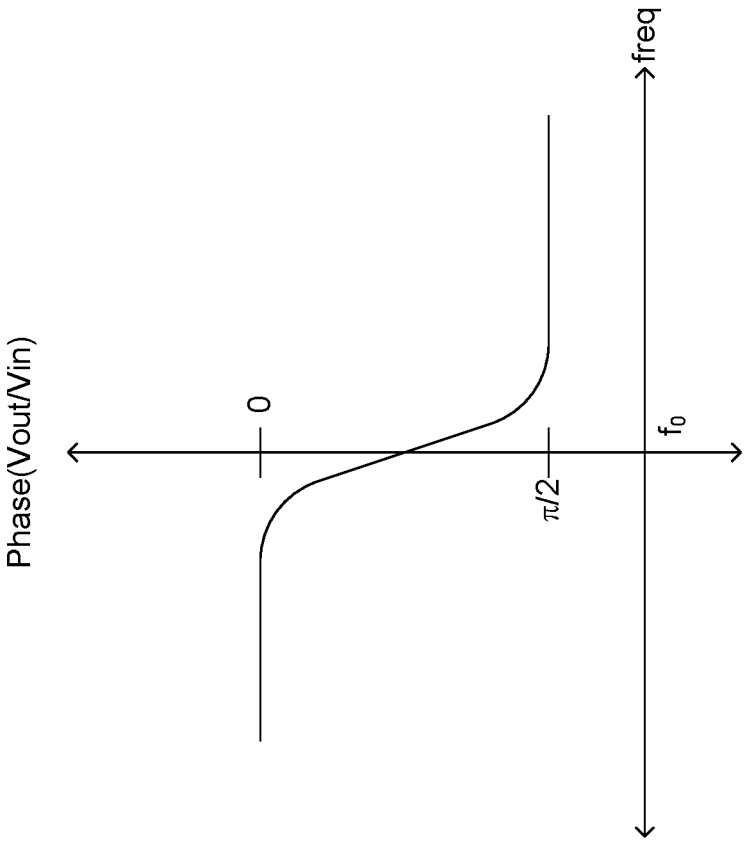


FIG. 3

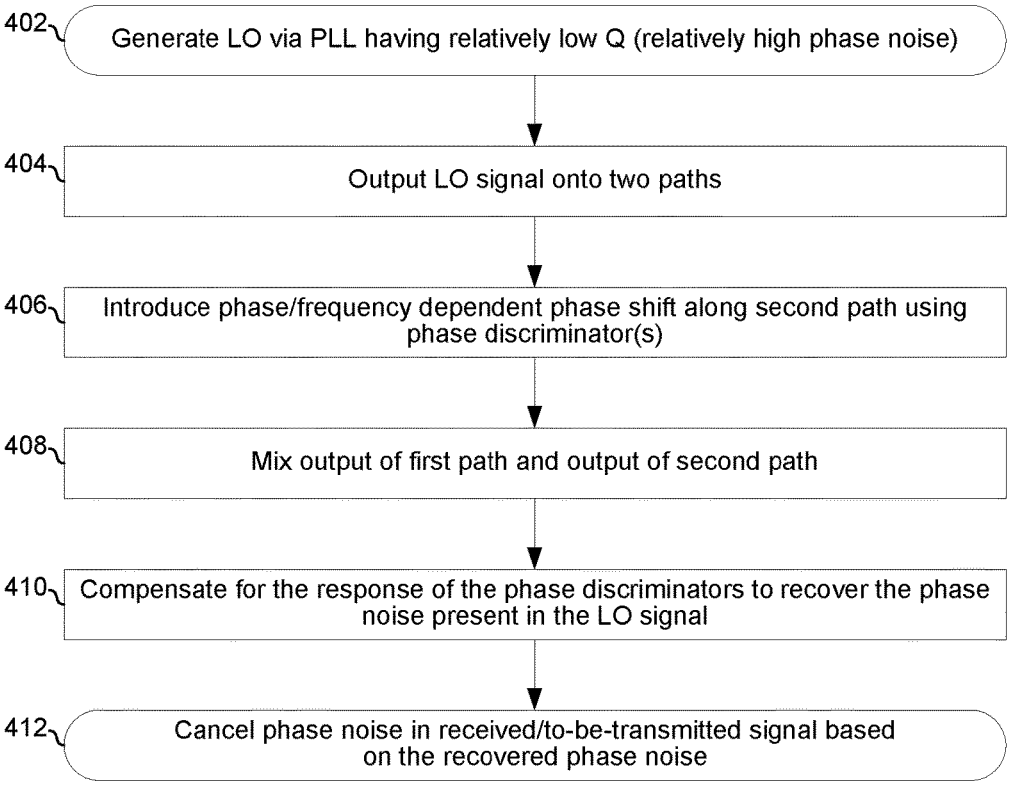

402
Generate LO via PLL having relatively low Q (relatively high phase noise)
404
Output LO signal onto two paths
406
Introduce phase/frequency dependent phase shift along second path using phase discriminator(s)
408
Mix output of first path and output of second path
410
Compensate for the response of the phase discriminators to recover the phase noise present in the LO signal
412
Cancel phase noise in received/to-be-transmitted signal based on the recovered phase noise

FIG. 4

PHASE NOISE SUPPRESSION

PRIORITY CLAIM

[0001] This application claims priority to the following application, which is hereby incorporated herein by reference: U.S. provisional patent application 62/066,591 titled "Phase Noise Suppression" filed on Oct. 21, 2014.

BACKGROUND

[0002] Limitations and disadvantages of conventional methods and systems for handling phase noise will become apparent to one of skill in the art, through comparison of such systems with some aspects of the present invention as set forth in the remainder of the present application with reference to the drawings.

BRIEF SUMMARY

[0003] Systems and methods are provided for phase noise suppression, substantially as shown in and/or described in connection with at least one of the figures, as set forth more completely in the claims.

[0004] These and other advantages, aspects and novel features of the present invention, as well as details of an illustrated embodiment thereof, will be more fully understood from the following description and drawings.

BRIEF DESCRIPTION OF SEVERAL VIEWS OF THE DRAWINGS

[0005] FIG. **1**A is a diagram illustrating portions of an example receiver operable to suppress phase noise in accordance with aspects of this disclosure.

[0006] FIG. **1**B is a diagram illustrating portions of an example transmitter operable to suppress phase noise in accordance with aspects of this disclosure

[0007] FIG. **2** is a diagram illustrating example circuitry for phase noise suppression.

[0008] FIG. **3** depicts the phase transfer function of an example phase discriminator.

[0009] FIG. **4** is a flowchart illustrating an example process for phase noise suppression in accordance with aspects of this disclosure.

DETAILED DESCRIPTION

[0010] FIG. **1**A is a diagram illustrating portions of an example receiver operable to suppress phase noise in accordance with aspects of this disclosure. The receiver **100** comprises an amplifier **102**, mixers **104***i* and **104***q*, filters **106***i* and **106***q*, analog-to-digital converters (ADCs) **108***i* and **108***q*, digital signal processing circuitry (**110**), phase locked loop (PLL) **112**, phase splitter **114**, phase noise determination circuitry **116** (comprising an analog portion **116**A and digital portion **116**B), and phase noise removal circuitry **118**.

[0011] The amplifier **102** comprises circuitry operable to amplify the received signal **101** (e.g., a signal from a microwave backhaul link in the 6 to 42 GHz band) to generate the signal **103**. The mixer **104***i* comprises circuitry operable to mix the in-phase LO signal **115***i* with the signal **103** to generate signal **105***i*, and the mixer **104***q* comprises circuitry operable to mix the quadrature phase LO signal **115***q* with the signal **103** to generate signal **105***q*. The filter **106***i* comprises circuitry operable to filter out undesired frequencies from the signal **105***i*, resulting in signal **107***i*. The filter **106***q* comprises circuitry operable to filter out undesired frequencies from the signal **105***q*, resulting in signal **107***q*. The ADC **108***i* digitizes the signal **107***i* to generate signal **109***i*. The ADC **108***q* digitizes the signal **107***q* to generate signal **109***q*.

[0012] The PLL **112** generates a local oscillator signal **113** which is split into two phases by phase splitter **114**, resulting in in-phase LO signal **115***i* and quadrature-phase LO signal **115***q*.

[0013] The phase noise determination circuitry **116** processes the LO signal **113** to determine phase noise present in the signal **113**, and output an indication of this phase noise as signal **117**.

[0014] The phase noise removal circuit **118** is operable to cancel/compensate phase noise introduced by the signals **115***i* and **115***q* based on the signal **117**. Signal **117** may contain a wide range of signals including desired and undesired (blocking) signals, such as may be the case in receivers which concurrently capture and digitize an entire frequency band containing multiple channels. In such a system, removal of phase noise by block **118** allows the invention to suppress the reciprocal mixing caused by the product of blockers with the phase noise during the down-conversion process.

[0015] FIG. **1**B is a diagram illustrating portions of an example transmitter operable to suppress phase noise in accordance with aspects of this disclosure. The transmitter **150** comprises digital-to-analog converters **158***i* and **158***q*, filters **156***i* and **156***q*, mixers **154***i* and **154***q*, combiner **156**, amplifier **152**, the PLL **112**, the phase splitter **114**, the phase noise determination circuitry **116**, and the phase noise compensation circuitry **118**. The transmitter **150** may reside in the same housing and/or on the same chip as the receiver **100** and components with common reference designators may be shared between the transmitter **150** and receiver **100**.

[0016] The DAC **158***i* comprises circuitry operable to convert the signal **119***i* to analog representation **159***i*. The DAC **158***q* comprises circuitry operable to convert the signal **119***q* to analog representation **159***q*. The filter **156***i* comprises circuitry operable to filter out undesired frequencies from the signal **159***i*, resulting in signal **157***i*. The filter **156***q* comprises circuitry operable to filter out undesired frequencies from the signal **159***q*, resulting in signal **157***q*. The mixer **154***i* comprises circuitry operable to mix the in-phase LO signal **115***i* with the signal **157***i* to generate signal **155***i*, and the mixer **154***q* comprises circuitry operable to mix the quadrature-phase LO signal **115***q* with the signal **157***q* to generate signal **155***q*. The combiner comprises circuitry operable to combine signals **155***i* and **155***q* to generate signal **157** (e.g., a microwave signal in the 6 to 42 GHz band).

[0017] The modulator circuit **120** is operable to receive the estimated phase noise **117** from **116**B and cancel/compensate for phase noise in the modulated transmit waveform prior to upconversion.

[0018] The amplifier **152** comprises circuitry operable to amplify the signal **157** to generate the signal **103** for transmission onto a communication medium (e.g., onto a microwave backhaul link via one or more antennas).

[0019] The PLL **112** generates a local oscillator signal **113** which is split into two phases by phase splitter **114**, resulting in in-phase LO signal **115***i* and quadrature-phase LO signal **115***q*.

[0020] The phase noise determination circuitry **116** processes the LO signal **113** to determine phase noise present in the signal **113**, and output an indication of this phase noise as signal **117**.

[0021] FIG. **2** is a diagram illustrating example circuitry for phase noise suppression. Shown again in FIG. **2** are the PLL **112**, the phase noise determination circuitry **116**, and the phase noise removal circuitry **118**, but with additional details of example implementations of the PLL **112** and phase noise determination circuitry **116**A.

[0022] The PLL **112** uses a crystal oscillator **200** as a reference and comprises a VCO **206**, frequency divider **210**, phase detector **208**, and loop filter **204**. The PLL **112** may operate at the desired carrier frequency (e.g., 42 GHz) or may operate at some harmonic or sub-harmonic thereof, with appropriate frequency multiplication or division then performed to arrive at the desired carrier frequency.

[0023] The digital signal processing circuitry **110** comprises the portion **116**B of the phase noise determination circuitry and may comprise at least a portion of the phase noise removal circuitry **118** and/or modulator **120**.

[0024] The phase noise processing circuitry **116**A comprises limiting amplifiers **212**, **224** and **230**$_1$-**230**$_N$ (N being an integer equal to or greater than 1), phase discriminators **228**$_1$-**228**$_N$, mixer **214**, combiner **216**, filter **218**, ADC **220**, and DAC **222**.

[0025] Each of the limiting amplifiers **212**, **224** and **230**$_1$-**230**$_N$ comprises circuitry operable to amplify its input signal such that its output signal has a desired peak-to-peak voltage. In an example implementation the output of limiting amplifiers **212**, **224** and **230**$_1$-**230**$_N$ may simply saturate to restore full swing between two voltage rails (e.g., VDD and GND). Each of the limiting amplifiers **230**$_1$-**230**$_N$ is paired with a corresponding one of the phase discriminators **228**$_1$-**228**$_N$.

[0026] Each phase discriminator **228**$_n$ comprises circuitry operable to introduce a frequency-dependent phase shift. In the example implementation shown, each phase discriminator **228**$_n$ ($1 \leq n \leq N$) comprises a capacitor C_1, and a tank circuit comprising capacitor C_{tank} and inductor L_{tank}. The phase and amplitude of the output voltage, V_{out} (present across C_1), varies proportionally to the frequency of the input signal V_{in}. The amplitude variation is removed by limiting amplifier **230**$_n$ such that the output of stage **226**$_n$ is equal to the input of stage **226**$_n$ but with a frequency-dependent phase shift, as shown in FIG. **3**. The limiter also provides isolation between stages. Cascading successive stages of phase discriminators **226**$_n$ increases the slope of the phase transfer function, which may make the phase error easier to detect/recover. For each phase discriminator **228**$_n$, the slope of the transfer function around f_0 depends on the quality factor (Q) of the tank formed by C_{tank} and L_{tank}. Accordingly, one way to increase the slope is to increase the Q of the tank. This may be done by, for example, using negative resistances, n-path filter circuits, etc. Another way is to increase N (i.e., increase the number of cascaded stages). These techniques may be used in conjunction with one another. Although adding additional stages may incur a noise penalty, the noise may be relatively low, and numerous stages (e.g., up to 10 or 20 or more) may be tolerated before the additional noise becomes a limiting factor in operation of the phase noise determination circuitry **116**.

[0027] Returning to FIG. **2**, a result of the stages **226**$_1$-**226**$_N$ is that the phase error present in the signal **213** is phase shifted by some amount θ in the signal **231**, where θ depends on its frequency offset from the center frequency of the PLL.

[0028] The mixer **214** mixes signal **213** with signal **231** to generate a baseband signal **215**. Because the signal **231** is just a phase-shifted version of the signal **213**, the amplitude of the signal **215** is proportional to the phase difference between signals **213** and **231**.

[0029] The DC component of signal **215** is suppressed by combiner **216**, resulting in signal **217**. Signal **217** is then filtered by filter **218** before being converted to a digital signal by ADC **220**. The signal output by ADC **220** is thus a digital baseband signal corresponding to a scaled phase difference between the signals **213** and **231**. The phase noise determination circuitry **116**B then compensates for the slope of the phase shift introduced by the one or more stages **226**$_n$, such that the original phase error present in signal **213** is recovered and output as signal **117**.

[0030] FIG. **4** is a flowchart illustrating an example process for phase noise suppression in accordance with aspects of this disclosure. In block **402**, the PLL **112**, having relatively low Q/high phase noise (relative to the demands of the communication system in which the PLL **112** is being used), generates LO signal **113**. In block **404**, the LO signal **113** is output onto two paths (e.g., the first path comprising amplifier **212** and the second path comprising amplifier **224** and stages **228**$_1$-**228**$_N$). In block **406**, one or more phase discriminators (e.g., **228**$_1$-**228**$_N$) introduce a frequency-dependent phase shift to the LO signal. In block **408**, the outputs of the two paths (e.g., signals **213** and **231**) are mixed together (e.g., by mixer **214**). In block **410**, the phase determination circuitry **116**B compensates for the response of the phase discriminator(s) used in block **406** to recover the original phase noise present in the LO signal. In block **412**, the recovered phase noise (e.g., provided via signal **117**) is used to compensate for phase noise present in a received signal or to-be-transmitted signal as a result of the noisy PLL.

[0031] In accordance with an example implementation of this disclosure, a transceiver comprises local oscillator circuitry (e.g., **112**), phase noise determination circuitry (e.g., **116**), mixing circuitry (e.g., **214**, **216**, and **218**), and digital signal processing circuitry (e.g., **110**). The local oscillator circuitry is operable to generate a local oscillator signal (e.g., **113**). The phase noise determination circuitry is operable to introduce a frequency-dependent phase shift to the local oscillator signal to generate a phase-shifted version of the local oscillator signal (e.g., **231**). The mixing circuitry operable to mix the local oscillator signal and the phase-shifted version of the local oscillator to generate a baseband signal (e.g., **219**) having an amplitude proportional to a phase difference between the local oscillator signal and the phase-shifted version of the local oscillator signal. The digital signal processing circuity is operable to process the baseband signal to determine a phase error of the local oscillator signal, and perform signal compensation based on the determined phase error. The phase noise determination circuitry may comprises a phase discriminator (e.g., **228**$_1$) cascaded with a limiting amplifier (e.g., **230**$_1$). The phase discriminator may comprise a capacitive inductive tank circuit. The phase noise determination circuitry may comprise a multi-stage phase discriminator (e.g., **226**$_1$-**226**$_N$). Each stage of the multi-stage phase discriminator may comprise a phase discriminator and a limiting amplifier. One or more limiting amplifiers may be operable to restore levels

of the local oscillator signal and the phase-shifted version of the local oscillator signal prior to the mixing of the local oscillator signal and the phase-shifted version of the oscillator signal. The digital signal processing circuitry may be operable to remove the frequency-dependent phase shift from the baseband signal to determine the phase error of the local oscillator signal. The signal compensation may comprise removal of phase error from a received signal (e.g., **109***i* or **109***q*) downconverted using the local oscillator signal. The signal compensation may comprise compensation of a signal (e.g., **119**I or **119**Q) to be upconverted using the local oscillator signal. The system may comprise direct current (DC) suppression circuitry operable to suppress a DC component of the baseband signal.

[0032] In accordance with an example implementation of this disclosure, a transceiver comprises local oscillator circuitry (e.g., **112**), analog circuitry (e.g., **116**A), and digital circuitry (e.g., **110**). The local oscillator circuitry is operable to generate a local oscillator signal (e.g., **113**) having phase error. The analog circuitry includes one or more phase discriminators (e.g., **228**) and a mixer (e.g., **214**), operable to generate a signal representative of the phase error of the local oscillator signal. The digital circuitry is operable to perform signal compensation based on the signal representative of the phase error. The analog circuitry may be operable to introduce, via the one or more phase discriminators, a frequency-dependent phase shift to the local oscillator signal to generate a phase-shifted local oscillator signal (e.g., **231**). The analog circuitry may be operable to mix, via the mixer, the local oscillator signal and the phase-shifted version of the local oscillator signal. The digital circuitry may be operable to compensate the signal representative of the phase error based on the frequency-dependent phase shift.

[0033] The present method and/or system may be realized in hardware, software, or a combination of hardware and software. The present methods and/or systems may be realized in a centralized fashion in at least one computing system, or in a distributed fashion where different elements are spread across several interconnected computing systems. Any kind of computing system or other apparatus adapted for carrying out the methods described herein is suited. A typical combination of hardware and software may be a general-purpose computing system with a program or other code that, when being loaded and executed, controls the computing system such that it carries out the methods described herein. Another typical implementation may comprise an application specific integrated circuit or chip. Some implementations may comprise a non-transitory machine-readable (e.g., computer readable) medium (e.g., FLASH drive, optical disk, magnetic storage disk, or the like) having stored thereon one or more lines of code executable by a machine, thereby causing the machine to perform processes as described herein.

[0034] While the present method and/or system has been described with reference to certain implementations, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted without departing from the scope of the present method and/or system. In addition, many modifications may be made to adapt a particular situation or material to the teachings of the present disclosure without departing from its scope. Therefore, it is intended that the present method and/or system not be limited to the particular implementations disclosed, but that the present method and/or system will include all implementations falling within the scope of the appended claims.

[0035] As utilized herein the terms "circuits" and "circuitry" refer to physical electronic components (i.e. hardware) and any software and/or firmware ("code") which may configure the hardware, be executed by the hardware, and or otherwise be associated with the hardware. As used herein, for example, a particular processor and memory may comprise a first "circuit" when executing a first one or more lines of code and may comprise a second "circuit" when executing a second one or more lines of code. As utilized herein, "and/or" means any one or more of the items in the list joined by "and/or". As an example, "x and/or y" means any element of the three-element set {(x), (y), (x, y)}. In other words, "x and/or y" means "one or both of x and y". As another example, "x, y, and/or z" means any element of the seven-element set {(x), (y), (z), (x, y), (x, z), (y, z), (x, y, z)}. In other words, "x, y and/or z" means "one or more of x, y and z". As utilized herein, the term "exemplary" means serving as a non-limiting example, instance, or illustration. As utilized herein, the terms "e.g.," and "for example" set off lists of one or more non-limiting examples, instances, or illustrations. As utilized herein, circuitry is "operable" to perform a function whenever the circuitry comprises the necessary hardware and code (if any is necessary) to perform the function, regardless of whether performance of the function is disabled or not enabled (e.g., by a user-configurable setting, factory trim, etc.).

What is claimed is:

1-20. (canceled)

21. A system comprising:

a local oscillator operable to generate a local oscillator signal;

an amplifier circuit operable to add a phase-shift to the local oscillator signal to generate a phase-shifted local oscillator signal, wherein the phase-shift is frequency-dependent;

a mixer operable to mix the local oscillator signal and the phase-shifted local oscillator signal to generate a baseband signal having an amplitude proportional to a phase difference between the local oscillator signal and the phase-shifted local oscillator signal; and

a digital signal processor (DSP) operable to compensate a received signal based on a phase error of the local oscillator signal, wherein the DSP is operable to determine the phase error of the local oscillator signal according to the baseband signal.

22. The system of claim **21**, wherein the amplifier circuit comprises a limiting amplifier.

23. The system of claim **21**, wherein the amplifier circuit comprises a phase discriminator.

24. The system of claim **21**, wherein the amplifier circuit comprises a multi-stage phase discriminator.

25. The system of claim **24**, wherein each stage of the multi-stage phase discriminator comprises a phase discriminator and a limiting amplifier.

26. The system of claim **21**, wherein the system comprises one or more limiting amplifiers operable to restore levels of the local oscillator signal and the phase-shifted version of the local oscillator signal prior to the mixing of the local oscillator signal and the phase-shifted version of the oscillator signal.

27. The system of claim **21**, wherein the DSP is operable to remove the frequency-dependent phase shift from the baseband signal to determine the phase error of the local oscillator signal.

28. The system of claim **21**, wherein the received signal is generated by a downconversion using the local oscillator signal.

29. The system of claim **21**, wherein the received signal is upconverted by the local oscillator signal.

30. The system of claim **21**, wherein the system comprises direct current (DC) suppression circuit operable to suppress a DC component of the baseband signal.

31. A method comprising:

generating, by local oscillator circuitry, a local oscillator signal;

introducing, by an amplifier circuit, a frequency-dependent phase shift to the local oscillator signal to generate a phase-shifted version of the local oscillator signal;

mixing the local oscillator signal and the phase-shifted version of the local oscillator to generate a baseband signal having an amplitude proportional to a phase difference between the local oscillator signal and the phase-shifted version of the local oscillator signal;

processing, by a digital signal processor (DSP), the baseband signal to determine a phase error of the local oscillator signal; and

performing, by the DSP, signal compensation based on the determined phase error.

32. The method of claim **31**, wherein the method comprises restoring, by one or more limiting amplifiers, levels of the local oscillator signal and the phase-shifted version of the local oscillator signal prior to the mixing the local oscillator signal and the phase-shifted version of the oscillator signal.

33. The method of claim **31**, wherein the method comprises removing, by the DSP, the frequency-dependent phase shift from the baseband signal to determine the phase error of the local oscillator signal.

34. The method of claim **31**, comprising:

downconverting a received signal using the local oscillator signal; and

removing phase error from the downconverted received signal based on the determined phase error.

35. The method of claim **31**, comprising:

compensating a signal to be transmitted based on the determined phase error; and

upconverting the compensated signal to be transmitted using the local oscillator signal.

36. The method of claim **31**, comprising generating, by the DSP, a direct current (DC) suppression signal for suppressing a DC component of the baseband signal.

37. A system comprising:

a local oscillator operable to generate a local oscillator signal having phase error;

an analog circuit, including one or more phase discriminators and a mixer, operable to generate a signal representative of the phase error; and

a digital signal processor (DSP) operable to perform signal compensation based on the signal representative of the phase error.

38. The system of claim **37**, wherein the analog circuit is operable to introduce, via the one or more phase discriminators, a frequency-dependent phase shift to the local oscillator signal to generate a phase-shifted local oscillator signal.

39. The system of claim **38**, wherein the analog circuitry is operable to mix, via the mixer, the local oscillator signal and the phase-shifted version of the local oscillator signal.

40. The system of claim **37**, wherein the DSP is operable to compensate the signal representative of the phase error based on the frequency-dependent phase shift.

* * * * *