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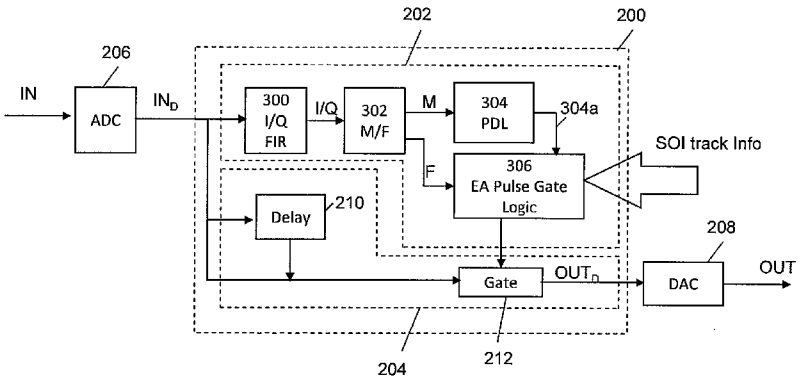

FIG. 2

(57) Abstract: A signal repeater (200) includes a signal processing part (202) and a signal repeating part (204). The signal processing part includes a converter (300) configured to receive an input signal and to convert the input signal into quadrature signals, and a processor (302, 304, 306) configured to process the quadrature signals to determine one or more characteristics of the input signal, and to compare the one or more characteristics of the input signal and a plurality of predetermined characteristics to generate a comparison result. The signal repeating part (204) is configured to selectively repeat the input signal as a repeated signal in accordance with the comparison result.

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WIDEBAND LOW LATENCY REPEATER AND METHODS

FIELD

[0001] Aspects of the present disclosure generally relate to radar systems, and, more specifically, to signal repeaters for electronic attack systems and methods.

BACKGROUND

[0002] In modern warfare, radar guided weapons are widely deployed. For example, a radar guided missile can home in on an enemy target from a great distance at a high rate of speed. Therefore, slow moving targets such as surface ships are highly vulnerable to radar guided missiles due to their relatively slow maneuvering speed. Accordingly, surface ships or other slow moving or stationary platforms have been equipped with advanced defense system that can provide electronic attack/self protect capabilities against radar guided weapons. Such a defense system should be able to take immediate and appropriate responses to the radar signals emitted by fast approaching missiles or other radar guided weapons.

[0002a] Throughout this specification the word "comprise", or variations such as "comprises" or "comprising", will be understood to imply the inclusion of a stated element, integer or step, or group of elements, integers or steps, but not the exclusion of any other element, integer or step, or group of elements, integers or steps.

[0002b] Any discussion of documents, acts, materials, devices, articles or the like which has been included in the present specification is not to be taken as an admission that any or all of these matters form part of the prior art base or were common general knowledge in the field relevant to the present disclosure as it existed before the priority date of each claim of this application.

SUMMARY

[0003] A signal repeater is provided. The signal repeater includes a signal processing part and a signal repeating part. The signal processing part includes a converter configured to receive an input signal and to convert the input signal into quadrature signals, and a processor configured to process the quadrature signals to determine one

or more characteristics of the input signal and to compare the one or more characteristics of the input signal with a plurality of predetermined characteristics to generate a comparison result. The signal repeating part is configured to selectively repeat the input signal as a repeated signal in accordance with the comparison result.

[0004] A method for operating a signal repeater is provided. The method includes: receiving an input signal and converting the input signal into quadrature signals; processing the quadrature signals to determine one or more characteristics of the input signal, and to compare the one or more characteristics of the input signal with a plurality of predetermined characteristics to generate a comparison result; and selectively repeating the input signal as a repeated signal in accordance with the comparison result.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] The above and other features of the present disclosure will become more apparent by describing in detail embodiments thereof with reference to the attached drawings.

[0006] FIG. 1 is a block diagram of a signal repeater with a quench path and a repeater path according to an embodiment of the present disclosure.

[0007] FIG. 2 is a block diagram conceptually illustrating the signal repeater of FIG. 1 in more details according to an embodiment of the present disclosure.

[0008] FIG. 3 is a block diagram conceptually illustrating a magnitude and frequency processor of the signal repeater of FIG. 2 according to an embodiment of the present disclosure.

[0009] FIG. 4 is a block diagram conceptually illustrating a delay of the signal repeater of FIG. 2 according to an embodiment of the present disclosure.

[0010] FIG. 5 is a flowchart illustrating a method of operating a signal repeater according to an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0011] Embodiments of the present disclosure are directed to a signal repeater that can support functions such as electronic attack (EA) technique, low latency threat

emitter measurements for inhibiting EA on non-threat emitters, and realistic and flexible radar reflection synthesis. Generally known implementations of signal repeaters have been based on RF analog design, which are generally inflexible and have very restricted threat emitter measurement capabilities. According to embodiments of the present disclosure, a signal repeater can augment a legacy system such as an integrated receiver techniques generator (IRTG) to provide EA capabilities for threats requiring relatively low latency. However, the present disclosure is not limited to IRTG applications. In addition, the signal repeater of the present disclosure enables EA on a current received pulse to cope with frequency agility and to enable first pulse response.

[0012] FIG. 1 is a block diagram of a signal repeater 100 according to an embodiment of the present disclosure. The signal repeater 100 includes two paths: a quench path 101 and a repeater path 102. Both the quench path 101 and the repeater path 102 receive an input signal. The quench path 101 processes the input signal in the digital domain and performs emitter signal measurements on the input signal. If the measurements do not agree with preselected *a priori* information (e.g., predetermined characteristics), then the repeater path 102 is inhibited (or quenched). When the repeater path 102 is inhibited, the input signal is not repeated by the repeater path 102. In other words, the quench path 101 controls the repeater path 102 to selectively repeat the input signal.

[0013] FIG. 2 is a block diagram conceptually illustrating a signal repeater 200 according to an embodiment of the present disclosure. Referring to FIG. 2, the signal repeater 200 includes a signal processing part 202 and a signal repeating part 204. An analog input signal IN (e.g., an IF signal) is converted to its corresponding digital signal IN_D by an analog-to-digital converter (ADC) 206. Then, the digital signal IN_D is processed by the signal processing part 202 and selectively repeated by the signal repeating part 204 as an output signal OUT_D under the control of the signal processing part 202. The digital output signal OUT_D can be converted back to an analog signal OUT by a suitable digital-to-analog converter (DAC) 208. The signal repeating part 204 has relatively low latency (e.g., a few nanoseconds), except for a delay 210, which will be described in more detail below. The signal processing part 202 performs various

functions such as pulse detect and magnitude/frequency measurement functions, which introduce some latency (generally less than 30 nanoseconds in several embodiments).

[0014] The signal processing part 202 is provided with *a priori* information (e.g., signal of interest tracking information, hereafter "SOI track info") corresponding to the predetermined characteristics of the signals to be detected. The SOI track info enables the signal processing part 202 to recognize signals from predetermined hostile emitters, and can be provided by any suitable sources such as an IRTG. Provided with the SOI track info, the signal processing part 202 can determine whether the received signal IN comes from a friendly emitter or a hostile emitter. If the received signal IN is determined to be from a friendly emitter, the signal processing part 202 is configured to control the signal repeating part 204 such that the input signal IN_D is not repeated (i.e., inhibited or quenched) as the output signal OUT_D at the output of the signal repeating part 204.

[0015] In FIG. 2, the signal repeating part 204 includes a gate 212 that is controlled by the signal processing part 202. The signal processing part 202 outputs a control signal to enable or disable the gate 212. When the gate 212 is enabled, the input signal IN_D is repeated as the output signal OUT_D. Therefore, when the received input signal IN is determined to be from a hostile emitter, the gate 212 is enabled so that the signal repeating part 204 can repeat the signal at the output thereof. The signal processing part 202 and the signal repeating part 204 will be described in more detail below.

[0016] Still referring to FIG 2, the signal processing part 202 includes an I/Q FIR 300, a magnitude/frequency (M/F) processor 302, a pulse detect logic (PDL) 304, and an EA pulse gate logic (PGL) 306. The I/Q FIR 300 (e.g., a short non-decimated quadrature FIR) receives and converts the digitized IN_D signal into corresponding I and Q signals for further processing. The M/F processor 302 calculates the magnitude (M) and frequency (F) of the input signal from the I and Q signals. The PDL 304 receives the magnitude (M) and is configured to detect the presence of a signal pulse in the input signal IN that corresponds to a preselected pulse profile according to the SOI track info. The EA PGL 306 receives a pulse presence signal 304a, which indicates a signal pulse is detected, from the PDL 304 and the frequency (F) from the M/F processor 302. The pulse presence signal 304a and the frequency (F) are compared with a number of

parameters (e.g., predicted pulse gate, jitter, frequency ranges, pulse amplitude, etc.) of the SOI track info to determine whether the input signal IN is from a friendly emitter or a hostile emitter.

[0017] FIG. 3 is a block diagram of the M/F processor 302 according to an embodiment of the present disclosure. The M/F processor 302 calculates the magnitude and frequency of the input signal IN from the I and Q samples of the signal. The I and Q samples can be represented in an exponential format such as $Ae^{(j2\Pi*f*Ts*n)}$, which can be interpreted as a rotating vector with a variable *n*, where A = amplitude (or magnitude), f = frequency , Ts = sample period (second), n = n^{th} sample (or sample index number in a series of samples). Using the exponential format, a constant expression, $A2e^{(j2\Pi*f*Ts)}$, can be calculated by conjugate multiplying a current I/Q sample with a previous I/Q sample. Then, the phase of the input signal IN can be determined as phase = $ATAN(Q/I)$, and frequency can be scaled from the phase.

[0018] Referring to FIG. 3, a magnitude calculation block 400 is configured to calculate the magnitude (M) of the input signal IN based on the IQ samples. An IQ multiply block 402 and a delay 403 are configured to perform conjugate multiply of a current IQ sample and a previous IQ sample. While FIG. 3 illustrates the input and output connections of the magnitude calculation block 400 and the IQ multiply block 402 with single lines for clarity, each of the single lines represents multiple branches (e.g., eight branches). For each branch of the IQ samples, the magnitude calculation block 400 estimates the magnitude of the signal as Magnitude = L + S/2, where L = largest of $|I|$ or $|Q|$, and S = smallest of $|I|$ or $|Q|$. The above described estimation of the magnitude can provide an accuracy of about six percent. Then, an average magnitude of the magnitudes of all the magnitude branches (e.g., eight branches) are calculated by an averaging circuit 404 to generate an average sample magnitude. However, the present disclosure is not limited to the above described estimation method, and other suitable estimation methods can be used.

[0019] Still referring to FIG. 3, the input IQ samples include polyphase samples. At the output of the IQ multiply block 402, respective I and Q parts of the polyphase samples are obtained. Here, frequency of the input signal IN can be calculated from the values of the I and Q parts. In order to improve the signal-to-noise ratio (SNR) to be

greater than about six dB or so for reliable results, the effective SNR can be improved for weak signals in the wide bandwidth by averaging multiple samples (e.g., eight samples) of the I parts and Q parts by averaging circuits 406 and 408, respectively. With the calculated average I and Q, the M/F processor 302 includes a frequency logic 410 configured to calculate the phase of the input signal. Because the phase can be expressed in terms of frequency as $Phase = 2\Pi * f * Ts$ (where Ts is sampling period), the average frequency of the input signal can be calculated as $f = Phase/2\Pi * Ts$.

[0020] FIG. 4 is a block diagram conceptually illustrating the delay 210 according to an embodiment of the present disclosure. In FIG. 4, the delay 210 is implemented as a tap delay that includes multiple programmable delay blocks (500a–500n), scalers (K_1–K_n), a combiner 502, and an adder 504. The delay 210 can be configured to add at least one clock latency to the signal repeating part 204 (see FIG. 2). In one embodiment, the delay blocks (500a–500n) can be implemented with block RAMs (e.g., dual port RAM) to generate different delays or latencies that can be programmable. The scalers (K_1–K_n) scale the signals from the delay blocks (500a–500n) according to their corresponding scaling factors (e.g., K_1, K_2 … K_n). The combiner 502 combines the scaled signals to generate a combined signal, which is added to a undelayed scaled (e.g., K_{00}) input signal to synthesize a realistic radar return from the single received pulse. In one embodiment, the delay 210 includes sixteen delay blocks and sixteen scalers.

[0021] With the delay 210, the signal repeating part 204 can simulate realistic radar return signals that include individual reflections from various aspects of the targeted structure, which in turn occur at slightly different ranges or delays. Therefore, the programmable delay blocks (500a–500n) of the delay 210 can simulate structure reflections (relative delays) and their combinations. However, the present disclosure is not limited to the delay 210 as illustrated in FIG. 4. In several embodiments, other suitable delay configurations may be used. In some embodiments, the delay 210 may not be included or used. It should be appreciated that while the signal repeater 200 is described above in terms of a number of functional blocks and units, the signal repeater 200 is not limited thereto. To the contrary, the signal repeater 200 can include other parts or components that are commonly known in the art. Further, the various

components of the signal repeater 200 can be implemented by a single circuit component (e.g., FPGA) or multiple circuit components operatively coupled together.

[0022] In several embodiments, the signal repeater 200 can be operated in two modes. In a first mode, a threat signal-of-interest (SOI) is being tracked in time by a suitable tracker (e.g., IRTG Tracker). The tracker predicts the occurrence of future pulses of a pulse train. A Time Gate is generated that spans the time extent of a predicted future pulse. This Time Gate is utilized to pass signals that occur within the Time Gate and inhibit signals that occur outside the Time Gate. Typical radars exhibit a duty factor (portion of the total time the radar is transmitting) of less than one percent, so that the Time Gate can inhibit the preponderance of undesired signals. For Frequency Agile radars, the radio frequency (RF) of the emitted signal is random so it cannot be predicted from the tracker. The RF is measured in the quench path when a pulse is detected, along with other parameters such as pulse width. These measurements on a received pulse are input to the EA Pulse Gate Logic where it is reconciled with the SOI Track Info. If the pulse measurements do not agree with the SOI Track Info, the repeater path is quenched (inhibited).

[0023] In the second mode, the SOI is not tracked in time, so the pulse Time Gate is not available, and the measurements are wide open in time. This mode can be used for the situation where EA is performed on the first radar pulses emitted, i.e. pulses that occur before the IRTG can establish a track. Nonetheless, measurements are then performed on every received pulse. These pulse measurements are reconciled with SOI Track Info as before in mode one. The SOI Track Info also includes track information on all visible emitters that is used to inhibit jamming non-threat emitters, thus simplifying the recognition of a new threat SOI.

[0024] FIG. 5 is a flowchart illustrating a method of operating a signal repeater according to an embodiment of the present disclosure. In block S10, the signal repeater is operated to receive and convert an input signal into quadrature signals. In block S20, the signal repeater is operated to process the quadrature signals to determine one or more characteristics of the input signal, and to compare the one or more characteristics of the input signal with a plurality of predetermined characteristics (e.g., a pulse gate, a frequency range, a pulse amplitude, etc.) to generate a comparison result. In block S30,

the signal repeater is operated to selectively repeat the input signal as a repeated signal in accordance with the comparison result.

[0025] According to embodiments of the present disclosure, a digital wideband repeater with relatively low latency quench/inhibit functions as compared to the related art can be provided. Low latency signal parameter measurements and processing are facilitated by converting the signal of interest into corresponding I and Q parts by a suitable digital quadrature FIR. Then, the frequency of the signal can be efficiently derived from a conjugate multiply which in turn is I/Q averaged to improve wideband SNR by about seven dB, prior to the arc-tangent calculation that requires at least six dB SNR. Magnitude of the signal is approximated and is also averaged. The calculated frequency is reconciled with an *a priori* input for possible quench action.

[0026] In the above described embodiments, the process or method can perform the sequence of actions in a different order. In another embodiment, the process or method can skip one or more of the actions. In other embodiments, one or more of the actions are performed simultaneously or concurrently. In some embodiments, additional actions can be performed.

[0027] While the above description contains many specific embodiments of the disclosure, these should not be construed as limitations on the scope of the disclosure, but rather as examples of specific embodiments thereof. Accordingly, the scope of the disclosure should be determined not by the embodiments illustrated, but by the appended claims and their equivalents.

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WHAT IS CLAIMED IS:

1. A signal repeater comprising:

a signal processing part comprising:

a converter configured to receive an input signal and to convert the input signal into quadrature signals; and

a processor configured to: process the quadrature signals to determine one or more characteristics of the input signal, and to compare the one or more characteristics of the input signal with a plurality of predetermined characteristics to generate a comparison result; and

a signal repeating part configured to selectively repeat the input signal as a repeated signal in accordance with the comparison result.

2. The signal repeater of claim 1, wherein the converter comprises a quadrature FIR configured to generate the quadrature signals.

3. The signal repeater of claims 1 or 2, wherein the processor is configured to calculate a magnitude and a frequency of the input signal in accordance with the quadrature signals.

4. The signal repeater of claim 3, wherein the processor is configured to calculate the frequency of the input signal by conjugate-multiplying a current sample of the quadrature signals with a previous sample of the quadrature signals.

5. The signal repeater of claim 3 or 4, wherein the processor is configured to calculate the magnitude of the input signal according to an equation defined as

Magnitude = L + S/2, where L = largest of | I | or | Q | of the quadrature signals, and S = smallest of | I | or | Q | of the quadrature signals.

6. The signal repeater of any one of the preceding claims, wherein the quadrature signals comprise a plurality of polyphase samples, and the processor is

configured to calculate a magnitude and a frequency for each of the plurality of polyphase samples, and to calculate an average magnitude and an average frequency based on the magnitudes and the frequencies of the plurality of polyphase samples.

7. The signal repeater of any one of the preceding claims, wherein the plurality of predetermined characteristics comprise at least one of a pulse gate, a frequency range, or a pulse amplitude.

8. The signal repeater of any one of the preceding claims, wherein the signal repeating part is configured to inhibit the input signal when the characteristics of the input signal do not correspond to the plurality of predetermined characteristics.

9. The signal repeater of any one of the preceding claims, wherein the signal repeating part is configured to repeat the input signal when at least one of the characteristics of the input signal matches a corresponding one of the plurality of predetermined characteristics.

10. The signal repeater of any one of the preceding claims, wherein the signal repeating part further comprises a delay configured to delay the input signal by different latencies.

11. A method for operating a signal repeater, the method comprising:

receiving an input signal and converting the input signal into quadrature signals;

processing the quadrature signals to determine one or more characteristics of the input signal, and to compare the one or more characteristics of the input signal with a plurality of predetermined characteristics to generate a comparison result; and

selectively repeating the input signal as a repeated signal in accordance with the comparison result.

12. The method of claim 11, further comprising operating a quadrature FIR to convert the input signal into the quadrature signals.

13. The method of claims 11 or 12, further comprising calculating a magnitude and a frequency of the input signal in accordance with the quadrature signals.

14. The method of claim 13, wherein the frequency of the input signal is calculated by conjugate-multiplying a current sample of the quadrature signals with a previous sample of the quadrature signals.

15. The method of claim 13 or 14, wherein the magnitude of the input signal is calculated according to an equation defined as

Magnitude = L + S/2, where L = largest of | I | or | Q | of the quadrature signals, and S = smallest of | I | or | Q | of the quadrature signals.

16. The method of any one of claims 11 to 15, wherein the quadrature signals comprise a plurality of polyphase samples, and the method further comprises:

calculating a magnitude and a frequency for each of the plurality of polyphase samples; and

calculating an average magnitude and an average frequency based on the magnitudes and the frequencies of the plurality of polyphase samples.

17. The method of any one of claims 11 to 16, wherein the plurality of predetermined characteristics comprise at least one of a pulse gate, a frequency range, or a pulse amplitude.

18. The method of any one of claims 11 to 17, further comprising inhibiting the input signal when the characteristics of the input signal do not correspond to the plurality of predetermined characteristics.

19. The method of any one of claims 11 to 18, wherein the selectively repeating the input signal comprises repeating the input signal when at least one of the characteristics of the input signal matches a corresponding one of the plurality of predetermined characteristics.

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20. The method of any one of claims 11 to 19, further comprising delaying the input signal by different latencies.

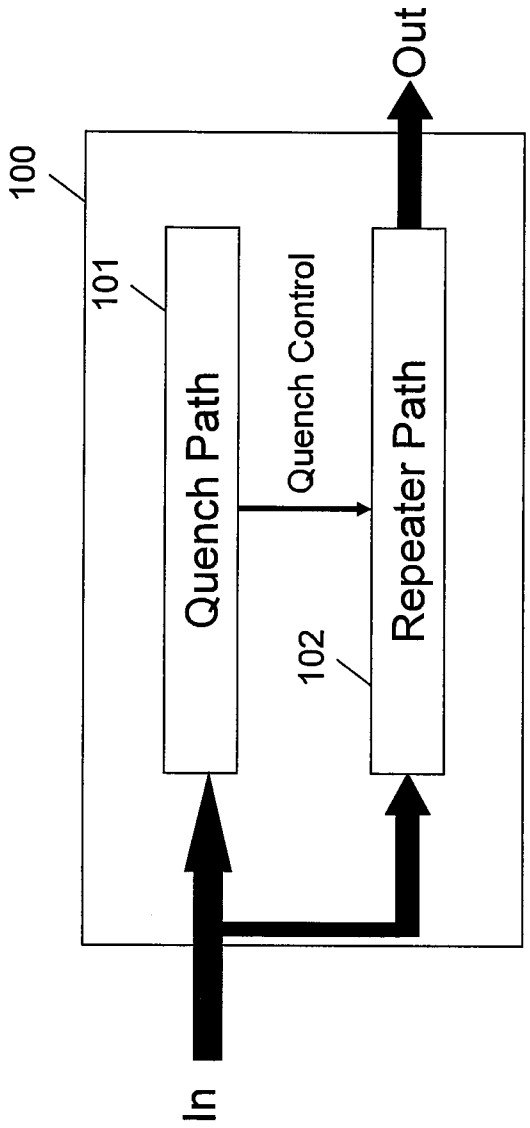
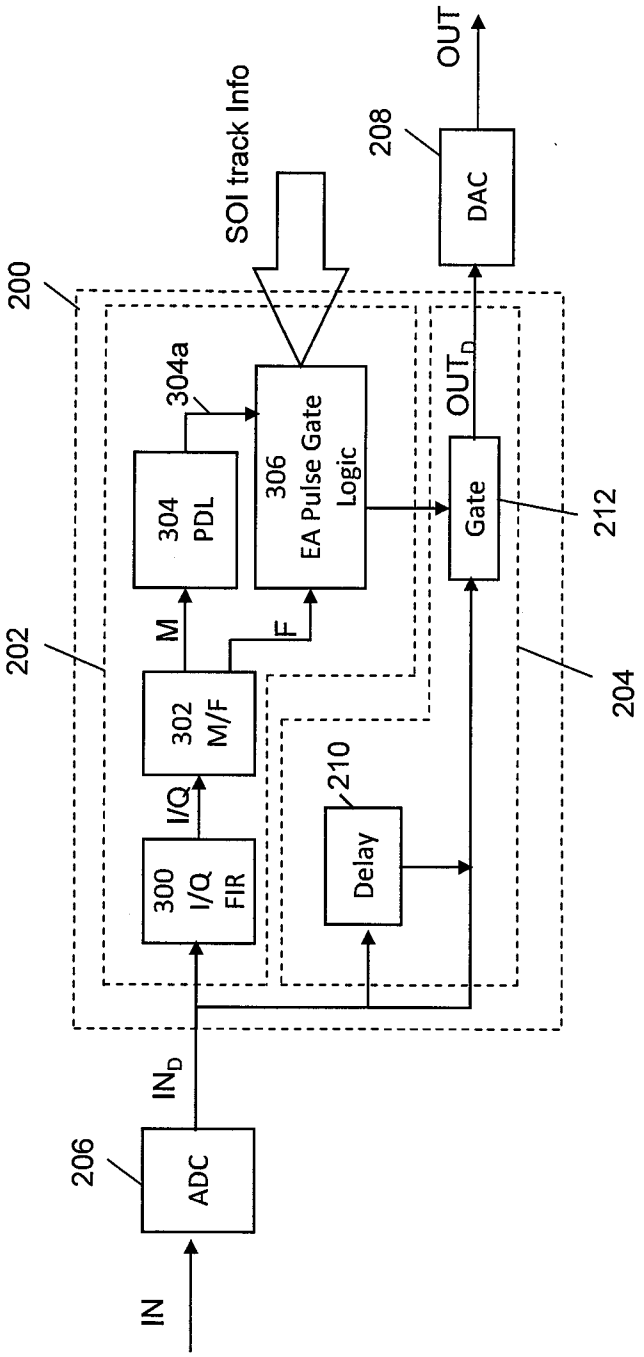


FIG. 1


IN
ADC
206
IN_D
200
202
204
300
I/Q
FIR
I/Q
302
M/F
M
F
304
PDL
304a
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EA Pulse Gate
Logic
SOI track Info
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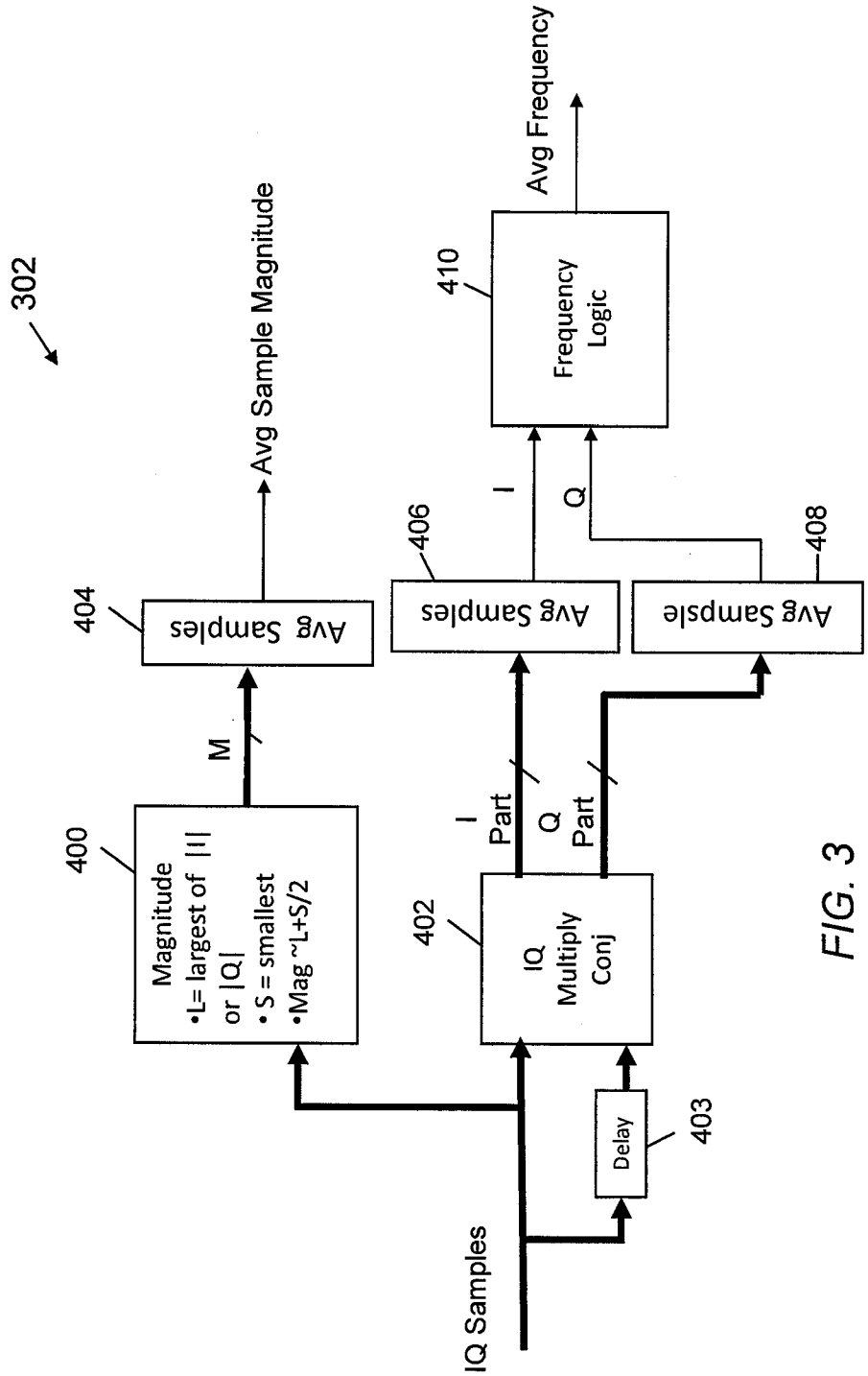
Delay
OUT_D
Gate
212
208
DAC
OUT

FIG. 2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Avg Frequency
410
Frequency Logic
I
Q
406
408
404
Avg Samples
Avg Samples
Avg Sample
M
400
Magnitude
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•S = smallest
•Mag ~L+S/2
I Part
Q Part
402
IQ Multiply Conj
Delay
403
IQ Samples

FIG. 3

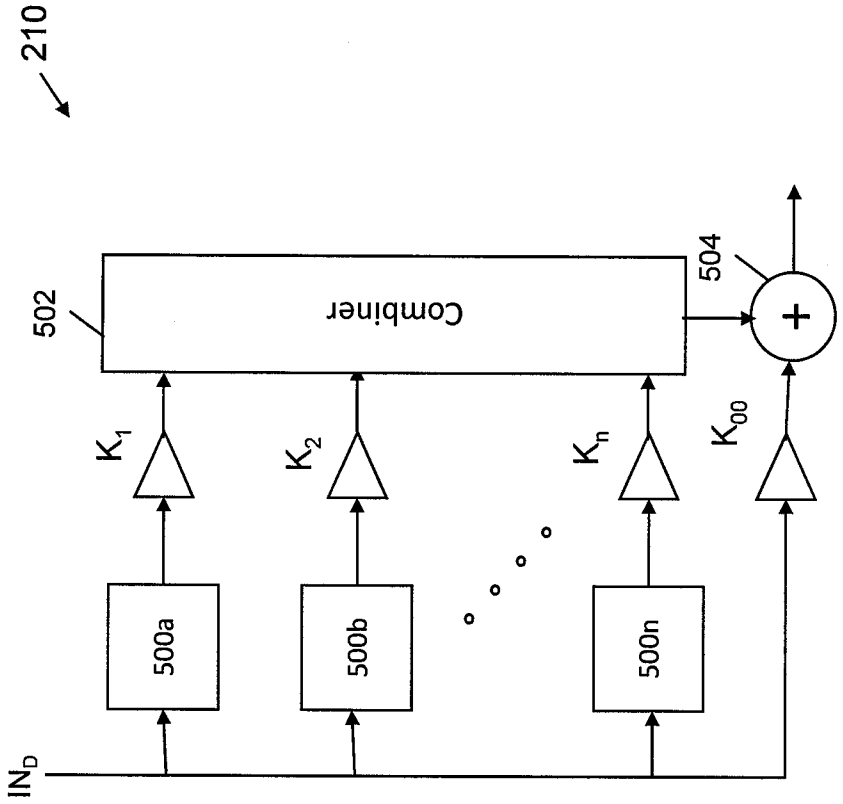

FIG. 4

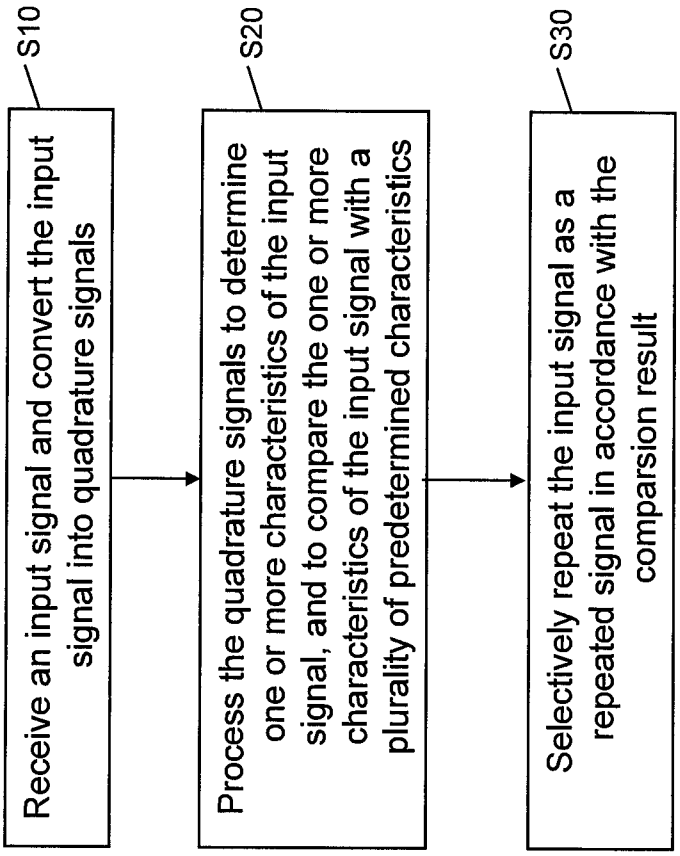
S10
Receive an input signal and convert the input signal into quadrature signals
S20
Process the quadrature signals to determine one or more characteristics of the input signal, and to compare the one or more characteristics of the input signal with a plurality of predetermined characteristics
S30
Selectively repeat the input signal as a repeated signal in accordance with the comparsion result

FIG. 5